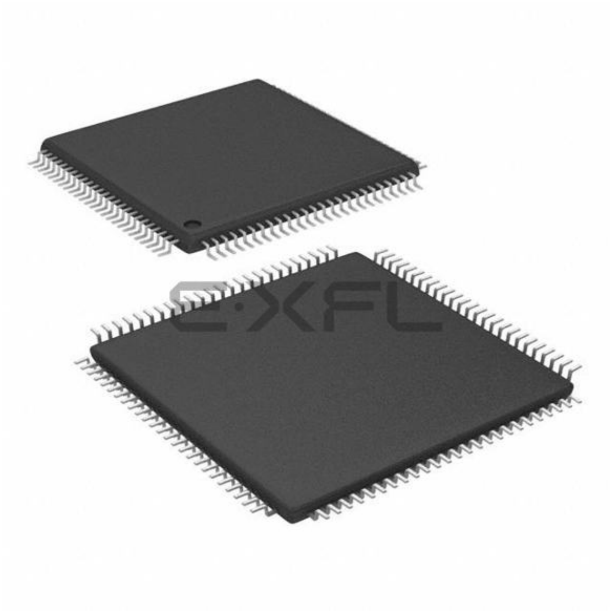

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	40 MIPs
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	85
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 32x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24hj256gp210a-e-pf

PIC24H PRODUCT FAMILIES

The PIC24H Family of devices is ideal for a wide variety of 16-bit MCU embedded applications. The device names, pin counts, memory sizes and peripheral availability of each device are listed below, followed by their pinout diagrams.

PIC24H Family Controllers

Device	Pins	Program Flash Memory (KB)	RAM[1] (KB)	DMA Channels	Timer 16-bit	Input Capture	Output Compare Std. PWM	Codec Interface	ADC	UART	SPI	I^2C™	CAN	I/O Pins (Max)[2]	Packages
PIC24HJ64GP206A	64	64	8	8	9	8	8	0	1 ADC, 18 ch	2	2	1	0	53	PT, MR
PIC24HJ64GP210A	100	64	8	8	9	8	8	0	1 ADC, 32 ch	2	2	2	0	85	PF, PT
PIC24HJ64GP506A	64	64	8	8	9	8	8	0	1 ADC, 18 ch	2	2	2	1	53	PT, MR
PIC24HJ64GP510A	100	64	8	8	9	8	8	0	1 ADC, 32 ch	2	2	2	1	85	PF, PT
PIC24HJ128GP206A	64	128	8	8	9	8	8	0	1 ADC, 18 ch	2	2	2	0	53	PT, MR
PIC24HJ128GP210A	100	128	8	8	9	8	8	0	1 ADC, 32 ch	2	2	2	0	85	PF, PT
PIC24HJ128GP506A	64	128	8	8	9	8	8	0	1 ADC, 18 ch	2	2	2	1	53	PT, MR
PIC24HJ128GP510A	100	128	8	8	9	8	8	0	1 ADC, 32 ch	2	2	2	1	85	PF, PT
PIC24HJ128GP306A	64	128	16	8	9	8	8	0	1 ADC, 18 ch	2	2	2	0	53	PT, MR
PIC24HJ128GP310A	100	128	16	8	9	8	8	0	1 ADC, 32 ch	2	2	2	0	85	PF, PT
PIC24HJ256GP206A	64	256	16	8	9	8	8	0	1 ADC, 18 ch	2	2	2	0	53	PT, MR
PIC24HJ256GP210A	100	256	16	8	9	8	8	0	1 ADC, 32 ch	2	2	2	0	85	PF, PT
PIC24HJ256GP610A	100	256	16	8	9	8	8	0	2 ADC, 32 ch	2	2	2	2	85	PF, PT

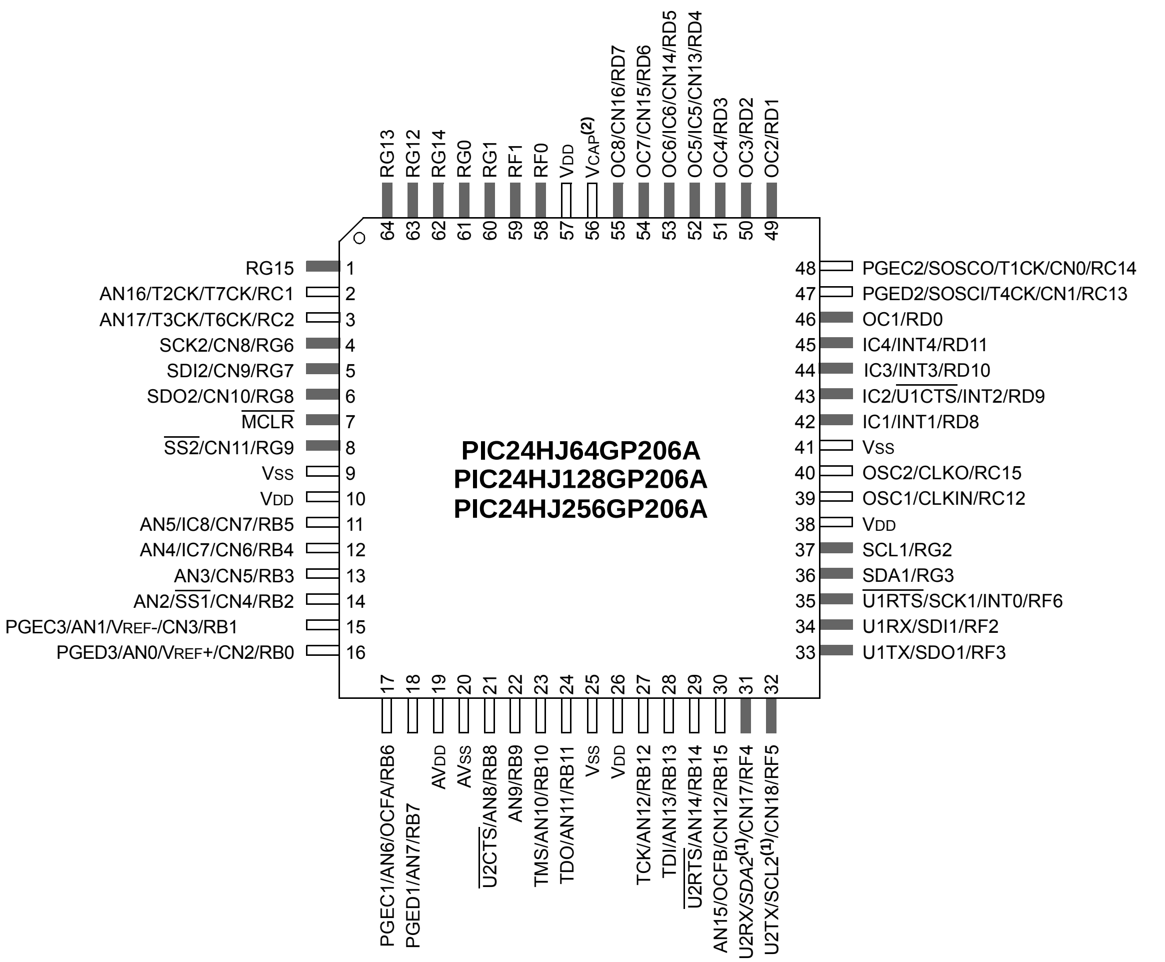
Note 1: RAM size is inclusive of 2 Kbytes DMA RAM.

2: Maximum I/O pin count includes pins shared by the peripheral functions.

Pin Diagrams (Continued)

64-Pin TQFP

■ = Pins are up to 5V tolerant



Note 1: This pin is not present on the PIC24HJ64GP206A device.

2: Refer to **Section 2.3 "CPU Logic Filter Capacitor Connection (V_{CAP})"** for proper connection to this pin.

Referenced Sources

This device data sheet is based on the following individual chapters of the *"dsPIC33F/PIC24H Family Reference Manual"*. These documents should be considered as the general reference for the operation of a particular module or device feature.

> **Note:** To access the documents listed below, browse to the documentation section of the PIC24HJ256GP610A product page on the Microchip web site (www.microchip.com) or by selecting a family reference manual section from the following list.
>
> In addition to parameters, features, and other documentation, the resulting page provides links to the related family reference manual sections.

- **Section 1. "Introduction"** (DS70197)
- **Section 2. "CPU"** (DS70204)
- **Section 3. "Data Memory"** (DS70202)
- **Section 4. "Program Memory"** (DS70203)
- **Section 5. "Flash Programming"** (DS70191)
- **Section 6. "Interrupts"** (DS70184)
- **Section 7. "Oscillator"** (DS70186)
- **Section 8. "Reset"** (DS70192)
- **Section 9. "Watchdog Timer and Power-Saving Modes"** (DS70196)
- **Section 10. "I/O Ports"** (DS70193)
- **Section 11. "Timers"** (DS70205)
- **Section 12. "Input Capture"** (DS70198)
- **Section 13. "Output Compare"** (DS70209)
- **Section 16. "Analog-to-Digital Converter (ADC)"** (DS70183)
- **Section 17. "UART"** (DS70188)
- **Section 18. "Serial Peripheral Interface (SPI)"** (DS70206)
- **Section 19. "Inter-Integrated Circuit™ (I2C™)"** (DS70195)
- **Section 20. "Data Converter Interface (DCI)"** (DS70288)
- **Section 21. "Enhanced Controller Area Network (ECAN™)"** (DS70185)
- **Section 22. "Direct Memory Access (DMA)"** (DS70182)
- **Section 23. "CodeGuard™ Security"** (DS70199)
- **Section 24. "Programming and Diagnostics"** (DS70207)
- **Section 25. "Device Configuration"** (DS70194)

1.0 DEVICE OVERVIEW

> **Note:** This data sheet summarizes the features of the PIC24HJXXXGPX06A/X08A/X10A family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the latest family reference sections of the *"dsPIC33F/PIC24H Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

This document contains device specific information for the following devices:

- PIC24HJ64GP206A
- PIC24HJ64GP210A
- PIC24HJ64GP506A
- PIC24HJ64GP510A
- PIC24HJ128GP206A
- PIC24HJ128GP210A
- PIC24HJ128GP506A
- PIC24HJ128GP510A
- PIC24HJ128GP306A
- PIC24HJ128GP310A
- PIC24HJ256GP206A
- PIC24HJ256GP210A
- PIC24HJ256GP610A

The PIC24HJXXXGPX06A/X08A/X10A device family includes devices with different pin counts (64 and 100 pins), different program memory sizes (64 Kbytes, 128 Kbytes and 256 Kbytes) and different RAM sizes (8 Kbytes and 16 Kbytes).

This makes these families suitable for a wide variety of high-performance digital signal control applications. The devices are pin compatible with the dsPIC33F family of devices, and also share a very high degree of compatibility with the dsPIC30F family devices. This allows easy migration between device families as may be necessitated by the specific functionality, computational resource and system cost requirements of the application.

The PIC24HJXXXGPX06A/X08A/X10A device family employs a powerful 16-bit architecture, ideal for applications that rely on high-speed, repetitive computations, as well as control.

The 17 x 17 multiplier, hardware support for division operations, multi-bit data shifter, a large array of 16-bit working registers and a wide variety of data addressing modes, together provide the PIC24HJXXXGPX06A/X08A/X10A Central Processing Unit (CPU) with extensive mathematical processing capability. Flexible and deterministic interrupt handling, coupled with a powerful array of peripherals, renders the PIC24HJXXXGPX06A/X08A/X10A devices suitable for control applications. Further, Direct Memory Access (DMA) enables overhead-free transfer of data between several peripherals and a dedicated DMA RAM. Reliable, field programmable Flash program memory ensures scalability of applications that use PIC24HJXXXGPX06A/X08A/X10A devices.

Figure 1-1 shows a general block diagram of the various core and peripheral modules in the PIC24HJXXXGPX06A/X08A/X10A family of devices, while Table 1-1 lists the functions of the various pins shown in the pinout diagrams.

TABLE 4-8: OUTPUT COMPARE REGISTER MAP

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
OC1RS	0180	Output Compare 1 Secondary Register																xxxx
OC1R	0182	Output Compare 1 Register																xxxx
OC1CON	0184	—	—	OCSIDL	—	—	—	—	—	—	—	—	OCFLT	OCTSEL	OCM<2:0>			0000
OC2RS	0186	Output Compare 2 Secondary Register																xxxx
OC2R	0188	Output Compare 2 Register																xxxx
OC2CON	018A	—	—	OCSIDL	—	—	—	—	—	—	—	—	OCFLT	OCTSEL	OCM<2:0>			0000
OC3RS	018C	Output Compare 3 Secondary Register																xxxx
OC3R	018E	Output Compare 3 Register																xxxx
OC3CON	0190	—	—	OCSIDL	—	—	—	—	—	—	—	—	OCFLT	OCTSEL	OCM<2:0>			0000
OC4RS	0192	Output Compare 4 Secondary Register																xxxx
OC4R	0194	Output Compare 4 Register																xxxx
OC4CON	0196	—	—	OCSIDL	—	—	—	—	—	—	—	—	OCFLT	OCTSEL	OCM<2:0>			0000
OC5RS	0198	Output Compare 5 Secondary Register																xxxx
OC5R	019A	Output Compare 5 Register																xxxx
OC5CON	019C	—	—	OCSIDL	—	—	—	—	—	—	—	—	OCFLT	OCTSEL	OCM<2:0>			0000
OC6RS	019E	Output Compare 6 Secondary Register																xxxx
OC6R	01A0	Output Compare 6 Register																xxxx
OC6CON	01A2	—	—	OCSIDL	—	—	—	—	—	—	—	—	OCFLT	OCTSEL	OCM<2:0>			0000
OC7RS	01A4	Output Compare 7 Secondary Register																xxxx
OC7R	01A6	Output Compare 7 Register																xxxx
OC7CON	01A8	—	—	OCSIDL	—	—	—	—	—	—	—	—	OCFLT	OCTSEL	OCM<2:0>			0000
OC8RS	01AA	Output Compare 8 Secondary Register																xxxx
OC8R	01AC	Output Compare 8 Register																xxxx
OC8CON	01AE	—	—	OCSIDL	—	—	—	—	—	—	—	—	OCFLT	OCTSEL	OCM<2:0>			0000

Legend: x = unknown value on Reset, — = unimplemented, read as ‘0’. Reset values are shown in hexadecimal for PinHigh devices.

4.4.2 DATA ACCESS FROM PROGRAM MEMORY USING TABLE INSTRUCTIONS

The TBLRDL and TBLWTL instructions offer a direct method of reading or writing the lower word of any address within the program space without going through data space. The TBLRDH and TBLWTH instructions are the only method to read or write the upper 8 bits of a program space word as data.

The PC is incremented by two for each successive 24-bit program word. This allows program memory addresses to directly map to data space addresses. Program memory can thus be regarded as two 16-bit, word wide address spaces, residing side by side, each with the same address range. TBLRDL and TBLWTL access the space which contains the least significant data word and TBLRDH and TBLWTH access the space which contains the upper data byte.

Two table instructions are provided to move byte or word sized (16-bit) data to and from program space. Both function as either byte or word operations.

1. TBLRDL (Table Read Low): In Word mode, it maps the lower word of the program space location (P<15:0>) to a data address (D<15:0>).

   In Byte mode, either the upper or lower byte of the lower program word is mapped to the lower byte of a data address. The upper byte is selected when Byte Select is ‘1’; the lower byte is selected when it is ‘0’.

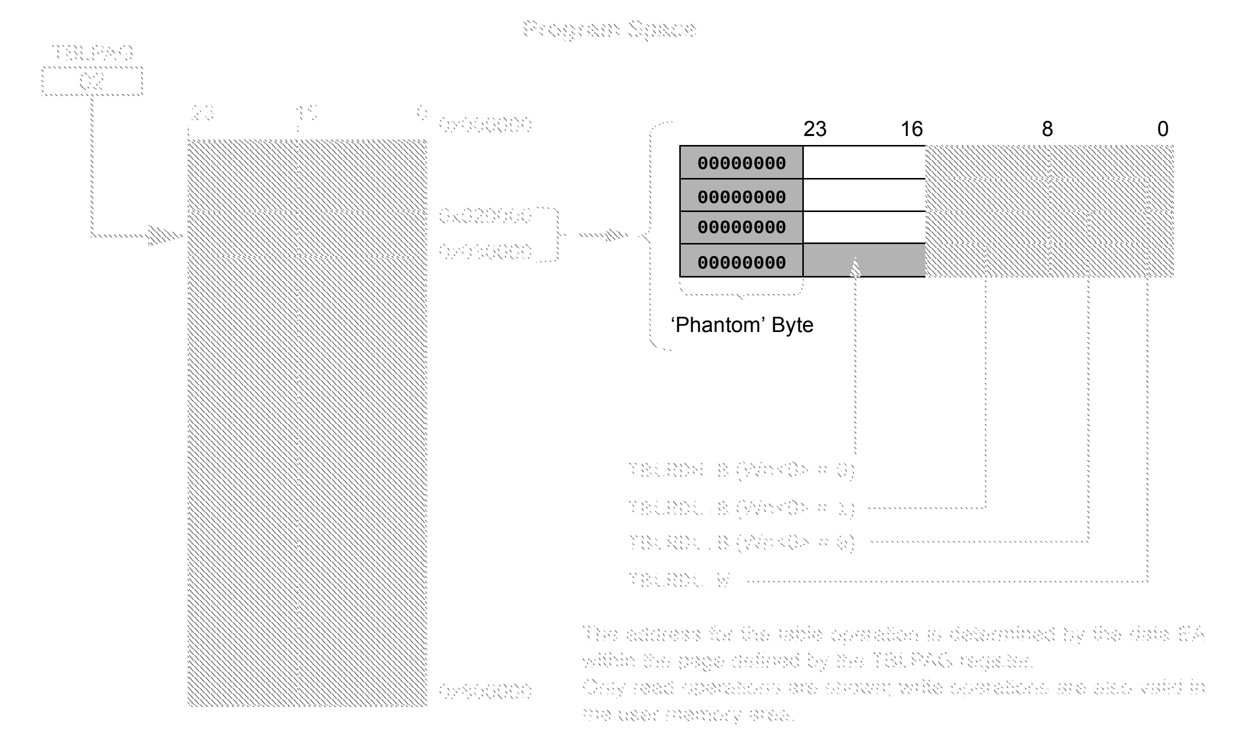
2. TBLRDH (Table Read High): In Word mode, it maps the entire upper word of a program address (P<23:16>) to a data address. Note that D<15:8>, the ‘phantom byte’, will always be ‘0’.

   In Byte mode, it maps the upper or lower byte of the program word to D<7:0> of the data address, as above. Note that the data will always be ‘0’ when the upper ‘phantom’ byte is selected (Byte Select = 1).

In a similar fashion, two table instructions, TBLWTH and TBLWTL, are used to write individual bytes or words to a program space address. The details of their operation are explained in **Section 5.0 “Flash Program Memory”**.

For all table operations, the area of program memory space to be accessed is determined by the Table Page register (TBLPAG). TBLPAG covers the entire program memory space of the device, including user and configuration spaces. When TBLPAG<7> = 0, the table page is located in the user memory space. When TBLPAG<7> = 1, the page is located in configuration space.

FIGURE 4-7: ACCESSING PROGRAM MEMORY WITH TABLE INSTRUCTIONS



The address for the table operation is determined by the data EA within the page defined by the TBLPAG register.
Only read operations are shown; write operations are also valid in the user memory area.

5.0 FLASH PROGRAM MEMORY

> **Note 1:** This data sheet summarizes the features of the PIC24HJXXXGPX06A/X08A/X10A family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 5. "Flash Programming"** (DS70191) of the *"dsPIC33F/PIC24H Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).
>
> **2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The PIC24HJXXXGPX06A/X08A/X10A devices contain internal Flash program memory for storing and executing application code. The memory is readable, writable and erasable during normal operation over the entire VDD range.

Flash memory can be programmed in two ways:

1. In-Circuit Serial Programming™ (ICSP™) programming capability
2. Run-Time Self-Programming (RTSP)

ICSP programming capability allows a PIC24HJXXXGPX06A/X08A/X10A device to be serially programmed while in the end application circuit. This is simply done with two lines for programming clock and programming data (one of the alternate programming pin pairs: PGECx/PGEDx, and three other lines for power (VDD), ground (VSS) and Master Clear (MCLR). This allows customers to manufacture boards with unprogrammed devices and then program the digital signal controller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

RTSP is accomplished using TBLRD (table read) and TBLWT (table write) instructions. With RTSP, the user can write program memory data either in blocks or 'rows' of 64 instructions (192 bytes) at a time, or single instructions and erase program memory in blocks or 'pages' of 512 instructions (1536 bytes) at a time.

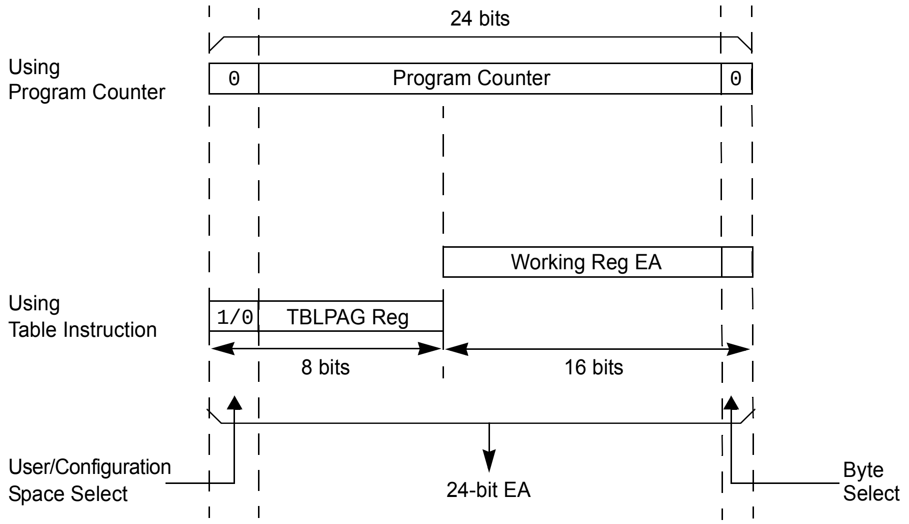
5.1 Table Instructions and Flash Programming

Regardless of the method used, all programming of Flash memory is done with the table read and table write instructions. These allow direct read and write access to the program memory space from the data memory while the device is in normal operating mode. The 24-bit target address in the program memory is formed using bits<7:0> of the TBLPAG register and the Effective Address (EA) from a W register specified in the table instruction, as shown in Figure 5-1.

The TBLRDL and the TBLWTL instructions are used to read or write to bits<15:0> of program memory. TBLRDL and TBLWTL can access program memory in both Word and Byte modes.

The TBLRDH and TBLWTH instructions are used to read or write to bits<23:16> of program memory. TBLRDH and TBLWTH can also access program memory in Word or Byte mode.

FIGURE 5-1: ADDRESSING FOR TABLE REGISTERS



REGISTER 8-3: DMAxSTA: DMA CHANNEL x RAM START ADDRESS OFFSET REGISTER A

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STA<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STA<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **STA<15:0>:** Primary DMA RAM Start Address bits (source or destination)

REGISTER 8-4: DMAxSTB: DMA CHANNEL x RAM START ADDRESS OFFSET REGISTER B

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STB<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STB<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **STB<15:0>:** Secondary DMA RAM Start Address bits (source or destination)

REGISTER 10-2: PMD2: PERIPHERAL MODULE DISABLE CONTROL REGISTER 2 (CONTINUED)

bit 3 **OC4MD:** Output Compare 4 Module Disable bit

1 = Output Compare 4 module is disabled
0 = Output Compare 4 module is enabled

bit 2 **OC3MD:** Output Compare 3 Module Disable bit

1 = Output Compare 3 module is disabled
0 = Output Compare 3 module is enabled

bit 1 **OC2MD:** Output Compare 2 Module Disable bit

1 = Output Compare 2 module is disabled
0 = Output Compare 2 module is enabled

bit 0 **OC1MD:** Output Compare 1 Module Disable bit

1 = Output Compare 1 module is disabled
0 = Output Compare 1 module is enabled

NOTES:

REGISTER 17-1: I2CxCON: I2Cx CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-1 HC	R/W-0	R/W-0	R/W-0	R/W-0
I2CEN	—	I2CSIDL	SCLREL	IPMIEN	A10M	DISSLW	SMEN
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0 HC	R/W-0 HC	R/W-0 HC	R/W-0 HC	R/W-0 HC
GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN
bit 7							bit 0

Legend:	U = Unimplemented bit, read as ‘0’		
R = Readable bit	W = Writable bit	HS = Set in hardware	HC = Cleared in hardware
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **I2CEN:** I2Cx Enable bit

1 = Enables the I2Cx module and configures the SDAx and SCLx pins as serial port pins
0 = Disables the I2Cx module. All I^{2}C pins are controlled by port functions.

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **I2CSIDL:** Stop in Idle Mode bit

1 = Discontinue module operation when device enters an Idle mode
0 = Continue module operation in Idle mode

bit 12 **SCLREL:** SCLx Release Control bit (when operating as I^{2}C slave)

1 = Release SCLx clock
0 = Hold SCLx clock low (clock stretch)

If STREN = 1:
Bit is R/W (i.e., software may write ‘0’ to initiate stretch and write ‘1’ to release clock). Hardware clear at beginning of slave transmission. Hardware clear at end of slave reception.

If STREN = 0:
Bit is R/S (i.e., software may only write ‘1’ to release clock). Hardware clear at beginning of slave transmission.

bit 11 **IPMIEN:** Intelligent Peripheral Management Interface (IPMI) Enable bit

1 = IPMI mode is enabled; all addresses Acknowledged
0 = IPMI mode disabled

bit 10 **A10M:** 10-bit Slave Address bit

1 = I2CxADD is a 10-bit slave address
0 = I2CxADD is a 7-bit slave address

bit 9 **DISSLW:** Disable Slew Rate Control bit

1 = Slew rate control disabled
0 = Slew rate control enabled

bit 8 **SMEN:** SMBus Input Levels bit

1 = Enable I/O pin thresholds compliant with SMBus specification
0 = Disable SMBus input thresholds

bit 7 **GCEN:** General Call Enable bit (when operating as I^{2}C slave)

1 = Enable interrupt when a general call address is received in the I2CxRSR (module is enabled for reception)
0 = General call address disabled

bit 6 **STREN:** SCLx Clock Stretch Enable bit (when operating as I^{2}C slave)

Used in conjunction with SCLREL bit.
1 = Enable software or receive clock stretching
0 = Disable software or receive clock stretching

REGISTER 19-4: CiFCTRL: ECAN™ MODULE FIFO CONTROL REGISTER

R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
DMABS<2:0>			—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	FSA<4:0>				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-13 **DMABS<2:0>:** DMA Buffer Size bits

111 = Reserved; do not use
110 = 32 buffers in DMA RAM
101 = 24 buffers in DMA RAM
100 = 16 buffers in DMA RAM
011 = 12 buffers in DMA RAM
010 = 8 buffers in DMA RAM
001 = 6 buffers in DMA RAM
000 = 4 buffers in DMA RAM

bit 12-5 **Unimplemented:** Read as ‘0’

bit 4-0 **FSA<4:0>:** FIFO Area Starts with Buffer bits

11111 = RB31 buffer
11110 = RB30 buffer
•
•
•
00001 = TRB1 buffer
00000 = TRB0 buffer

REGISTER 19-18: CiFMSKSEL1: ECAN™ MODULE FILTER 7-0 MASK SELECTION REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F7MSK<1:0>		F6MSK<1:0>		F5MSK<1:0>		F4MSK<1:0>	
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F3MSK<1:0>		F2MSK<1:0>		F1MSK<1:0>		F0MSK<1:0>	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **F7MSK<1:0>:** Mask Source for Filter 7 bit
11 = Reserved; do not use
10 = Acceptance Mask 2 registers contain mask
01 = Acceptance Mask 1 registers contain mask
00 = Acceptance Mask 0 registers contain mask

bit 13-12 **F6MSK<1:0>:** Mask Source for Filter 6 bit
11 = Reserved; do not use
10 = Acceptance Mask 2 registers contain mask
01 = Acceptance Mask 1 registers contain mask
00 = Acceptance Mask 0 registers contain mask

bit 11-10 **F5MSK<1:0>:** Mask Source for Filter 5 bit
11 = Reserved; do not use
10 = Acceptance Mask 2 registers contain mask
01 = Acceptance Mask 1 registers contain mask
00 = Acceptance Mask 0 registers contain mask

bit 9-8 **F4MSK<1:0>:** Mask Source for Filter 4 bit
11 = Reserved; do not use
10 = Acceptance Mask 2 registers contain mask
01 = Acceptance Mask 1 registers contain mask
00 = Acceptance Mask 0 registers contain mask

bit 7-6 **F3MSK<1:0>:** Mask Source for Filter 3 bit
11 = Reserved; do not use
10 = Acceptance Mask 2 registers contain mask
01 = Acceptance Mask 1 registers contain mask
00 = Acceptance Mask 0 registers contain mask

bit 5-4 **F2MSK<1:0>:** Mask Source for Filter 2 bit
11 = Reserved; do not use
10 = Acceptance Mask 2 registers contain mask
01 = Acceptance Mask 1 registers contain mask
00 = Acceptance Mask 0 registers contain mask

bit 3-2 **F1MSK<1:0>:** Mask Source for Filter 1 bit
11 = Reserved; do not use
10 = Acceptance Mask 2 registers contain mask
01 = Acceptance Mask 1 registers contain mask
00 = Acceptance Mask 0 registers contain mask

bit 1-0 **F0MSK<1:0>:** Mask Source for Filter 0 bit
11 = Reserved; do not use
10 = Acceptance Mask 2 registers contain mask
01 = Acceptance Mask 1 registers contain mask
00 = Acceptance Mask 0 registers contain mask

TABLE 21-2: CONFIGURATION BITS DESCRIPTION (CONTINUED)

Bit Field	Register	RTSP Effect	Description
SSS<2:0>	FSS	Immediate	Secure Segment Program Flash Code Protection Size (**FOR 128K and 256K DEVICES**) X11 = No Secure program Flash segment Secure space is 8K IW less BS 110 = Standard security; secure program Flash segment starts at End of BS, ends at 0x003FFE 010 = High security; secure program Flash segment starts at End of BS, ends at 0x003FFE Secure space is 16K IW less BS 101 = Standard security; secure program Flash segment starts at End of BS, ends at 0x007FFE 001 = High security; secure program Flash segment starts at End of BS, ends at 0x007FFE Secure space is 32K IW less BS 100 = Standard security; secure program Flash segment starts at End of BS, ends at 0x00FFFE 000 = High security; secure program Flash segment starts at End of BS, ends at 0x00FFFE (**FOR 64K DEVICES**) X11 = No Secure program Flash segment Secure space is 4K IW less BS 110 = Standard security; secure program Flash segment starts at End of BS, ends at 0x001FFE 010 = High security; secure program Flash segment starts at End of BS, ends at 0x001FFE Secure space is 8K IW less BS 101 = Standard security; secure program Flash segment starts at End of BS, ends at 0x003FFE 001 = High security; secure program Flash segment starts at End of BS, ends at 0x003FFE Secure space is 16K IW less BS 100 = Standard security; secure program Flash segment starts at End of BS, ends at 0x007FFE 000 = High security; secure program Flash segment starts at End of BS, ends at 0x007FFE
RSS<1:0>	FSS	Immediate	Secure Segment RAM Code Protection 11 = No Secure RAM defined 10 = Secure RAM is 256 Bytes less BS RAM 01 = Secure RAM is 2048 Bytes less BS RAM 00 = Secure RAM is 4096 Bytes less BS RAM
GSS<1:0>	FGS	Immediate	General Segment Code-Protect bit 11 = User program memory is not code-protected 10 = Standard Security; general program Flash segment starts at End of SS, ends at EOM 0x = High Security; general program Flash segment starts at End of ESS, ends at EOM
GWRP	FGS	Immediate	General Segment Write-Protect bit 1 = User program memory is not write-protected 0 = User program memory is write-protected

22.0 INSTRUCTION SET SUMMARY

Note: This data sheet summarizes the features of the PIC24HJXXXGPX06A/X08A/X10A families of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section in the *"dsPIC33F/PIC24H Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

The PIC24H instruction set is identical to that of the PIC24F, and is a subset of the dsPIC30F/33F instruction set.

Most instructions are a single program memory word (24 bits). Only three instructions require two program memory locations.

Each single-word instruction is a 24-bit word, divided into an 8-bit opcode, which specifies the instruction type and one or more operands, which further specify the operation of the instruction.

The instruction set is highly orthogonal and is grouped into five basic categories:

- Word or byte-oriented operations
- Bit-oriented operations
- Literal operations
- DSP operations
- Control operations

Table 22-1 shows the general symbols used in describing the instructions.

The PIC24H instruction set summary in Table 22-2 lists all the instructions, along with the status flags affected by each instruction.

Most word or byte-oriented W register instructions (including barrel shift instructions) have three operands:

- The first source operand which is typically a register 'Wb' without any address modifier
- The second source operand which is typically a register 'Ws' with or without an address modifier
- The destination of the result which is typically a register 'Wd' with or without an address modifier

However, word or byte-oriented file register instructions have two operands:

- The file register specified by the value 'f'
- The destination, which could either be the file register 'f' or the W0 register, which is denoted as 'WREG'

Most bit-oriented instructions (including simple rotate/shift instructions) have two operands:

- The W register (with or without an address modifier) or file register (specified by the value of 'Ws' or 'f')
- The bit in the W register or file register (specified by a literal value or indirectly by the contents of register 'Wb')

The literal instructions that involve data movement may use some of the following operands:

- A literal value to be loaded into a W register or file register (specified by the value of 'k')
- The W register or file register where the literal value is to be loaded (specified by 'Wb' or 'f')

However, literal instructions that involve arithmetic or logical operations use some of the following operands:

- The first source operand which is a register 'Wb' without any address modifier
- The second source operand which is a literal value
- The destination of the result (only if not the same as the first source operand) which is typically a register 'Wd' with or without an address modifier

The control instructions may use some of the following operands:

- A program memory address
- The mode of the table read and table write instructions

All instructions are a single word, except for certain double word instructions, which were made double word instructions so that all the required information is available in these 48 bits. In the second word, the 8 MSbs are '0's. If this second word is executed as an instruction (by itself), it will execute as a NOP.

Most single-word instructions are executed in a single instruction cycle, unless a conditional test is true, or the program counter is changed as a result of the instruction. In these cases, the execution takes two instruction cycles with the additional instruction cycle(s) executed as a NOP. Notable exceptions are the BRA (unconditional/computed branch), indirect CALL/GOTO, all table reads and writes and RETURN/RETFIE instructions, which are single-word instructions but take two or three cycles. Certain instructions that involve skipping over the subsequent instruction require either two or three cycles if the skip is performed, depending on whether the instruction being skipped is a single-word or double word instruction. Moreover, double word moves require two cycles. The double word instructions execute in two instruction cycles.

Note: For more details on the instruction set, refer to the *"16-bit MCU and DSC Programmer's Reference Manual"* (DS70157).

TABLE 22-1: SYMBOLS USED IN OPCODE DESCRIPTIONS

Field	Description
#text	Means literal defined by “text”
(text)	Means “content of text”
[text]	Means “the location addressed by text”
{ }	Optional field or operation
<n:m>	Register bit field
.b	Byte mode selection
.d	Double Word mode selection
.S	Shadow register select
.w	Word mode selection (default)
bit4	4-bit bit selection field (used in word addressed instructions) ∈ {0...15}
C, DC, N, OV, Z	MCU Status bits: Carry, Digit Carry, Negative, Overflow, Sticky Zero
Expr	Absolute address, label or expression (resolved by the linker)
f	File register address ∈ {0x0000...0x1FFF}
lit1	1-bit unsigned literal ∈ {0,1}
lit4	4-bit unsigned literal ∈ {0...15}
lit5	5-bit unsigned literal ∈ {0...31}
lit8	8-bit unsigned literal ∈ {0...255}
lit10	10-bit unsigned literal ∈ {0...255} for Byte mode, {0:1023} for Word mode
lit14	14-bit unsigned literal ∈ {0...16384}
lit16	16-bit unsigned literal ∈ {0...65535}
lit23	23-bit unsigned literal ∈ {0...8388608}; LSB must be ‘0’
None	Field does not require an entry, may be blank
PC	Program Counter
Slit10	10-bit signed literal ∈ {-512...511}
Slit16	16-bit signed literal ∈ {-32768...32767}
Slit6	6-bit signed literal ∈ {-16...16}
Wb	Base W register ∈ {W0..W15}
Wd	Destination W register ∈ { Wd, [Wd], [Wd++], [Wd--], [++Wd], [--Wd] }
Wdo	Destination W register ∈ { Wnd, [Wnd], [Wnd++], [Wnd--], [++Wnd], [--Wnd], [Wnd+Wb] }
Wm,Wn	Dividend, Divisor working register pair (direct addressing)
Wm*Wm	Multiplicand and Multiplier working register pair for Square instructions ∈ {W4 * W4,W5 * W5,W6 * W6,W7 * W7}
Wm*Wn	Multiplicand and Multiplier working register pair for DSP instructions ∈ {W4 * W5,W4 * W6,W4 * W7,W5 * W6,W5 * W7,W6 * W7}
Wn	One of 16 working registers ∈ {W0..W15}
Wnd	One of 16 destination working registers ∈ {W0...W15}
Wns	One of 16 source working registers ∈ {W0...W15}
WREG	W0 (working register used in file register instructions)
Ws	Source W register ∈ { Ws, [Ws], [Ws++], [Ws--], [++Ws], [--Ws] }
Wso	Source W register ∈ { Wns, [Wns], [Wns++], [Wns--], [++Wns], [--Wns], [Wns+Wb] }

23.7 MPLAB SIM Software Simulator

The MPLAB SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC® DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB SIM Software Simulator fully supports symbolic debugging using the MPLAB C Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

23.8 MPLAB REAL ICE In-Circuit Emulator System

MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs PIC® Flash MCUs and dsPIC® Flash DSCs with the easy-to-use, powerful graphical user interface of the MPLAB Integrated Development Environment (IDE), included with each kit.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB IDE. In upcoming releases of MPLAB IDE, new devices will be supported, and new features will be added. MPLAB REAL ICE offers significant advantages over competitive emulators including low-cost, full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, a ruggedized probe interface and long (up to three meters) interconnection cables.

23.9 MPLAB ICD 3 In-Circuit Debugger System

MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost effective high-speed hardware debugger/programmer for Microchip Flash Digital Signal Controller (DSC) and microcontroller (MCU) devices. It debugs and programs PIC® Flash microcontrollers and dsPIC® DSCs with the powerful, yet easy-to-use graphical user interface of MPLAB Integrated Development Environment (IDE).

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

23.10 PICkit 3 In-Circuit Debugger/ Programmer and PICkit 3 Debug Express

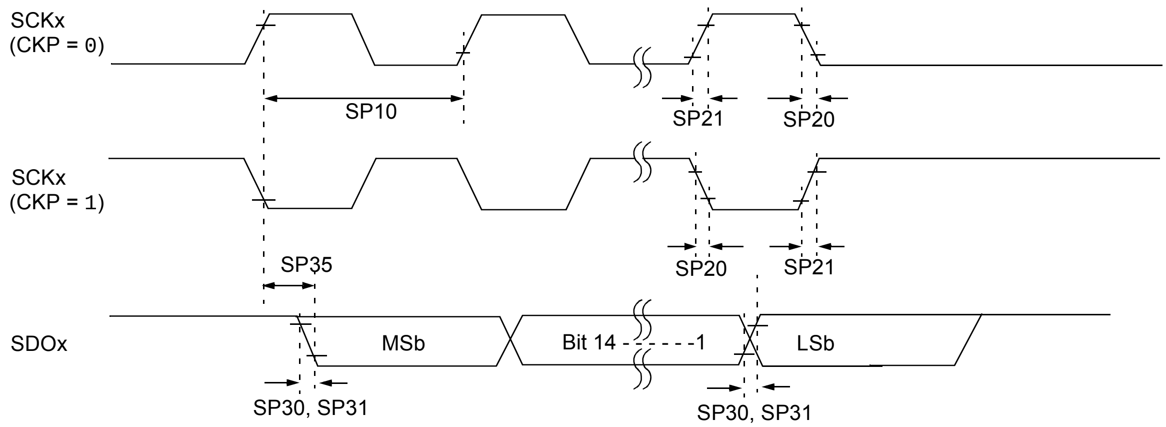
The MPLAB PICkit 3 allows debugging and programming of PIC® and dsPIC® Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB Integrated Development Environment (IDE). The MPLAB PICkit 3 is connected to the design engineer's PC using a full speed USB interface and can be connected to the target via an Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the reset line to implement in-circuit debugging and In-Circuit Serial Programming™.

The PICkit 3 Debug Express include the PICkit 3, demo board and microcontroller, hookup cables and CDROM with user's guide, lessons, tutorial, compiler and MPLAB IDE software.

TABLE 24-28: SPIx MAXIMUM DATA/CLOCK RATE SUMMARY

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Maximum Data Rate	**Master Transmit Only (Half-Duplex)**	**Master Transmit/Receive (Full-Duplex)**	**Slave Transmit/Receive (Full-Duplex)**	**CKE**	**CKP**	**SMP**
15 MHz	Table 24-29	—	—	0,1	0,1	0,1
10 MHz	—	Table 24-30	—	1	0,1	1
10 MHz	—	Table 24-31	—	0	0,1	1
15 MHz	—	—	Table 24-32	1	0	0
11 MHz	—	—	Table 24-33	1	1	0
15 MHz	—	—	Table 24-34	0	1	0
11 MHz	—	—	Table 24-35	0	0	0

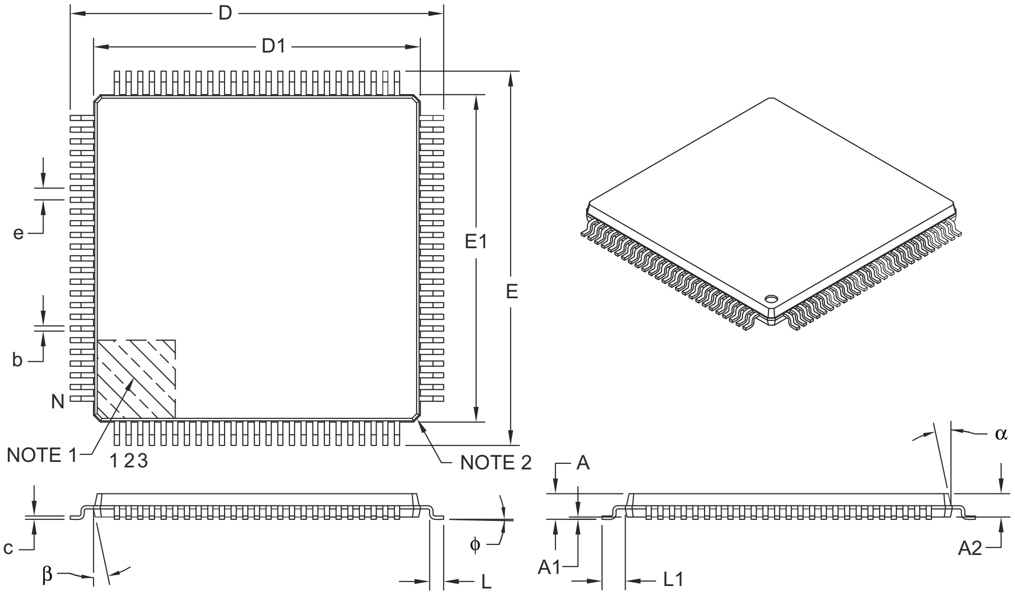
FIGURE 24-9: SPIx MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY CKE = 0) TIMING CHARACTERISTICS



Note: Refer to Figure 24-1 for load conditions.

100-Lead Plastic Thin Quad Flatpack (PF) – 14x14x1 mm Body, 2.00 mm Footprint [TQFP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



		Units	MILLIMETERS		
		Dimension Limits	MIN	NOM	MAX
Number of Leads	N			100	
Lead Pitch	e			0.50 BSC	
Overall Height	A		–	–	1.20
Molded Package Thickness	A2		0.95	1.00	1.05
Standoff	A1		0.05	–	0.15
Foot Length	L		0.45	0.60	0.75
Footprint	L1			1.00 REF	
Foot Angle	ϕ		0°	3.5°	7°
Overall Width	E			16.00 BSC	
Overall Length	D			16.00 BSC	
Molded Package Width	E1			14.00 BSC	
Molded Package Length	D1			14.00 BSC	
Lead Thickness	c		0.09	–	0.20
Lead Width	b		0.17	0.22	0.27
Mold Draft Angle Top	α		11°	12°	13°
Mold Draft Angle Bottom	β		11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

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