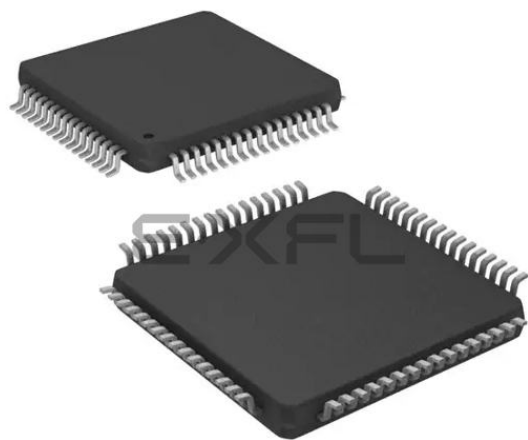




Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	40 MIPS
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	53
Program Memory Size	64KB (22K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 18x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24hj64gp206a-i-pt

PIC24HJXXXGPX06A/X08A/X10A

PIC24H PRODUCT FAMILIES

The PIC24H Family of devices is ideal for a wide variety of 16-bit MCU embedded applications. The device names, pin counts, memory sizes and peripheral availability of each device are listed below, followed by their pinout diagrams.

PIC24H Family Controllers

Device	Pins	Program Flash Memory (KB)	RAM ⁽¹⁾ (KB)	DMA Channels	Timer 16-bit	Input Capture	Output Compare Std. PWM	Codec Interface	ADC	UART	SPI	I ² C™	CAN	I/O Pins (Max) ⁽²⁾	Packages
PIC24HJ64GP206A	64	64	8	8	9	8	8	0	1 ADC, 18 ch	2	2	1	0	53	PT, MR
PIC24HJ64GP210A	100	64	8	8	9	8	8	0	1 ADC, 32 ch	2	2	2	0	85	PF, PT
PIC24HJ64GP506A	64	64	8	8	9	8	8	0	1 ADC, 18 ch	2	2	2	1	53	PT, MR
PIC24HJ64GP510A	100	64	8	8	9	8	8	0	1 ADC, 32 ch	2	2	2	1	85	PF, PT
PIC24HJ128GP206A	64	128	8	8	9	8	8	0	1 ADC, 18 ch	2	2	2	0	53	PT, MR
PIC24HJ128GP210A	100	128	8	8	9	8	8	0	1 ADC, 32 ch	2	2	2	0	85	PF, PT
PIC24HJ128GP506A	64	128	8	8	9	8	8	0	1 ADC, 18 ch	2	2	2	1	53	PT, MR
PIC24HJ128GP510A	100	128	8	8	9	8	8	0	1 ADC, 32 ch	2	2	2	1	85	PF, PT
PIC24HJ128GP306A	64	128	16	8	9	8	8	0	1 ADC, 18 ch	2	2	2	0	53	PT, MR
PIC24HJ128GP310A	100	128	16	8	9	8	8	0	1 ADC, 32 ch	2	2	2	0	85	PF, PT
PIC24HJ256GP206A	64	256	16	8	9	8	8	0	1 ADC, 18 ch	2	2	2	0	53	PT, MR
PIC24HJ256GP210A	100	256	16	8	9	8	8	0	1 ADC, 32 ch	2	2	2	0	85	PF, PT
PIC24HJ256GP610A	100	256	16	8	9	8	8	0	2 ADC, 32 ch	2	2	2	2	85	PF, PT

Note 1: RAM size is inclusive of 2 Kbytes DMA RAM.

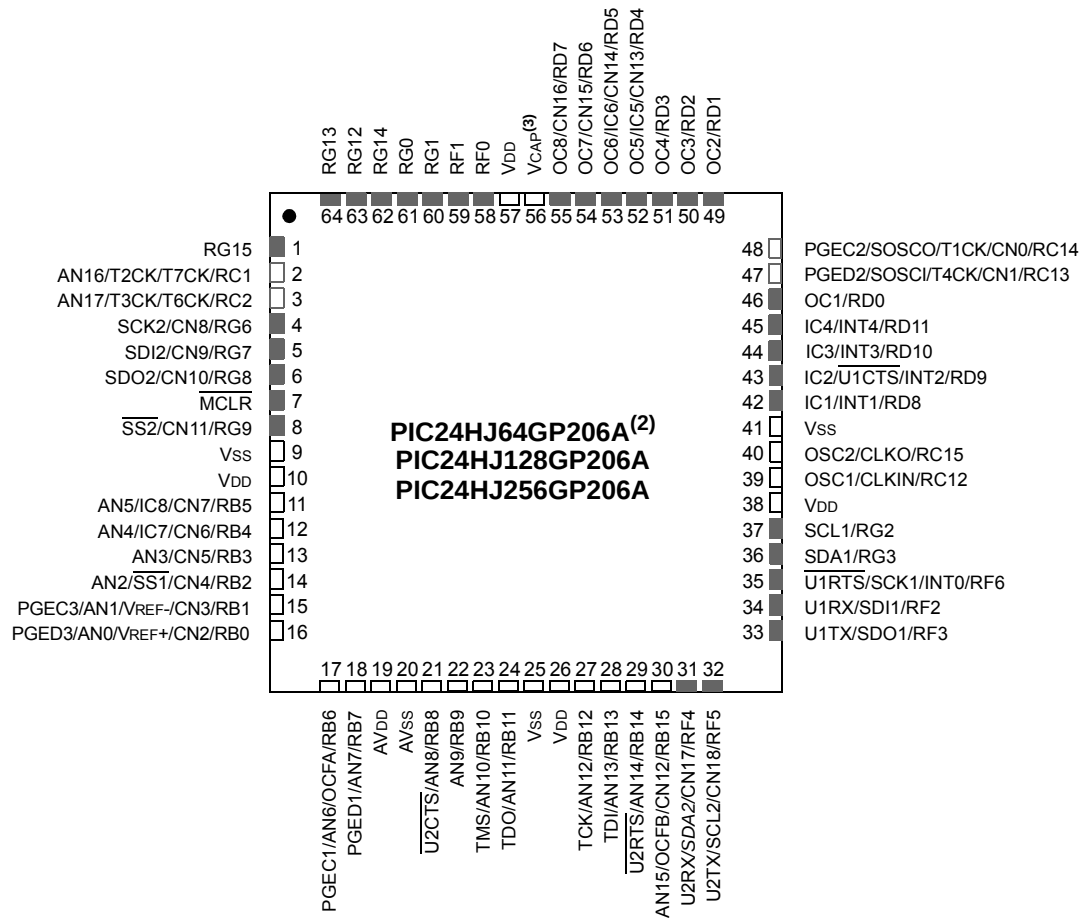
Note 2: Maximum I/O pin count includes pins shared by the peripheral functions.

PIC24HJXXXGPX06A/X08A/X10A

Pin Diagrams

64-Pin QFN⁽¹⁾

■ = Pins are up to 5V tolerant



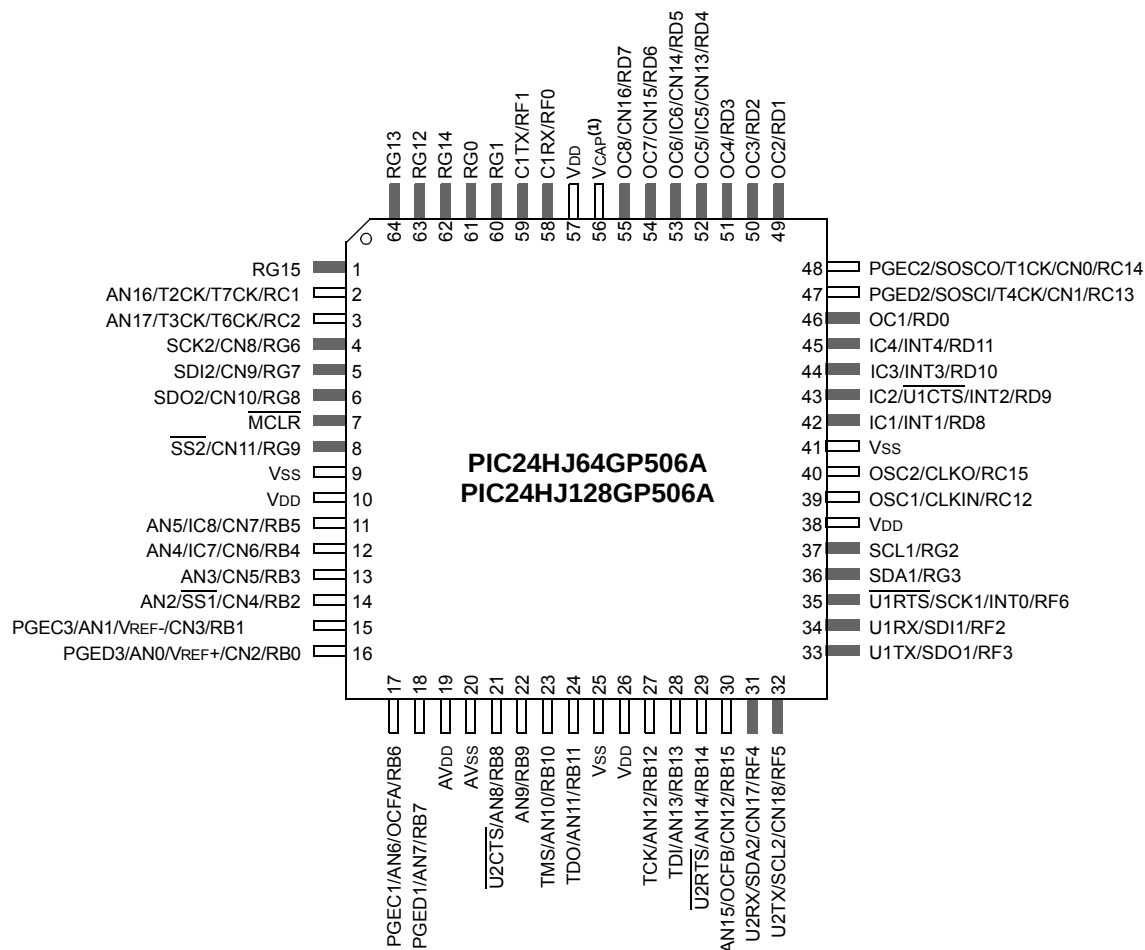
- Note 1:** The metal plane at the bottom of the device is not connected to any pins and should be connected to Vss externally.
- Note 2:** The PIC24HJ64GP206A device does not have the SCL2 and SDA2 pins.
- Note 3:** Refer to **Section 2.3 "CPU Logic Filter Capacitor Connection (VCAP)"** for proper connection to this pin.

PIC24HJXXXGPX06A/X08A/X10A

Pin Diagrams (Continued)

64-Pin TQFP

■ = Pins are up to 5V tolerant



Note 1: Refer to Section 2.3 "CPU Logic Filter Capacitor Connection (Vcap)" for proper connection to this pin.

TABLE 4-19: ECAN1 REGISTER MAP WHEN C1CTRL1.WIN = 0 FOR PIC24HJXXXGP506A/510A/610A DEVICES ONLY

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
	0400-041E	See definition when WIN = x																
C1RXFUL1	0420	RXFUL15	RXFUL14	RXFUL13	RXFUL12	RXFUL11	RXFUL10	RXFUL9	RXFUL8	RXFUL7	RXFUL6	RXFUL5	RXFUL4	RXFUL3	RXFUL2	RXFUL1	RXFUL0	0000
C1RXFUL2	0422	RXFUL31	RXFUL30	RXFUL29	RXFUL28	RXFUL27	RXFUL26	RXFUL25	RXFUL24	RXFUL23	RXFUL22	RXFUL21	RXFUL20	RXFUL19	RXFUL18	RXFUL17	RXFUL16	0000
C1RXOVF1	0428	RXOVF15	RXOVF14	RXOVF13	RXOVF12	RXOVF11	RXOVF10	RXOVF9	RXOVF8	RXOVF7	RXOVF6	RXOVF5	RXOVF4	RXOVF3	RXOVF2	RXOVF1	RXOVF0	0000
C1RXOVF2	042A	RXOVF31	RXOVF30	RXOVF29	RXOVF28	RXOVF27	RXOVF26	RXOVF25	RXOVF24	RXOVF23	RXOVF22	RXOVF21	RXOVF20	RXOVF19	RXOVF18	RXOVF17	RXOVF16	0000
C1TR01CON	0430	TXEN1	TX ABT1	TX LARB1	TX ERR1	TX REQ1	RTREN1	TX1PRI<1:0>		TXEN0	TX ABAT0	TX LARB0	TX ERR0	TX REQ0	RTREN0	TX0PRI<1:0>		0000
C1TR23CON	0432	TXEN3	TX ABT3	TX LARB3	TX ERR3	TX REQ3	RTREN3	TX3PRI<1:0>		TXEN2	TX ABAT2	TX LARB2	TX ERR2	TX REQ2	RTREN2	TX2PRI<1:0>		0000
C1TR45CON	0434	TXEN5	TX ABT5	TX LARB5	TX ERR5	TX REQ5	RTREN5	TX5PRI<1:0>		TXEN4	TX ABAT4	TX LARB4	TX ERR4	TX REQ4	RTREN4	TX4PRI<1:0>		0000
C1TR67CON	0436	TXEN7	TX ABT7	TX LARB7	TX ERR7	TX REQ7	RTREN7	TX7PRI<1:0>		TXEN6	TX ABAT6	TX LARB6	TX ERR6	TX REQ6	RTREN6	TX6PRI<1:0>		xxxx
C1RXD	0440	Recieved Data Word																xxxx
C1TXD	0442	Transmit Data Word																xxxx

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal for PinHigh devices.

TABLE 4-20: ECAN1 REGISTER MAP WHEN C1CTRL1.WIN = 1 FOR PIC24HJXXXGP506A/510A/610A DEVICES ONLY

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets	
	0400-041E	See definition when WIN = x																	
C1BUFPNT1	0420	F3BP<3:0>				F2BP<3:0>				F1BP<3:0>				F0BP<3:0>				0000	
C1BUFPNT2	0422	F7BP<3:0>				F6BP<3:0>				F5BP<3:0>				F4BP<3:0>				0000	
C1BUFPNT3	0424	F11BP<3:0>				F10BP<3:0>				F9BP<3:0>				F8BP<3:0>				0000	
C1BUFPNT4	0426	F15BP<3:0>				F14BP<3:0>				F13BP<3:0>				F12BP<3:0>				0000	
C1RXM0SID	0430	SID<10:3>								SID<2:0>			—	MIDE	—	EID<17:16>		xxxx	
C1RXM0EID	0432	EID<15:8>								EID<7:0>									xxxx
C1RXM1SID	0434	SID<10:3>								SID<2:0>			—	MIDE	—	EID<17:16>		xxxx	
C1RXM1EID	0436	EID<15:8>								EID<7:0>									xxxx
C1RXM2SID	0438	SID<10:3>								SID<2:0>			—	MIDE	—	EID<17:16>		xxxx	
C1RXM2EID	043A	EID<15:8>								EID<7:0>									xxxx
C1RXF0SID	0440	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx	
C1RXF0EID	0442	EID<15:8>								EID<7:0>									xxxx
C1RXF1SID	0444	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx	

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal for PinHigh devices.

TABLE 4-21: ECAN2 REGISTER MAP WHEN C2CTRL1.WIN = 0 OR 1 FOR PIC24HJ256GP610A DEVICES ONLY

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets	
C2CTRL1	0500	—	—	CSIDL	ABAT	—	REQOP<2:0>			OPMODE<2:0>			—	CANCAP	—	—	WIN	0480	
C2CTRL2	0502	—	—	—	—	—	—	—	—	—	—	—	DNCNT<4:0>					0000	
C2VEC	0504	—	—	—	FILHIT<4:0>					—	ICODE<6:0>							0000	
C2FCTRL	0506	DMABS<2:0>			—	—	—	—	—	—	—	—	FSA<4:0>					0000	
C2FIFO	0508	—	—	FBP<5:0>						—	—	FNRB<5:0>						0000	
C2INTF	050A	—	—	TXBO	TXBP	RXBP	TXWAR	RXWAR	EWARN	IVRIF	WAKIF	ERRIF	—	FIFOIF	RBOVIF	RBIF	TBIF	0000	
C2INTE	050C	—	—	—	—	—	—	—	—	IVRIE	WAKIE	ERRIE	—	FIFOIE	RBOVIE	RBIE	TBIE	0000	
C2EC	050E	TERRCNT<7:0>								RERRCNT<7:0>								0000	
C2CFG1	0510	—	—	—	—	—	—	—	—	SJW<1:0>		BRP<5:0>							0000
C2CFG2	0512	—	WAKFIL	—	—	—	SEG2PH<2:0>			SEG2PHTS	SAM	SEG1PH<2:0>			PRSEG<2:0>			0000	
C2FEN1	0514	FLTEN15	FLTEN14	FLTEN13	FLTEN12	FLTEN11	FLTEN10	FLTEN9	FLTEN8	FLTEN7	FLTEN6	FLTEN5	FLTEN4	FLTEN3	FLTEN2	FLTEN1	FLTEN0	FFFF	
C2FMSKSEL1	0518	F7MSK<1:0>			F6MSK<1:0>		F5MSK<1:0>		F4MSK<1:0>		F3MSK<1:0>		F2MSK<1:0>		F1MSK<1:0>		F0MSK<1:0>	0000	
C2FMSKSEL2	051A	F15MSK<1:0>			F14MSK<1:0>		F13MSK<1:0>		F12MSK<1:0>		F11MSK<1:0>		F10MSK<1:0>		F9MSK<1:0>		F8MSK<1:0>	0000	

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal for PinHigh devices.

TABLE 4-22: ECAN2 REGISTER MAP WHEN C2CTRL1.WIN = 0 FOR PIC24HJ256GP610A DEVICES ONLY

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
	0500-051E	See definition when WIN = x																
C2RXFUL1	0520	RXFUL15	RXFUL14	RXFUL13	RXFUL12	RXFUL11	RXFUL10	RXFUL9	RXFUL8	RXFUL7	RXFUL6	RXFUL5	RXFUL4	RXFUL3	RXFUL2	RXFUL1	RXFUL0	0000
C2RXFUL2	0522	RXFUL31	RXFUL30	RXFUL29	RXFUL28	RXFUL27	RXFUL26	RXFUL25	RXFUL24	RXFUL23	RXFUL22	RXFUL21	RXFUL20	RXFUL19	RXFUL18	RXFUL17	RXFUL16	0000
C2RXOVF1	0528	RXOVF15	RXOVF14	RXOVF13	RXOVF12	RXOVF11	RXOVF10	RXOVF09	RXOVF08	RXOVF7	RXOVF6	RXOVF5	RXOVF4	RXOVF3	RXOVF2	RXOVF1	RXOVF0	0000
C2RXOVF2	052A	RXOVF31	RXOVF30	RXOVF29	RXOVF28	RXOVF27	RXOVF26	RXOVF25	RXOVF24	RXOVF23	RXOVF22	RXOVF21	RXOVF20	RXOVF19	RXOVF18	RXOVF17	RXOVF16	0000
C2TR01CON	0530	TXEN1	TX ABAT1	TX LARB1	TX ERR1	TX REQ1	RTREN1	TX1PRI<1:0>		TXEN0	TX ABAT0	TX LARB0	TX ERR0	TX REQ0	RTREN0	TX0PRI<1:0>		0000
C2TR23CON	0532	TXEN3	TX ABAT3	TX LARB3	TX ERR3	TX REQ3	RTREN3	TX3PRI<1:0>		TXEN2	TX ABAT2	TX LARB2	TX ERR2	TX REQ2	RTREN2	TX2PRI<1:0>		0000
C2TR45CON	0534	TXEN5	TX ABAT5	TX LARB5	TX ERR5	TX REQ5	RTREN5	TX5PRI<1:0>		TXEN4	TX ABAT4	TX LARB4	TX ERR4	TX REQ4	RTREN4	TX4PRI<1:0>		0000
C2TR67CON	0536	TXEN7	TX ABAT7	TX LARB7	TX ERR7	TX REQ7	RTREN7	TX7PRI<1:0>		TXEN6	TX ABAT6	TX LARB6	TX ERR6	TX REQ6	RTREN6	TX6PRI<1:0>		xxxx
C2RXD	0540	Recieved Data Word																xxxx
C2TXD	0542	Transmit Data Word																xxxx

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal for PinHigh devices.

PIC24HJXXXGPX06A/X08A/X10A

7.0 INTERRUPT CONTROLLER

Note 1: This data sheet summarizes the features of the PIC24HJXXXGPX06A/X08A/X10A family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 6. “Interrupts”** (DS70184) of the “*dsPIC33F/PIC24H Family Reference Manual*”, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The PIC24HJXXXGPX06A/X08A/X10A interrupt controller reduces the numerous peripheral interrupt request signals to a single interrupt request signal to the PIC24HJXXXGPX06A/X08A/X10A CPU. It has the following features:

- Up to 8 processor exceptions and software traps
- 7 user-selectable priority levels
- Interrupt Vector Table (IVT) with up to 118 vectors
- A unique vector for each interrupt or exception source
- Fixed priority within a specified user priority level
- Alternate Interrupt Vector Table (AIVT) for debug support
- Fixed interrupt entry and return latencies

7.1 Interrupt Vector Table

The Interrupt Vector Table (IVT) is shown in Figure 7-1. The IVT resides in program memory, starting at location 000004h. The IVT contains 126 vectors consisting of 8 nonmaskable trap vectors plus up to 118 sources of interrupt. In general, each interrupt source has its own vector. Each interrupt vector contains a 24-bit wide address. The value programmed into each interrupt vector location is the starting address of the associated Interrupt Service Routine (ISR).

Interrupt vectors are prioritized in terms of their natural priority; this priority is linked to their position in the vector table. All other things being equal, lower addresses have a higher natural priority. For example, the interrupt associated with vector 0 will take priority over interrupts at any other vector address.

PIC24HJXXXGPX06A/X08A/X10A devices implement up to 61 unique interrupts and 5 nonmaskable traps. These are summarized in Table 7-1 and Table 7-2.

7.1.1 ALTERNATE VECTOR TABLE

The Alternate Interrupt Vector Table (AIVT) is located after the IVT, as shown in Figure 7-1. Access to the AIVT is provided by the ALTIVT control bit (INTCON2<15>). If the ALTIVT bit is set, all interrupt and exception processes use the alternate vectors instead of the default vectors. The alternate vectors are organized in the same manner as the default vectors.

The AIVT supports debugging by providing a means to switch between an application and a support environment without requiring the interrupt vectors to be reprogrammed. This feature also enables switching between applications for evaluation of different software algorithms at run time. If the AIVT is not needed, the AIVT should be programmed with the same addresses used in the IVT.

7.2 Reset Sequence

A device Reset is not a true exception because the interrupt controller is not involved in the Reset process. The PIC24HJXXXGPX06A/X08A/X10A device clears its registers in response to a Reset which forces the PC to zero. The digital signal controller then begins program execution at location 0x000000. The user programs a GOTO instruction at the Reset address which redirects program execution to the appropriate start-up routine.

Note: Any unimplemented or unused vector locations in the IVT and AIVT should be programmed with the address of a default interrupt handler routine that contains a RESET instruction.

PIC24HJXXXGPX06A/X08A/X10A

REGISTER 7-6: IFS1: INTERRUPT FLAG STATUS REGISTER 1 (CONTINUED)

bit 3	CNIF: Input Change Notification Interrupt Flag Status bit 1 = Interrupt request has occurred 0 = Interrupt request has not occurred
bit 2	Unimplemented: Read as '0'
bit 1	MI2C1IF: I2C1 Master Events Interrupt Flag Status bit 1 = Interrupt request has occurred 0 = Interrupt request has not occurred
bit 0	SI2C1IF: I2C1 Slave Events Interrupt Flag Status bit 1 = Interrupt request has occurred 0 = Interrupt request has not occurred

PIC24HJXXXGPX06A/X08A/X10A

REGISTER 7-32: IPC17: INTERRUPT PRIORITY CONTROL REGISTER 17

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	C2TXIP<2:0>			—	C1TXIP<2:0>		
bit 15				bit 8			

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	DMA7IP<2:0>			—	DMA6IP<2:0>		
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **C2TXIP<2:0>**: ECAN2 Transmit Data Request Interrupt Priority bits

111 = Interrupt is priority 7 (highest priority interrupt)

•
•
•

001 = Interrupt is priority 1

000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **C1TXIP<2:0>**: ECAN1 Transmit Data Request Interrupt Priority bits

111 = Interrupt is priority 7 (highest priority interrupt)

•
•
•

001 = Interrupt is priority 1

000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **DMA7IP<2:0>**: DMA Channel 7 Data Transfer Complete Interrupt Priority bits

111 = Interrupt is priority 7 (highest priority interrupt)

•
•
•

001 = Interrupt is priority 1

000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **DMA6IP<2:0>**: DMA Channel 6 Data Transfer Complete Interrupt Priority bits

111 = Interrupt is priority 7 (highest priority interrupt)

•
•
•

001 = Interrupt is priority 1

000 = Interrupt source is disabled

PIC24HJXXXGPX06A/X08A/X10A

REGISTER 8-2: DMAxREQ: DMA CHANNEL x IRQ SELECT REGISTER

R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
FORCE ⁽¹⁾	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	IRQSEL6 ⁽²⁾	IRQSEL5 ⁽²⁾	IRQSEL4 ⁽²⁾	IRQSEL3 ⁽²⁾	IRQSEL2 ⁽²⁾	IRQSEL1 ⁽²⁾	IRQSEL0 ⁽²⁾
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **FORCE:** Force DMA Transfer bit⁽¹⁾

1 = Force a single DMA transfer (Manual mode)

0 = Automatic DMA transfer initiation by DMA request

bit 14-7 **Unimplemented:** Read as '0'

bit 6-0 **IRQSEL<6:0>:** DMA Peripheral IRQ Number Select bits⁽²⁾

0000000-1111111 = DMAIRQ0-DMAIRQ127 selected to be Channel DMAREQ

Note 1: The FORCE bit cannot be cleared by the user. The FORCE bit is cleared by hardware when the forced DMA transfer is complete.

2: Please see Table 8-1 for a complete listing of IRQ numbers for all interrupt sources.

PIC24HJXXXGPX06A/X08A/X10A

NOTES:

PIC24HJXXXGPX06A/X08A/X10A

REGISTER 10-2: PMD2: PERIPHERAL MODULE DISABLE CONTROL REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IC8MD	IC7MD	IC6MD	IC5MD	IC4MD	IC3MD	IC2MD	IC1MD
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OC8MD	OC7MD	OC6MD	OC5MD	OC4MD	OC3MD	OC2MD	OC1MD
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15 **IC8MD:** Input Capture 8 Module Disable bit
 1 = Input Capture 8 module is disabled
 0 = Input Capture 8 module is enabled
- bit 14 **IC7MD:** Input Capture 7 Module Disable bit
 1 = Input Capture 7 module is disabled
 0 = Input Capture 7 module is enabled
- bit 13 **IC6MD:** Input Capture 6 Module Disable bit
 1 = Input Capture 6 module is disabled
 0 = Input Capture 6 module is enabled
- bit 12 **IC5MD:** Input Capture 5 Module Disable bit
 1 = Input Capture 5 module is disabled
 0 = Input Capture 5 module is enabled
- bit 11 **IC4MD:** Input Capture 4 Module Disable bit
 1 = Input Capture 4 module is disabled
 0 = Input Capture 4 module is enabled
- bit 10 **IC3MD:** Input Capture 3 Module Disable bit
 1 = Input Capture 3 module is disabled
 0 = Input Capture 3 module is enabled
- bit 9 **IC2MD:** Input Capture 2 Module Disable bit
 1 = Input Capture 2 module is disabled
 0 = Input Capture 2 module is enabled
- bit 8 **IC1MD:** Input Capture 1 Module Disable bit
 1 = Input Capture 1 module is disabled
 0 = Input Capture 1 module is enabled
- bit 7 **OC8MD:** Output Compare 8 Module Disable bit
 1 = Output Compare 8 module is disabled
 0 = Output Compare 8 module is enabled
- bit 6 **OC7MD:** Output Compare 4 Module Disable bit
 1 = Output Compare 7 module is disabled
 0 = Output Compare 7 module is enabled
- bit 5 **OC6MD:** Output Compare 6 Module Disable bit
 1 = Output Compare 6 module is disabled
 0 = Output Compare 6 module is enabled
- bit 4 **OC5MD:** Output Compare 5 Module Disable bit
 1 = Output Compare 5 module is disabled
 0 = Output Compare 5 module is enabled

PIC24HJXXXGPX06A/X08A/X10A

11.2 Open-Drain Configuration

In addition to the PORT, LAT and TRIS registers for data control, some port pins can also be individually configured for either digital or open-drain output. This is controlled by the Open-Drain Control register, ODCx, associated with each port. Setting any of the bits configures the corresponding pin to act as an open-drain output.

The open-drain feature allows the generation of outputs higher than VDD (e.g., 5V) on any desired 5V tolerant pins by using external pull-up resistors. The maximum open-drain voltage allowed is the same as the maximum VIH specification.

See the “Pin Diagrams” section for the available pins and their functionality.

11.3 Configuring Analog Port Pins

The use of the ADxPCFGH, ADxPCFGL and TRIS registers control the operation of the Analog-to-Digital port pins. The port pins that are desired as analog inputs must have their corresponding TRIS bit set (input). If the TRIS bit is cleared (output), the digital output level (VOH or VOL) is converted.

Clearing any bit in the ADxPCFGH or ADxPCFGL register configures the corresponding bit to be an analog pin. This is also the Reset state of any I/O pin that has an analog (ANx) function associated with it.

Note: In devices with two ADC modules, if the corresponding PCFG bit in either AD1PCFGH(L) and AD2PCFGH(L) is cleared, the pin is configured as an analog input.

When reading the PORT register, all pins configured as analog input channels will read as cleared (a low level).

Pins configured as digital inputs will not convert an analog input. Analog levels on any pin that is defined as a digital input (including the ANx pins) can cause the input buffer to consume current that exceeds the device specifications.

Note: The voltage on an analog input pin can be between -0.3V to (VDD + 0.3 V).

11.4 I/O Port Write/Read Timing

One instruction cycle is required between a port direction change or port write operation and a read operation of the same port. Typically, this instruction would be a NOP.

11.5 Input Change Notification

The input change notification function of the I/O ports allows the PIC24HJXXXGPX06A/X08A/X10A devices to generate interrupt requests to the processor in response to a change-of-state on selected input pins. This feature is capable of detecting input change-of-states even in Sleep mode, when the clocks are disabled. Depending on the device pin count, there are up to 24 external signals (CN0 through CN23) that can be selected (enabled) for generating an interrupt request on a change-of-state.

There are four control registers associated with the CN module. The CNEN1 and CNEN2 registers contain the CN interrupt enable (CNxIE) control bits for each of the CN input pins. Setting any of these bits enables a CN interrupt for the corresponding pins.

Each CN pin also has a weak pull-up connected to it. The pull-ups act as a current source that is connected to the pin and eliminate the need for external resistors when push button or keypad devices are connected. The pull-ups are enabled separately using the CNPU1 and CNPU2 registers, which contain the weak pull-up enable (CNxPUE) bits for each of the CN pins. Setting any of the control bits enables the weak pull-ups for the corresponding pins.

Note: Pull-ups on change notification pins should always be disabled whenever the port pin is configured as a digital output.

EXAMPLE 11-1: PORT WRITE/READ EXAMPLE

```
MOV    0xFF00, W0          ; Configure PORTB<15:8> as inputs
MOV    W0, TRISBB          ; and PORTB<7:0> as outputs
NOP                      ; Delay 1 cycle
btss   PORTB, #13          ; Next Instruction
```

PIC24HJXXXGPX06A/X08A/X10A

REGISTER 13-1: TxCON (T2CON, T4CON, T6CON OR T8CON) CONTROL REGISTER

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
TON	—	TSIDL	—	—	—	—	—
bit 15						bit 8	

U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0
—	TGATE	TCKPS<1:0>		T32	—	TCS ⁽¹⁾	—
bit 7					bit 0		

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **TON:** Timerx On bit

When T32 = 1:

1 = Starts 32-bit Timerx/y

0 = Stops 32-bit Timerx/y

When T32 = 0:

1 = Starts 16-bit Timerx

0 = Stops 16-bit Timerx

bit 14 **Unimplemented:** Read as '0'

bit 13 **TSIDL:** Stop in Idle Mode bit

1 = Discontinue module operation when device enters Idle mode

0 = Continue module operation in Idle mode

bit 12-7 **Unimplemented:** Read as '0'

bit 6 **TGATE:** Timerx Gated Time Accumulation Enable bit

When TCS = 1:

This bit is ignored.

When TCS = 0:

1 = Gated time accumulation enabled

0 = Gated time accumulation disabled

bit 5-4 **TCKPS<1:0>:** Timerx Input Clock Prescale Select bits

11 = 1:256

10 = 1:64

01 = 1:8

00 = 1:1

bit 3 **T32:** 32-bit Timer Mode Select bit

1 = Timerx and Timery form a single 32-bit timer

0 = Timerx and Timery act as two 16-bit timers

bit 2 **Unimplemented:** Read as '0'

bit 1 **TCS:** Timerx Clock Source Select bit⁽¹⁾

1 = External clock from pin TxCK (on the rising edge)

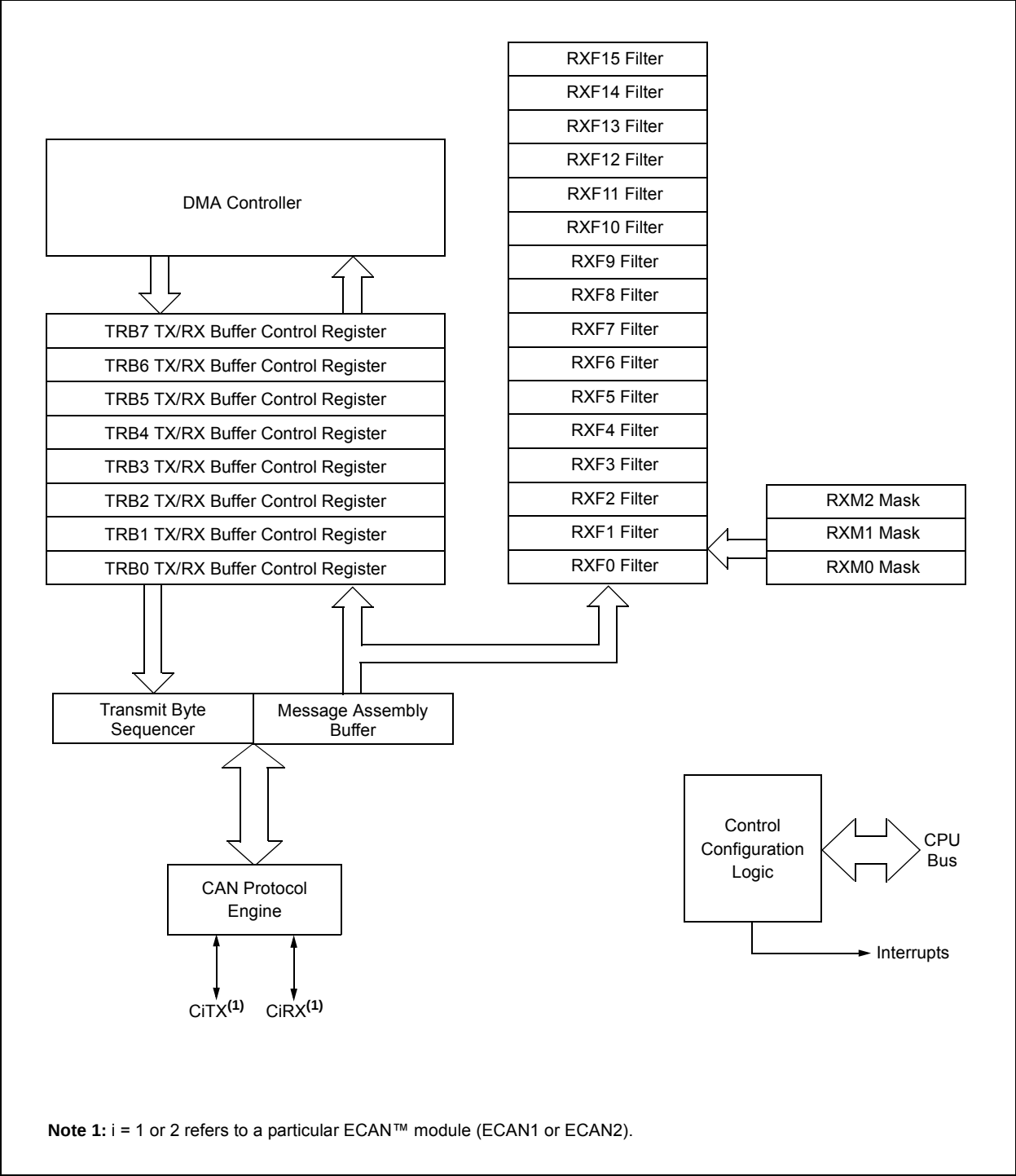
0 = Internal clock (Fcy)

bit 0 **Unimplemented:** Read as '0'

Note 1: The TxCK pin is not available on all timers. Refer to the “Pin Diagrams” section for the available pins.

PIC24HJXXXGPX06A/X08A/X10A

FIGURE 19-1: ECAN™ MODULE BLOCK DIAGRAM



PIC24HJXXXGPX06A/X08A/X10A

REGISTER 19-6: CILNTF: ECAN™ MODULE INTERRUPT FLAG REGISTER

U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
—	—	TXBO	TXBP	RXBP	TXWAR	RXWAR	EWARN
bit 15							
							bit 8

R/C-0	R/C-0	R/C-0	U-0	R/C-0	R/C-0	R/C-0	R/C-0
IVRIF	WAKIF	ERRIF	—	FIFOIF	RBOVIF	RBIF	TBIF
bit 7							
							bit 0

Legend:	C = Clear only bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 15-14	Unimplemented: Read as '0'
bit 13	TXBO: Transmitter in Error State Bus Off bit 1 = Transmitter is in Bus Off state 0 = Transmitter is not in Bus Off state
bit 12	TXBP: Transmitter in Error State Bus Passive bit 1 = Transmitter is in Bus Passive state 0 = Transmitter is not in Bus Passive state
bit 11	RXBP: Receiver in Error State Bus Passive bit 1 = Receiver is in Bus Passive state 0 = Receiver is not in Bus Passive state
bit 10	TXWAR: Transmitter in Error State Warning bit 1 = Transmitter is in Error Warning state 0 = Transmitter is not in Error Warning state
bit 9	RXWAR: Receiver in Error State Warning bit 1 = Receiver is in Error Warning state 0 = Receiver is not in Error Warning state
bit 8	EWARN: Transmitter or Receiver in Error State Warning bit 1 = Transmitter or receiver is in Error Warning state 0 = Transmitter or receiver is not in Error Warning state
bit 7	IVRIF: Invalid Message Received Interrupt Flag bit 1 = Interrupt request has occurred 0 = Interrupt request has not occurred
bit 6	WAKIF: Bus Wake-up Activity Interrupt Flag bit 1 = Interrupt request has occurred 0 = Interrupt request has not occurred
bit 5	ERRIF: Error Interrupt Flag bit (multiple sources in CILNTF<13:8> register) 1 = Interrupt request has occurred 0 = Interrupt request has not occurred
bit 4	Unimplemented: Read as '0'
bit 3	FIFOIF: FIFO Almost Full Interrupt Flag bit 1 = Interrupt request has occurred 0 = Interrupt request has not occurred
bit 2	RBOVIF: RX Buffer Overflow Interrupt Flag bit 1 = Interrupt request has occurred 0 = Interrupt request has not occurred
bit 1	RBIF: RX Buffer Interrupt Flag bit 1 = Interrupt request has occurred 0 = Interrupt request has not occurred
bit 0	TBIF: TX Buffer Interrupt Flag bit 1 = Interrupt request has occurred 0 = Interrupt request has not occurred

PIC24HJXXXGPX06A/X08A/X10A

REGISTER 19-20: CiRXMnSID: ECAN™ MODULE ACCEPTANCE FILTER MASK n STANDARD IDENTIFIER

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
SID<10:3>							
bit 15				bit 8			

R/W-x	R/W-x	R/W-x	U-0	R/W-x	U-0	R/W-x	R/W-x
SID<2:0>			—	MIDE	—	EID<17:16>	
bit 7			bit 0				

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15-5 **SID<10:0>**: Standard Identifier bits
 1 = Include bit SIDx in filter comparison
 0 = Bit SIDx is don't care in filter comparison
- bit 4 **Unimplemented**: Read as '0'
- bit 3 **MIDE**: Identifier Receive Mode bit
 1 = Match only message types (standard or extended address) that correspond to EXIDE bit in filter
 0 = Match either standard or extended address message if filters match
 (i.e., if (Filter SID) = (Message SID) or if (Filter SID/EID) = (Message SID/EID))
- bit 2 **Unimplemented**: Read as '0'
- bit 1-0 **EID<17:16>**: Extended Identifier bits
 1 = Include bit EIDx in filter comparison
 0 = Bit EIDx is don't care in filter comparison

REGISTER 19-21: CiRXMnEID: ECAN™ TECHNOLOGY ACCEPTANCE FILTER MASK n EXTENDED IDENTIFIER

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID<15:8>							
bit 15				bit 8			

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15-0 **EID<15:0>**: Extended Identifier bits
 1 = Include bit EIDx in filter comparison
 0 = Bit EIDx is don't care in filter comparison

PIC24HJXXXGPX06A/X08A/X10A

TABLE 21-2: CONFIGURATION BITS DESCRIPTION

Bit Field	Register	RTSP Effect	Description
BWRP	FBS	Immediate	Boot Segment Program Flash Write Protection 1 = Boot segment may be written 0 = Boot segment is write-protected
BSS<2:0>	FBS	Immediate	Boot Segment Program Flash Code Protection Size X11 = No Boot program Flash segment Boot space is 1K IW less VS 110 = Standard security; boot program Flash segment starts at End of VS, ends at 0x0007FE 010 = High security; boot program Flash segment starts at End of VS, ends at 0x0007FE Boot space is 4K IW less VS 101 = Standard security; boot program Flash segment starts at End of VS, ends at 0x001FFE 001 = High security; boot program Flash segment starts at End of VS, ends at 0x001FFE Boot space is 8K IW less VS 100 = Standard security; boot program Flash segment starts at End of VS, ends at 0x003FFE 000 = High security; boot program Flash segment starts at End of VS, ends at 0x003FFE
RBS<1:0>	FBS	Immediate	Boot Segment RAM Code Protection 11 = No Boot RAM defined 10 = Boot RAM is 128 Bytes 01 = Boot RAM is 256 Bytes 00 = Boot RAM is 1024 Bytes
SWRP	FSS	Immediate	Secure Segment Program Flash Write Protection 1 = Secure segment may be written 0 = Secure segment is write-protected

PIC24HJXXXGPX06A/X08A/X10A

TABLE 21-2: CONFIGURATION BITS DESCRIPTION (CONTINUED)

Bit Field	Register	RTSP Effect	Description
IESO	FOSCSEL	Immediate	Internal External Start-up Option bit 1 = Start-up device with FRC, then automatically switch to the user-selected oscillator source when ready 0 = Start-up device with user-selected oscillator source
FNOSC<2:0>	FOSCSEL	If clock switch is enabled, RTSP effect is on any device Reset; otherwise, Immediate	Initial Oscillator Source Selection bits 111 = Internal Fast RC (FRC) oscillator with postscaler 110 = Reserved 101 = LPRC oscillator 100 = Secondary (LP) oscillator 011 = Primary (XT, HS, EC) oscillator with PLL 010 = Primary (XT, HS, EC) oscillator 001 = Internal Fast RC (FRC) oscillator with PLL 000 = FRC oscillator
FCKSM<1:0>	FOSC	Immediate	Clock Switching Mode bits 1x = Clock switching is disabled, Fail-Safe Clock Monitor is disabled 01 = Clock switching is enabled, Fail-Safe Clock Monitor is disabled 00 = Clock switching is enabled, Fail-Safe Clock Monitor is enabled
OSCIOFNC	FOSC	Immediate	OSC2 Pin Function bit (except in XT and HS modes) 1 = OSC2 is clock output 0 = OSC2 is general purpose digital I/O pin
POSCMD<1:0>	FOSC	Immediate	Primary Oscillator Mode Select bits 11 = Primary oscillator disabled 10 = HS Crystal Oscillator mode 01 = XT Crystal Oscillator mode 00 = EC (External Clock) mode
FWDTEN	FWDT	Immediate	Watchdog Timer Enable bit 1 = Watchdog Timer always enabled (LPRC oscillator cannot be disabled. Clearing the SWDTEN bit in the RCON register will have no effect.) 0 = Watchdog Timer enabled/disabled by user software (LPRC can be disabled by clearing the SWDTEN bit in the RCON register)
WINDIS	FWDT	Immediate	Watchdog Timer Window Enable bit 1 = Watchdog Timer in Non-Window mode 0 = Watchdog Timer in Window mode
PLLKEN	FWDT	Immediate	PLL Lock Enable bit 1 = Clock switch to PLL source will wait until the PLL lock signal is valid. 0 = Clock switch will not wait for the PLL lock signal.
WDTPRE	FWDT	Immediate	Watchdog Timer Prescaler bit 1 = 1:128 0 = 1:32
WDTPOST	FWDT	Immediate	Watchdog Timer Postscaler bits 1111 = 1:32,768 1110 = 1:16,384 • • • 0001 = 1:2 0000 = 1:1

PIC24HJXXXGPX06A/X08A/X10A

TABLE 25-12: SPIx MODULE SLAVE MODE (CKE = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$ for High Temperature					
Param No.	Symbol	Characteristic ⁽¹⁾	Min	Typ	Max	Units	Conditions
HSP35	Tsch2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	—	35	ns	—
HSP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	25	—	—	ns	—
HSP41	Tsch2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	25	—	—	ns	—
HSP51	TssH2doZ	$\overline{\text{SSx}}$ $\uparrow$ to SDOx Output High-Impedance	15	—	55	ns	See Note 2

Note 1: These parameters are characterized but not tested in manufacturing.

2: Assumes 50 pF load on all SPIx pins.

TABLE 25-13: SPIx MODULE SLAVE MODE (CKE = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$ for High Temperature					
Param No.	Symbol	Characteristic ⁽¹⁾	Min	Typ	Max	Units	Conditions
HSP35	Tsch2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	—	35	ns	—
HSP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	25	—	—	ns	—
HSP41	Tsch2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	25	—	—	ns	—
HSP51	TssH2doZ	$\overline{\text{SSx}}$ $\uparrow$ to SDOx Output High-Impedance	15	—	55	ns	See Note 2
HSP60	TssL2doV	SDOx Data Output Valid after $\overline{\text{SSx}}$ Edge	—	—	55	ns	—

Note 1: These parameters are characterized but not tested in manufacturing.

2: Assumes 50 pF load on all SPIx pins.

PIC24HJXXXGPX06A/X08A/X10A

F

Flash Program Memory	59
Control Registers	60
Operations	60
Programming Algorithm	62
RTSP Operation	60
Table Instructions	59
Flexible Configuration	221
FSCM	
Delay for Crystal and PLL Clock Sources	68
Device Resets	68

H

High Temperature Electrical Characteristics	287
---	-----

I

I/O Ports	141
Parallel I/O (PIO)	141
Write/Read Timing	142
I ² C	
Operating Modes	165
Registers	167
I ² C Module	
I2C1 Register Map	40
I2C2 Register Map	40
In-Circuit Debugger	228
In-Circuit Emulation	221
In-Circuit Serial Programming (ICSP)	221, 228
Input Capture	
Registers	154
Input Change Notification Module	142
Instruction Addressing Modes	53
File Register Instructions	53
Fundamental Modes Supported	54
MCU Instructions	53
Move and Accumulator Instructions	54
Other Instructions	54
Instruction Set	
Overview	231
Summary	229
Instruction-Based Power-Saving Modes	133
Idle	134
Sleep	133
Internal RC Oscillator	
Use with WDT	227
Internet Address	321
Interrupt Control and Status Registers	73
IECx	73
IFSx	73
INTCON1	73
INTCON2	73
INTTREG	73
IPCx	73
Interrupt Setup Procedures	111
Initialization	111
Interrupt Disable	111
Interrupt Service Routine	111
Trap Service Routine	111
Interrupt Vector Table (IVT)	69
Interrupts Coincident with Power Save Instructions	134

J

JTAG Boundary Scan Interface	221
------------------------------------	-----

M

Memory Organization	29
Microchip Internet Web Site	321
Modes of Operation	
Disable	181
Initialization	181
Listen All Messages	181
Listen Only	181
Loopback	181
Normal Operation	181
MPLAB ASM30 Assembler, Linker, Librarian	238
MPLAB Integrated Development	
Environment Software	237
MPLAB PM3 Device Programmer	240
MPLAB REAL ICE In-Circuit Emulator System	239
MPLINK Object Linker/MPLIB Object Librarian	238
Multi-Bit Data Shifter	28

N

NVM Module	
Register Map	52

O

Open-Drain Configuration	142
Output Compare	155

P

Packaging	301
Details	304
Marking	301
Peripheral Module Disable (PMD)	134
Pinout I/O Descriptions (table)	17
PMD Module	
Register Map	52
POR and Long Oscillator Start-up Times	68
PORTA	
Register Map	50
PORTB	
Register Map	50
PORTC	
Register Map	50
PORTD	
Register Map	50
PORTE	
Register Map	51
PORTF	
Register Map	51
PORTG	
Register Map	51
Power-Saving Features	133
Clock Frequency and Switching	133
Program Address Space	29
Construction	55
Data Access from Program Memory Using	
Program Space Visibility	58
Data Access from Program Memory	
Using Table Instructions	57
Data Access from, Address Generation	56
Memory Map	29
Table Read Instructions	
TBLRDH	57
TBLRDL	57
Visibility Operation	58
Program Memory	
Interrupt Vector	30
Organization	30
Reset Vector	30