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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	40 MIPs
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	85
Program Memory Size	64KB (22K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 32x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24hj64gp210a-i-pt

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

SCK1 I/O ST Synchronous serial clock input/output for SP11. SD11 I ST SP11 data in. SD01 O — SP11 data out. SST I/O ST SP11 data out. SCK2 I/O ST SP11 salve synchronization or frame pulse I/O. SD12 I ST SP12 data out. SD2 O — SP12 data out. SS2 I/O ST Synchronous serial clock input/output for I2C1. SCL1 I/O ST Synchronous serial data input/output for I2C2. SDA1 I/O ST Synchronous serial data input/output for I2C2. SDA2 I/O ST Synchronous serial data input/output for I2C2. SOSCI I ST/CMOS 32.768 Hz low-power oscillator crystal output. TMS I ST JTAG test clock input. TCK I ST Timer1 external clock input. TCK I ST Timer2 external clock input. TCK I ST Timer3 external clock input. TCK I ST Timer4 exte	Pin Name	Pin Type	Buffer Type	Description
SDI1 I ST SPI1 data out. SS1 I/O ST SPI1 data out. SCK2 I/O ST SPI1 slave synchronization or frame pulse I/O. SD02 O - SPI2 data in. SD02 O - SPI2 data out. SD2 O - SPI2 data out. SS2 I/O ST Synchronous serial clock input/output for I2C1. SCL1 I/O ST Synchronous serial data input/output for I2C2. SDA2 I/O ST Synchronous serial data input/output for I2C2. SDA2 I/O ST Synchronous serial data input/output for I2C2. SDA2 I/O ST Synchronous serial data input/output for I2C2. SOSCI I ST(CMOS 32.768 kHz low-power oscillator crystal input; CMOS otherwise. SOSCO O - 32.768 kHz low-power oscillator crystal output. TMS I ST JTAG test clock input pin. TDI I ST JTAG test clock input. TCK I ST Timer1 external clock input. T2CK I ST Timer2 external clock input. T2CK I ST Timer3 external clock input. T3CK I	SCK1	I/O	ST	Synchronous serial clock input/output for SPI1.
SDO1 0	SDI1	I	ST	SPI1 data in.
SST I/O ST SPI1 slave synchronization or frame pulse I/O. SCK2 I/O ST Synchronous serial clock input/output for SPI2. SD2 O - SPI2 data in. SD2 O - SPI2 data out. SS2 I/O ST Synchronous serial clock input/output for I2C1. SDA1 I/O ST Synchronous serial clock input/output for I2C2. SDA2 I/O ST Synchronous serial clock input/output for I2C2. SDA2 I/O ST Synchronous serial clock input/output for I2C2. SDA2 I/O ST Synchronous serial clock input/output for I2C2. SOSCI I STICMOS 32.768 kHz low-power oscillator crystal input; CMOS otherwise. SOSCO O - 32.768 kHz low-power oscillator crystal output. TMS I ST JTAG test clock input pin. TDI I ST JTAG test clock input pin. TDI I ST Timer external clock input. T2CK I ST Timere external clock input. T3CK I ST Timere external clock input. T4CK I ST Timere external clock input. T6CK I ST Timere external	SDO1	0	_	SPI1 data out.
SCK2 I/O ST Synchronous serial clock input/output for SPI2. SDI2 I ST SPI2 data out. SDO2 O	SS1	I/O	ST	SPI1 slave synchronization or frame pulse I/O.
SD12 I ST SP12 data in. SD02 O SP12 data out. SS2 I/O ST SP12 slave synchronization or frame pulse I/O. SCL1 I/O ST Synchronous serial clock input/output for I2C1. SDA1 I/O ST Synchronous serial clock input/output for I2C1. SDA2 I/O ST Synchronous serial clock input/output for I2C2. SDA2 I/O ST Synchronous serial clock input/output for I2C2. SOSCO O 32.768 kHz low-power oscillator crystal input; CMOS otherwise. SOSCO O 32.768 kHz low-power oscillator crystal output. TMS I ST JTAG test clock input pin. TCK I ST JTAG test data input pin. TDD I ST Timer1 external clock input. T2CK I ST Timer2 external clock input. T3CK I ST Timer3 external clock input. T4CK I ST Timer4 external clock input. T5CK I ST Timer6 external clock input. T6CK I ST Timer6 external clock input. T6CK I ST Timer6 external clock input.	SCK2	I/O	ST	Synchronous serial clock input/output for SPI2.
SDD2 SS20 I/OSPI2 data out. SPI2 slave synchronization or frame pulse I/O.SCL1I/OSTSynchronous serial clock input/output for I2C1. SCL2SDA1I/OSTSynchronous serial data input/output for I2C2.SDA2I/OSTSynchronous serial data input/output for I2C2.SDA2I/OSTSynchronous serial data input/output for I2C2.SOSCIIST/CMOSS2.768 kHz low-power oscillator crystal input. CMOS otherwise.SOSCOO32.768 kHz low-power oscillator crystal output.TMSISTJTAG Test mode select pin.TDIISTJTAG Test mode select pin.TDOOJTAG test data input pin.TDOOJTAG test data output pin.TCKISTTimer1 external clock input.TXCKISTTimer1 external clock input.TACKISTTimer3 external clock input.TACKISTTimer4 external clock input.TACKISTTimer6 external clock input.TACK <t< td=""><td>SDI2</td><td>I</td><td>ST</td><td>SPI2 data in.</td></t<>	SDI2	I	ST	SPI2 data in.
SS2 I/O ST SPI2 slave synchronization or frame pulse I/O. SCL1 I/O ST Synchronous serial clock input/output for 12C1. SDA1 I/O ST Synchronous serial data input/output for 12C1. SDA2 I/O ST Synchronous serial data input/output for 12C2. SOSCI I ST/CMOS 32.768 kHz low-power oscillator crystal input; CMOS otherwise. SOSCO O - 32.768 kHz low-power oscillator crystal output. TMS I ST JTAG Test mode select pin. TCK I ST JTAG test data input pin. TDI I ST Time1 external clock input. T2CK I ST Timer1 external clock input. T3CK I ST Timer2 external clock input. T1CK I ST Timer2 external clock input. T3CK I ST Timer4 external clock input. T4CK I ST Timer4 external clock input. T6CK I ST Timer6 external clock input. T6CK I ST Timer6 external clock input. T6CK I ST Timer7 external clock input. T7CK I ST Timer6 external clock input.	SDO2	0	_	SPI2 data out.
SCL1 I/O ST Synchronous serial clock input/output for I2C1. SDA1 I/O ST Synchronous serial data input/output for I2C1. SCL2 I/O ST Synchronous serial clock input/output for I2C2. SDA2 I/O ST Synchronous serial clock input/output for I2C2. SOSCI I ST/CMOS 32.768 kHz low-power oscillator crystal input; CMOS otherwise. SOSCO O - 32.768 kHz low-power oscillator crystal output. TMS I ST JTAG test data input pin. TDI I ST JTAG test data input pin. TDO O - JTAG test data output pin. TICK I ST Timer1 external clock input. T2CK I ST Timer2 external clock input. T3CK I ST Timer3 external clock input. T3CK I ST Timer6 external clock input. T6CK I ST Timer6 external clock input. T8CK I ST Timer6 external clock input.	SS2	I/O	ST	SPI2 slave synchronization or frame pulse I/O.
SDA1I/OSTSynchronous serial data input/output for I2C1.SCL2I/OSTSynchronous serial data input/output for I2C2.SDA2I/OSTSynchronous serial data input/output for I2C2.SOSCIIST/CMOS32.768 kHz low-power oscillator crystal input; CMOS otherwise.SOSCOO32.768 kHz low-power oscillator crystal output.TMSISTJTAG test mode select pin.TCKISTJTAG test dock input pin.TDIISTJTAG test data output pin.TDOOJTAG test data output pin.TCKISTTimer1 external clock input.T3CKISTTimer2 external clock input.T3CKISTTimer3 external clock input.T4CKISTTimer6 external clock input.T6CKISTTimer6 external clock input.T6CKISTTimer6 external clock input.T7CKISTTimer9 external clock input.T8CKISTTimer9 external clock input.T9CKISTUART1 clear to send.U1RTSOUART1 ready to send.U1RXISTUART2 receive.U2RTSOUART2 receive.U2RTXOUART2 receive.U2RTXOCPU logic filter capacitor connection.VssPCPU logic filter capacitor connection.VssPGround	SCL1	I/O	ST	Synchronous serial clock input/output for I2C1.
SCL2 I/O ST Synchronous serial clock input/output for I2C2. SDA2 I/O ST Synchronous serial data input/output for I2C2. SOSCI I ST/CMOS 32.768 kHz low-power oscillator crystal input; CMOS otherwise. SOSCO 0 - 32.768 kHz low-power oscillator crystal output. TMS I ST JTAG test dock input pin. TDI I ST JTAG test data input pin. TDO 0 - JTAG test data output pin. TCK I ST Timer1 external clock input. T2CK I ST Timer2 external clock input. T3CK I ST Timer3 external clock input. T3CK I ST Timer4 external clock input. T5CK I ST Timer6 external clock input. T6CK I ST Timer6 external clock input. T7CK I ST Timer6 external clock input. T6CK I ST Timer6 external clock input. T7CK I ST Timer6 external clock input. T0CTS I ST	SDA1	I/O	ST	Synchronous serial data input/output for I2C1.
SDA2 I/O ST Synchronous serial data input/output for I2C2. SOSCI I ST/CMOS 32.768 KHz low-power oscillator crystal input; CMOS otherwise. SOSCO O 32.768 kHz low-power oscillator crystal output. TMS I ST JTAG Test mode select pin. TCK I ST JTAG test data input pin. TDI I ST JTAG test data output pin. TDO O JTAG test data output pin. TCK I ST Timer1 external clock input. TZCK I ST Timer2 external clock input. T3CK I ST Timer3 external clock input. T4CK I ST Timer6 external clock input. T6CK I ST Timer6 external clock input. T6CK I ST Timer6 external clock input. T7CK I ST Timer6 external clock input. T6CK I ST Timer6 external clock input. T0KK I ST Timer6 external clock input. U1RTS O	SCL2	I/O	ST	Synchronous serial clock input/output for I2C2.
SOSCI I ST/CMOS 32.768 kHz low-power oscillator crystal input; CMOS otherwise. SOSCO O - 32.768 kHz low-power oscillator crystal output. TMS I ST JTAG Test mode select pin. TCK I ST JTAG test clock input pin. TDI I ST JTAG test data input pin. TDO O - JTAG test data output pin. TICK I ST Timer external clock input. TZCK I ST Timer1 external clock input. TAG test data output pin. Timer3 external clock input. Timer3 external clock input. TAGK I ST Timer3 external clock input. TSCK I ST Timer6 external clock input. TSCK I ST Timer6 external clock input. TSCK I ST Timer9 external clock input. TGK I ST Timer9 external clock input. TGK I ST Timer9 external clock input. TGK I ST Timer9 external clock input. TGKK I ST U	SDA2	I/O	ST	Synchronous serial data input/output for I2C2.
SOSCOO—32.768 kHz low-power oscillator crystal output.TMSISTJTAG Test mode select pin.TCKISTJTAG test data input pin.TDIISTJTAG test data input pin.TDOO—JTAG test data input pin.T1CKISTTimer1 external clock input.T2CKISTTimer2 external clock input.T3CKISTTimer3 external clock input.T4CKISTTimer4 external clock input.T5CKISTTimer6 external clock input.T6CKISTTimer6 external clock input.T6CKISTTimer6 external clock input.T7CKISTTimer6 external clock input.T8CKISTTimer6 external clock input.T8CKISTTimer6 external clock input.T9CKISTTimer9 external clock input.UICTSISTUART1 clear to send.U1RXISTUART1 receive.U1RXISTUART1 receive.U2CTSISTUART2 ready to send.U2RXISTUART2 receive.U2RXISTUART2 receive.U2RXISTUART2 receive.U2RXISTUART2 receive.U2RXISTGround reference for logic and I/O pins.VcAPP—Ground reference for logic and I/O pins.VREF+I <t< td=""><td>SOSCI</td><td>I</td><td>ST/CMOS</td><td>32.768 kHz low-power oscillator crystal input; CMOS otherwise.</td></t<>	SOSCI	I	ST/CMOS	32.768 kHz low-power oscillator crystal input; CMOS otherwise.
TMSISTJTAG Test mode select pin.TCKISTJTAG test clock input pin.TDIISTJTAG test data output pin.TDOO-JTAG test data output pin.T1CKISTTimer1 external clock input.T2CKISTTimer2 external clock input.T3CKISTTimer3 external clock input.T4CKISTTimer6 external clock input.T5CKISTTimer6 external clock input.T6CKISTTimer6 external clock input.T6CKISTTimer6 external clock input.T7CKISTTimer6 external clock input.T8CKISTTimer6 external clock input.T7CKISTTimer7 external clock input.T9CKISTTimer9 external clock input.UICTSISTUART1 clear to send.U1RXISTUART1 receive.U1RXISTUART1 receive.U2CTSISTUART2 ready to send.U2RXISTUART2 receive.U2RXISTUART2 receive.U2RXISTUART2 receive.U2RXISTUART2 receive.U2RXP—CPU logic filter capacitor connection.VssP—Ground reference for logic and I/O pins.VCAPP—Ground reference for logic and I/O pins.VREF+IAnalog<	SOSCO	0	—	32.768 kHz low-power oscillator crystal output.
TCKISTJTAG test clock input pin.TDIISTJTAG test data input pin.TDOO-JTAG test data output pin.T1CKISTTimer1 external clock input.T2CKISTTimer2 external clock input.T3CKISTTimer3 external clock input.T4CKISTTimer6 external clock input.T6CKISTTimer6 external clock input.T6CKISTTimer6 external clock input.T6CKISTTimer6 external clock input.T7CKISTTimer7 external clock input.T8CKISTTimer9 external clock input.T9CKISTTimer9 external clock input.UICTSISTUART1 clear to send.U1RTSO-UART1 ready to send.U1RXISTUART2 receive.U2RTSO-UART2 receive.U2RTSO-UART2 receive.U2TXO-UART2 transmit.VDDP-Positive supply for peripheral logic and I/O pins.VCAPP-CPU logic filter capacitor connection.VssP-Ground reference for logic and I/O pins.VREF+IAnalogAnalog voltage reference (low) input.	TMS	I	ST	JTAG Test mode select pin.
TDIISTJTAG test data input pin.TDOO-JTAG test data output pin.T1CKISTTimer1 external clock input.T2CKISTTimer2 external clock input.T3CKISTTimer3 external clock input.T4CKISTTimer4 external clock input.T5CKISTTimer6 external clock input.T6CKISTTimer6 external clock input.T7CKISTTimer6 external clock input.T8CKISTTimer7 external clock input.T8CKISTTimer9 external clock input.T8CKISTTimer9 external clock input.T9CKISTTimer9 external clock input.UTTSO-UART1 clear to send.U1RTSO-UART1 receive.U1RXISTUART1 receive.U1RXISTUART2 clear to send.U2RTSO-UART2 receive.U2RXISTUART2 receive.U2RXISTUART2 receive.U2RXISTUART2 receive.U2RXISTCPU logic filter capacitor connection.VbDP-CPU logic filter capacitor connection.VssP-Ground reference for logic and I/O pins.VREF+IAnalogAnalog voltage reference (low) input.	TCK	I	ST	JTAG test clock input pin.
TDOO—JTAG test data output pin.T1CKISTTimer1 external clock input.T2CKISTTimer2 external clock input.T3CKISTTimer3 external clock input.T4CKISTTimer4 external clock input.T5CKISTTimer6 external clock input.T6CKISTTimer6 external clock input.T7CKISTTimer6 external clock input.T8CKISTTimer6 external clock input.T8CKISTTimer7 external clock input.T9CKISTTimer9 external clock input.UTTSO—UART1 clear to send.UIRTSO—UART1 receive.U1RXISTUART1 receive.U2CTSISTUART2 receive.U2RTSO—UART2 receive.U2RXISTUART2 receive.U2TXO—PVDDP—Positive supply for peripheral logic and I/O pins.VCAPP—CPU logic filter capacitor connection.VSSP—Ground reference for logic and I/O pins.VREF+IAnalogAnalog voltage reference (low) input.	TDI		ST	JTAG test data input pin.
T1CKISTTimer1 external clock input.T2CKISTTimer2 external clock input.T3CKISTTimer3 external clock input.T4CKISTTimer4 external clock input.T5CKISTTimer6 external clock input.T6CKISTTimer6 external clock input.T7CKISTTimer7 external clock input.T7CKISTTimer9 external clock input.T8CKISTTimer9 external clock input.T9CKISTUART1 clear to send.UIRTSO-UART1 receive.U1RXISTUART1 receive.U2CTSISTUART2 clear to send.U2RTSO-UART1 receive.U2RTSO-UART2 receive.U2RXISTUART2 receive.U2RXO-UART2 receive.U2RXO-CPU logic filter capacitor connection.VssP-Ground reference for logic and I/O pins.VREF+IAnalogAnalog voltage reference (low) input.	TDO	0	—	JTAG test data output pin.
T2CKISTTimer2 external clock input.T3CKISTTimer3 external clock input.T4CKISTTimer4 external clock input.T5CKISTTimer6 external clock input.T6CKISTTimer6 external clock input.T7CKISTTimer6 external clock input.T8CKISTTimer6 external clock input.T7CKISTTimer6 external clock input.T8CKISTTimer9 external clock input.T9CKISTUART1 clear to send.U1RTSO-UART1 receive.U1RXISTUART1 receive.U1RXISTUART2 clear to send.U2CTSISTUART2 receive.U2RTSO-UART2 receive.U2RXISTUART2 receive.U2RXISTUART2 receive.U2TXO-UART2 transmit.VobP-CPU logic filter capacitor connection.VssP-Ground reference for logic and I/O pins.VREF+IAnalogAnalog voltage reference (high) input.	T1CK	I	ST	Timer1 external clock input.
T3CKISTTimer3 external clock input.T4CKISTTimer4 external clock input.T5CKISTTimer5 external clock input.T6CKISTTimer6 external clock input.T7CKISTTimer7 external clock input.T8CKISTTimer9 external clock input.T9CKISTTimer9 external clock input.UICTSISTUART1 clear to send.U1RTSO-UART1 receive.U1RXISTUART1 receive.U1TXO-UART1 transmit.U2CTSISTUART2 clear to send.U2RXISTUART2 receive.U2RXISTUART2 receive.U2TXO-UART2 receive.VDDP-Positive supply for peripheral logic and I/O pins.VCAPP-CPU logic filter capacitor connection.VssP-Ground reference for logic and I/O pins.VREF+IAnalogAnalog voltage reference (low) input.	T2CK	I	ST	Timer2 external clock input.
T4CKISTTimer4 external clock input.T5CKISTTimer5 external clock input.T6CKISTTimer6 external clock input.T7CKISTTimer7 external clock input.T8CKISTTimer9 external clock input.U1CTSISTUART1 clear to send.U1RXISTUART1 ready to send.U1TXO-UART1 receive.U1TXO-UART2 clear to send.U2CTSISTUART2 clear to send.U2RTSO-UART1 receive.U2RTSISTUART2 receive.U2RTSO-UART2 receive.U2RXISTUART2 receive.U2TXO-UART2 receive.VDDP-Positive supply for peripheral logic and I/O pins.VCAPP-CPU logic filter capacitor connection.VssP-Ground reference for logic and I/O pins.VREF+IAnalogAnalog voltage reference (low) input.	T3CK	I	ST	Timer3 external clock input.
T5CKISTTimer5 external clock input.T6CKISTTimer6 external clock input.T7CKISTTimer7 external clock input.T8CKISTTimer8 external clock input.T9CKISTTimer9 external clock input.UICTSISTUART1 clear to send.UIRTSO-UART1 ready to send.U1RXISTUART1 receive.U1TXO-UART1 transmit.U2CTSISTUART2 clear to send.U2RTSO-UART1 transmit.U2RTSISTUART2 receive.U2RXISTUART2 receive.U2TXO-UART2 receive.U2TXO-UART2 transmit.VDDP-Positive supply for peripheral logic and I/O pins.VCAPP-CPU logic filter capacitor connection.VssP-Ground reference for logic and I/O pins.VREF+IAnalogAnalog voltage reference (high) input.VREF-IAnalogAnalog voltage reference (low) input.	T4CK		ST	Timer4 external clock input.
T6CKISTTimer6 external clock input.T7CKISTTimer7 external clock input.T8CKISTTimer8 external clock input.T9CKISTTimer9 external clock input.U1CTSISTUART1 clear to send.U1RTSO-UART1 ready to send.U1RXISTUART1 receive.U1TXO-UART1 receive.U1TXO-UART1 transmit.U2CTSISTUART2 clear to send.U2RTSO-UART2 ready to send.U2RXISTUART2 receive.U2TXO-UART2 receive.U2TXO-UART2 receive.VDDP-Positive supply for peripheral logic and I/O pins.VCAPP-CPU logic filter capacitor connection.VssP-Ground reference for logic and I/O pins.VREF+IAnalog voltage reference (low) input.VREF-IAnalog voltage reference (low) input.	T5CK	I	ST	Timer5 external clock input.
T7CKISTTimer7 external clock input.T8CKISTTimer8 external clock input.T9CKISTTimer9 external clock input.U1CTSISTUART1 clear to send.U1RTSO-UART1 ready to send.U1RXISTUART1 receive.U1TXO-UART1 transmit.U2CTSISTUART2 clear to send.U2RTSO-UART2 ready to send.U2RXISTUART2 receive.U2TXO-UART2 receive.U2TXO-UART2 transmit.VDDP-Positive supply for peripheral logic and I/O pins.VCAPP-CPU logic filter capacitor connection.VREF+IAnalogAnalog voltage reference (high) input.VREF-IAnalogAnalog voltage reference (low) input.	T6CK	I	ST	Timer6 external clock input.
T8CKISTTimer8 external clock input.T9CKISTTimer9 external clock input.U1CTSISTUART1 clear to send.U1RTSO-UART1 ready to send.U1RXISTUART1 receive.U1TXO-UART1 transmit.U2CTSISTUART2 clear to send.U2RXISTUART2 ready to send.U2RXISTUART2 receive.U2TXO-UART2 receive.U2TXO-UART2 transmit.VDDP-Positive supply for peripheral logic and I/O pins.VCAPP-CPU logic filter capacitor connection.VssP-Ground reference for logic and I/O pins.VREF+IAnalogAnalog voltage reference (low) input.VREF-IAnalogAnalog voltage reference (low) input.	T7CK	I	ST	Timer7 external clock input.
T9CKISTTimer9 external clock input.U1CTSISTUART1 clear to send.U1RTSO—UART1 ready to send.U1RXISTUART1 receive.U1TXO—UART1 transmit.U2CTSISTUART2 clear to send.U2RXISTUART2 ready to send.U2RXISTUART2 receive.U2TXO—UART2 receive.U2TXO—UART2 transmit.VDDP—Positive supply for peripheral logic and I/O pins.VCAPP—CPU logic filter capacitor connection.VssP—Ground reference for logic and I/O pins.VREF+IAnalogAnalog voltage reference (high) input.VREF-IAnalogAnalog voltage reference (low) input.	T8CK	I	ST	Timer8 external clock input.
UICTSISTUART1 clear to send.U1RTSO-UART1 ready to send.U1RXISTUART1 receive.U1TXO-UART1 transmit.U2CTSISTUART2 clear to send.U2RTSO-UART2 ready to send.U2RXISTUART2 receive.U2TXO-UART2 receive.U2TXO-UART2 transmit.VDDP-Positive supply for peripheral logic and I/O pins.VCAPP-CPU logic filter capacitor connection.VssP-Ground reference for logic and I/O pins.VREF+IAnalogAnalog voltage reference (high) input.	T9CK	I	ST	Timer9 external clock input.
U1RTSO—UART1 ready to send.U1RXISTUART1 receive.U1TXO—UART1 transmit.U2CTSISTUART2 clear to send.U2RTSO—UART2 ready to send.U2RXISTUART2 receive.U2TXO—UART2 transmit.VDDP—Positive supply for peripheral logic and I/O pins.VCAPP—CPU logic filter capacitor connection.VssP—Ground reference for logic and I/O pins.VREF+IAnalogAnalog voltage reference (high) input.VREF-IAnalogAnalog voltage reference (low) input.	U1CTS	I	ST	UART1 clear to send.
U1RXISTUART1 receive.U1TXO-UART1 transmit.U2CTSISTUART2 clear to send.U2RTSO-UART2 ready to send.U2RXISTUART2 receive.U2TXO-UART2 transmit.VDDP-Positive supply for peripheral logic and I/O pins.VCAPP-CPU logic filter capacitor connection.VssP-Ground reference for logic and I/O pins.VREF+IAnalogAnalog voltage reference (high) input.VREF-IAnalogAnalog voltage reference (low) input.	U1RTS	0	—	UART1 ready to send.
U1TXO—UART1 transmit.U2CTSISTUART2 clear to send.U2RTSO—UART2 ready to send.U2RXISTUART2 receive.U2TXO—UART2 transmit.VDDP—Positive supply for peripheral logic and I/O pins.VCAPP—CPU logic filter capacitor connection.VssP—Ground reference for logic and I/O pins.VREF+IAnalogAnalog voltage reference (high) input.VREF-IAnalogAnalog voltage reference (low) input.	U1RX	I	ST	UART1 receive.
U2CTSISTUART2 clear to send.U2RTSO-UART2 ready to send.U2RXISTUART2 receive.U2TXO-UART2 transmit.VDDP-Positive supply for peripheral logic and I/O pins.VCAPP-CPU logic filter capacitor connection.VssP-Ground reference for logic and I/O pins.VREF+IAnalogAnalog voltage reference (high) input.VREF-IAnalogAnalog voltage reference (low) input.	U1TX	0	—	UART1 transmit.
U2RTS O — UART2 ready to send. U2RX I ST UART2 receive. U2TX O — UART2 transmit. VDD P — Positive supply for peripheral logic and I/O pins. VCAP P — CPU logic filter capacitor connection. Vss P — Ground reference for logic and I/O pins. VREF+ I Analog Analog voltage reference (high) input. VREF- I Analog Analog voltage reference (low) input.	U2CTS	I	ST	UART2 clear to send.
U2RX I ST UART2 receive. U2TX O UART2 transmit. VDD P Positive supply for peripheral logic and I/O pins. VCAP P CPU logic filter capacitor connection. Vss P Ground reference for logic and I/O pins. VREF+ I Analog Analog voltage reference (high) input. VREF- I Analog Analog voltage reference (low) input.	U2RTS	0		UART2 ready to send.
U2TX O — UART2 transmit. VDD P — Positive supply for peripheral logic and I/O pins. VCAP P — CPU logic filter capacitor connection. Vss P — Ground reference for logic and I/O pins. VREF+ I Analog Analog voltage reference (high) input. VREF- I Analog Analog voltage reference (low) input.	U2RX	I	ST	UART2 receive.
VDD P — Positive supply for peripheral logic and I/O pins. VCAP P — CPU logic filter capacitor connection. Vss P — Ground reference for logic and I/O pins. VREF+ I Analog Analog voltage reference (high) input. VREF- I Analog Analog voltage reference (low) input.	U2TX	0	—	UART2 transmit.
VCAP P — CPU logic filter capacitor connection. Vss P — Ground reference for logic and I/O pins. VREF+ I Analog Analog voltage reference (high) input. VREF- I Analog Analog voltage reference (low) input.	Vdd	Р	—	Positive supply for peripheral logic and I/O pins.
Vss P — Ground reference for logic and I/O pins. VREF+ I Analog Analog voltage reference (high) input. VREF- I Analog Analog voltage reference (low) input.	VCAP	Р	—	CPU logic filter capacitor connection.
VREF+ I Analog Analog voltage reference (high) input. VREF- I Analog Analog voltage reference (low) input.	Vss	Р		Ground reference for logic and I/O pins.
VREF- I Analog Analog voltage reference (low) input.	VREF+	1	Analog	Analog voltage reference (high) input.
	VREF-	Ι	Analog	Analog voltage reference (low) input.

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Legend: CMOS = CMOS compatible input or output ST = Schmitt Trigger input with CMOS levels

Analog = Analog input O = Output P = Power I = Input

REGISTER 5-1: NVMCON: FLASH MEMORY CONTROL REGISTER

R/SO-0 ⁽¹⁾	R/W-0 ⁽¹⁾	R/W-0 ⁽¹⁾	U-0	U-0	U-0	U-0	U-0
WR	WREN	WRERR	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0 ⁽¹⁾	U-0	U-0	R/W-0 ⁽¹⁾	R/W-0 ⁽¹⁾	R/W-0 ⁽¹⁾	R/W-0 ⁽¹⁾
_	ERASE	_			NVMOF	<3:0>(2)	
bit 7							bit 0

Legend:	5	SO = Settable only bit		
R = Readable	bit V	V = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at P	OR "	1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
bit 15	WR: Write Cont	trol bit		
	1 = Initiates a l	Flash memory program or	erase operation. The operation	on is self-timed and the bit is
	cleared by	hardware once operation is	s complete	
hit 14		nable bit		
Dit 14	1 = Enable Fla	sh program/erase operation	ns	
	0 = Inhibit Flas	h program/erase operation	S	
bit 13	WRERR: Write	Sequence Error Flag bit		
	1 = An imprope	er program or erase sequer	nce attempt or termination has	s occurred (bit is set
	automatica	lly on any set attempt of th	e WR bit)	
hit 10 7	0 = The progra	m or erase operation comp	pleted normally	
DIT 6	1 - Porform th	Program Enable bit	by $N/MOR<3.05$ on the post	WP command
	0 = Perform the	e program operation specified	ied by NVMOP<3:0> on the next	ext WR command
bit 5-4	Unimplemente	d: Read as '0'	,	
bit 3-0	NVMOP<3:0>:	NVM Operation Select bits	(2)	
	1111 = Memory	y bulk erase operation (ER	ASE = 1) or no operation (ER.	ASE = 0)
	1110 = Reserve	ed		
	1101 = Erase (General Segment and FGS $= 1$ or polynomial (EP)	Configuration Register	
	1100 = Erase S	Secure Segment and FSS (Configuration Register	
	(ERAS	E = 1) or no operation (ER	ASE = 0)	
	1011 = Reserve	ed		
	•			
	•			
	• 0100 - Poson"	ed		
	0011 = Memory	y word program operation (ERASE = 0) or no operation (ERASE = 1)
	0010 = Memory	y page erase operation (EF	RASE = 1) or no operation (EF	RASE = 0)
	0001 = Memory	y row program operation (E	RASE = 0) or no operation (E	RASE = 1)
	0000 = Program	n or erase a single Configu	iration register byte	

Note 1: These bits can only be reset on a POR.

2: All other combinations of NVMOP<3:0> are unimplemented.

REGIST	ER 6-1: RCO	N: RESET COI		GISTER ⁽¹⁾			
R/W-	-0 R/W-0	U-0	U-0	U-0	U-0	U-0	R/W-0
TRAF	PR IOPUWR		—			—	VREGS ⁽³⁾
bit 15	·						bit 8
R/M	0 R/W-0	R/M-0	R/\/_0	R/\/_0	R/\\/_0	R/M/-1	R/M-1
FXT	R SWR					BOR	POR
bit 7		OWBTEN	WBIO	OLLLI	IDEE	Bort	bit 0
Legend:			L :4			l = = (0)	
R = Read			DIT		mented dit, read		
-n = valu	e at POR	"1" = Bit is set		$0^{\circ} = Bit is cle$	eared	x = Bit is unk	nown
bit 15	TRAPR: Tra	ap Reset Flag bit					
	$1 = A \operatorname{Trap} ($	Conflict Reset ha	s occurred	ما			
L:1 4 4		Jonflict Reset na	s not occurre	a M A	-4 [] 1:4		
DIC 14	1 = An illect	al opcode of	ction, an ille	vv Access Res dal address m	ode or uninitial	lized W registe	er used as an
	Addres	s Pointer caused	a Reset	ga: aaa.ccc			
	0 = An illeg	al opcode or uni	nitialized W F	Reset has not o	ccurred		
bit 13-9	Unimpleme	ented: Read as '	כ'	(2)			
bit 8	VREGS: Vo	Itage Regulator	Standby Durii	ng Sleep bit ⁽³⁾			
	\perp = Voltage	Regulator is acti Regulator goes i	nto standby i	ep mode mode durina SI	een		
bit 7	EXTR: Exte	rnal Reset (MCL	\overline{R}) Pin bit		000		
	1 = A Maste	er Clear (pin) Res	set has occur	red			
	0 = A Maste	er Clear (pin) Res	set has not or	ccurred			
bit 6	SWR: Softw	are Reset (Instru	uction) Flag b	oit .			
	1 = A RESE	r instruction has	not been exe	ed Souted			
bit 5	SWDTEN: S	Software Enable/	Disable of W	DT bit ⁽²⁾			
	1 = WDT is	enabled					
	0 = WDT is	disabled					
bit 4	WDTO: Wat	tchdog Timer Tim	ne-out Flag b	it			
	1 = WD1 tin 0 = WDT tin	ne-out has occur	red				
hit 3	SI FFP: Wa	ke-un from Slee	n Flag hit				
	1 = Device h	has been in Slee	p mode				
	0 = Device ł	has not been in S	Sleep mode				
bit 2	IDLE: Wake	-up from Idle Fla	ıg bit				
	1 = Device	was in Idle mode	ode				
bit 1	BOR: Brown	n-out Reset Flag	bit				
	1 = A Brown	n-out Reset has o	occurred				
	0 = A Browr	n-out Reset has r	not occurred				
bit 0	POR: Powe	r-on Reset Flag	bit				
	1 = A Power0 = A Power	r-on Reset has o r-on Reset has n	ccurred				
		I-OII Reset has h					
Note 1:	All of the Reset s	tatus bits may be	set or cleare	ed in software.	Setting one of th	iese bits in soft	ware does not
	cause a device R	Reset.					
2:	If the FWDTEN C	Configuration bit i	is '1' (unprog	rammed), the V	NDT is always e	enabled, regard	lless of the
٦.	For PIC24H.1256		(10A devices	this bit is unin	nplemented and	l reads back or	ogrammed

3: For PIC24HJ256GPX06A/X08A/X10A devices, this bit is unimplemented and reads back programmed value.

REGISTER 7-5: IFS0: INTERRUPT FLAG STATUS REGISTER 0

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DMA1IF	AD1IF	U1TXIF	U1RXIF	SPI1IF	SPI1EIF	T3IF
bit 15							bit 8
							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
T2IF	OC2IF	IC2IF	DMA01IF	T1IF	OC1IF	IC1IF	INT0IF
bit 7							bit 0
Logond							
R = Readable	bit	W = Writable	bit	l I = l Inimplei	mented hit read	d as '0'	
-n = Value at F	POR	'1' = Bit is se	t	'0' = Bit is cle	eared	x = Bit is unkn	iown
			-				-
bit 15	Unimplemen	ted: Read as	0'				
bit 14	DMA1IF: DM	A Channel 1 D	ata Transfer C	Complete Interr	rupt Flag Status	bit	
	1 = Interrupt r 0 = Interrupt r	request has oc request has no	curred t occurred				
bit 13	AD1IF: ADC1	Conversion C	Complete Interi	rupt Flag Statu	is bit		
	1 = Interrupt r 0 = Interrupt r	request has oc request has no	curred t occurred				
bit 12	U1TXIF: UAR	RT1 Transmitte	r Interrupt Flag	g Status bit			
	1 = Interrupt r	request has oc	curred				
	0 = Interrupt r	request has no	t occurred				
DIT 11		KI 1 Receiver I	nterrupt Flag S	Status dit			
	0 = Interrupt r	request has oc	t occurred				
bit 10	SPI1IF: SPI1	Event Interrup	ot Flag Status b	oit			
	1 = Interrupt r 0 = Interrupt r	request has oc request has no	curred t occurred				
bit 9	SPI1EIF: SPI	1 Fault Interru	pt Flag Status	bit			
	1 = Interrupt r	request has oc	curred				
h :t 0	0 = Interrupt r	request has no	t occurred				
DIT 8	1 3IF: Inmer3	Interrupt Flag	Status bit				
	0 = Interrupt r	request has oc	t occurred				
bit 7	T2IF: Timer2	Interrupt Flag	Status bit				
	1 = Interrupt r	request has oc	curred				
		request has no	t occurred		1.11		
bit 6	1 = Interrupt r	ut Compare Cr	annel 2 Interr	upt Flag Status	s dit		
	0 = Interrupt r	request has oc	t occurred				
bit 5	IC2IF: Input C	Capture Chann	el 2 Interrupt I	-lag Status bit			
	1 = Interrupt r	request has oc	curred				
	0 = Interrupt r	request has no	t occurred			- I- 14	
DIT 4	1 = Interrupt r	VIA Channel U		Complete Inte	rrupt Flag Statu	IS DIT	
	0 = Interrupt r	request has no	t occurred				
bit 3	T1IF: Timer1	Interrupt Flag	Status bit				
	1 = Interrupt r	request has oc	curred				
	0 = Interrupt r	request has no	t occurred				

REGISTER 7-6:	IFS1: INTERRUPT FLAG STATUS REGISTER 1
---------------	--

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
U2TXIF	U2RXIF	INT2IF	T5IF	T4IF	OC4IF	OC3IF	DMA21IF
bit 15							bit 8
							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
IC8IF	IC7IF	AD2IF	INT1IF	CNIF	—	MI2C1IF	SI2C1IF
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimple	mented bit read	1 as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unkr	nown
bit 15	U2TXIF: UAF	RT2 Transmitter	Interrupt Fla	g Status bit			
	1 = Interrupt i	request has occ	curred				
	0 = Interrupt i	request has not	occurred				
bit 14	U2RXIF: UAF	RT2 Receiver Ir	nterrupt Flag	Status bit			
	1 = Interrupt i	request has occ request has not	currea t occurred				
bit 13	INT2IF: Exter	nal Interrupt 2	Flag Status b	it			
	1 = Interrupt I	request has occ	curred				
	0 = Interrupt I	request has not	toccurred				
bit 12	T5IF: Timer5	Interrupt Flag S	Status bit				
	1 = Interrupt I	request has occ request has not	curred				
bit 11	T4IF: Timer4	Interrupt Flag S	Status bit				
	1 = Interrupt I	request has occ	curred				
	0 = Interrupt I	request has not	occurred				
bit 10	OC4IF: Outpu	ut Compare Ch	annel 4 Interr	upt Flag Status	s bit		
	1 = Interrupt i 0 = Interrupt i	request has occ request has not	curred t occurred				
bit 9	OC3IF: Outpu	ut Compare Ch	annel 3 Interr	upt Flag Statu	s bit		
	1 = Interrupt I	request has occ	curred				
h # 0		request has not	t occurred	Complete Inte	must Flag. Otati	a hit	
DIL 8	1 = Interrunt u	via Unannei 2 L request has occ		Complete inte	errupt Flag Statu	IS DIL	
	0 = Interrupt i	request has not	toccurred				
bit 7	IC8IF: Input C	Capture Channe	el 8 Interrupt	Flag Status bit			
	1 = Interrupt i	request has occ	curred				
hit 6		Capture Chappe	occurred	Elaa Status bit			
DIL O	1 = Interrupt i	request has occ	curred	riay Status Dit			
	0 = Interrupt i	request has not	toccurred				
bit 5	AD2IF: ADC2	2 Conversion C	omplete Inter	rupt Flag Statu	ıs bit		
	1 = Interrupt I	request has occ	curred				
hit 4		request has not		:+			
UIL 4		request has one	riay status D curred	IL			
	0 = Interrupt i	request has not	occurred				

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
		IC5IP<2:0>		—		IC4IP<2:0>	
bit 15							bit 8
U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
		IC3IP<2:0>				DMA3IP<2:0>	
bit 7							bit 0
Legend:							
R = Readabl	e bit	W = Writable I	bit	U = Unimple	mented bit, re	ad as '0'	
-n = Value at	POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unkn	own
I							
bit 15	Unimpleme	ented: Read as ')'				
bit 14-12	IC5IP<2:0>:	: Input Capture C	hannel 5 Inte	errupt Priority b	oits		
	111 = Interr	upt is priority 7 (I	nighest priori	ty interrupt)			
	•		0	, i,			
	•						
	• 001 = Interr	unt is priority 1					
	000 = Interr	upt source is disa	abled				
bit 11	Unimpleme	nted: Read as ')'				
bit 10-8	IC4IP<2:0>:	: Input Capture C	hannel 4 Inte	errupt Priority b	oits		
	111 = Interr	upt is priority 7 (I	nighest priori	ty interrupt)			
	•						
	•						
	• 001 = Interr	upt is priority 1					
	000 = Interr	upt source is disa	abled				
bit 7	Unimpleme	ented: Read as 'o)'				
bit 6-4	IC3IP<2:0>	: Input Capture C	hannel 3 Inte	errupt Priority b	oits		
	111 = Interr	upt is priority 7 (ł	nighest priori	ty interrupt)			
	•						
	•						
	001 = Interr	upt is priority 1					
	000 = Interr	upt source is disa	abled				
bit 3	Unimpleme	ented: Read as 'o)'				
bit 2-0	DMA3IP<2:	0>: DMA Channe	el 3 Data Tra	nsfer Complete	e Interrupt Prid	ority bits	
	111 = Interr	upt is priority 7 (ł	nighest priori	ty interrupt)			
	•						
	•						
	001 = Interr	upt is priority 1					
	000 = Interr	upt source is dis	abled				

REGISTER 7-24: IPC9: INTERRUPT PRIORITY CONTROL REGISTER 9

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
_		T6IP<2:0>				DMA4IP<2:0>	
bit 15					·		bit 8
U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-0
	—	—	_	—		OC8IP<2:0>	
bit 7							bit 0
Legend:							
R = Readab	le bit	W = Writable	bit	U = Unimple	mented bit, rea	d as '0'	
-n = Value a	t POR	'1' = Bit is set	t	'0' = Bit is cle	eared	x = Bit is unkr	nown
bit 15	Unimplemen	ted: Read as '	0'				
bit 14-12	T6IP<2:0>: ⊺	imer6 Interrupt	Priority bits				
	111 = Interru	pt is priority 7 (highest priori	ty interrupt)			
	•						
	•						
	001 = Interru	pt is priority 1					
	000 = Interru	pt source is dis	sabled				
bit 11	Unimplemen	ted: Read as '	0'				
bit 10-8	DMA4IP<2:0	>: DMA Chann	iel 4 Data Tra	nsfer Complete	e Interrupt Prior	ity bits	
	111 = Interru	pt is priority 7 (highest priori	ty interrupt)			
	•						
	•						
	001 = Interru	pt is priority 1					
		pt source is dis	sabled				
bit 7-3	Unimplemen	ted: Read as	0'				
bit 2-0	OC8IP<2:0>:	Output Compa	are Channel 8	3 Interrupt Prior	rity bits		
	111 = Interru	pt is priority 7 (nignest priori	ty interrupt)			
	•						
	•						
	001 = Interru	pt is priority 1					
	000 = Interru	pt source is dis	sabled				

REGISTER 7-26: IPC11: INTERRUPT PRIORITY CONTROL REGISTER 11

U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-0
—	—	—	—	—		U2EIP<2:0>	
bit 15							bit 8
U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
_		U1EIP<2:0>			—	—	
bit 7							bit 0
Legend:							
R = Readable	e bit	W = Writable I	bit	U = Unimpler	mented bit, rea	d as '0'	
-n = Value at	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkn	own
bit 15-11	Unimplemen	ted: Read as 'd)'				
bit 10-8	U2EIP<2:0>:	UART2 Error Ir	nterrupt Priori	ty bits			
	111 = Interru	pt is priority 7 (ł	nighest priorit	y interrupt)			
	•						
	•						
	001 = Interru	pt is priority 1					
	000 = Interru	pt source is disa	abled				
bit 7	Unimplemen	ted: Read as 'o)'				
bit 6-4	U1EIP<2:0>:	UART1 Error Ir	nterrupt Priori	ty bits			
	111 = Interru	pt is priority 7 (ł	nighest priorit	y interrupt)			
	•						
	•						
	001 = Interru	pt is priority 1					
	000 = Interru	pt source is disa	abled				
bit 3-0	Unimplemen	ted: Read as 'o)'				

REGISTER 7-31: IPC16: INTERRUPT PRIORITY CONTROL REGISTER 16

REGISTER 9-1: OSCCON: OSCILLATOR CONTROL REGISTER^(1,3) (CONTINUED)

bit 1	LPOSCEN: Secondary (LP) Oscillator Enable bit
	1 = Enable secondary oscillator
	0 = Disable secondary oscillator
bit 0	OSWEN: Oscillator Switch Enable bit
	1 = Request oscillator switch to selection specified by NOSC<2:0> bits
	0 = Oscillator switch is complete

- Note 1: Writes to this register require an unlock sequence. Refer to Section 7. "Oscillator" (DS70186) in the "dsPIC33F/PIC24H Family Reference Manual" for details.
 - 2: Direct clock switches between any primary oscillator mode with PLL and FRCPLL mode are not permitted. This applies to clock switches in either direction. In these instances, the application must switch to FRC mode as a transition clock source between the two PLL modes.
 - 3: This register is reset only on a Power-on Reset (POR).

14.1 Input Capture Registers

REGISTER 14-1: ICxCON: INPUT CAPTURE x CONTROL REGISTER

U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0	
		ICSIDL		_	_			
bit 15							bit 8	
								
R/W-0	R/W-0	R/W-0	R-0, HC	R-0, HC	R/W-0	R/W-0	R/W-0	
ICTMR ⁽¹⁾	ICI<	1:0>	ICOV	ICBNE ICM<2:0>				
bit 7							bit 0	
Legend:								
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	d as '0'		
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	Iown	
bit 15-14	Unimplement	ted: Read as '	כ'					
bit 13	ICSIDL: Input	Capture Modu	ile Stop in Idle	e Control bit				
	1 = Input capt	ure module wil	I halt in CPU	Idle mode	l Idla mada			
bit 12 9		ted: Road as '	' continue to c					
bit 7		Conture Timer	Soloct hite(1)					
	1 = TMR2 cor	tents are cant	ured on cantu	re event				
	0 = TMR3 cor	itents are capt	ured on captu	re event				
bit 6-5	ICI<1:0>: Sele	ect Number of	Captures per	Interrupt bits				
	11 = Interrupt	on every fourt	h capture eve	nt				
	10 = Interrupt	on every third	capture even	t vent				
	00 = Interrupt	on every capt	ure event	CIIL				
bit 4	ICOV: Input C	apture Overflo	w Status Flag	bit (read-only))			
	1 = Input capt	ure overflow o	ccurred					
	0 = No input c	apture overflow	w occurred					
bit 3	ICBNE: Input	Capture Buffe	Empty Status	s bit (read-only	') 			
	1 = Input capt 0 = Input capt	ure buffer is no ure buffer is er	ot empty, at le npty	ast one more o	capture value c	an be read		
bit 2-0	ICM<2:0>: Inp	out Capture Mo	de Select bits	6				
	111 = Input ca	apture function	s as interrupt	pin only when	device is in Sle	eep or Idle mode	e	
	(Rising	edge detect o	nly, all other o	control bits are	not applicable.)		
	101 = Capture	e mode, everv	16th risina ed	ae				
	100 = Capture	e mode, every	4th rising edg	e				
	011 = Capture	e mode, every	rising edge					
	010 = Capture 001 = Capture	e mode, every	edge (rising a	nd falling)				
	(ICI<1:	0> bits do not	control interru	pt generation	for this mode.)			
	000 = Input ca	apture module	turned off					

15.0 OUTPUT COMPARE

- Note 1: This data sheet summarizes the features of the PIC24HJXXXGPX06A/X08A/X10A families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the "dsPIC33F/PIC24H Family Reference Manual", Section 13. "Output Compare" (DS70209), which is available on the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The output compare module can select either Timer2 or Timer3 for its time base. The module compares the value of the timer with the value of one or two Compare registers depending on the operating mode selected. The state of the output pin changes when the timer value matches the Compare register value. The output compare module generates either a single output pulse, or a sequence of output pulses, by changing the state of the output pin on the compare match events. The output compare module can also generate interrupts on compare match events.

The output compare module has multiple operating modes:

- Active-Low One-Shot mode
- Active-High One-Shot mode
- Toggle mode
- · Delayed One-Shot mode
- Continuous Pulse mode
- PWM mode without Fault Protection
- PWM mode with Fault Protection

FIGURE 15-1: OUTPUT COMPARE MODULE BLOCK DIAGRAM



16.0 SERIAL PERIPHERAL INTERFACE (SPI)

- Note 1: This data sheet summarizes the features of the PIC24HJXXXGPX06A/X08A/X10A family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the "dsPIC33F/PIC24H Family Reference Manual", Section 18. "Serial Peripheral Interface (SPI)" (DS70206), which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The Serial Peripheral Interface (SPI) module is a synchronous serial interface useful for communicating with other peripheral or microcontroller devices. These peripheral devices may be serial EEPROMs, shift registers, display drivers, Analog-to-Digital converters, etc. The SPI module is compatible with SPI and SIOP from Motorola[®].

Note: In this section, the SPI modules are referred to together as SPIx, or separately as SPI1 and SPI2. Special Function Registers will follow a similar notation. For example, SPIxCON refers to the control register for the SPI1 or SPI2 module.

Each SPI module consists of a 16-bit shift register, SPIxSR (where x = 1 or 2), used for shifting data in and out, and a buffer register, SPIxBUF. A control register, SPIxCON, configures the module. Additionally, a status register, SPIxSTAT, indicates various status conditions.

The serial interface consists of 4 pins: SDIx (serial data input), SDOx (serial data output), SCKx (shift clock input or output), and SSx (active-low slave select).

In Master mode operation, SCK is a clock output but in Slave mode, it is a clock input.



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FIGURE 16-1: SPI MODULE BLOCK DIAGRAM

20.6 ADC Control Registers

REGISTER 20-1: ADxCON1: ADCx CONTROL REGISTER 1(where x = 1 or 2)

R/W-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
ADON	—	ADSIDL	ADDMABM		AD12B	FORM	1<1:0>
bit 15							bit 8
R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/C-0
						HC,HS	HC, HS
	SSRC<2:0>		_	SIMSAM	ASAM	SAMP	DONE
bit 7							bit 0

Legend:	HC = Cleared by hardware	re HS = Set by hardware	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	d as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15	ADON: ADC Operating Mode bit
	1 = ADC module is operating
	0 = ADC module is off
bit 14	Unimplemented: Read as '0'
bit 13	ADSIDL: Stop in Idle Mode bit
	1 = Discontinue module operation when device enters Idle mode
	0 = Continue module operation in Idle mode
bit 12	ADDMABM: DMA Buffer Build Mode bit
	1 = DMA buffers are written in the order of conversion. The module will provide an address to the DMA channel that is the same as the address used for the non-DMA stand-alone buffer.
	 DMA buffers are written in Scatter/Gather mode. The module will provide a scatter/gather address to the DMA channel, based on the index of the analog input and the size of the DMA buffer
bit 11	Unimplemented: Read as '0'
bit 10	AD12B: 10-Bit or 12-Bit Operation Mode bit
	1 = 12-bit, 1-channel ADC operation
	0 = 10-bit, 4-channel ADC operation
bit 9-8	FORM<1:0>: Data Output Format bits
	For 10-bit operation:
	11 = Reserved
	10 = Reserved
	01 = Signed Integer (DOUT = SSSS SSSA dada adad, where S = .NOT.d<9>) 00 = Integer (DOUT = 0000 00dd dddd dddd)
	For 12-bit operation:
	11 = Reserved
	10 = Reserved
	01 = Signed Integer (DOUT = ssss sddd dddd dddd, where s = .NOT.d<11>)
	00 = Integer (DOUT = 0000 dddd dddd)
bit 7-5	SSRC<2:0>: Sample Clock Source Select bits
	111 = Internal counter ends sampling and starts conversion (auto-convert)
	101 = Reserved
	100 = GP timer (Timer5 for ADC1, Timer3 for ADC2) compare ends sampling and starts conversion
	011 = Reserved 010 = CP timer (Timer3 for ADC1, Timer5 for ADC2) compare ends sampling and starts conversion
	001 = Active transition on INTO pin ends sampling and starts conversion

TABLE 22-2:	INSTRUCTION SET OVERVIEW (CONTINUED)
--------------------	---

Base Instr #	Assembly Mnemonic		Assembly Syntax	Description	# of Words	# of Cycles	Status Flags Affected
12	BTST	BTST	f,#bit4	Bit Test f	1	1	Z
		BTST.C	Ws,#bit4	Bit Test Ws to C	1	1	С
		BTST.Z	Ws,#bit4	Bit Test Ws to Z	1	1	Z
		BTST.C	Ws,Wb	Bit Test Ws <wb> to C</wb>	1	1	С
		BTST.Z	Ws,Wb	Bit Test Ws <wb> to Z</wb>	1	1	Z
13	BTSTS	BTSTS	f,#bit4	Bit Test then Set f	1	1	Z
		BTSTS.C	Ws,#bit4	Bit Test Ws to C, then Set	1	1	С
		BTSTS.Z	Ws,#bit4	Bit Test Ws to Z, then Set	1	1	Z
14	CALL	CALL	lit23	Call subroutine	2	2	None
		CALL	Wn	Call indirect subroutine	1	2	None
15	CLR	CLR	f	f = 0x0000	1	1	None
		CLR	WREG	WREG = 0x0000	1	1	None
		CLR	Ws	Ws = 0x0000	1	1	None
16	CLRWDT	CLRWDT		Clear Watchdog Timer	1	1	WDTO,Sleep
17	COM	COM	f	f = f	1	1	N,Z
		COM	f,WREG	WREG = \overline{f}	1	1	N,Z
		COM	Ws,Wd	$Wd = \overline{Ws}$	1	1	N,Z
18	CP	CP	f	Compare f with WREG	1	1	C,DC,N,OV,Z
		CP	Wb,#lit5	Compare Wb with lit5	1	1	C,DC,N,OV,Z
		CP	Wb,Ws	Compare Wb with Ws (Wb – Ws)	1	1	C,DC,N,OV,Z
19	CP0	CP0	f	Compare f with 0x0000	1	1	C,DC,N,OV,Z
		CP0	Ws	Compare Ws with 0x0000	1	1	C,DC,N,OV,Z
20	CPB	CPB	f	Compare f with WREG, with Borrow	1	1	C,DC,N,OV,Z
		CPB	Wb,#lit5	Compare Wb with lit5, with Borrow	1	1	C,DC,N,OV,Z
		СРВ	Wb,Ws	Compare Wb with Ws, with Borrow $(Wb - Ws - \overline{C})$	1	1	C,DC,N,OV,Z
21	CPSEQ	CPSEQ	Wb, Wn	Compare Wb with Wn, skip if =	1	1 (2 or 3)	None
22	CPSGT	CPSGT	Wb, Wn	Compare Wb with Wn, skip if >	1	1 (2 or 3)	None
23	CPSLT	CPSLT	Wb, Wn	Compare Wb with Wn, skip if <	1	1 (2 or 3)	None
24	CPSNE	CPSNE	Wb, Wn	Compare Wb with Wn, skip if ≠	1	1 (2 or 3)	None
25	DAW	DAW	Wn	Wn = decimal adjust Wn	1	1	С
26	DEC	DEC	f	f = f - 1	1	1	C,DC,N,OV,Z
		DEC	f,WREG	WREG = f – 1	1	1	C,DC,N,OV,Z
		DEC	Ws,Wd	Wd = Ws - 1	1	1	C,DC,N,OV,Z
27	DEC2	DEC2	f	f = f - 2	1	1	C,DC,N,OV,Z
		DEC2	f,WREG	WREG = f – 2	1	1	C,DC,N,OV,Z
		DEC2	Ws,Wd	Wd = Ws - 2	1	1	C,DC,N,OV,Z
28	DISI	DISI	#lit14	Disable Interrupts for k instruction cycles	1	1	None
29	DIV	DIV.S	Wm,Wn	Signed 16/16-bit Integer Divide	1	18	N,Z,C,OV
		DIV.SD	Wm,Wn	Signed 32/16-bit Integer Divide	1	18	N,Z,C,OV
		DIV.U	Wm,Wn	Unsigned 16/16-bit Integer Divide	1	18	N,Z,C,OV
		DIV.UD	Wm,Wn	Unsigned 32/16-bit Integer Divide	1	18	N,Z,C,OV
30	EXCH	EXCH	Wns,Wnd	Swap Wns with Wnd	1	1	None
31	FBCL	FBCL	Ws,Wnd	Find Bit Change from Left (MSb) Side	1	1	С
32	FF1L	FF1L	Ws,Wnd	Find First One from Left (MSb) Side	1	1	С
33	FF1R	FF1R	Ws,Wnd	Find First One from Right (LSb) Side	1	1	С
34	GOTO	GOTO	Expr	Go to address	2	2	None
		GOTO	Wn	Go to indirect	1	2	None

TABLE 24-28: SPIx MAXIMUM DATA/CLOCK RATE SUMMARY

AC CHARA	CTERISTICS		$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Indus} \\ -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Exterm} \end{array}$			
Maximum Data Rate	Master Transmit Only (Half-Duplex)	Master Transmit/Receive (Full-Duplex)	Slave Transmit/Receive (Full-Duplex)	CKE	СКР	SMP
15 MHz	Table 24-29	—	—	0,1	0,1	0,1
10 MHz	—	Table 24-30	—	1	0,1	1
10 MHz	—	Table 24-31	—	0	0,1	1
15 MHz	—	—	Table 24-32	1	0	0
11 MHz	—	—	Table 24-33	1	1	0
15 MHz	_	_	Table 24-34	0	1	0
11 MHz	_	_	Table 24-35	0	0	0

FIGURE 24-9: SPIX MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY CKE = 0) TIMING CHARACTERISTICS



			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)						
AC CHA	RACTERIS	TICS	Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial						
-		1		1		-40°C ≤ `	TA \leq +125°C for Extended		
Param No.	Symbol	Characteristic	Min.	Тур	Max.	Units	Conditions		
		ADC Accuracy (10-bit Mode	e) – Meas	uremen	ts with e	xternal	VREF+/VREF-		
AD20b	Nr	Resolution	1	0 data b	its	bits			
AD21b	INL	Integral Nonlinearity	-1.5	-	+1.5	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V		
AD22b	DNL	Differential Nonlinearity	>-1	-	<1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V		
AD23b	Gerr	Gain Error	—	3	6	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V		
AD24b	EOFF	Offset Error	—	2	5	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V		
AD25b	—	Monotonicity	—	—	_	_	Guaranteed		
		ADC Accuracy (10-bit Mode	e) – Meas	uremen	ts with i	nternal V	VREF+/VREF-		
AD20b	Nr	Resolution	1	0 data b	its	bits			
AD21b	INL	Integral Nonlinearity	-1	—	+1	LSb	VINL = AVSS = 0V, AVDD = 3.6V		
AD22b	DNL	Differential Nonlinearity	>-1	—	<1	LSb	VINL = AVSS = 0V, AVDD = 3.6V		
AD23b	Gerr	Gain Error	—	7	15	LSb	VINL = AVSS = 0V, AVDD = 3.6V		
AD24b	EOFF	Offset Error	—	3	7	LSb	VINL = AVSS = 0V, AVDD = 3.6V		
AD25b	—	Monotonicity	—	—		—	Guaranteed		
		Dynamic I	Performa	ance (10	-bit Mod	e)			
AD30b	THD	Total Harmonic Distortion	—	—	-64	dB	_		
AD31b	SINAD	Signal to Noise and Distortion	57	58.5	_	dB	—		
AD32b	SFDR	Spurious Free Dynamic Range	72	—	_	dB	_		
AD33b	FNYQ	Input Signal Bandwidth	_	_	550	kHz	_		
AD34b	ENOB	Effective Number of Bits	9.16	9.4		bits	—		

TABLE 24-41: ADC MODULE SPECIFICATIONS (10-BIT MODE)⁽¹⁾

Note 1: Injection currents > |0| can affect the ADC results by approximately 4-6 counts (i.e., VIH source > (VDD + 0.3) or VIL source < (VSS - 0.3)).

NOTES:

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body with 5.40 x 5.40 Exposed Pad [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS			
Dimension	Limits	MIN	NOM	MAX	
Number of Pins	N	64			
Pitch	е		0.50 BSC		
Overall Height	Α	0.80	0.90	1.00	
Standoff	A1	0.00	0.02	0.05	
Contact Thickness	A3	0.20 REF			
Overall Width	E	9.00 BSC			
Exposed Pad Width	E2	5.30	5.40	5.50	
Overall Length	D		9.00 BSC		
Exposed Pad Length	D2	5.30	5.40	5.50	
Contact Width	b	0.20	0.25	0.30	
Contact Length	L	0.30 0.40 0.50			
Contact-to-Exposed Pad	K	0.20	-	-	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Package is saw singulated.

3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-154A Sheet 2 of 2

APPENDIX A: MIGRATING FROM PIC24HJXXXGPX06/ X08/X10 DEVICES TO PIC24HJXXXGPX06A/ X08A/X10A DEVICES

The PIC24HJXXXGPX06A/X08A/X10A devices were designed to enhance the PIC24HJXXXGPX06/X08/ X10 families of devices.

In general, the PIC24HJXXXGPX06A/X08A/X10A devices are backward-compatible with PIC24HJXXXGPX06/X08/X10 devices; however, manufacturing differences may cause PIC24HJXXXGPX06A/X08A/X10A devices to behave differently from PIC24HJXXXGPX06/X08/X10 devices. Therefore, complete system test and characterization is recommended if PIC24HJXXXGPX06A/X08A/X10A devices are used to replace PIC24HJXXXGPX06/X08/ X10 devices.

The following enhancements were introduced:

- Extended temperature support of up to +125°C
- Enhanced Flash module with higher endurance and retention
- New PLL Lock Enable configuration bit
- Added Timer5 trigger for ADC1 and Timer3 trigger for ADC2

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