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Details

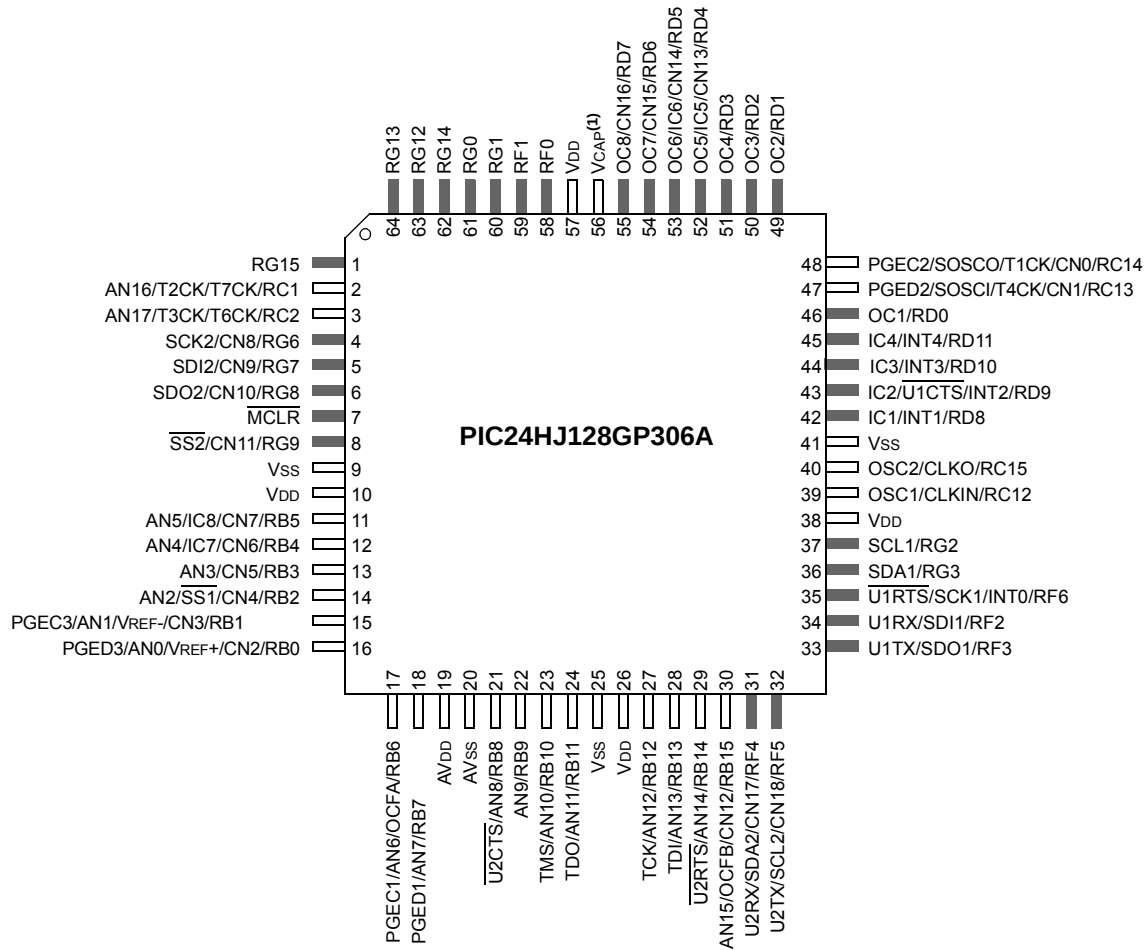
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	40 MIPS
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	53
Program Memory Size	64KB (22K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 18x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24hj64gp506a-e-pt

PIC24HJXXXGPX06A/X08A/X10A

Pin Diagrams (Continued)

64-Pin TQFP

■ = Pins are up to 5V tolerant



Note 1: Refer to Section 2.3 "CPU Logic Filter Capacitor Connection (VCAP)" for proper connection to this pin.

PIC24HJXXXGPX06A/X08A/X10A

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Type	Buffer Type	Description
SCK1	I/O	ST	Synchronous serial clock input/output for SPI1.
SDI1	I	ST	SPI1 data in.
SDO1	O	—	SPI1 data out.
SS1	I/O	ST	SPI1 slave synchronization or frame pulse I/O.
SCK2	I/O	ST	Synchronous serial clock input/output for SPI2.
SDI2	I	ST	SPI2 data in.
SDO2	O	—	SPI2 data out.
SS2	I/O	ST	SPI2 slave synchronization or frame pulse I/O.
SCL1	I/O	ST	Synchronous serial clock input/output for I2C1.
SDA1	I/O	ST	Synchronous serial data input/output for I2C1.
SCL2	I/O	ST	Synchronous serial clock input/output for I2C2.
SDA2	I/O	ST	Synchronous serial data input/output for I2C2.
SOSCI	I	ST/CMOS	32.768 kHz low-power oscillator crystal input; CMOS otherwise.
SOSCO	O	—	32.768 kHz low-power oscillator crystal output.
TMS	I	ST	JTAG Test mode select pin.
TCK	I	ST	JTAG test clock input pin.
TDI	I	ST	JTAG test data input pin.
TDO	O	—	JTAG test data output pin.
T1CK	I	ST	Timer1 external clock input.
T2CK	I	ST	Timer2 external clock input.
T3CK	I	ST	Timer3 external clock input.
T4CK	I	ST	Timer4 external clock input.
T5CK	I	ST	Timer5 external clock input.
T6CK	I	ST	Timer6 external clock input.
T7CK	I	ST	Timer7 external clock input.
T8CK	I	ST	Timer8 external clock input.
T9CK	I	ST	Timer9 external clock input.
U1CTS	I	ST	UART1 clear to send.
U1RTS	O	—	UART1 ready to send.
U1RX	I	ST	UART1 receive.
U1TX	O	—	UART1 transmit.
U2CTS	I	ST	UART2 clear to send.
U2RTS	O	—	UART2 ready to send.
U2RX	I	ST	UART2 receive.
U2TX	O	—	UART2 transmit.
VDD	P	—	Positive supply for peripheral logic and I/O pins.
VCAP	P	—	CPU logic filter capacitor connection.
VSS	P	—	Ground reference for logic and I/O pins.
VREF+	I	Analog	Analog voltage reference (high) input.
VREF-	I	Analog	Analog voltage reference (low) input.

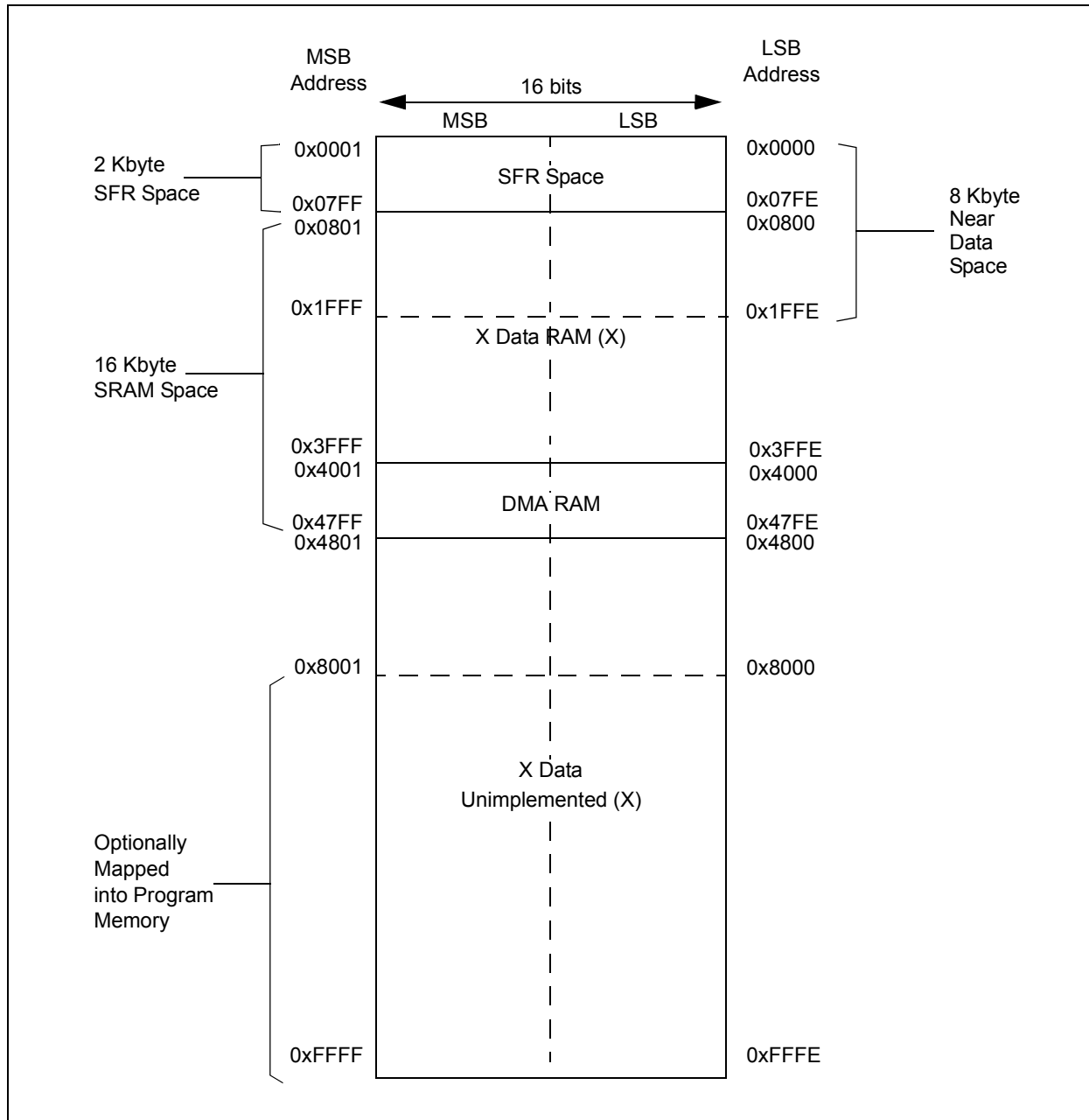
Legend: CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels

Analog = Analog input
O = Output

P = Power
I = Input

PIC24HJXXXGPX06A/X08A/X10A

FIGURE 4-4: DATA MEMORY MAP FOR PIC24HJXXXGPX06A/X08A/X10A DEVICES WITH 16 KB RAM



4.2.5 DMA RAM

Every PIC24HJXXXGPX06A/X08A/X10A device contains 2 Kbytes of dual ported DMA RAM located at the end of data space. Memory locations in the DMA RAM space are accessible simultaneously by the CPU and the DMA controller module. DMA RAM is utilized by the DMA controller to store data to be transferred to various peripherals using DMA, as well as data

transferred from various peripherals using DMA. The DMA RAM can be accessed by the DMA controller without having to steal cycles from the CPU.

When the CPU and the DMA controller attempt to concurrently write to the same DMA RAM location, the hardware ensures that the CPU is given precedence in accessing the DMA RAM location. Therefore, the DMA RAM provides a reliable means of transferring DMA data without ever having to stall the CPU.

Note: DMA RAM can be used for general purpose data storage if the DMA function is not required in an application.

TABLE 4-17: DMA REGISTER MAP (CONTINUED)

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets	
DMA5PAD	03C4	PAD<15:0>																0000	
DMA5CNT	03C6	—	—	—	—	—	—	CNT<9:0>										0000	
DMA6CON	03C8	CHEN	SIZE	DIR	HALF	NULLW	—	—	—	—	—	AMODE<1:0>		—	—	MODE<1:0>		0000	
DMA6REQ	03CA	FORCE	—	—	—	—	—	—	—	—	IRQSEL<6:0>								0000
DMA6STA	03CC	STA<15:0>																0000	
DMA6STB	03CE	STB<15:0>																0000	
DMA6PAD	03D0	PAD<15:0>																0000	
DMA6CNT	03D2	—	—	—	—	—	—	CNT<9:0>										0000	
DMA7CON	03D4	CHEN	SIZE	DIR	HALF	NULLW	—	—	—	—	—	AMODE<1:0>		—	—	MODE<1:0>		0000	
DMA7REQ	03D6	FORCE	—	—	—	—	—	—	—	—	IRQSEL<6:0>								0000
DMA7STA	03D8	STA<15:0>																0000	
DMA7STB	03DA	STB<15:0>																0000	
DMA7PAD	03DC	PAD<15:0>																0000	
DMA7CNT	03DE	—	—	—	—	—	—	CNT<9:0>										0000	
DMACS0	03E0	PWCOL7	PWCOL6	PWCOL5	PWCOL4	PWCOL3	PWCOL2	PWCOL1	PWCOL0	XWCOL7	XWCOL6	XWCOL5	XWCOL4	XWCOL3	XWCOL2	XWCOL1	XWCOL0	0000	
DMACS1	03E2	—	—	—	—	LSTCH<3:0>				PPST7	PPST6	PPST5	PPST4	PPST3	PPST2	PPST1	PPST0	0000	
DSADR	03E4	DSADR<15:0>																0000	

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal for PinHigh devices.

TABLE 4-18: ECAN1 REGISTER MAP WHEN C1CTRL1.WIN = 0 OR 1 FOR PIC24HJXXXGP506A/510A/610A DEVICES ONLY

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
C1CTRL1	0400	—	—	CSIDL	ABAT	—	REQOP<2:0>			OPMODE<2:0>			—	CANCAP	—	—	WIN	0480
C1CTRL2	0402	—	—	—	—	—	—	—	—	—	—	—	DNCNT<4:0>					0000
C1VEC	0404	—	—	—	FILHIT<4:0>					—	ICODE<6:0>							0000
C1FCTRL	0406	DMABS<2:0>			—	—	—	—	—	—	—	—	FSA<4:0>					0000
C1FIFO	0408	—	—	FBP<5:0>						—	—	FNRB<5:0>						0000
C1INTF	040A	—	—	TXBO	TXBP	RXBP	TXWAR	RXWAR	EWARN	IVRIF	WAKIF	ERRIF	—	FIFOIF	RBOVIF	RBIF	TBIF	0000
C1INTE	040C	—	—	—	—	—	—	—	—	IVRIE	WAKIE	ERRIE	—	FIFOIE	RBOVIE	RBIE	TBIE	0000
C1EC	040E	TERRCNT<7:0>								RERRCNT<7:0>								0000
C1CFG1	0410	—	—	—	—	—	—	—	—	SJW<1:0>		BRP<5:0>						0000
C1CFG2	0412	—	WAKFIL	—	—	—	SEG2PH<2:0>			SEG2PHTS	SAM	SEG1PH<2:0>			PRSEG<2:0>			0000
C1FEN1	0414	FLTEN15	FLTEN14	FLTEN13	FLTEN12	FLTEN11	FLTEN10	FLTEN9	FLTEN8	FLTEN7	FLTEN6	FLTEN5	FLTEN4	FLTEN3	FLTEN2	FLTEN1	FLTEN0	FFFF
C1FMSKSEL1	0418	F7MSK<1:0>		F6MSK<1:0>		F5MSK<1:0>		F4MSK<1:0>		F3MSK<1:0>		F2MSK<1:0>		F1MSK<1:0>		F0MSK<1:0>		0000
C1FMSKSEL2	041A	F15MSK<1:0>		F14MSK<1:0>		F13MSK<1:0>		F12MSK<1:0>		F11MSK<1:0>		F10MSK<1:0>		F9MSK<1:0>		F8MSK<1:0>		0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal for PinHigh devices.

PIC24HJXXXGPX06A/X08A/X10A

REGISTER 7-22: IPC7: INTERRUPT PRIORITY CONTROL REGISTER 7

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	U2TXIP<2:0>			—	U2RXIP<2:0>		
bit 15				bit 8			

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	INT2IP<2:0>			—	T5IP<2:0>		
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15 **Unimplemented:** Read as '0'
- bit 14-12 **U2TXIP<2:0>:** UART2 Transmitter Interrupt Priority bits
 111 = Interrupt is priority 7 (highest priority interrupt)
 .
 .
 .
 001 = Interrupt is priority 1
 000 = Interrupt source is disabled
- bit 11 **Unimplemented:** Read as '0'
- bit 10-8 **U2RXIP<2:0>:** UART2 Receiver Interrupt Priority bits
 111 = Interrupt is priority 7 (highest priority interrupt)
 .
 .
 .
 001 = Interrupt is priority 1
 000 = Interrupt source is disabled
- bit 7 **Unimplemented:** Read as '0'
- bit 6-4 **INT2IP<2:0>:** External Interrupt 2 Priority bits
 111 = Interrupt is priority 7 (highest priority interrupt)
 .
 .
 .
 001 = Interrupt is priority 1
 000 = Interrupt source is disabled
- bit 3 **Unimplemented:** Read as '0'
- bit 2-0 **T5IP<2:0>:** Timer5 Interrupt Priority bits
 111 = Interrupt is priority 7 (highest priority interrupt)
 .
 .
 .
 001 = Interrupt is priority 1
 000 = Interrupt source is disabled

9.2 Clock Switching Operation

Applications are free to switch between any of the four clock sources (Primary, LP, FRC and LPRC) under software control at any time. To limit the possible side effects that could result from this flexibility, PIC24HJXXXGPX06A/X08A/X10A devices have a safeguard lock built into the switch process.

Note: Primary Oscillator mode has three different submodes (XT, HS and EC) which are determined by the POSCMD<1:0> Configuration bits. While an application can switch to and from Primary Oscillator mode in software, it cannot switch between the different primary submodes without reprogramming the device.

9.2.1 ENABLING CLOCK SWITCHING

To enable clock switching, the FCKSM1 Configuration bit in the Configuration register must be programmed to '0'. (Refer to **Section 21.1 "Configuration Bits"** for further details.) If the FCKSM1 Configuration bit is unprogrammed ('1'), the clock switching function and Fail-Safe Clock Monitor function are disabled. This is the default setting.

The NOSC control bits (OSCCON<10:8>) do not control the clock selection when clock switching is disabled. However, the COSC bits (OSCCON<14:12>) reflect the clock source selected by the FNOSC Configuration bits.

The OSWEN control bit (OSCCON<0>) has no effect when clock switching is disabled. It is held at '0' at all times.

9.2.2 OSCILLATOR SWITCHING SEQUENCE

At a minimum, performing a clock switch requires this basic sequence:

1. If desired, read the COSC bits (OSCCON<14:12>) to determine the current oscillator source.
2. Perform the unlock sequence to allow a write to the OSCCON register high byte.
3. Write the appropriate value to the NOSC control bits (OSCCON<10:8>) for the new oscillator source.
4. Perform the unlock sequence to allow a write to the OSCCON register low byte.
5. Set the OSWEN bit to initiate the oscillator switch.

Once the basic sequence is completed, the system clock hardware responds automatically as follows:

1. The clock switching hardware compares the COSC status bits with the new value of the NOSC control bits. If they are the same, the clock switch is a redundant operation. In this case, the OSWEN bit is cleared automatically and the clock switch is aborted.

2. If a valid clock switch has been initiated, the LOCK (OSCCON<5>) and the CF (OSCCON<3>) status bits are cleared.
3. The new oscillator is turned on by the hardware if it is not currently running. If a crystal oscillator must be turned on, the hardware waits until the Oscillator Start-up Timer (OST) expires. If the new source is using the PLL, the hardware waits until a PLL lock is detected (LOCK = 1).
4. The hardware waits for 10 clock cycles from the new clock source and then performs the clock switch.
5. The hardware clears the OSWEN bit to indicate a successful clock transition. In addition, the NOSC bit values are transferred to the COSC status bits.
6. The old clock source is turned off at this time, with the exception of LPRC (if WDT or FSCM are enabled) or LP (if LPOSCEN remains set).

Note 1: The processor continues to execute code throughout the clock switching sequence. Timing sensitive code should not be executed during this time.

- 2: Direct clock switches between any primary oscillator mode with PLL and FRCPLL mode are not permitted. This applies to clock switches in either direction. In these instances, the application must switch to FRC mode as a transition clock source between the two PLL modes.

- 3: Refer to **Section 7. "Oscillator"** (DS70186) in the *"dsPIC33F/PIC24H Family Reference Manual"* for details.

9.3 Fail-Safe Clock Monitor (FSCM)

The Fail-Safe Clock Monitor (FSCM) allows the device to continue to operate even in the event of an oscillator failure. The FSCM function is enabled by programming. If the FSCM function is enabled, the LPRC internal oscillator runs at all times (except during Sleep mode) and is not subject to control by the Watchdog Timer.

If an oscillator failure occurs, the FSCM generates a clock failure trap event and switches the system clock over to the FRC oscillator. Then the application program can either attempt to restart the oscillator or execute a controlled shutdown. The trap can be treated as a warm Reset by simply loading the Reset address into the oscillator fail trap vector.

If the PLL multiplier is used to scale the system clock, the internal FRC is also multiplied by the same factor on clock failure. Essentially, the device switches to FRC with PLL on a clock failure.

PIC24HJXXXGPX06A/X08A/X10A

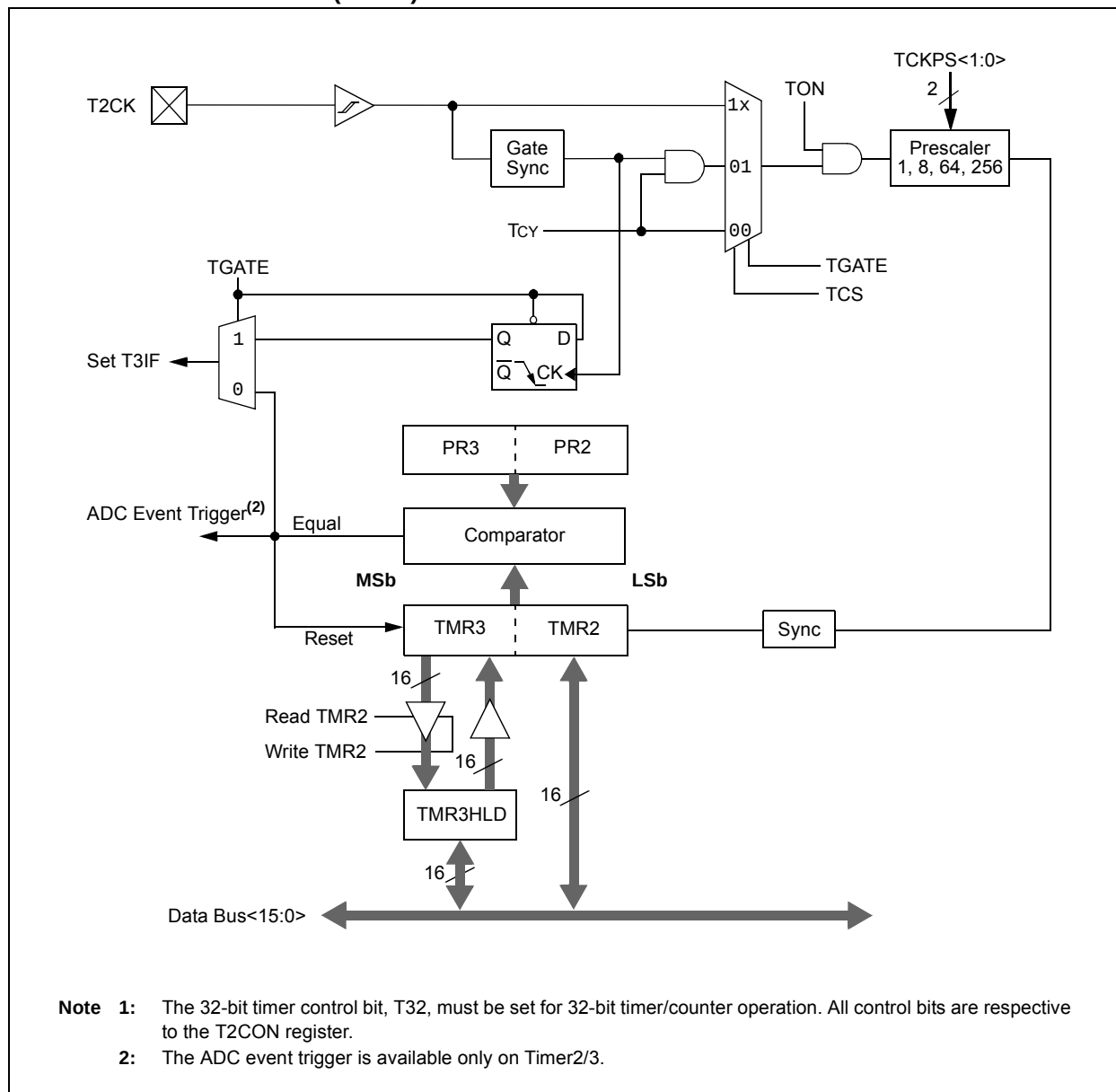
NOTES:

PIC24HJXXXGPX06A/X08A/X10A

A block diagram for a 32-bit timer pair (Timer4/5) example is shown in Figure 13-1 and a timer (Timer4) operating in 16-bit mode example is shown in Figure 13-2.

Note: Only Timer2 and Timer3 can trigger a DMA data transfer.

FIGURE 13-1: TIMER2/3 (32-BIT) BLOCK DIAGRAM⁽¹⁾



PIC24HJXXXGPX06A/X08A/X10A

NOTES:

PIC24HJXXXGPX06A/X08A/X10A

REGISTER 19-7: CIINTE: ECAN™ MODULE INTERRUPT ENABLE REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
IVRIE	WAKIE	ERRIE	—	FIFOIE	RBOVIE	RBIE	TBIE
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15-8 **Unimplemented:** Read as '0'
- bit 7 **IVRIE:** Invalid Message Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled
- bit 6 **WAKIE:** Bus Wake-up Activity Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled
- bit 5 **ERRIE:** Error Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled
- bit 4 **Unimplemented:** Read as '0'
- bit 3 **FIFOIE:** FIFO Almost Full Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled
- bit 2 **RBOVIE:** RX Buffer Overflow Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled
- bit 1 **RBIE:** RX Buffer Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled
- bit 0 **TBIE:** TX Buffer Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

PIC24HJXXXGPX06A/X08A/X10A

REGISTER 19-16: CiRxFnSID: ECAN™ MODULE ACCEPTANCE FILTER n STANDARD IDENTIFIER
(n = 0, 1, ..., 15)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
SID<10:3>							
bit 15				bit 8			

R/W-x	R/W-x	R/W-x	U-0	R/W-x	U-0	R/W-x	R/W-x
SID<2:0>			—	EXIDE	—	EID<17:16>	
bit 7			bit 0				

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15-5 **SID<10:0>**: Standard Identifier bits
 1 = Message address bit SIDx must be '1' to match filter
 0 = Message address bit SIDx must be '0' to match filter
- bit 4 **Unimplemented**: Read as '0'
- bit 3 **EXIDE**: Extended Identifier Enable bit
 If MIDE = 1:
 1 = Match only messages with extended identifier addresses
 0 = Match only messages with standard identifier addresses
 If MIDE = 0:
 Ignore EXIDE bit.
- bit 2 **Unimplemented**: Read as '0'
- bit 1-0 **EID<17:16>**: Extended Identifier bits
 1 = Message address bit EIDx must be '1' to match filter
 0 = Message address bit EIDx must be '0' to match filter

REGISTER 19-17: CiRxFnEID: ECAN™ MODULE ACCEPTANCE FILTER n EXTENDED IDENTIFIER
(n = 0, 1, ..., 15)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID<15:8>							
bit 15				bit 8			

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15-0 **EID<15:0>**: Extended Identifier bits
 1 = Message address bit EIDx must be '1' to match filter
 0 = Message address bit EIDx must be '0' to match filter

PIC24HJXXXGPX06A/X08A/X10A

REGISTER 20-9: AD1PCFGH: ADC1 PORT CONFIGURATION REGISTER HIGH^(1,2,3,4)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PCFG31	PCFG30	PCFG29	PCFG28	PCFG27	PCFG26	PCFG25	PCFG24
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PCFG23	PCFG22	PCFG21	PCFG20	PCFG19	PCFG18	PCFG17	PCFG16
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **PCFG<31:16>:** ADC Port Configuration Control bits

1 = Port pin in Digital mode, port read input enabled, ADC input multiplexer connected to AVss

0 = Port pin in Analog mode, port read input disabled, ADC samples pin voltage

Note 1: On devices without 32 analog inputs, all PCFG bits are R/W by user. However, PCFG bits are ignored on ports without a corresponding input on device.

2: ADC2 only supports analog inputs AN0-AN15; therefore, no ADC2 high port Configuration register exists.

3: PCFGx = ANx, where x = 16 through 31.

4: PCFGx bits will have no effect if ADC module is disabled by setting ADxMD bit in the PMDx register. In this case all port pins multiplexed with ANx will be in Digital mode.

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TABLE 22-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles	Status Flags Affected
12	BTST	BTST f, #bit4	Bit Test f	1	1	Z
		BTST.C ws, #bit4	Bit Test Ws to C	1	1	C
		BTST.Z ws, #bit4	Bit Test Ws to Z	1	1	Z
		BTST.C ws, Wb	Bit Test Ws<Wb> to C	1	1	C
		BTST.Z ws, Wb	Bit Test Ws<Wb> to Z	1	1	Z
13	BTSTS	BTSTS f, #bit4	Bit Test then Set f	1	1	Z
		BTSTS.C ws, #bit4	Bit Test Ws to C, then Set	1	1	C
		BTSTS.Z ws, #bit4	Bit Test Ws to Z, then Set	1	1	Z
14	CALL	CALL lit23	Call subroutine	2	2	None
		CALL Wn	Call indirect subroutine	1	2	None
15	CLR	CLR f	f = 0x0000	1	1	None
		CLR WREG	WREG = 0x0000	1	1	None
		CLR ws	Ws = 0x0000	1	1	None
16	CLRWDT	CLRWDT	Clear Watchdog Timer	1	1	WDTO, Sleep
17	COM	COM f	f = $\bar{f}$	1	1	N, Z
		COM f, WREG	WREG = $\bar{f}$	1	1	N, Z
		COM ws, Wd	Wd = $\overline{Ws}$	1	1	N, Z
18	CP	CP f	Compare f with WREG	1	1	C, DC, N, OV, Z
		CP Wb, #lit5	Compare Wb with lit5	1	1	C, DC, N, OV, Z
		CP Wb, Ws	Compare Wb with Ws (Wb – Ws)	1	1	C, DC, N, OV, Z
19	CP0	CP0 f	Compare f with 0x0000	1	1	C, DC, N, OV, Z
		CP0 ws	Compare Ws with 0x0000	1	1	C, DC, N, OV, Z
20	CPB	CPB f	Compare f with WREG, with Borrow	1	1	C, DC, N, OV, Z
		CPB Wb, #lit5	Compare Wb with lit5, with Borrow	1	1	C, DC, N, OV, Z
		CPB Wb, Ws	Compare Wb with Ws, with Borrow (Wb – Ws – C)	1	1	C, DC, N, OV, Z
21	CPSEQ	CPSEQ Wb, Wn	Compare Wb with Wn, skip if =	1	1 (2 or 3)	None
22	CPSGT	CPSGT Wb, Wn	Compare Wb with Wn, skip if >	1	1 (2 or 3)	None
23	CPSLT	CPSLT Wb, Wn	Compare Wb with Wn, skip if <	1	1 (2 or 3)	None
24	CPSNE	CPSNE Wb, Wn	Compare Wb with Wn, skip if ≠	1	1 (2 or 3)	None
25	DAW	DAW Wn	Wn = decimal adjust Wn	1	1	C
26	DEC	DEC f	f = f – 1	1	1	C, DC, N, OV, Z
		DEC f, WREG	WREG = f – 1	1	1	C, DC, N, OV, Z
		DEC ws, Wd	Wd = Ws – 1	1	1	C, DC, N, OV, Z
27	DEC2	DEC2 f	f = f – 2	1	1	C, DC, N, OV, Z
		DEC2 f, WREG	WREG = f – 2	1	1	C, DC, N, OV, Z
		DEC2 ws, Wd	Wd = Ws – 2	1	1	C, DC, N, OV, Z
28	DISI	DISI #lit14	Disable Interrupts for k instruction cycles	1	1	None
29	DIV	DIV.S Wm, Wn	Signed 16/16-bit Integer Divide	1	18	N, Z, C, OV
		DIV.SD Wm, Wn	Signed 32/16-bit Integer Divide	1	18	N, Z, C, OV
		DIV.U Wm, Wn	Unsigned 16/16-bit Integer Divide	1	18	N, Z, C, OV
		DIV.UD Wm, Wn	Unsigned 32/16-bit Integer Divide	1	18	N, Z, C, OV
30	EXCH	EXCH Wns, Wnd	Swap Wns with Wnd	1	1	None
31	FBCL	FBCL ws, Wnd	Find Bit Change from Left (MSb) Side	1	1	C
32	FF1L	FF1L ws, Wnd	Find First One from Left (MSb) Side	1	1	C
33	FF1R	FF1R ws, Wnd	Find First One from Right (LSb) Side	1	1	C
34	GOTO	GOTO Expr	Go to address	2	2	None
		GOTO Wn	Go to indirect	1	2	None

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TABLE 24-7: DC CHARACTERISTICS: POWER-DOWN CURRENT (IPD)

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended			
Parameter No. ⁽³⁾	Typical ⁽²⁾	Max	Units	Conditions		
Power-Down Current (IPD) ⁽¹⁾						
DC60d	50	200	μA	-40°C	3.3V	Base Power-Down Current ⁽³⁾
DC60a	50	200	μA	+25°C		
DC60b	200	500	μA	+85°C		
DC60c	600	1000	μA	+125°C		
DC61d	8	13	μA	-40°C	3.3V	Watchdog Timer Current: ΔIWD _T ⁽³⁾
DC61a	10	15	μA	+25°C		
DC61b	12	20	μA	+85°C		
DC61c	13	25	μA	+125°C		

Note 1: IPD (Sleep) current is measured as follows:

- CPU core is off, oscillator is configured in EC mode and external clock active, OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration word
- All I/O pins are configured as inputs and pulled to Vss
- $\text{MCLR} = \text{VDD}$, WDT and FSCM are disabled, all peripheral modules except the ADC are disabled (PMDx bits are all '1's). The following ADC settings are enabled for each ADC module (ADCx) prior to executing the PWRSAV instruction: ADON = 1, VCFG = 1, AD12B = 1 and ADxMD = 0.
- VREGS bit (RCON<8>) = 0 (i.e., core regulator is set to stand-by while the device is in Sleep mode)
- RTCC is disabled.
- JTAG is disabled

2: Data in the "Typ" column is at 3.3V, +25°C unless otherwise stated.

3: The Watchdog Timer Current is the additional current consumed when the WDT module is enabled. This current should be added to the base IPD current.

4: These currents are measured on the device containing the most memory in this family.

5: These parameters are characterized, but are not tested in manufacturing.

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FIGURE 24-3: CLKO AND I/O TIMING CHARACTERISTICS

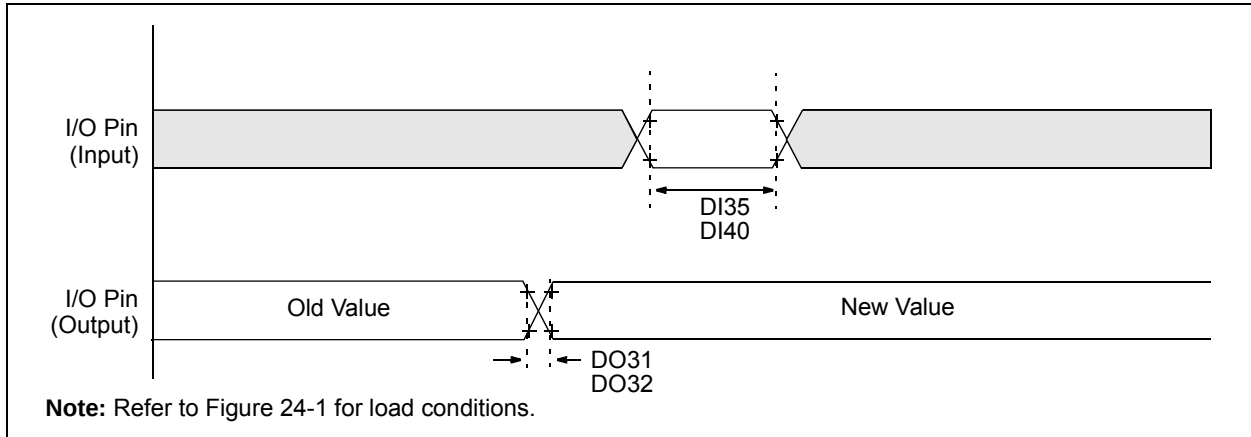


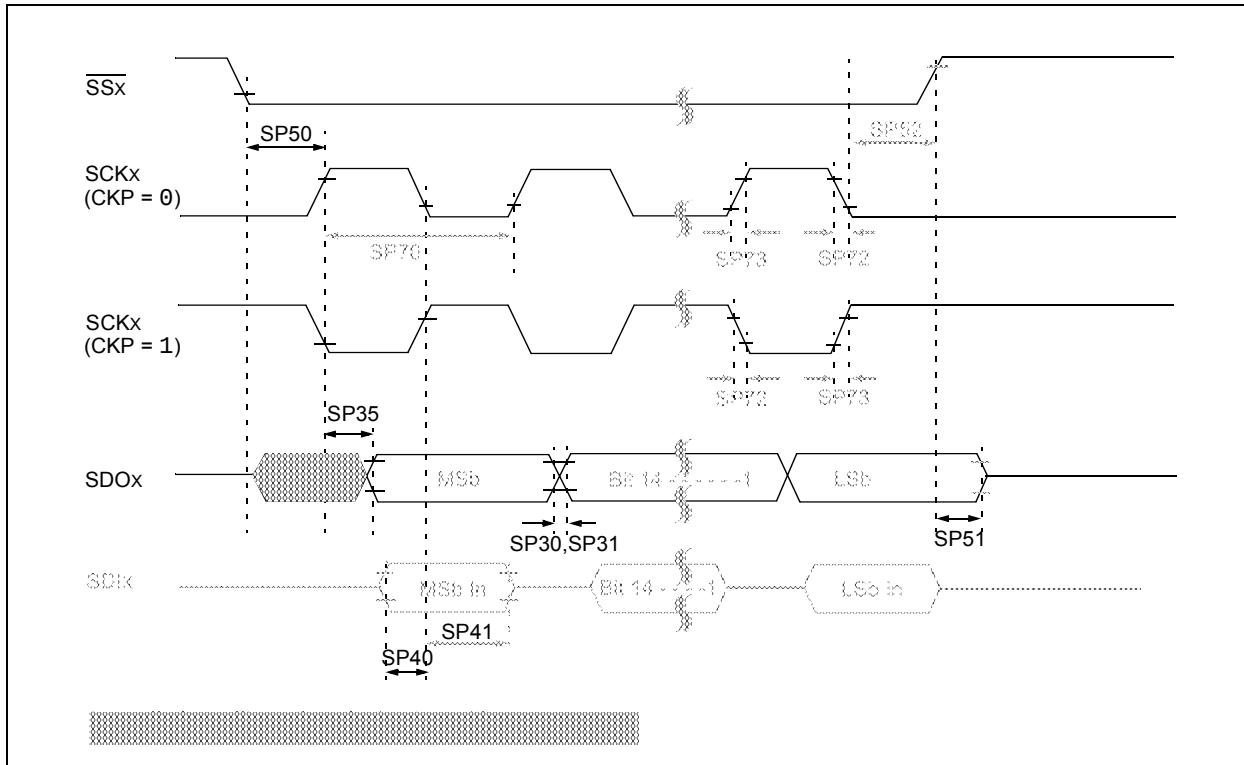
TABLE 24-20: I/O TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)				
			Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param No.	Symbol	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Conditions
DO31	TioR	Port Output Rise Time	—	10	25	ns	—
DO32	TioF	Port Output Fall Time	—	10	25	ns	—
DI35	TINP	INTx Pin High or Low Time (input)	20	—	—	ns	—
DI40	TRBP	CNx High or Low Time (input)	2	—	—	Tcy	—

Note 1: Data in “Typ” column is at 3.3V, 25°C unless otherwise stated.

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FIGURE 24-15: SPIx SLAVE MODE (FULL-DUPLEX CKE = 0, CKP = 1, SMP = 0) TIMING CHARACTERISTICS



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TABLE 25-14: ADC MODULE SPECIFICATIONS

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$ for High Temperature					
Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
Reference Inputs							
HAD08	IREF	Current Drain	—	250	600	μA	ADC operating, See Note 1
			—	—	50	μA	ADC off, See Note 1

Note 1: These parameters are not characterized or tested in manufacturing.

2: These parameters are characterized, but are not tested in manufacturing.

TABLE 25-15: ADC MODULE SPECIFICATIONS (12-BIT MODE)⁽³⁾

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$ for High Temperature					
Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
ADC Accuracy (12-bit Mode) – Measurements with external VREF+/VREF- ⁽¹⁾							
AD23a	GERR	Gain Error	—	5	10	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V
AD24a	EOFF	Offset Error	—	2	5	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V
ADC Accuracy (12-bit Mode) – Measurements with internal VREF+/VREF- ⁽¹⁾							
AD23a	GERR	Gain Error	2	10	20	LSb	VINL = AVSS = 0V, AVDD = 3.6V
AD24a	EOFF	Offset Error	2	5	10	LSb	VINL = AVSS = 0V, AVDD = 3.6V
Dynamic Performance (12-bit Mode) ⁽²⁾							
HAD33a	FNYQ	Input Signal Bandwidth	—	—	200	kHz	—

Note 1: These parameters are characterized, but are tested at 20 kps only.

2: These parameters are characterized by similarity, but are not tested in manufacturing.

3: Injection currents $> |0|$ can affect the ADC results by approximately 4-6 counts.

TABLE 25-16: ADC MODULE SPECIFICATIONS (10-BIT MODE)⁽³⁾

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$ for High Temperature					
Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
ADC Accuracy (12-bit Mode) – Measurements with external VREF+/VREF- ⁽¹⁾							
AD23b	GERR	Gain Error	—	3	6	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V
AD24b	EOFF	Offset Error	—	2	5	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V
ADC Accuracy (12-bit Mode) – Measurements with internal VREF+/VREF- ⁽¹⁾							
AD23b	GERR	Gain Error	—	7	15	LSb	VINL = AVSS = 0V, AVDD = 3.6V
AD24b	EOFF	Offset Error	—	3	7	LSb	VINL = AVSS = 0V, AVDD = 3.6V
Dynamic Performance (10-bit Mode) ⁽²⁾							
HAD33b	FNYQ	Input Signal Bandwidth	—	—	400	kHz	—

Note 1: These parameters are characterized, but are tested at 20 kps only.

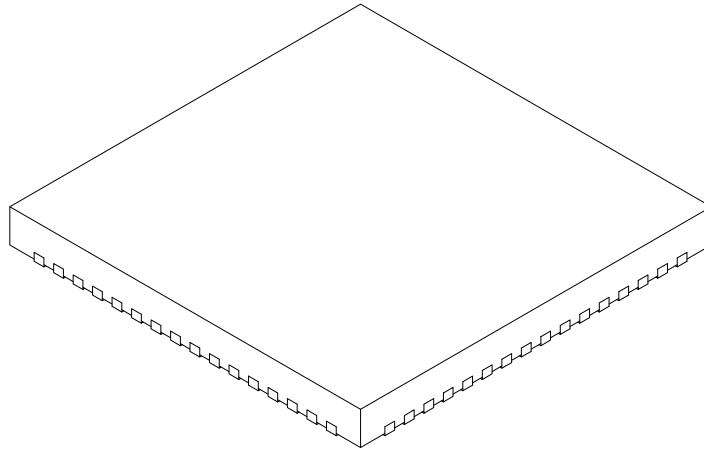
2: These parameters are characterized by similarity, but are not tested in manufacturing.

3: Injection currents $> |0|$ can affect the ADC results by approximately 4-6 counts.

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64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body with 5.40 x 5.40 Exposed Pad [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	64		
Pitch	e	0.50 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3	0.20 REF		
Overall Width	E	9.00 BSC		
Exposed Pad Width	E2	5.30	5.40	5.50
Overall Length	D	9.00 BSC		
Exposed Pad Length	D2	5.30	5.40	5.50
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 - REF: Reference Dimension, usually without tolerance, for information purposes only.

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TABLE B-2: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
Section 24.0 “Electrical Characteristics”	Removed Note 4 from the DC Temperature and Voltage Specifications (see Table 24-4). Updated the maximum value for parameter DI19 and added parameters DI28, DI29, DI60a, DI60b, and DI60c to the I/O Pin Input Specifications (see Table 24-9). Removed Note 2 from the AC Characteristics: Internal RC Accuracy (see Table 24-18). Updated the characteristic description for parameter DI35 in the I/O Timing Requirements (see Table 24-20). Updated the ADC Module Specification minimum values for parameters AD05 and AD07, and updated the maximum value for parameter AD06 (see Table 24-39). Added Note 1 to the ADC Module Specifications (12-bit Mode) (see Table 24-40). Added Note 1 to the ADC Module Specifications (10-bit Mode) (see Table 24-41). Added DMA Read/Write Timing Requirements (see Table 24-44).
Section 25.0 “High Temperature Electrical Characteristics”	Updated all ambient temperature end range values to +150°C throughout the chapter. Updated the storage temperature end range to +160°C. Updated the maximum junction temperature from +145°C to +155°C. Updated the maximum values for High Temperature Devices in the Thermal Operating Conditions (see Table 25-2). Added Note 3 and updated the ADC Module Specifications (12-bit Mode), removing all parameters with the exception of HAD33a (see Table 25-15). Added Note 3 and updated the ADC Module Specifications (10-bit Mode), removing all parameters with the exception of HAD33b (see Table 25-16).

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