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### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

### Details

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Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	40 MIPs
Connectivity	CANbus, I <sup>2</sup> C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	53
Program Memory Size	64KB (22K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 18x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24hj64gp506a-i-mr

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### Pin Diagrams (Continued)



### 3.0 CPU

- Note 1: This data sheet summarizes the features of the PIC24HJXXXGPX06A/X08A/X10A family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 2. "CPU" (DS70204) of the "dsPIC33F/PIC24H Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
  - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The PIC24HJXXXGPX06A/X08A/X10A CPU module has a 16-bit (data) modified Harvard architecture with an enhanced instruction set and addressing modes. The CPU has a 24-bit instruction word with a variable length opcode field. The Program Counter (PC) is 23 bits wide and addresses up to 4M x 24 bits of user program memory space. The actual amount of program memory implemented varies by device. A single-cycle instruction prefetch mechanism is used to help maintain throughput and provides predictable execution. All instructions execute in a single cycle, with the exception of instructions that change the program flow, the double word move (MOV.D) instruction and the table instructions. Overhead-free, single-cycle program loop constructs are supported using the REPEAT instruction, which is interruptible at any point.

The PIC24HJXXXGPX06A/X08A/X10A devices have sixteen, 16-bit working registers in the programmer's model. Each of the working registers can serve as a data, address or address offset register. The 16th working register (W15) operates as a software Stack Pointer (SP) for interrupts and calls.

The PIC24HJXXXGPX06A/X08A/X10A instruction set includes many addressing modes and is designed for optimum C compiler efficiency. For most instructions, the PIC24HJXXXGPX06A/X08A/X10A is capable of executing a data (or program data) memory read, a working register (data) read, a data memory write and a program (instruction) memory read per instruction cycle. As a result, three parameter instructions can be supported, allowing A + B = C operations to be executed in a single cycle.

A block diagram of the CPU is shown in Figure 3-1, and the programmer's model for the PIC24HJXXXGPX06A/X08A/X10A is shown in Figure 3-2.

### 3.1 Data Addressing Overview

The data space can be linearly addressed as 32K words or 64 Kbytes using an Address Generation Unit (AGU). The upper 32 Kbytes of the data space memory map can optionally be mapped into program space at any 16K program word boundary defined by the 8-bit Program Space Visibility Page (PSVPAG) register. The program to data space mapping feature lets any instruction access program space as if it were data space.

The data space also includes 2 Kbytes of DMA RAM, which is primarily used for DMA data transfers, but may be used as general purpose RAM.

### 3.2 Special MCU Features

The PIC24HJXXXGPX06A/X08A/X10A features a 17-bit by 17-bit, single-cycle multiplier. The multiplier can perform signed, unsigned and mixed-sign multiplication. Using a 17-bit by 17-bit multiplier for 16-bit by 16-bit multiplication makes mixed-sign multiplication possible.

The PIC24HJXXXGPX06A/X08A/X10A supports 16/16 and 32/16 integer divide operations. All divide instructions are iterative operations. They must be executed within a REPEAT loop, resulting in a total execution time of 19 instruction cycles. The divide operation can be interrupted during any of those 19 cycles without loss of data.

A multi-bit data shifter is used to perform up to a 16-bit, left or right shift in a single cycle.



### FIGURE 4-3: DATA MEMORY MAP FOR PIC24HJXXXGPX06A/X08A/X10A DEVICES WITH 8 KB

IADLE 4-	<u>o.</u>	JUIFU			EGIST		F											
SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
OC1RS	0180							Ou	tput Compar	e 1 Second	ary Register							xxxx
OC1R	0182								Output Co	ompare 1 Re	egister							xxxx
OC1CON	0184	—	_	OCSIDL	—	—	_	_	_	_	_	_	OCFLT	OCTSEL		OCM<2:0>		0000
OC2RS	0186							Ou	tput Compar	e 2 Second	ary Register							xxxx
OC2R	0188								Output Co	ompare 2 Re	egister							xxxx
OC2CON	018A	_	_	OCSIDL	_	_	_	_	_	_	_	_	OCFLT	OCTSEL		OCM<2:0>		0000
OC3RS	018C							Ou	tput Compar	e 3 Second	ary Register							xxxx
OC3R	018E								Output Co	ompare 3 Re	egister							xxxx
OC3CON	0190	_	_	OCSIDL	_	_	_	_	_	_	_	_	OCFLT	OCTSEL		OCM<2:0>		0000
OC4RS	0192							Ou	tput Compar	e 4 Second	ary Register							XXXX
OC4R	0194								Output Co	ompare 4 Re	egister							XXXX
OC4CON	0196	_	—	OCSIDL	—	—	_	_	_	_	—	—	OCFLT	OCTSEL		OCM<2:0>		0000
OC5RS	0198							Ou	tput Compar	e 5 Second	ary Register							xxxx
OC5R	019A								Output Co	ompare 5 Re	egister							xxxx
OC5CON	019C		—	OCSIDL	—	—	_	—		_	—	—	OCFLT	OCTSEL		OCM<2:0>		0000
OC6RS	019E							Ou	tput Compar	e 6 Second	ary Register							xxxx
OC6R	01A0								Output Co	ompare 6 Re	egister							xxxx
OC6CON	01A2	_	_	OCSIDL	_	_	_	_		_	_	_	OCFLT	OCTSEL		OCM<2:0>		0000
OC7RS	01A4							Ou	tput Compar	e 7 Second	ary Register							xxxx
OC7R	01A6								Output Co	ompare 7 Re	egister							xxxx
OC7CON	01A8		—	OCSIDL	—	—	_	—		_	—	—	OCFLT	OCTSEL		OCM<2:0>		0000
OC8RS	01AA							Ou	tput Compar	e 8 Second	ary Register							xxxx
OC8R	01AC								Output Co	ompare 8 Re	egister							xxxx
OC8CON	01AE	_	_	OCSIDL	_	_		_			_	_	OCFLT	OCTSEL		OCM<2:0>		0000
1 1						1 (-1					<b>D</b>							

### TABLE 4-8: OUTPUT COMPARE REGISTER MAP

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal for PinHigh devices.

# \_\_\_\_\_

### TABLE 4-12: UART2 REGISTER MAP

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
U2MODE	0230	UARTEN	—	USIDL	IREN	RTSMD	_	UEN1	UEN0	WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSE	_<1:0>	STSEL	0000
U2STA	0232	UTXISEL1	UTXINV	UTXISEL0	_	UTXBRK	UTXEN	UTXBF	TRMT	URXISE	EL<1:0>	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
U2TXREG	0234	_	_	_	_	_	-					UART	Transmit Re	egister				xxxx
U2RXREG	0236	_	_	_	_	_	-					UART	Receive Re	gister				0000
U2BRG	0238							Bauc	Rate Gen	erator Presca	aler							0000

Legend: x = unknown value on Reset, - = unimplemented, read as '0'. Reset values are shown in hexadecimal for PinHigh devices.

### TABLE 4-13: SPI1 REGISTER MAP

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
SPI1STAT	0240	SPIEN	_	SPISIDL	_	_	—	—	—	_	SPIROV	_	—	—	—	SPITBF	SPIRBF	0000
SPI1CON1	0242	_	_	_	DISSCK	DISSDO	MODE16	SMP	CKE	SSEN	CKP	MSTEN		SPRE<2:0>	<b>`</b>	PPRE	<1:0>	0000
SPI1CON2	0244	FRMEN	SPIFSD	FRMPOL	_	_	_	_	_	—	_	_	_	—	_	FRMDLY	—	0000
SPI1BUF	0248							SPI1 Trans	smit and Re	ceive Buffer	Register							0000

Legend: x = unknown value on Reset, - = unimplemented, read as '0'. Reset values are shown in hexadecimal for PinHigh devices.

### TABLE 4-14: SPI2 REGISTER MAP

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
SPI2STAT	0260	SPIEN	—	SPISIDL	_	—	_	-	_	-	SPIROV	—	_	—	_	SPITBF	SPIRBF	0000
SPI2CON1	0262	_	_	_	DISSCK	DISSDO	MODE16	SMP	CKE	SSEN	CKP	MSTEN		SPRE<2:0>		PPRE	<1:0>	0000
SPI2CON2	0264	FRMEN	SPIFSD	FRMPOL	_	_	_	_	_	_	_	_	_	_	_	FRMDLY	_	0000
SPI2BUF	0268							SPI2 Tran	smit and Re	ceive Buffer	Register							0000

Legend: x = unknown value on Reset, - = unimplemented, read as '0'. Reset values are shown in hexadecimal for PinHigh devices.

### REGISTER 7-3: INTCON1: INTERRUPT CONTROL REGISTER 1

R/W-0	U-0						
NSTDIS	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
—	DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFAIL	—
bit 7							bit 0

Legend:				
R = Readable	bit	W = Writable bit	U = Unimplemented bit,	read as '0'
-n = Value at F	POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
bit 15	NSTDIS:	nterrupt Nesting Disable bit	t	
	1 = Interru	pt nesting is disabled		
	0 = Interru	ipt nesting is enabled		
bit 14-7	Unimplem	nented: Read as '0'		
bit 6	DIV0ERR:	Arithmetic Error Status bit		
	1 = Math e	error trap was caused by a c	divide by zero v a divide by zero	
bit 5	DMACER	R: DMA Controller Error Sta	atus bit	
	1 = DMA c	controller error trap has occ	urred	
	0 = DMA c	controller error trap has not	occurred	
bit 4	MATHERF	R: Arithmetic Error Status bi	t	
	1 = Math e	error trap has occurred		
	0 = Math e	error trap has not occurred		
bit 3	ADDRER	R: Address Error Trap Statu	is bit	
	1 = Addres	ss error trap has occurred	a d	
1.11 O		ss error trap has not occurre	ea	
bit 2	SIKERR:	Stack Error Trap Status bit		
	$\perp = Stack$	error trap has occurred		
hit 1		Chor trap has not occurred	tue hit	
DIL		tor failure trap has occurred	d	
	1 = Oscillar0 = Oscillar	ator failure trap has occurre	urred	
bit 0	Unimplem	nented: Read as '0'		
	-			

### REGISTER 7-5: IFS0: INTERRUPT FLAG STATUS REGISTER 0

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DMA1IF	AD1IF	U1TXIF	U1RXIF	SPI1IF	SPI1EIF	T3IF
bit 15							bit 8
<b></b>							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
T2IF	OC2IF	IC2IF	DMA01IF	T1IF	OC1IF	IC1IF	INT0IF
bit 7							bit 0
Logond							
R = Readable	bit	W = Writable	bit	l I = l Inimplei	mented hit read	d as '0'	
-n = Value at F	POR	'1' = Bit is se	t	'0' = Bit is cle	eared	x = Bit is unkn	iown
			-				-
bit 15	Unimplemen	ted: Read as	0'				
bit 14	DMA1IF: DM	A Channel 1 D	ata Transfer C	Complete Interr	rupt Flag Status	bit	
	1 = Interrupt r 0 = Interrupt r	request has oc request has no	curred t occurred				
bit 13	AD1IF: ADC1	Conversion C	Complete Interi	rupt Flag Statu	is bit		
	1 = Interrupt r 0 = Interrupt r	request has oc request has no	curred t occurred				
bit 12	U1TXIF: UAR	RT1 Transmitte	r Interrupt Flag	g Status bit			
	1 = Interrupt r	request has oc	curred				
	0 = Interrupt r	request has no	t occurred				
DIT 11		KI 1 Receiver I	nterrupt Flag S	Status dit			
	0 = Interrupt r	request has oc	t occurred				
bit 10	SPI1IF: SPI1	Event Interrup	ot Flag Status b	oit			
	1 = Interrupt r 0 = Interrupt r	request has oc request has no	curred t occurred				
bit 9	SPI1EIF: SPI	1 Fault Interru	pt Flag Status	bit			
	1 = Interrupt r	request has oc	curred				
<b>h</b> :t 0	0 = Interrupt r	request has no	t occurred				
DIT 8	1 3IF: Inmer3	Interrupt Flag	Status bit				
	0 = Interrupt r	request has oc	t occurred				
bit 7	T2IF: Timer2	Interrupt Flag	Status bit				
	1 = Interrupt r	request has oc	curred				
		request has no	t occurred		1.11		
bit 6	1 = Interrupt r	ut Compare Cr	annel 2 Interr	upt Flag Status	s dit		
	0 = Interrupt r	request has oc	t occurred				
bit 5	IC2IF: Input C	Capture Chann	el 2 Interrupt I	-lag Status bit			
	1 = Interrupt r	request has oc	curred				
	0 = Interrupt r	request has no	t occurred			- I- 14	
DIT 4	1 = Interrupt r	VIA Channel U		Complete Inte	rrupt Flag Statu	IS DIT	
	0 = Interrupt r	request has no	t occurred				
bit 3	T1IF: Timer1	Interrupt Flag	Status bit				
	1 = Interrupt r	request has oc	curred				
	0 = Interrupt r	request has no	t occurred				

REGISTER 7-6:	IFS1: INTERRUPT FLAG STATUS REGISTER 1
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R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
U2TXIF	U2RXIF	INT2IF	T5IF	T4IF	OC4IF	OC3IF	DMA21IF
bit 15							bit 8
<b></b>							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
IC8IF	IC7IF	AD2IF	INT1IF	CNIF	—	MI2C1IF	SI2C1IF
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimple	mented bit read	1 as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unkr	nown
bit 15	U2TXIF: UAF	RT2 Transmitter	Interrupt Fla	g Status bit			
	1 = Interrupt i	request has occ	curred				
	0 = Interrupt i	request has not	occurred				
bit 14	U2RXIF: UAF	RT2 Receiver Ir	nterrupt Flag	Status bit			
	1 = Interrupt i	request has occ request has not	currea t occurred				
bit 13	INT2IF: Exter	nal Interrupt 2	Flag Status b	it			
	1 = Interrupt I	request has occ	curred				
	0 = Interrupt I	request has not	toccurred				
bit 12	T5IF: Timer5	Interrupt Flag S	Status bit				
	1 = Interrupt I	request has occ request has not	curred				
bit 11	T4IF: Timer4	Interrupt Flag S	Status bit				
	1 = Interrupt I	request has occ	curred				
	0 = Interrupt i	request has not	occurred				
bit 10	OC4IF: Outpu	ut Compare Ch	annel 4 Interr	upt Flag Status	s bit		
	1 = Interrupt i 0 = Interrupt i	request has occ request has not	curred t occurred				
bit 9	OC3IF: Outpu	ut Compare Ch	annel 3 Interr	upt Flag Statu	s bit		
	1 = Interrupt I	request has occ	curred				
<b>h</b> # 0		request has not	t occurred	Complete Inte	must Elea Otati	a hit	
DIL 8	1 = Interrunt u	via Unannei 2 L request has occ		Complete inte	rrupt Flag Statu	IS DIL	
	0 = Interrupt i	request has not	toccurred				
bit 7	IC8IF: Input C	Capture Channe	el 8 Interrupt	Flag Status bit			
	1 = Interrupt i	request has occ	curred				
hit 6		Capture Chappe	occurred	Elaa Status bit			
DIL O	1 = Interrupt i	request has occ	curred	riay Status Dit			
	0 = Interrupt i	request has not	toccurred				
bit 5	AD2IF: ADC2	2 Conversion C	omplete Inter	rupt Flag Statu	ıs bit		
	1 = Interrupt I	request has occ	curred				
hit 4		request has not		:+			
UIL 4		request has one	riay status D curred	IL			
	0 = Interrupt i	request has not	occurred				

### 9.2 Clock Switching Operation

Applications are free to switch between any of the four clock sources (Primary, LP, FRC and LPRC) under software control at any time. To limit the possible side effects that could result from this flexibility, PIC24HJXXXGPX06A/X08A/X10A devices have a safeguard lock built into the switch process.

Note: Primary Oscillator mode has three different submodes (XT, HS and EC) which are determined by the POSCMD<1:0> Configuration bits. While an application can switch to and from Primary Oscillator mode in software, it cannot switch between the different primary submodes without reprogramming the device.

### 9.2.1 ENABLING CLOCK SWITCHING

To enable clock switching, the FCKSM1 Configuration bit in the Configuration register must be programmed to '0'. (Refer to **Section 21.1 "Configuration Bits"** for further details.) If the FCKSM1 Configuration bit is unprogrammed ('1'), the clock switching function and Fail-Safe Clock Monitor function are disabled. This is the default setting.

The NOSC control bits (OSCCON<10:8>) do not control the clock selection when clock switching is disabled. However, the COSC bits (OSCCON<14:12>) reflect the clock source selected by the FNOSC Configuration bits.

The OSWEN control bit (OSCCON<0>) has no effect when clock switching is disabled. It is held at '0' at all times.

### 9.2.2 OSCILLATOR SWITCHING SEQUENCE

At a minimum, performing a clock switch requires this basic sequence:

- 1. If desired, read the COSC bits (OSCCON<14:12>) to determine the current oscillator source.
- 2. Perform the unlock sequence to allow a write to the OSCCON register high byte.
- Write the appropriate value to the NOSC control bits (OSCCON<10:8>) for the new oscillator source.
- 4. Perform the unlock sequence to allow a write to the OSCCON register low byte.
- 5. Set the OSWEN bit to initiate the oscillator switch.

Once the basic sequence is completed, the system clock hardware responds automatically as follows:

1. The clock switching hardware compares the COSC status bits with the new value of the NOSC control bits. If they are the same, the clock switch is a redundant operation. In this case, the OSWEN bit is cleared automatically and the clock switch is aborted.

- If a valid clock switch has been initiated, the LOCK (OSCCON<5>) and the CF (OSCCON<3>) status bits are cleared.
- The new oscillator is turned on by the hardware if it is not currently running. If a crystal oscillator must be turned on, the hardware waits until the Oscillator Start-up Timer (OST) expires. If the new source is using the PLL, the hardware waits until a PLL lock is detected (LOCK = 1).
- 4. The hardware waits for 10 clock cycles from the new clock source and then performs the clock switch.
- The hardware clears the OSWEN bit to indicate a successful clock transition. In addition, the NOSC bit values are transferred to the COSC status bits.
- 6. The old clock source is turned off at this time, with the exception of LPRC (if WDT or FSCM are enabled) or LP (if LPOSCEN remains set).
  - Note 1: The processor continues to execute code throughout the clock switching sequence. Timing sensitive code should not be executed during this time.
    - 2: Direct clock switches between any primary oscillator mode with PLL and FRCPLL mode are not permitted. This applies to clock switches in either direction. In these instances, the application must switch to FRC mode as a transition clock source between the two PLL modes.
    - 3: Refer to Section 7. "Oscillator" (DS70186) in the "dsPIC33F/PIC24H Family Reference Manual" for details.

### 9.3 Fail-Safe Clock Monitor (FSCM)

The Fail-Safe Clock Monitor (FSCM) allows the device to continue to operate even in the event of an oscillator failure. The FSCM function is enabled by programming. If the FSCM function is enabled, the LPRC internal oscillator runs at all times (except during Sleep mode) and is not subject to control by the Watchdog Timer.

If an oscillator failure occurs, the FSCM generates a clock failure trap event and switches the system clock over to the FRC oscillator. Then the application program can either attempt to restart the oscillator or execute a controlled shutdown. The trap can be treated as a warm Reset by simply loading the Reset address into the oscillator fail trap vector.

If the PLL multiplier is used to scale the system clock, the internal FRC is also multiplied by the same factor on clock failure. Essentially, the device switches to FRC with PLL on a clock failure.

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NEOIOTEN.							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
T5MD	T4MD	T3MD	T2MD	T1MD	<u> </u>	—	
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
I2C1MD	U2MD	U1MD	SPI2MD	SPI1MD	C2MD	C1MD	AD1MD <sup>(1)</sup>
bit 7							bit 0
r							
Legend:							
R = Readable	e bit	W = Writable I	oit	U = Unimplen	nented bit, read	l as '0'	
-n = Value at	POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	IOWN
bit 15	T5MD: Timer	5 Module Disab	le bit				
	1 = 1  mer5 m 0 = 1  mer5 m	odule is disable odule is enable	d d				
hit 14	T4MD. Timer	1 Module Disah	le hit				
bit 14	1 = Timer4 mc	odule is disable	ed				
	0 = Timer4 mo	odule is enable	d				
bit 13	T3MD: Timer3	3 Module Disab	le bit				
	1 = Timer3 mo	odule is disable	ed				
	0 = Timer3 mo	odule is enable	d				
bit 12	T2MD: Timer2	2 Module Disab	le bit				
	1 = 1  mer 2  me 0 = 1  mer 2  me	odule is disable odule is enable	d d				
bit 11	T1MD. Timer1	I Module Disah	u Ie hit				
	1 = Timer1 mc	odule is disable	ed				
	0 = Timer1 mc	odule is enable	d				
bit 10-8	Unimplement	ted: Read as 'd	)'				
bit 7	<b>I2C1MD:</b> I <sup>2</sup> C1	Module Disab	le bit				
	$1 = I^2C1 \mod 0$ $0 = I^2C1 \mod 0$	ule is disabled ule is enabled					
bit 6	U2MD: UART	2 Module Disa	ble bit				
	1 = UART2 m	odule is disable	ed				
	0 = UART2 m	odule is enable	ed				
bit 5	U1MD: UART	1 Module Disa	ble bit				
	1 = UART1 m 0 = UART1 m	odule is disable odule is enable	ed ed				
bit 4	SPI2MD: SPI2	2 Module Disat	ole bit				
	1 = SPI2 mod 0 = SPI2 mod	ule is disabled ule is enabled					
bit 3	SPI1MD: SPI	1 Module Disab	ole bit				
	1 = SPI1 mod	ule is disabled					
	0 = SPI1 mod	ule is enabled					
bit 2	C2MD: ECAN	2 Module Disa	ble bit				
	1 = ECAN2 m 0 = ECAN2 m	odule is disable odule is enable	ed ed				

### REGISTER 10-1: PMD1: PERIPHERAL MODULE DISABLE CONTROL REGISTER 1

**Note 1:** PCFGx bits have no effect if ADC module is disabled by setting this bit. In this case all port pins multiplexed with ANx will be in Digital mode.

REGISTER						GIJIER Z	
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IC8MD	IC7MD	IC6MD	IC5MD	IC4MD	IC3MD	IC2MD	IC1MD
bit 15							bit 8
DAMO	DAMA	DAMA	DAALO		DAMA	DAALO	DAALO
R/W-U	R/W-0	R/W-U	R/W-U	R/W-0	R/W-U	R/W-U	R/W-U
DC8IVID	OC/MD	OC6MD	OC5MD	OC4MD	OC3IVID	OC2MD	
							DILU
Legend:							
R = Readable	e bit	W = Writable I	oit	U = Unimpler	nented bit, read	l as '0'	
-n = Value at	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown
bit 15	IC8MD: Input	Capture 8 Mod	lule Disable bi	t			
	1 = Input Cap	ture 8 module i	s disabled				
bit 11		oture 8 module i	s enabled Iule Dischle hi				
DIL 14	1 = Input Can	ture 7 module i	s disabled	L			
	0 = Input Cap	oture 7 module i	s enabled				
bit 13	IC6MD: Input	Capture 6 Mod	lule Disable bi	t			
	1 = Input Cap	ture 6 module i	s disabled				
	0 = Input Cap	ture 6 module i	s enabled				
bit 12	IC5MD: Input	Capture 5 Mod	lule Disable bi	t			
	0 = Input Cap	oture 5 module i	s enabled				
bit 11	IC4MD: Input	Capture 4 Mod	lule Disable bi	t			
	1 = Input Cap	ture 4 module i	s disabled				
	0 = Input Cap	ture 4 module i	s enabled				
bit 10	IC3MD: Input	Capture 3 Mod	lule Disable bi	t			
	1 = Input Cap 0 = Input Cap	iture 3 module i iture 3 module i	s enabled				
bit 9	IC2MD: Input	Capture 2 Mod	lule Disable bi	t			
	1 = Input Cap	oture 2 module i	s disabled				
	0 = Input Cap	ture 2 module i	s enabled				
bit 8	IC1MD: Input	Capture 1 Mod	lule Disable bi	t			
	1 = Input Cap 0 = Input Cap	oture 1 module i oture 1 module i	s disabled s enabled				
bit 7	OC8MD: Out	put Compare 8	Module Disab	le bit			
	1 = Output Co	ompare 8 modu	le is disabled				
	0 = Output Co	ompare 8 modu	le is enabled				
bit 6	OC7MD: Out	put Compare 4	Module Disab	le bit			
	1 = Output Co	ompare 7 modu ompare 7 modu	le is disabled				
bit 5	OC6MD: Out	out Compare 6	Module Disab	le bit			
Site	1 = Output Co	ompare 6 modu	le is disabled				
	0 = Output Co	ompare 6 modu	le is enabled				
bit 4	OC5MD: Out	put Compare 5	Module Disab	le bit			
	1 = Output Co	ompare 5 modu	le is disabled				
		Sinpare Siniouu	IC IS CHADIEU				

### REGISTER 10-2: PMD2: PERIPHERAL MODULE DISABLE CONTROL REGISTER 2

### 13.0 TIMER2/3, TIMER4/5, TIMER6/7 AND TIMER8/9

- Note 1: This data sheet summarizes the features of the PIC24HJXXXGPX06A/X08A/X10A family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 11. "Timers" (DS70205) of the "dsPIC33F/PIC24H Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
  - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The Timer2/3, Timer4/5, Timer6/7 and Timer8/9 modules are 32-bit timers, which can also be configured as four independent 16-bit timers with selectable operating modes.

As a 32-bit timer, Timer2/3, Timer4/5, Timer6/7 and Timer8/9 operate in three modes:

- Two Independent 16-bit Timers (e.g., Timer2 and Timer3) with all 16-bit operating modes (except Asynchronous Counter mode)
- Single 32-bit Timer
- Single 32-bit Synchronous Counter

They also support these features:

- Timer Gate Operation
- Selectable Prescaler Settings
- Timer Operation during Idle and Sleep modes
- Interrupt on a 32-bit Period Register Match
- Time Base for Input Capture and Output Compare Modules (Timer2 and Timer3 only)
- ADC1 Event Trigger (Timer2/3 only)
- ADC2 Event Trigger (Timer4/5 only)

Individually, all eight of the 16-bit timers can function as synchronous timers or counters. They also offer the features listed above, except for the event trigger; this is implemented only with Timer2/3. The operating modes and enabled features are determined by setting the appropriate bit(s) in the T2CON, T3CON, T4CON, T5CON, T6CON, T7CON, T8CON and T9CON registers. T2CON, T4CON, T6CON and T8CON are shown in generic form in Register 13-1. T3CON, T5CON, T7CON and T9CON are shown in Register 13-2. For 32-bit timer/counter operation, Timer2, Timer4, Timer6 or Timer8 is the least significant word; Timer3, Timer5, Timer7 or Timer9 is the most significant word of the 32-bit timers.

Note:	For 32-bit operation, T3CON, T5CON,
	T7CON and T9CON control bits are
	ignored. Only T2CON, T4CON, T6CON
	and T8CON control bits are used for setup
	and control. Timer2, Timer4, Timer6 and
	Timer8 clock and gate inputs are utilized
	for the 32-bit timer modules, but an inter-
	rupt is generated with the Timer3, Timer5,
	Ttimer7 and Timer9 interrupt flags.

To configure Timer2/3, Timer4/5, Timer6/7 or Timer8/9 for 32-bit operation:

- 1. Set the corresponding T32 control bit.
- 2. Select the prescaler ratio for Timer2, Timer4, Timer6 or Timer8 using the TCKPS<1:0> bits.
- 3. Set the Clock and Gating modes using the corresponding TCS and TGATE bits.
- 4. Load the timer period value. PR3, PR5, PR7 or PR9 contains the most significant word of the value, while PR2, PR4, PR6 or PR8 contains the least significant word.
- 5. If interrupts are required, set the interrupt enable bit, T3IE, T5IE, T7IE or T9IE. Use the priority bits, T3IP<2:0>, T5IP<2:0>, T7IP<2:0> or T9IP<2:0>, to set the interrupt priority. While Timer2, Timer4, Timer6 or Timer8 control the timer, the interrupt appears as a Timer3, Timer5, Timer7 or Timer9 interrupt.
- 6. Set the corresponding TON bit.

The timer value at any point is stored in the register pair, TMR3:TMR2, TMR5:TMR4, TMR7:TMR6 or TMR9:TMR8. TMR3, TMR5, TMR7 or TMR9 always contains the most significant word of the count, while TMR2, TMR4, TMR6 or TMR8 contains the least significant word.

To configure any of the timers for individual 16-bit operation:

- 1. Clear the T32 bit corresponding to that timer.
- 2. Select the timer prescaler ratio using the TCKPS<1:0> bits.
- 3. Set the Clock and Gating modes using the TCS and TGATE bits.
- 4. Load the timer period value into the PRx register.
- 5. If interrupts are required, set the interrupt enable bit, TxIE. Use the priority bits, TxIP<2:0>, to set the interrupt priority.
- 6. Set the TON bit.

### REGISTER 13-2: TyCON (T3CON, T5CON, T7CON OR T9CON) CONTROL REGISTER

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
TON <sup>(1)</sup>		TSIDL <sup>(2)</sup>	—	-	—	—	_
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	U-0
—	TGATE <sup>(1)</sup>	TCKPS	<1:0>(1)	—	—	TCS <sup>(1,3)</sup>	_
bit 7							bit 0

Legend:				
R = Readabl	e bit	W = Writable bit	U = Unimplemented bit, read	1 as '0'
-n = Value at POR		'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
bit 15	TON: Timery	On bit <sup>(1)</sup>		
	1 = Starts 16-	bit Timery		
	0 = Stops 16-	bit Timery		
bit 14	Unimplemen	ited: Read as '0'		
bit 13	TSIDL: Stop	in Idle Mode bit <sup>(2)</sup>		
	1 = Discontin 0 = Continue	ue module operation when o module operation in Idle mo	levice enters Idle mode de	
bit 12-7	Unimplemen	ted: Read as '0'		
bit 6	TGATE: Time	ery Gated Time Accumulation	n Enable bit <sup>(1)</sup>	
	When TCS =	<u>1:</u>		
	This bit is ign	ored.		
	$\frac{\text{VVnen } 1\text{ CS} =}{1 = \text{Gated tim}}$	<u>0:</u> he accumulation enabled		
	0 = Gated tim	ne accumulation disabled		
bit 5-4	TCKPS<1:0>	: Timer3 Input Clock Presca	le Select bits <sup>(1)</sup>	
	11 <b>= 1:256</b>			
	10 <b>= 1:64</b>			
	01 = 1:8 00 = 1:1			
bit 3-2	Unimplemen	ted: Read as '0'		
bit 1	TCS: Timerv	Clock Source Select bit <sup>(1,3)</sup>		
~	1 = External of	clock from pin TvCK (on the	risina edae)	
	0 = Internal c	lock (Fcy)		
bit 0	Unimplemen	ted: Read as '0'		
Note 1: W	/hen 32-bit opera nctions are set tl	tion is enabled (T2CON<3> hrough T2CON.	= 1), these bits have no effect (	on Timery operation; all timer

- 2: When 32-bit timer operation is enabled (T32 = 1) in the Timer Control register (TxCON<3>), the TSIDL bit must be cleared to operate the 32-bit timer in Idle mode.
- 3: The TyCK pin is not available on all timers. Refer to the "Pin Diagrams" section for the available pins.

### 15.1 Output Compare Modes

Configure the Output Compare modes by setting the appropriate Output Compare Mode (OCM<2:0>) bits in the Output Compare Control (OCxCON<2:0>) register. Table 15-1 lists the different bit settings for the Output Compare modes. Figure 15-2 illustrates the output compare operation for various modes. The user

TABLE 15-1: OUTPUT COMPARE MODES

application must disable the associated timer when writing to the Output Compare Control registers to avoid malfunctions.

Note:	See Section 13. "Output Compare"
	(DS70209) in the "dsPIC33F/PIC24H
	Family Reference Manual" for OCxR and
	OCxRS register restrictions.

OCM<2:0>	Mode	OCx Pin Initial State	OCx Interrupt Generation
000	Module Disabled	Controlled by GPIO register	—
001	Active-Low One-Shot	0	OCx rising edge
010	Active-High One-Shot	1	OCx falling edge
011	Toggle	Current output is maintained	OCx rising and falling edge
100	Delayed One-Shot	0	OCx falling edge
101	Continuous Pulse	0	OCx falling edge
110	PWM without Fault Protection	ʻ0', if OCxR is zero ʻ1', if OCxR is non-zero	No interrupt
111	PWM with Fault Protection	<ul><li>'0', if OCxR is zero</li><li>'1', if OCxR is non-zero</li></ul>	OCFA falling edge for OC1 to OC4

### FIGURE 15-2: OUTPUT COMPARE OPERATION



### **19.3 Modes of Operation**

The CAN module can operate in one of several operation modes selected by the user. These modes include:

- Initialization Mode
- Disable Mode
- Normal Operation Mode
- Listen Only Mode
- Listen All Messages Mode
- Loopback Mode

Modes are requested by setting the REQOP<2:0> bits (CiCTRL1<10:8>). Entry into a mode is Acknowledged by monitoring the OPMODE<2:0> bits (CiCTRL1<7:5>). The module will not change the mode and the OPMODE bits until a change in mode is acceptable, generally during bus Idle time, which is defined as at least 11 consecutive recessive bits.

### 19.3.1 INITIALIZATION MODE

In the Initialization mode, the module will not transmit or receive. The error counters are cleared and the interrupt flags remain unchanged. The programmer will have access to Configuration registers that are access restricted in other modes. The module will protect the user from accidentally violating the CAN protocol through programming errors. All registers which control the configuration of the module cannot be modified while the module is on-line. The CAN module will not be allowed to enter the Configuration mode while a transmission is taking place. The Configuration mode serves as a lock to protect the following registers.

- All Module Control Registers
- Baud Rate and Interrupt Configuration Registers
- Bus Timing Registers
- Identifier Acceptance Filter Registers
- Identifier Acceptance Mask Registers

### 19.3.2 DISABLE MODE

In Disable mode, the module will not transmit or receive. The module has the ability to set the WAKIF bit due to bus activity, however, any pending interrupts will remain and the error counters will retain their value.

If the REQOP<2:0> bits (CiCTRL1<10:8>) = 001, the module will enter the Module Disable mode. If the module is active, the module will wait for 11 recessive bits on the CAN bus, detect that condition as an Idle bus, then accept the module disable command. When the OPMODE<2:0> bits (CiCTRL1<7:5>) = 001, that indicates whether the module successfully went into Module Disable mode. The I/O pins will revert to normal I/O function when the module is in the Module Disable mode.

The module can be programmed to apply a low-pass filter function to the CiRX input line while the module or the CPU is in Sleep mode. The WAKFIL bit (CiCFG2<14>) enables or disables the filter.

Note: Typically, if the CAN module is allowed to transmit in a particular mode of operation and a transmission is requested immediately after the CAN module has been placed in that mode of operation, the module waits for 11 consecutive recessive bits on the bus before starting transmission. If the user application switches to Disable mode within this 11-bit period, the transmission is then aborted and the corresponding TXABT bit is set and the TXREQ bit is cleared.

### 19.3.3 NORMAL OPERATION MODE

Normal Operation mode is selected when REQOP<2:0> = 000. In this mode, the module is activated and the I/O pins will assume the CAN bus functions. The module will transmit and receive CAN bus messages via the CiTX and CiRX pins.

### 19.3.4 LISTEN ONLY MODE

If the Listen Only mode is activated, the module on the CAN bus is passive. The transmitter buffers revert to the port I/O function. The receive pins remain inputs. For the receiver, no error flags or Acknowledge signals are sent. The error counters are deactivated in this state. The Listen Only mode can be used for detecting the baud rate on the CAN bus. To use this, it is necessary that there are at least two further nodes that communicate with each other.

### 19.3.5 LISTEN ALL MESSAGES MODE

The module can be set to ignore all errors and receive any message. The Listen All Messages mode is activated by setting REQOP<2:0> = '111'. In this mode, the data which is in the message assembly buffer, until the time an error occurred, is copied in the receive buffer and can be read via the CPU interface.

### 19.3.6 LOOPBACK MODE

If the Loopback mode is activated, the module will connect the internal transmit signal to the internal receive signal at the module boundary. The transmit and receive pins revert to their port I/O function.

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_	—	_	_	—	—	_	—
bit 15							bit 8
R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
IVRIE	WAKIE	ERRIE		FIFOIE	RBOVIE	RBIE	TBIE
bit 7							bit 0
Legend:							
R = Readab	le bit	W = Writable	bit	U = Unimpler	mented bit, read	l as '0'	
-n = Value a	t POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unknown	
bit 15-8	Unimplemen	ted: Read as '	0'				
bit 7	IVRIE: Invalio	Message Inte	rrupt Enable b	bit			
	1 = Interrupt	request enable					
bit 6		Make up Activi	tv Intorrunt Er	ablo bit			
	1 = Interrupt	request enable	d niterrupt Er				
	0 = Interrupt i	request not ena	abled				
bit 5	ERRIE: Error	Interrupt Enab	le bit				
	1 = Interrupt	request enable	d				
	0 = Interrupt	request not ena	abled				
bit 4	Unimplemen	ted: Read as '	0'				
bit 3	FIFOIE: FIFC	Almost Full In	terrupt Enable	e bit			
	1 = Interrupt I	request enable	u abled				
bit 2	RBOVIE: RX	Buffer Overflov	v Interrupt En	able bit			
	1 = Interrupt	request enable	d				
	0 = Interrupt	request not ena	abled				
bit 1	RBIE: RX Bu	ffer Interrupt Er	hable bit				
	1 = Interrupt i	request enable	d bled				
bit 0		fer Interrunt En	ahle hit				
	1 = Interrupt	request enable	d				
	0 = Interrupt i	request not ena	abled				

### **REGISTER 19-7:** CIINTE: ECAN™ MODULE INTERRUPT ENABLE REGISTER

### TABLE 24-28: SPIx MAXIMUM DATA/CLOCK RATE SUMMARY

AC CHARACTERISTICS			$\begin{tabular}{lllllllllllllllllllllllllllllllllll$				
Maximum Data Rate	Master Transmit Only (Half-Duplex)	Master Transmit/Receive (Full-Duplex)	Slave Transmit/Receive (Full-Duplex)	CKE	СКР	SMP	
15 MHz	Table 24-29	—	—	0,1	0,1	0,1	
10 MHz	—	Table 24-30	—	1	0,1	1	
10 MHz	—	Table 24-31	—	0	0,1	1	
15 MHz	—	—	Table 24-32	1	0	0	
11 MHz	—	—	Table 24-33	1	1	0	
15 MHz	_	_	Table 24-34	0	1	0	
11 MHz	_	_	Table 24-35	0	0	0	

### FIGURE 24-9: SPIX MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY CKE = 0) TIMING CHARACTERISTICS



# FIGURE 24-13: SPIX SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0) TIMING CHARACTERISTICS



## TABLE 24-34:SPIX SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0) TIMING<br/>REQUIREMENTS

AC CHARACTERISTICS			$\begin{tabular}{lllllllllllllllllllllllllllllllllll$				
Param No.	Symbol	Characteristic <sup>(1)</sup>	Min	Тур <sup>(2)</sup>	Max	Units	Conditions
SP70	TscP	Maximum SCK Input Frequency	—	_	15	MHz	See Note 3
SP72	TscF	SCKx Input Fall Time	—			ns	See parameter DO32 and <b>Note 4</b>
SP73	TscR	SCKx Input Rise Time	—			ns	See parameter DO31 and <b>Note 4</b>
SP30	TdoF	SDOx Data Output Fall Time	—			ns	See parameter DO32 and <b>Note 4</b>
SP31	TdoR	SDOx Data Output Rise Time	—		_	ns	See parameter DO31 and <b>Note 4</b>
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	6	20	ns	_
SP36	TdoV2scH, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	_	_	ns	—
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	_	_	ns	—
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30		-	ns	_
SP50	TssL2scH, TssL2scL	$\overline{SSx} \downarrow$ to SCKx $\uparrow$ or SCKx Input	120			ns	_
SP51	TssH2doZ	SSx ↑ to SDOx Output High-Impedance <sup>(4)</sup>	10	—	50	ns	—
SP52	TscH2ssH TscL2ssH	SSx after SCKx Edge	1.5 TCY + 40	_	_	ns	See Note 4

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated.

**3:** The minimum clock period for SCKx is 66.7 ns. Therefore, the SCK clock generated by the Master must not violate this specificiation.

**4:** Assumes 50 pF load on all SPIx pins.

### 25.0 HIGH TEMPERATURE ELECTRICAL CHARACTERISTICS

This section provides an overview of PIC24HJXXXGPX06A/X08A/X10A electrical characteristics for devices operating in an ambient temperature range of -40°C to +150°C.

The specifications between  $-40^{\circ}$ C to  $+150^{\circ}$ C are identical to those shown in **Section 24.0** "**Electrical Characteristics**" for operation between  $-40^{\circ}$ C to  $+125^{\circ}$ C, with the exception of the parameters listed in this section.

Parameters in this section begin with an H, which denotes High temperature. For example, parameter DC10 in **Section 24.0 "Electrical Characteristics"** is the Industrial and Extended temperature equivalent of HDC10.

Absolute maximum ratings for the PIC24HJXXXGPX06A/X08A/X10A high temperature devices are listed below. Exposure to these maximum rating conditions for extended periods can affect device reliability. Functional operation of the device at these or any other conditions above the parameters indicated in the operation listings of this specification is not implied.

### Absolute Maximum Ratings

### (See Note 1)

Ambient temperature under bias <sup>(4)</sup>	40°C to +150°C
Storage temperature	65°C to +160°C
Voltage on VDD with respect to Vss	-0.3V to +4.0V
Voltage on any pin that is not 5V tolerant with respect to Vss <sup>(5)</sup>	-0.3V to (VDD + 0.3V)
Voltage on any 5V tolerant pin with respect to Vss when $VDD < 3.0V^{(5)}$	0.3V to (VDD + 0.3V)
Voltage on any 5V tolerant pin with respect to Vss when VDD $\geq 3.0 V^{(5)}$	0.3V to 5.6V
Voltage on VCAP with respect to Vss	2.25V to 2.75V
Maximum current out of Vss pin	60 mA
Maximum current into VDD pin <sup>(2)</sup>	60 mA
Maximum junction temperature	+155°C
Maximum current sourced/sunk by any 2x I/O pin <sup>(3)</sup>	2 mA
Maximum current sourced/sunk by any 4x I/O pin <sup>(3)</sup>	4 mA
Maximum current sourced/sunk by any 8x I/O pin <sup>(3)</sup>	8 mA
Maximum current sunk by all ports combined	10 mA
Maximum current sourced by all ports combined <sup>(2)</sup>	10 mA

**Note 1:** Stresses above those listed under "Absolute Maximum Ratings" can cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods can affect device reliability.

- 2: Maximum allowable current is a function of device maximum power dissipation (see Table 25-2).
- **3:** Unlike devices at 125°C and below, the specifications in this section also apply to the CLKOUT, VREF+, VREF-, SCLx, SDAx, PGECx, and PGEDx pins.
- 4: AEC-Q100 reliability testing for devices intended to operate at 150°C is 1,000 hours. Any design in which the total operating time from 125°C to 150°C will be greater than 1,000 hours is not warranted without prior written approval from Microchip Technology Inc.
- 5: Refer to the "Pin Diagrams" section for 5V tolerant pins.