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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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#### Details

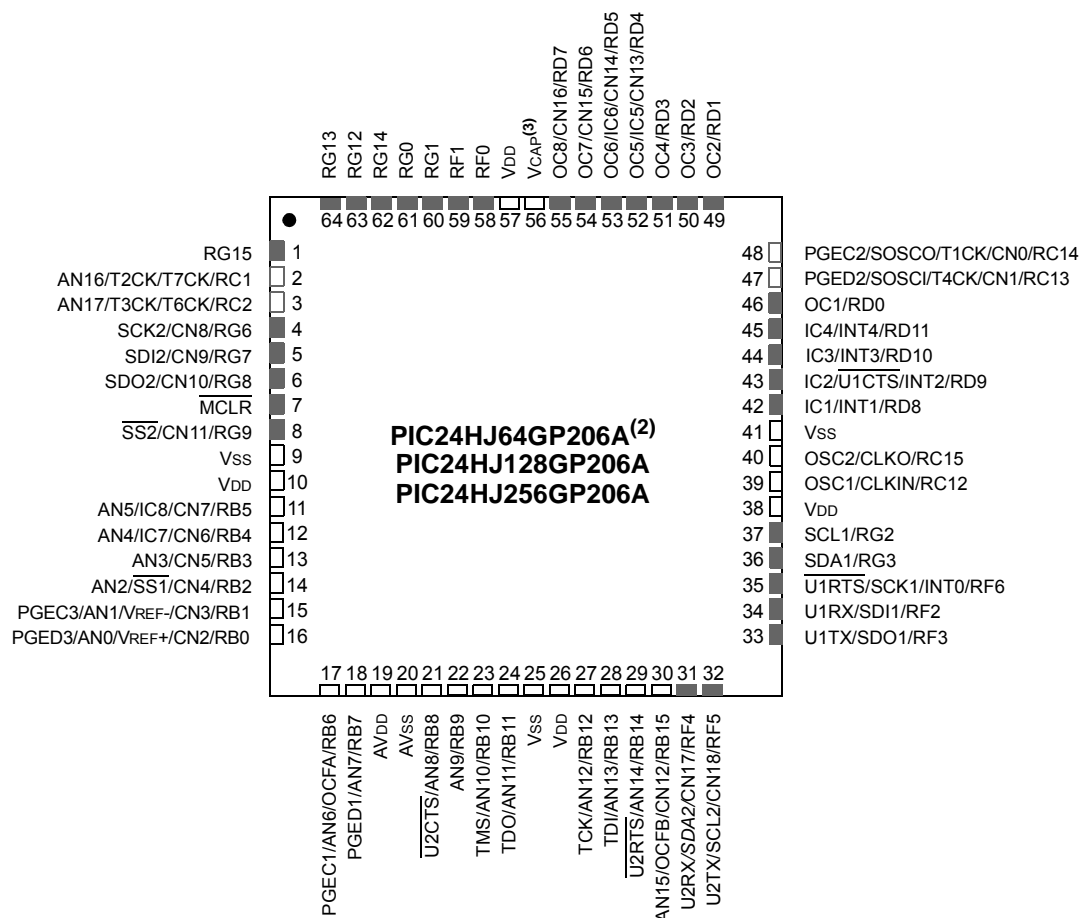
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	40 MIPS
Connectivity	CANbus, I <sup>2</sup> C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	53
Program Memory Size	64KB (22K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 18x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic24hj64gp506at-i-mr">https://www.e-xfl.com/product-detail/microchip-technology/pic24hj64gp506at-i-mr</a>

# PIC24HJXXXGPX06A/X08A/X10A

## Pin Diagrams

### 64-Pin QFN<sup>(1)</sup>

■ = Pins are up to 5V tolerant



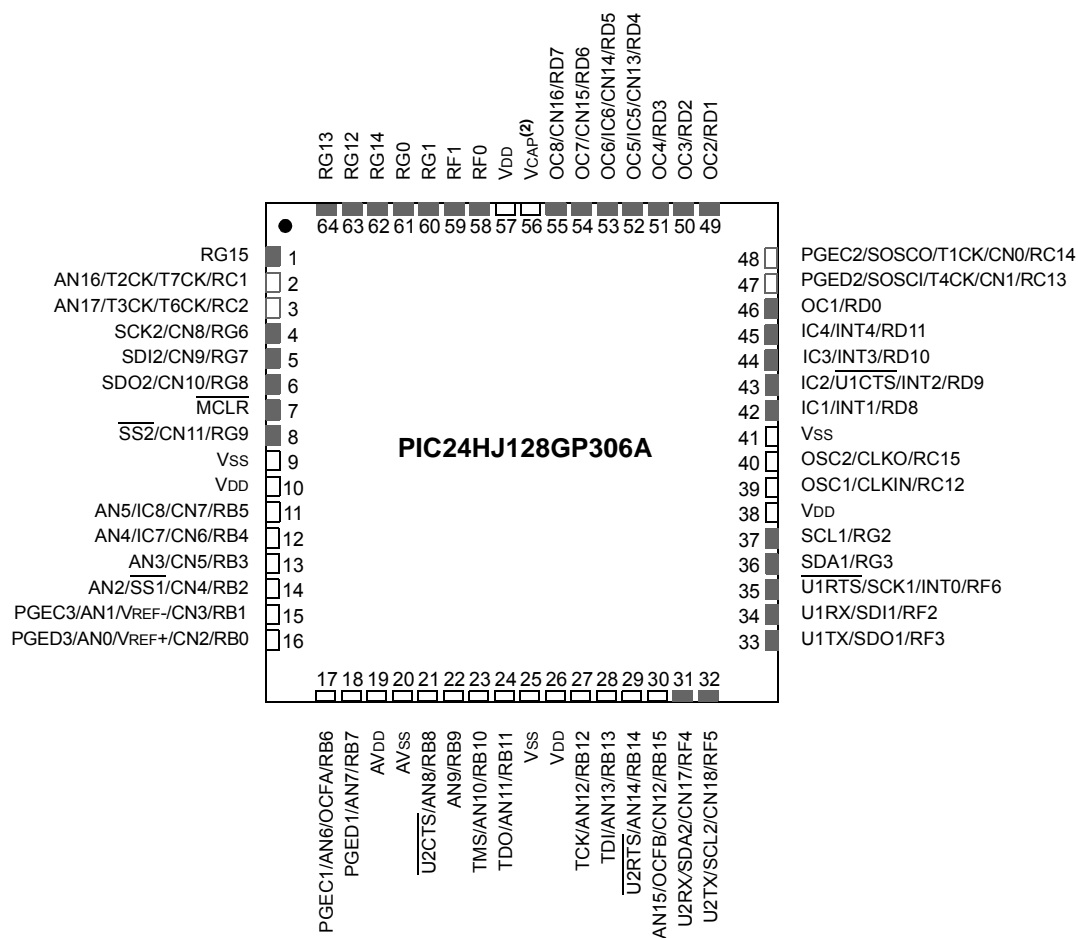
- Note** 1: The metal plane at the bottom of the device is not connected to any pins and should be connected to Vss externally.  
2: The PIC24HJ64GP206A device does not have the SCL2 and SDA2 pins.  
3: Refer to **Section 2.3 “CPU Logic Filter Capacitor Connection (VCAP)”** for proper connection to this pin.

# PIC24HJXXXGPX06A/X08A/X10A

## Pin Diagrams (Continued)

64-Pin QFN<sup>(1)</sup>

■ = Pins are up to 5V tolerant



- Note** 1: The metal plane at the bottom of the device is not connected to any pins and should be connected to Vss externally.  
 2: Refer to **Section 2.3 “CPU Logic Filter Capacitor Connection (VCAP)”** for proper connection to this pin.

# PIC24HJXXXGPX06A/X08A/X10A

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## Referenced Sources

This device data sheet is based on the following individual chapters of the “dsPIC33F/PIC24H Family Reference Manual”. These documents should be considered as the general reference for the operation of a particular module or device feature.

**Note:** To access the documents listed below, browse to the documentation section of the PIC24HJ256GP610A product page on the Microchip web site ([www.microchip.com](http://www.microchip.com)) or by selecting a family reference manual section from the following list.

In addition to parameters, features, and other documentation, the resulting page provides links to the related family reference manual sections.

- **Section 1. “Introduction”** (DS70197)
- **Section 2. “CPU”** (DS70204)
- **Section 3. “Data Memory”** (DS70202)
- **Section 4. “Program Memory”** (DS70203)
- **Section 5. “Flash Programming”** (DS70191)
- **Section 6. “Interrupts”** (DS70184)
- **Section 7. “Oscillator”** (DS70186)
- **Section 8. “Reset”** (DS70192)
- **Section 9. “Watchdog Timer and Power-Saving Modes”** (DS70196)
- **Section 10. “I/O Ports”** (DS70193)
- **Section 11. “Timers”** (DS70205)
- **Section 12. “Input Capture”** (DS70198)
- **Section 13. “Output Compare”** (DS70209)
- **Section 16. “Analog-to-Digital Converter (ADC)”** (DS70183)
- **Section 17. “UART”** (DS70188)
- **Section 18. “Serial Peripheral Interface (SPI)”** (DS70206)
- **Section 19. “Inter-Integrated Circuit™ (I2C™)”** (DS70195)
- **Section 20. “Data Converter Interface (DCI)”** (DS70288)
- **Section 21. “Enhanced Controller Area Network (ECAN™)”** (DS70185)
- **Section 22. “Direct Memory Access (DMA)”** (DS70182)
- **Section 23. “CodeGuard™ Security”** (DS70199)
- **Section 24. “Programming and Diagnostics”** (DS70207)
- **Section 25. “Device Configuration”** (DS70194)

# PIC24HJXXXGPX06A/X08A/X10A

## REGISTER 3-2: CORCON: CORE CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15						bit 8	

U-0	U-0	U-0	U-0	R/C-0	R/W-0	U-0	U-0
—	—	—	—	IPL3 <sup>(1)</sup>	PSV	—	—
bit 7						bit 0	

<b>Legend:</b>	C = Clear only bit		
R = Readable bit	W = Writable bit	-n = Value at POR	'1' = Bit is set
0' = Bit is cleared	'x' = Bit is unknown	U = Unimplemented bit, read as '0'	

- bit 15-4      **Unimplemented:** Read as '0'
- bit 3      **IPL3:** CPU Interrupt Priority Level Status bit 3<sup>(1)</sup>  
             1 = CPU interrupt priority level is greater than 7  
             0 = CPU interrupt priority level is 7 or less
- bit 2      **PSV:** Program Space Visibility in Data Space Enable bit  
             1 = Program space visible in data space  
             0 = Program space not visible in data space
- bit 1-0      **Unimplemented:** Read as '0'

**Note 1:** The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU interrupt priority level.

# PIC24HJXXGPX06A/X08A/X10A

## 4.0 MEMORY ORGANIZATION

**Note:** This data sheet summarizes the features of the PIC24HJXXXGPX06A/X08A/X10A family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 3. “Data Memory”** (DS70202) of the *“dsPIC33F/PIC24H Family Reference Manual”*, which is available from the Microchip web site ([www.microchip.com](http://www.microchip.com)).

The PIC24HJXXXGPX06A/X08A/X10A architecture features separate program and data memory spaces and buses. This architecture also allows the direct access of program memory from the data space during code execution.

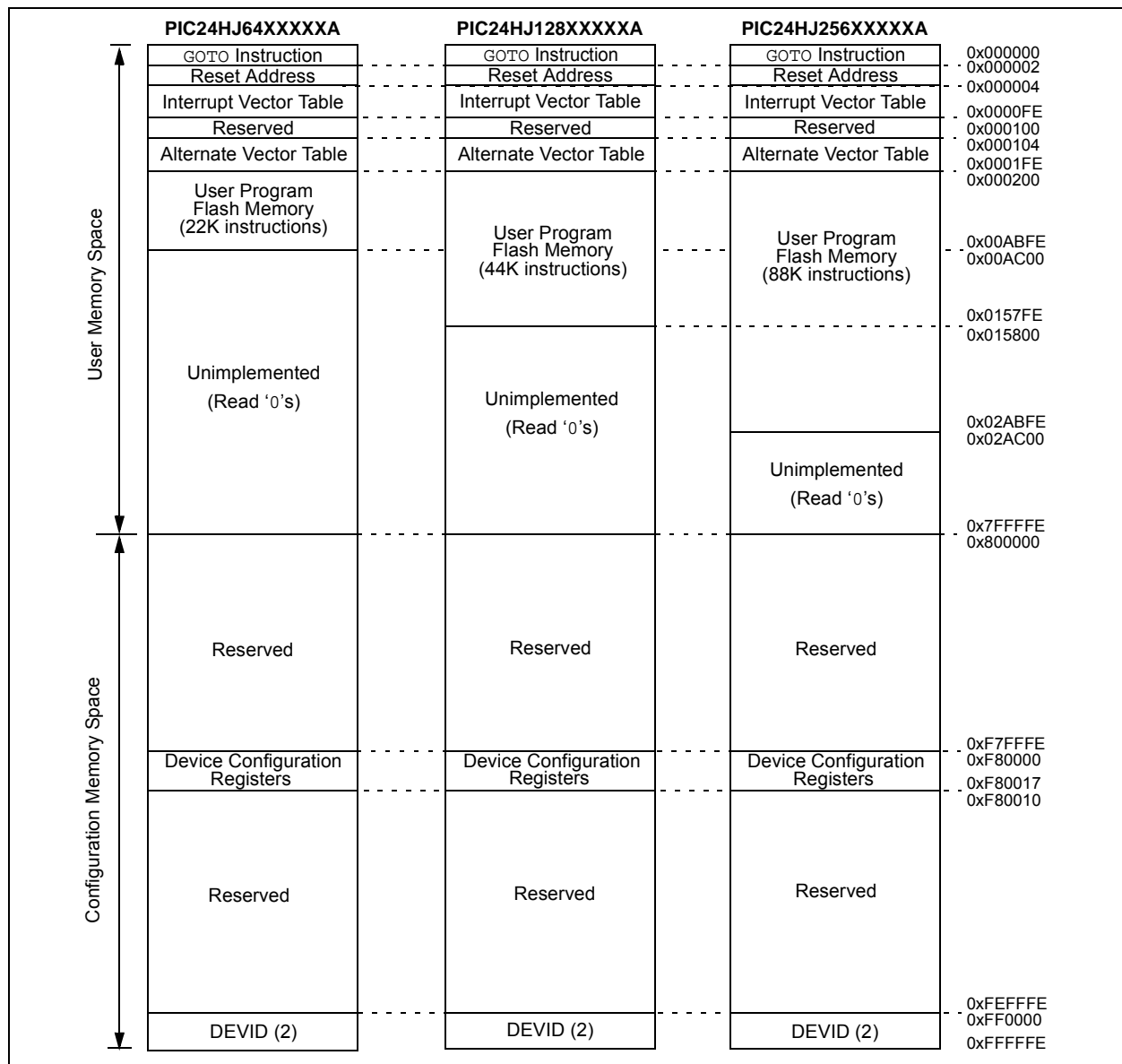
## 4.1 Program Address Space

The program address memory space of the PIC24HJXXXGPX06A/X08A/X10A devices is 4M instructions. The space is addressable by a 24-bit value derived from either the 23-bit Program Counter (PC) during program execution, or from table operation or data space remapping as described in **Section 4.4 “Interfacing Program and Data Memory Spaces”**.

User access to the program memory space is restricted to the lower half of the address range (0x000000 to 0x7FFFFFFF). The exception is the use of TBLRD/TBLWT operations, which use TBLPAG<7> to permit access to the Configuration bits and Device ID sections of the configuration memory space.

Memory maps for the PIC24HJXXGPX06A/X08A/X10A family of devices are shown in Figure 4-1.

**FIGURE 4-1: PROGRAM MEMORY MAP FOR PIC24HJXXXGPX06A/X08A/X10A FAMILY DEVICES**



**TABLE 4-20: ECAN1 REGISTER MAP WHEN C1CTRL1.WIN = 1 FOR PIC24HJXXXGP506A/510A/610A DEVICES ONLY (CONTINUED)**

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
C1RXF1EID	0446	EID<15:8>								EID<7:0>								xxxx
C1RXF2SID	0448	SID<10:3>								SID<2:0>		—	EXIDE	—	EID<17:16>			xxxx
C1RXF2EID	044A	EID<15:8>								EID<7:0>								xxxx
C1RXF3SID	044C	SID<10:3>								SID<2:0>		—	EXIDE	—	EID<17:16>			xxxx
C1RXF3EID	044E	EID<15:8>								EID<7:0>								xxxx
C1RXF4SID	0450	SID<10:3>								SID<2:0>		—	EXIDE	—	EID<17:16>			xxxx
C1RXF4EID	0452	EID<15:8>								EID<7:0>								xxxx
C1RXF5SID	0454	SID<10:3>								SID<2:0>		—	EXIDE	—	EID<17:16>			xxxx
C1RXF5EID	0456	EID<15:8>								EID<7:0>								xxxx
C1RXF6SID	0458	SID<10:3>								SID<2:0>		—	EXIDE	—	EID<17:16>			xxxx
C1RXF6EID	045A	EID<15:8>								EID<7:0>								xxxx
C1RXF7SID	045C	SID<10:3>								SID<2:0>		—	EXIDE	—	EID<17:16>			xxxx
C1RXF7EID	045E	EID<15:8>								EID<7:0>								xxxx
C1RXF8SID	0460	SID<10:3>								SID<2:0>		—	EXIDE	—	EID<17:16>			xxxx
C1RXF8EID	0462	EID<15:8>								EID<7:0>								xxxx
C1RXF9SID	0464	SID<10:3>								SID<2:0>		—	EXIDE	—	EID<17:16>			xxxx
C1RXF9EID	0466	EID<15:8>								EID<7:0>								xxxx
C1RXF10SID	0468	SID<10:3>								SID<2:0>		—	EXIDE	—	EID<17:16>			xxxx
C1RXF10EID	046A	EID<15:8>								EID<7:0>								xxxx
C1RXF11SID	046C	SID<10:3>								SID<2:0>		—	EXIDE	—	EID<17:16>			xxxx
C1RXF11EID	046E	EID<15:8>								EID<7:0>								xxxx
C1RXF12SID	0470	SID<10:3>								SID<2:0>		—	EXIDE	—	EID<17:16>			xxxx
C1RXF12EID	0472	EID<15:8>								EID<7:0>								xxxx
C1RXF13SID	0474	SID<10:3>								SID<2:0>		—	EXIDE	—	EID<17:16>			xxxx
C1RXF13EID	0476	EID<15:8>								EID<7:0>								xxxx
C1RXF14SID	0478	SID<10:3>								SID<2:0>		—	EXIDE	—	EID<17:16>			xxxx
C1RXF14EID	047A	EID<15:8>								EID<7:0>								xxxx
C1RXF15SID	047C	SID<10:3>								SID<2:0>		—	EXIDE	—	EID<17:16>			xxxx
C1RXF15EID	047E	EID<15:8>								EID<7:0>								xxxx

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal for PinHigh devices.

# PIC24HJXXXGPX06A/X08A/X10A

**REGISTER 6-1: RCON: RESET CONTROL REGISTER<sup>(1)</sup>**

R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0	R/W-0
TRAPR	IOPUWR	—	—	—	—	—	VREGS <sup>(3)</sup>
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1
EXTR	SWR	SWDTEN <sup>(2)</sup>	WDTO	SLEEP	IDLE	BOR	POR
bit 7							bit 0

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
 -n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

- bit 15      **TRAPR:** Trap Reset Flag bit  
             1 = A Trap Conflict Reset has occurred  
             0 = A Trap Conflict Reset has not occurred
- bit 14      **IOPUWR:** Illegal Opcode or Uninitialized W Access Reset Flag bit  
             1 = An illegal opcode detection, an illegal address mode or uninitialized W register used as an Address Pointer caused a Reset  
             0 = An illegal opcode or uninitialized W Reset has not occurred
- bit 13-9    **Unimplemented:** Read as '0'
- bit 8      **VREGS:** Voltage Regulator Standby During Sleep bit<sup>(3)</sup>  
             1 = Voltage Regulator is active during Sleep mode  
             0 = Voltage Regulator goes into standby mode during Sleep
- bit 7      **EXTR:** External Reset ( $\overline{\text{MCLR}}$ ) Pin bit  
             1 = A Master Clear (pin) Reset has occurred  
             0 = A Master Clear (pin) Reset has not occurred
- bit 6      **SWR:** Software Reset (Instruction) Flag bit  
             1 = A RESET instruction has been executed  
             0 = A RESET instruction has not been executed
- bit 5      **SWDTEN:** Software Enable/Disable of WDT bit<sup>(2)</sup>  
             1 = WDT is enabled  
             0 = WDT is disabled
- bit 4      **WDTO:** Watchdog Timer Time-out Flag bit  
             1 = WDT time-out has occurred  
             0 = WDT time-out has not occurred
- bit 3      **SLEEP:** Wake-up from Sleep Flag bit  
             1 = Device has been in Sleep mode  
             0 = Device has not been in Sleep mode
- bit 2      **IDLE:** Wake-up from Idle Flag bit  
             1 = Device was in Idle mode  
             0 = Device was not in Idle mode
- bit 1      **BOR:** Brown-out Reset Flag bit  
             1 = A Brown-out Reset has occurred  
             0 = A Brown-out Reset has not occurred
- bit 0      **POR:** Power-on Reset Flag bit  
             1 = A Power-on Reset has occurred  
             0 = A Power-on Reset has not occurred

- Note 1:** All of the Reset status bits may be set or cleared in software. Setting one of these bits in software does not cause a device Reset.
- 2:** If the FWDTEN Configuration bit is '1' (unprogrammed), the WDT is always enabled, regardless of the SWDTEN bit setting.
- 3:** For PIC24HJ256GPX06A/X08A/X10A devices, this bit is unimplemented and reads back programmed value.



# PIC24HJXXXGPX06A/X08A/X10A

## REGISTER 7-26: IPC11: INTERRUPT PRIORITY CONTROL REGISTER 11

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	T6IP<2:0>			—	DMA4IP<2:0>		
bit 15				bit 8			

U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-0
—	—	—	—	—	OC8IP<2:0>		
bit 7					bit 0		

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **T6IP<2:0>:** Timer6 Interrupt Priority bits

111 = Interrupt is priority 7 (highest priority interrupt)

•  
•  
•

001 = Interrupt is priority 1

000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **DMA4IP<2:0>:** DMA Channel 4 Data Transfer Complete Interrupt Priority bits

111 = Interrupt is priority 7 (highest priority interrupt)

•  
•  
•

001 = Interrupt is priority 1

000 = Interrupt source is disabled

bit 7-3 **Unimplemented:** Read as '0'

bit 2-0 **OC8IP<2:0>:** Output Compare Channel 8 Interrupt Priority bits

111 = Interrupt is priority 7 (highest priority interrupt)

•  
•  
•

001 = Interrupt is priority 1

000 = Interrupt source is disabled

# PIC24HJXXXGPX06A/X08A/X10A

## REGISTER 8-2: DMAxREQ: DMA CHANNEL x IRQ SELECT REGISTER

R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
FORCE <sup>(1)</sup>	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	IRQSEL6 <sup>(2)</sup>	IRQSEL5 <sup>(2)</sup>	IRQSEL4 <sup>(2)</sup>	IRQSEL3 <sup>(2)</sup>	IRQSEL2 <sup>(2)</sup>	IRQSEL1 <sup>(2)</sup>	IRQSEL0 <sup>(2)</sup>
bit 7							bit 0

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **FORCE:** Force DMA Transfer bit<sup>(1)</sup>

1 = Force a single DMA transfer (Manual mode)

0 = Automatic DMA transfer initiation by DMA request

bit 14-7 **Unimplemented:** Read as '0'

bit 6-0 **IRQSEL<6:0>:** DMA Peripheral IRQ Number Select bits<sup>(2)</sup>

0000000-1111111 = DMAIRQ0-DMAIRQ127 selected to be Channel DMAREQ

**Note 1:** The FORCE bit cannot be cleared by the user. The FORCE bit is cleared by hardware when the forced DMA transfer is complete.

**2:** Please see Table 8-1 for a complete listing of IRQ numbers for all interrupt sources.

# PIC24HJXXXGPX06A/X08A/X10A

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## REGISTER 8-7:     **DMACS0: DMA CONTROLLER STATUS REGISTER 0 (CONTINUED)**

- bit 3            **XWCOL3:** Channel 3 DMA RAM Write Collision Flag bit  
                 1 = Write collision detected  
                 0 = No write collision detected
- bit 2            **XWCOL2:** Channel 2 DMA RAM Write Collision Flag bit  
                 1 = Write collision detected  
                 0 = No write collision detected
- bit 1            **XWCOL1:** Channel 1 DMA RAM Write Collision Flag bit  
                 1 = Write collision detected  
                 0 = No write collision detected
- bit 0            **XWCOL0:** Channel 0 DMA RAM Write Collision Flag bit  
                 1 = Write collision detected  
                 0 = No write collision detected

# PIC24HJXXXGPX06A/X08A/X10A

**REGISTER 10-1: PMD1: PERIPHERAL MODULE DISABLE CONTROL REGISTER 1**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
T5MD	T4MD	T3MD	T2MD	T1MD	—	—	—
bit 15						bit 8	

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
I2C1MD	U2MD	U1MD	SPI2MD	SPI1MD	C2MD	C1MD	AD1MD <sup>(1)</sup>
bit 7						bit 0	

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **T5MD:** Timer5 Module Disable bit

1 = Timer5 module is disabled

0 = Timer5 module is enabled

bit 14 **T4MD:** Timer4 Module Disable bit

1 = Timer4 module is disabled

0 = Timer4 module is enabled

bit 13 **T3MD:** Timer3 Module Disable bit

1 = Timer3 module is disabled

0 = Timer3 module is enabled

bit 12 **T2MD:** Timer2 Module Disable bit

1 = Timer2 module is disabled

0 = Timer2 module is enabled

bit 11 **T1MD:** Timer1 Module Disable bit

1 = Timer1 module is disabled

0 = Timer1 module is enabled

bit 10-8 **Unimplemented:** Read as '0'

bit 7 **I2C1MD:** I<sup>2</sup>C1 Module Disable bit

1 = I<sup>2</sup>C1 module is disabled

0 = I<sup>2</sup>C1 module is enabled

bit 6 **U2MD:** UART2 Module Disable bit

1 = UART2 module is disabled

0 = UART2 module is enabled

bit 5 **U1MD:** UART1 Module Disable bit

1 = UART1 module is disabled

0 = UART1 module is enabled

bit 4 **SPI2MD:** SPI2 Module Disable bit

1 = SPI2 module is disabled

0 = SPI2 module is enabled

bit 3 **SPI1MD:** SPI1 Module Disable bit

1 = SPI1 module is disabled

0 = SPI1 module is enabled

bit 2 **C2MD:** ECAN2 Module Disable bit

1 = ECAN2 module is disabled

0 = ECAN2 module is enabled

**Note 1:** PCFGx bits have no effect if ADC module is disabled by setting this bit. In this case all port pins multiplexed with ANx will be in Digital mode.

# PIC24HJXXXGPX06A/X08A/X10A

## 14.1 Input Capture Registers

REGISTER 14-1: ICxCON: INPUT CAPTURE x CONTROL REGISTER

U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
—	—	ICSIDL	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R-0, HC	R-0, HC	R/W-0	R/W-0	R/W-0
ICTMR <sup>(1)</sup>	ICI<1:0>	ICOV	ICBNE	ICM<2:0>			
bit 7							bit 0

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-14      **Unimplemented:** Read as '0'

bit 13      **ICSIDL:** Input Capture Module Stop in Idle Control bit  
1 = Input capture module will halt in CPU Idle mode  
0 = Input capture module will continue to operate in CPU Idle mode

bit 12-8      **Unimplemented:** Read as '0'

bit 7      **ICTMR:** Input Capture Timer Select bits<sup>(1)</sup>  
1 = TMR2 contents are captured on capture event  
0 = TMR3 contents are captured on capture event

bit 6-5      **ICI<1:0>:** Select Number of Captures per Interrupt bits  
11 = Interrupt on every fourth capture event  
10 = Interrupt on every third capture event  
01 = Interrupt on every second capture event  
00 = Interrupt on every capture event

bit 4      **ICOV:** Input Capture Overflow Status Flag bit (read-only)  
1 = Input capture overflow occurred  
0 = No input capture overflow occurred

bit 3      **ICBNE:** Input Capture Buffer Empty Status bit (read-only)  
1 = Input capture buffer is not empty, at least one more capture value can be read  
0 = Input capture buffer is empty

bit 2-0      **ICM<2:0>:** Input Capture Mode Select bits  
111 = Input capture functions as interrupt pin only when device is in Sleep or Idle mode  
(Rising edge detect only, all other control bits are not applicable.)  
110 = Unused (module disabled)  
101 = Capture mode, every 16th rising edge  
100 = Capture mode, every 4th rising edge  
011 = Capture mode, every rising edge  
010 = Capture mode, every falling edge  
001 = Capture mode, every edge (rising and falling)  
(ICI<1:0> bits do not control interrupt generation for this mode.)  
000 = Input capture module turned off

# PIC24HJXXXGPX06A/X08A/X10A

## REGISTER 17-2: I2CxSTAT: I2Cx STATUS REGISTER

R-0 HSC	R-0 HSC	U-0	U-0	U-0	R/C-0 HS	R-0 HSC	R-0 HSC
ACKSTAT	TRSTAT	—	—	—	BCL	GCSTAT	ADD10
bit 15						bit 8	

R/C-0 HS	R/C-0 HS	R-0 HSC	R/C-0 HSC	R/C-0 HSC	R-0 HSC	R-0 HSC	R-0 HSC
IWCOL	I2COV	D_A	P	S	R_W	RBF	TBF
bit 7						bit 0	

<b>Legend:</b>	U = Unimplemented bit, read as '0'	C = Clear only bit
R = Readable bit	W = Writable bit	HS = Set in hardware
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

- bit 15      **ACKSTAT:** Acknowledge Status bit  
(when operating as I<sup>2</sup>C master, applicable to master transmit operation)  
1 = NACK received from slave  
0 = ACK received from slave  
Hardware set or clear at end of slave Acknowledge.
- bit 14      **TRSTAT:** Transmit Status bit (when operating as I<sup>2</sup>C master, applicable to master transmit operation)  
1 = Master transmit is in progress (8 bits + ACK)  
0 = Master transmit is not in progress  
Hardware set at beginning of master transmission. Hardware clear at end of slave Acknowledge.
- bit 13-11      **Unimplemented:** Read as '0'
- bit 10      **BCL:** Master Bus Collision Detect bit  
1 = A bus collision has been detected during a master operation  
0 = No collision  
Hardware set at detection of bus collision.
- bit 9      **GCSTAT:** General Call Status bit  
1 = General call address was received  
0 = General call address was not received  
Hardware set when address matches general call address. Hardware clear at Stop detection.
- bit 8      **ADD10:** 10-Bit Address Status bit  
1 = 10-bit address was matched  
0 = 10-bit address was not matched  
Hardware set at match of 2nd byte of matched 10-bit address. Hardware clear at Stop detection.
- bit 7      **IWCOL:** Write Collision Detect bit  
1 = An attempt to write the I2CxTRN register failed because the I<sup>2</sup>C module is busy  
0 = No collision  
Hardware set at occurrence of write to I2CxTRN while busy (cleared by software).
- bit 6      **I2COV:** Receive Overflow Flag bit  
1 = A byte was received while the I2CxRCV register is still holding the previous byte  
0 = No overflow  
Hardware set at attempt to transfer I2CxRSR to I2CxRCV (cleared by software).
- bit 5      **D\_A:** Data/Address bit (when operating as I<sup>2</sup>C slave)  
1 = Indicates that the last byte received was data  
0 = Indicates that the last byte received was device address  
Hardware clear at device address match. Hardware set by reception of slave byte.
- bit 4      **P:** Stop bit  
1 = Indicates that a Stop bit has been detected last  
0 = Stop bit was not detected last  
Hardware set or clear when Start, Repeated Start or Stop detected.

## 18.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

**Note 1:** This data sheet summarizes the features of the PIC24HJXXXGPX06A/X08A/X10A family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 17. “UART”** (DS70188) of the “dsPIC33F/PIC24H Family Reference Manual”, which is available from the Microchip web site (www.microchip.com).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The Universal Asynchronous Receiver Transmitter (UART) module is one of the serial I/O modules available in the PIC24HJXXXGPX06A/X08A/X10A device family. The UART is a full-duplex asynchronous system that can communicate with peripheral devices, such as personal computers, LIN, RS-232 and RS-485 interfaces. The module also supports a hardware flow control option with the UxCTS and UxRTS pins and also includes an IrDA® encoder and decoder.

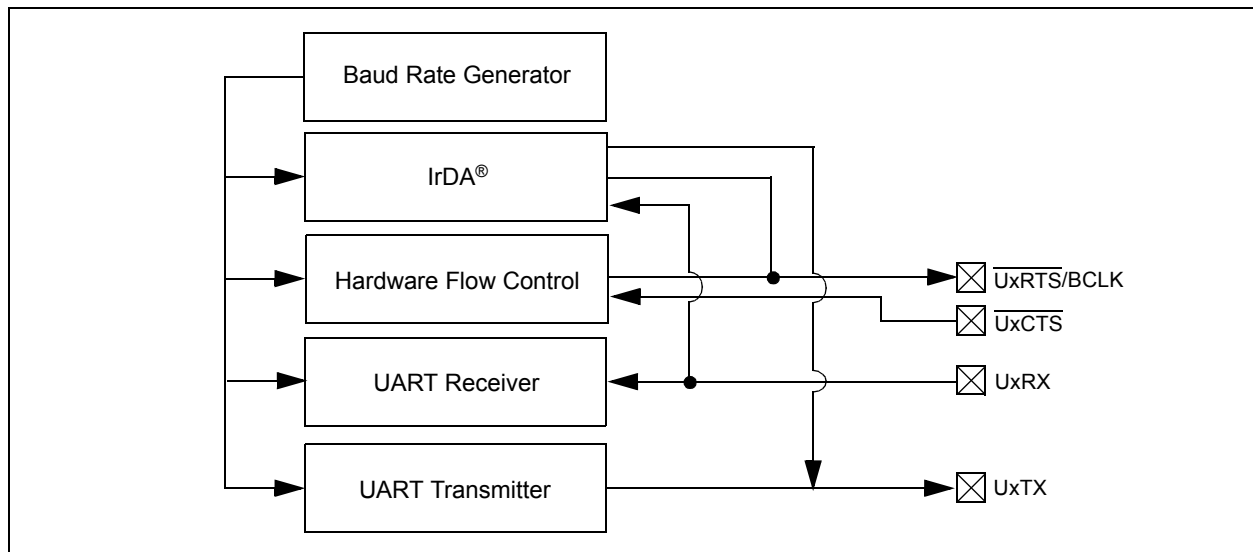
The primary features of the UART module are:

- Full-Duplex, 8 or 9-bit Data Transmission through the UxTX and UxRX pins
- Even, Odd or No Parity Options (for 8-bit data)
- One or Two Stop bits
- Hardware Flow Control Option with  $\overline{\text{UxCTS}}$  and  $\overline{\text{UxRTS}}$  pins
- Fully Integrated Baud Rate Generator with 16-bit Prescaler
- Baud rates ranging from 10 Mbps to 38 bps at 40 MIPS
- 4-deep First-In-First-Out (FIFO) Transmit Data Buffer
- 4-Deep FIFO Receive Data Buffer
- Parity, Framing and Buffer Overrun Error Detection
- Support for 9-bit mode with Address Detect (9th bit = 1)
- Transmit and Receive Interrupts
- A Separate Interrupt for all UART Error Conditions
- Loopback mode for Diagnostic Support
- Support for Sync and Break Characters
- Supports Automatic Baud Rate Detection
- IrDA® Encoder and Decoder Logic
- 16x Baud Clock Output for IrDA® Support

A simplified block diagram of the UART is shown in Figure 18-1. The UART module consists of the key important hardware elements:

- Baud Rate Generator
- Asynchronous Transmitter
- Asynchronous Receiver

**FIGURE 18-1: UART SIMPLIFIED BLOCK DIAGRAM**



**Note 1:** Both UART1 and UART2 can trigger a DMA data transfer. If U1TX, U1RX, U2TX or U2RX is selected as a DMA IRQ source, a DMA transfer occurs when the U1TXIF, U1RXIF, U2TXIF or U2RXIF bit gets set as a result of a UART1 or UART2 transmission or reception.

**2:** If DMA transfers are required, the UART TX/RX FIFO buffer must be set to a size of 1 byte/word (i.e., UTXISEL<1:0> = 00 and URXISEL<1:0> = 00).

## 19.0 ENHANCED CAN (ECAN™) MODULE

**Note 1:** This data sheet summarizes the features of the PIC24HJXXXGPX06A/X08A/X10A family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the “dsPIC33F/PIC24H Family Reference Manual”, **Section 21. “Enhanced Controller Area Network (ECAN™)”** (DS70185), which is available from the Microchip web site ([www.microchip.com](http://www.microchip.com)).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

### 19.1 Overview

The Enhanced Controller Area Network (ECAN™) module is a serial interface, useful for communicating with other CAN modules or microcontroller devices. This interface/protocol was designed to allow communications within noisy environments. The PIC24HJXXXGPX06A/X08A/X10A devices contain up to two ECAN modules.

The CAN module is a communication controller implementing the CAN 2.0 A/B protocol, as defined in the BOSCH specification. The module will support CAN 1.2, CAN 2.0A, CAN 2.0B Passive and CAN 2.0B Active versions of the protocol. The module implementation is a full CAN system. The CAN specification is not covered within this data sheet. The reader may refer to the BOSCH CAN specification for further details.

The module features are as follows:

- Implementation of the CAN protocol, CAN 1.2, CAN 2.0A and CAN 2.0B
- Standard and extended data frames
- 0-8 bytes data length
- Programmable bit rate up to 1 Mbit/sec
- Automatic response to remote transmission requests
- Up to 8 transmit buffers with application specified prioritization and abort capability (each buffer may contain up to 8 bytes of data)
- Up to 32 receive buffers (each buffer may contain up to 8 bytes of data)
- Up to 16 full (standard/extended identifier) acceptance filters
- 3 full acceptance filter masks
- DeviceNet™ addressing support
- Programmable wake-up functionality with integrated low-pass filter
- Programmable Loopback mode supports self-test operation

- Signaling via interrupt capabilities for all CAN receiver and transmitter error states
- Programmable clock source
- Programmable link to input capture module (IC2 for both CAN1 and CAN2) for time-stamping and network synchronization
- Low-power Sleep and Idle mode

The CAN bus module consists of a protocol engine and message buffering/control. The CAN protocol engine handles all functions for receiving and transmitting messages on the CAN bus. Messages are transmitted by first loading the appropriate data registers. Status and errors can be checked by reading the appropriate registers. Any message detected on the CAN bus is checked for errors and then matched against filters to see if it should be received and stored in one of the receive registers.

### 19.2 Frame Types

The CAN module transmits various types of frames which include data messages, remote transmission requests and as other frames that are automatically generated for control purposes. The following frame types are supported:

- **Standard Data Frame:**  
A standard data frame is generated by a node when the node wishes to transmit data. It includes an 11-bit standard identifier (SID) but not an 18-bit extended identifier (EID).
- **Extended Data Frame:**  
An extended data frame is similar to a standard data frame but includes an extended identifier as well.
- **Remote Frame:**  
It is possible for a destination node to request the data from the source. For this purpose, the destination node sends a remote frame with an identifier that matches the identifier of the required data frame. The appropriate data source node will then send a data frame as a response to this remote request.
- **Error Frame:**  
An error frame is generated by any node that detects a bus error. An error frame consists of two fields: an error flag field and an error delimiter field.
- **Overload Frame:**  
An overload frame can be generated by a node as a result of two conditions. First, the node detects a dominant bit during interframe space which is an illegal condition. Second, due to internal conditions, the node is not yet able to start reception of the next message. A node may generate a maximum of 2 sequential overload frames to delay the start of the next message.
- **Interframe Space:**  
Interframe space separates a proceeding frame (of whatever type) from a following data or remote frame.



# PIC24HJXXXGPX06A/X08A/X10A

**REGISTER 19-2: CICTRL2: ECAN™ MODULE CONTROL REGISTER 2**

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
—	—	—	DNCNT<4:0>				
bit 7							bit 0

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-5

**Unimplemented:** Read as '0'

bit 4-0

**DNCNT<4:0>:** DeviceNet™ Filter Bit Number bits

10010–11111 = Invalid selection

10001 = Compare up to data byte 3, bit 6 with EID<17>

•

•

•

00001 = Compare up to data byte 1, bit 7 with EID<0>

00000 = Do not compare data bytes

# PIC24HJXXXGPX06A/X08A/X10A

## REGISTER 19-10: C<sub>ICFG2</sub>: ECAN™ MODULE BAUD RATE CONFIGURATION REGISTER 2

U-0	R/W-x	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x
—	WAKFIL	—	—	—	SEG2PH<2:0>		
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
SEG2PHTS	SAM	SEG1PH<2:0>			PRSEG<2:0>		
bit 7							bit 0

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14 **WAKFIL:** Select CAN bus Line Filter for Wake-up bit

1 = Use CAN bus line filter for wake-up

0 = CAN bus line filter is not used for wake-up

bit 13-11 **Unimplemented:** Read as '0'

bit 10-8 **SEG2PH<2:0>:** Phase Buffer Segment 2 bits

111 = Length is 8 x T<sub>Q</sub>

000 = Length is 1 x T<sub>Q</sub>

bit 7 **SEG2PHTS:** Phase Segment 2 Time Select bit

1 = Freely programmable

0 = Maximum of SEG1PH bits or Information Processing Time (IPT), whichever is greater

bit 6 **SAM:** Sample of the CAN bus Line bit

1 = Bus line is sampled three times at the sample point

0 = Bus line is sampled once at the sample point

bit 5-3 **SEG1PH<2:0>:** Phase Buffer Segment 1 bits

111 = Length is 8 x T<sub>Q</sub>

000 = Length is 1 x T<sub>Q</sub>

bit 2-0 **PRSEG<2:0>:** Propagation Time Segment bits

111 = Length is 8 x T<sub>Q</sub>

000 = Length is 1 x T<sub>Q</sub>

# PIC24HJXXXGPX06A/X08A/X10A

## REGISTER 19-13: CiBUFPNT2: ECAN™ MODULE FILTER 4-7 BUFFER POINTER REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F7BP<3:0>				F6BP<3:0>			
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F5BP<3:0>				F4BP<3:0>			
bit 7				bit 0			

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-12 **F7BP<3:0>**: RX Buffer Written when Filter 7 Hits bits

1111 = Filter hits received in RX FIFO buffer

1110 = Filter hits received in RX Buffer 14

•  
•  
•

0001 = Filter hits received in RX Buffer 1

0000 = Filter hits received in RX Buffer 0

bit 11-8 **F6BP<3:0>**: RX Buffer Written when Filter 6 Hits bits

1111 = Filter hits received in RX FIFO buffer

1110 = Filter hits received in RX Buffer 14

•  
•  
•

0001 = Filter hits received in RX Buffer 1

0000 = Filter hits received in RX Buffer 0

bit 7-4 **F5BP<3:0>**: RX Buffer Written when Filter 5 Hits bits

1111 = Filter hits received in RX FIFO buffer

1110 = Filter hits received in RX Buffer 14

•  
•  
•

0001 = Filter hits received in RX Buffer 1

0000 = Filter hits received in RX Buffer 0

bit 3-0 **F4BP<3:0>**: RX Buffer Written when Filter 4 Hits bits

1111 = Filter hits received in RX FIFO buffer

1110 = Filter hits received in RX Buffer 14

•  
•  
•

0001 = Filter hits received in RX Buffer 1

0000 = Filter hits received in RX Buffer 0

# PIC24HJXXXGPX06A/X08A/X10A

**TABLE 24-41: ADC MODULE SPECIFICATIONS (10-BIT MODE)<sup>(1)</sup>**

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic	Min.	Typ	Max.	Units	Conditions
<b>ADC Accuracy (10-bit Mode) – Measurements with external VREF+/VREF-</b>							
AD20b	Nr	Resolution	10 data bits			bits	
AD21b	INL	Integral Nonlinearity	-1.5	—	+1.5	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V
AD22b	DNL	Differential Nonlinearity	>-1	—	<1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V
AD23b	GERR	Gain Error	—	3	6	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V
AD24b	EOFF	Offset Error	—	2	5	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V
AD25b	—	Monotonicity	—	—	—	—	Guaranteed
<b>ADC Accuracy (10-bit Mode) – Measurements with internal VREF+/VREF-</b>							
AD20b	Nr	Resolution	10 data bits			bits	
AD21b	INL	Integral Nonlinearity	-1	—	+1	LSb	VINL = AVSS = 0V, AVDD = 3.6V
AD22b	DNL	Differential Nonlinearity	>-1	—	<1	LSb	VINL = AVSS = 0V, AVDD = 3.6V
AD23b	GERR	Gain Error	—	7	15	LSb	VINL = AVSS = 0V, AVDD = 3.6V
AD24b	EOFF	Offset Error	—	3	7	LSb	VINL = AVSS = 0V, AVDD = 3.6V
AD25b	—	Monotonicity	—	—	—	—	Guaranteed
<b>Dynamic Performance (10-bit Mode)</b>							
AD30b	THD	Total Harmonic Distortion	—	—	-64	dB	—
AD31b	SINAD	Signal to Noise and Distortion	57	58.5	—	dB	—
AD32b	SFDR	Spurious Free Dynamic Range	72	—	—	dB	—
AD33b	FNYQ	Input Signal Bandwidth	—	—	550	kHz	—
AD34b	ENOB	Effective Number of Bits	9.16	9.4	—	bits	—

**Note 1:** Injection currents > | 0 | can affect the ADC results by approximately 4-6 counts (i.e., VIH source > (VDD + 0.3) or VIL source < (VSS – 0.3)).

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