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Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	40 MIPs
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	85
Program Memory Size	64KB (22K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 32x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24hj64gp510a-e-pf

PIC24HJXXXGPX06A/X08A/X10A

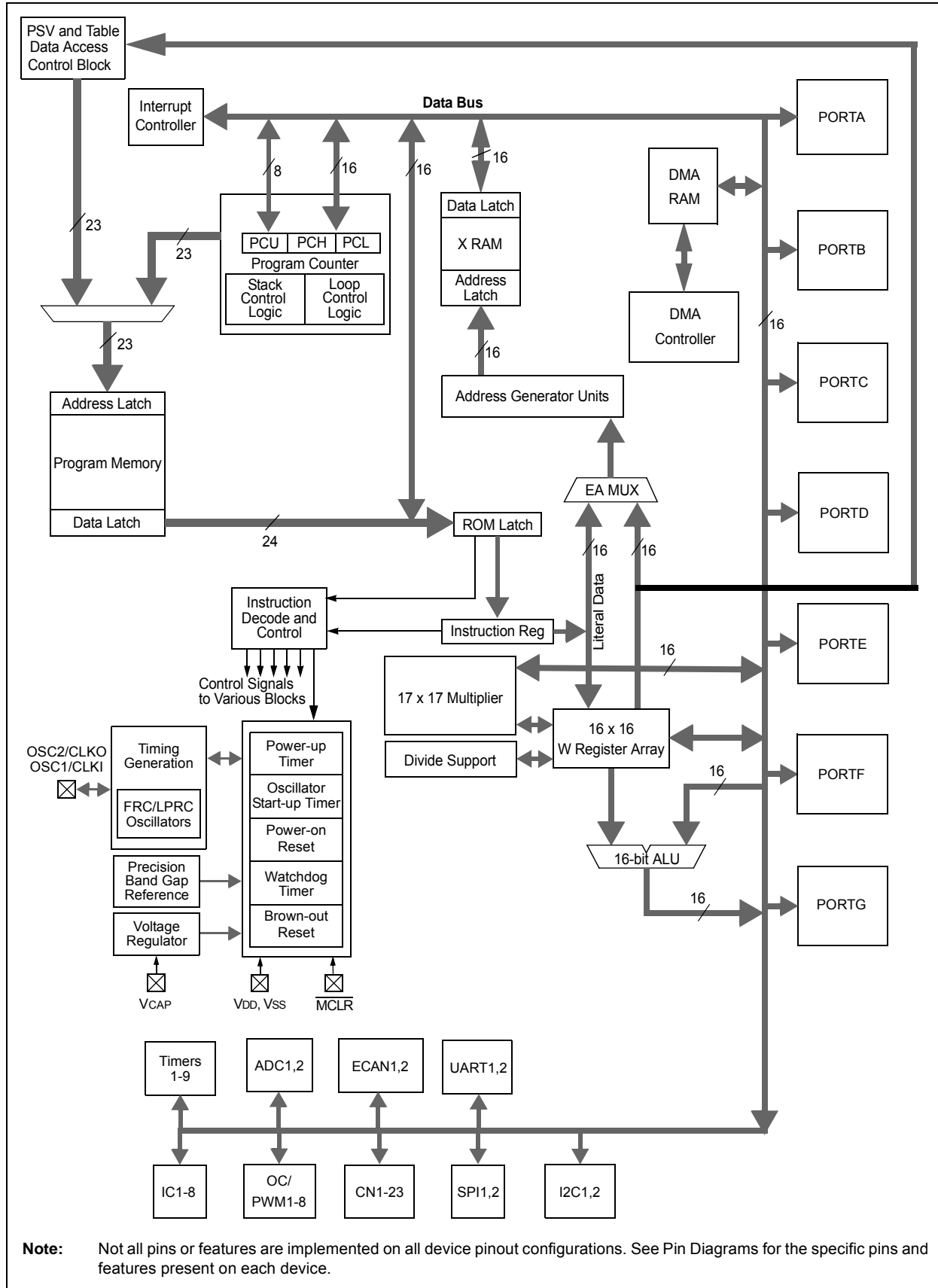**FIGURE 1-1:** **PIC24HJXXXGPX06A/X08A/X10A GENERAL BLOCK DIAGRAM**

Note: Not all pins or features are implemented on all device pinout configurations. See Pin Diagrams for the specific pins and features present on each device.

PIC24HJXXXGPX06A/X08A/X10A

TABLE 4-1: CPU CORE REGISTERS MAP

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
WREG0	0000								Working Register 0									xxxx
WREG1	0002								Working Register 1									xxxx
WREG2	0004								Working Register 2									xxxx
WREG3	0006								Working Register 3									xxxx
WREG4	0008								Working Register 4									xxxx
WREG5	000A								Working Register 5									xxxx
WREG6	000C								Working Register 6									xxxx
WREG7	000E								Working Register 7									xxxx
WREG8	0010								Working Register 8									xxxx
WREG9	0012								Working Register 9									xxxx
WREG10	0014								Working Register 10									xxxx
WREG11	0016								Working Register 11									xxxx
WREG12	0018								Working Register 12									xxxx
WREG13	001A								Working Register 13									xxxx
WREG14	001C								Working Register 14									xxxx
WREG15	001E								Working Register 15									0800
SPLIM	0020								Stack Pointer Limit Register									xxxx
PCL	002E								Program Counter Low Word Register									0000
PCH	0030	—	—	—	—	—	—	—	—	Program Counter High Byte Register								0000
TBLPAG	0032	—	—	—	—	—	—	—	—	Table Page Address Pointer Register								0000
PSVPAG	0034	—	—	—	—	—	—	—	—	Program Memory Visibility Page Address Pointer Register								0000
RCOUNT	0036								Repeat Loop Counter Register									xxxx
SR	0042	—	—	—	—	—	—	—	DC	IPL<2:0>			RA	N	OV	Z	C	0000
CORCON	0044	—	—	—	—	—	—	—	—	—	—	—	—	IPL3	PSV	—	—	0000
DISICNT	0052	—	—	Disable Interrupts Counter Register														xxxx
BSRAM	0750		—	—	—	—	—	—	—	—	—	—	—	IW_BSR	IR_BSR	RL_BSR		0000
SSRAM	0752		—	—	—	—	—	—	—	—	—	—	—	IW_SSR	IR_SSR	RL_SSR		0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal for PinHigh devices.

TABLE 4-20: **ECAN1 REGISTER MAP WHEN C1CTRL1.WIN = 1 FOR PIC24HJXXXGP506A/510A/610A DEVICES ONLY (CONTINUED)**

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
C1RXF1EID	0446	EID<15:8>								EID<7:0>								xxxx
C1RXF2SID	0448	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C1RXF2EID	044A	EID<15:8>								EID<7:0>								xxxx
C1RXF3SID	044C	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C1RXF3EID	044E	EID<15:8>								EID<7:0>								xxxx
C1RXF4SID	0450	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C1RXF4EID	0452	EID<15:8>								EID<7:0>								xxxx
C1RXF5SID	0454	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C1RXF5EID	0456	EID<15:8>								EID<7:0>								xxxx
C1RXF6SID	0458	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C1RXF6EID	045A	EID<15:8>								EID<7:0>								xxxx
C1RXF7SID	045C	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C1RXF7EID	045E	EID<15:8>								EID<7:0>								xxxx
C1RXF8SID	0460	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C1RXF8EID	0462	EID<15:8>								EID<7:0>								xxxx
C1RXF9SID	0464	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C1RXF9EID	0466	EID<15:8>								EID<7:0>								xxxx
C1RXF10SID	0468	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C1RXF10EID	046A	EID<15:8>								EID<7:0>								xxxx
C1RXF11SID	046C	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C1RXF11EID	046E	EID<15:8>								EID<7:0>								xxxx
C1RXF12SID	0470	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C1RXF12EID	0472	EID<15:8>								EID<7:0>								xxxx
C1RXF13SID	0474	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C1RXF13EID	0476	EID<15:8>								EID<7:0>								xxxx
C1RXF14SID	0478	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C1RXF14EID	047A	EID<15:8>								EID<7:0>								xxxx
C1RXF15SID	047C	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C1RXF15EID	047E	EID<15:8>								EID<7:0>								xxxx

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal for PinHigh devices.

PIC24HJXXXGPX06A/X08A/X10A

4.2.6 SOFTWARE STACK

In addition to its use as a working register, the W15 register in the PIC24HJXXXGPX06A/X08A/X10A devices is also used as a software Stack Pointer. The Stack Pointer always points to the first available free word and grows from lower to higher addresses. It pre-decrements for stack pops and post-increments for stack pushes, as shown in Figure 4-5. For a PC push during any CALL instruction, the MSB of the PC is zero-extended before the push, ensuring that the MSB is always clear.

> **Note:** A PC push during exception processing concatenates the SRL register to the MSB of the PC prior to the push.

The Stack Pointer Limit register (SPLIM) associated with the Stack Pointer sets an upper address boundary for the stack. SPLIM is uninitialized at Reset. As is the case for the Stack Pointer, SPLIM<0> is forced to '0' because all stack operations must be word-aligned. Whenever an EA is generated using W15 as a source or destination pointer, the resulting address is compared with the value in SPLIM. If the contents of the Stack Pointer (W15) and the SPLIM register are equal and a push operation is performed, a stack error trap will not occur. The stack error trap will occur on a subsequent push operation. Thus, for example, if it is desirable to cause a stack error trap when the stack grows beyond address 0x2000 in RAM, initialize the SPLIM with the value 0x1FFE.

Similarly, a Stack Pointer underflow (stack error) trap is generated when the Stack Pointer address is found to be less than 0x0800. This prevents the stack from interfering with the Special Function Register (SFR) space.

A write to the SPLIM register should not be immediately followed by an indirect read operation using W15.

FIGURE 4-5: **CALL STACK FRAME**
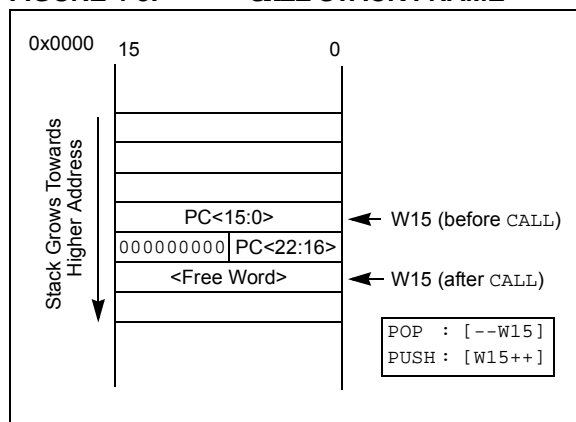
4.2.7 DATA RAM PROTECTION FEATURE

The PIC24H product family supports Data RAM protection features that enable segments of RAM to be protected when used in conjunction with Boot and Secure Code Segment Security. BSRAM (Secure RAM segment for BS) is accessible only from the Boot Segment Flash code, when enabled. SSRAM (Secure RAM segment for RAM) is accessible only from the Secure Segment Flash code, when enabled. See Table 4-1 for an overview of the BSRAM and SSRAM SFRs.

4.3 Instruction Addressing Modes

The addressing modes in Table 4-34 form the basis of the addressing modes optimized to support the specific features of individual instructions. The addressing modes provided in the MAC class of instructions are somewhat different from those in the other instruction types.

4.3.1 FILE REGISTER INSTRUCTIONS

Most file register instructions use a 13-bit address field (f) to directly address data present in the first 8192 bytes of data memory (Near Data Space). Most file register instructions employ a working register, W0, which is denoted as WREG in these instructions. The destination is typically either the same file register or WREG (with the exception of the MUL instruction), which writes the result to a register or register pair. The MOV instruction allows additional flexibility and can access the entire data space.

4.3.2 MCU INSTRUCTIONS

The 3-operand MCU instructions are of the form:

Operand 3 = Operand 1 <function> Operand 2

where:

Operand 1 is always a working register (i.e., the addressing mode can only be Register Direct) which is referred to as Wb.

Operand 2 can be a W register, fetched from data memory, or a 5-bit literal. The result location can be either a W register or a data memory location. The following addressing modes are supported by MCU instructions:

- Register Direct
- Register Indirect
- Register Indirect Post-Modified
- Register Indirect Pre-Modified
- 5-bit or 10-bit Literal

> **Note:** Not all instructions support all the addressing modes given above. Individual instructions may support different subsets of these addressing modes.

REGISTER 7-6:   IFS1: INTERRUPT FLAG STATUS REGISTER 1 (CONTINUED)

bit 3   **CNIF:** Input Change Notification Interrupt Flag Status bit

1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 2   **Unimplemented:** Read as '0'

bit 1   **MI2C1IF:** I2C1 Master Events Interrupt Flag Status bit

1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 0   **SI2C1IF:** I2C1 Slave Events Interrupt Flag Status bit

1 = Interrupt request has occurred
0 = Interrupt request has not occurred

REGISTER 7-10: IEC0: INTERRUPT ENABLE CONTROL REGISTER 0

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	DMA1IE	AD1IE	U1TXIE	U1RXIE	SPI1IE	SPI1EIE	T3IE
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
T2IE	OC2IE	IC2IE	DMA0IE	T1IE	OC1IE	IC1IE	INT0IE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14 **DMA1IE:** DMA Channel 1 Data Transfer Complete Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 13 **AD1IE:** ADC1 Conversion Complete Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 12 **U1TXIE:** UART1 Transmitter Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 11 **U1RXIE:** UART1 Receiver Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 10 **SPI1IE:** SPI1 Event Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 9 **SPI1EIE:** SPI1 Error Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 8 **T3IE:** Timer3 Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 7 **T2IE:** Timer2 Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 6 **OC2IE:** Output Compare Channel 2 Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 5 **IC2IE:** Input Capture Channel 2 Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 4 **DMA0IE:** DMA Channel 0 Data Transfer Complete Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 3 **T1IE:** Timer1 Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

REGISTER 7-22: **IPC7: INTERRUPT PRIORITY CONTROL REGISTER 7**

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	U2TXIP<2:0>			—	U2RXIP<2:0>		
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	INT2IP<2:0>			—	T5IP<2:0>		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15   **Unimplemented:** Read as '0'

bit 14-12   **U2TXIP<2:0>:** UART2 Transmitter Interrupt Priority bits
              111 = Interrupt is priority 7 (highest priority interrupt)
              •
              •
              •
              001 = Interrupt is priority 1
              000 = Interrupt source is disabled

bit 11   **Unimplemented:** Read as '0'

bit 10-8   **U2RXIP<2:0>:** UART2 Receiver Interrupt Priority bits
              111 = Interrupt is priority 7 (highest priority interrupt)
              •
              •
              •
              001 = Interrupt is priority 1
              000 = Interrupt source is disabled

bit 7   **Unimplemented:** Read as '0'

bit 6-4   **INT2IP<2:0>:** External Interrupt 2 Priority bits
              111 = Interrupt is priority 7 (highest priority interrupt)
              •
              •
              •
              001 = Interrupt is priority 1
              000 = Interrupt source is disabled

bit 3   **Unimplemented:** Read as '0'

bit 2-0   **T5IP<2:0>:** Timer5 Interrupt Priority bits
              111 = Interrupt is priority 7 (highest priority interrupt)
              •
              •
              •
              001 = Interrupt is priority 1
              000 = Interrupt source is disabled

8.0 DIRECT MEMORY ACCESS (DMA)

> **Note 1:** This data sheet summarizes the features of the PIC24HJXXXGPX06A/X08A/X10A family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 22. "Direct Memory Access (DMA)"** (DS70182) of the *"dsPIC33F/PIC24H Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).
>
> **2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

Direct Memory Access (DMA) is a very efficient mechanism of copying data between peripheral SFRs (e.g., UART Receive register, Input Capture 1 buffer), and buffers or variables stored in RAM, with minimal CPU intervention. The DMA controller can automatically copy entire blocks of data without requiring the user software to read or write the peripheral Special Function Registers (SFRs) every time a peripheral interrupt occurs. The DMA controller uses a dedicated bus for data transfers and, therefore, does not steal cycles from the code execution flow of the CPU. To exploit the DMA capability, the corresponding user buffers or variables must be located in DMA RAM.

The PIC24HJXXXGPX06A/X08A/X10A peripherals that can utilize DMA are listed in Table 8-1 along with their associated Interrupt Request (IRQ) numbers.

TABLE 8-1: PERIPHERALS WITH DMA SUPPORT

Peripheral	IRQ Number
INT0	0
Input Capture 1	1
Input Capture 2	5
Output Compare 1	2
Output Compare 2	6
Timer2	7
Timer3	8
SPI1	10
SPI2	33
UART1 Reception	11
UART1 Transmission	12
UART2 Reception	30
UART2 Transmission	31
ADC1	13
ADC2	21
ECAN1 Reception	34
ECAN1 Transmission	70
ECAN2 Reception	55
ECAN2 Transmission	71

The DMA controller features eight identical data transfer channels.

Each channel has its own set of control and status registers. Each DMA channel can be configured to copy data either from buffers stored in dual port DMA RAM to peripheral SFRs, or from peripheral SFRs to buffers in DMA RAM.

The DMA controller supports the following features:

- Word or byte sized data transfers
- Transfers from peripheral to DMA RAM or DMA RAM to peripheral
- Indirect Addressing of DMA RAM locations with or without automatic post-increment
- Peripheral Indirect Addressing – In some peripherals, the DMA RAM read/write addresses may be partially derived from the peripheral
- One-Shot Block Transfers – Terminating DMA transfer after one block transfer
- Continuous Block Transfers – Reloading DMA RAM buffer start address after every block transfer is complete
- Ping-Pong Mode – Switching between two DMA RAM start addresses between successive block transfers, thereby filling two buffers alternately
- Automatic or manual initiation of block transfers
- Each channel can select from 19 possible sources of data sources or destinations

For each DMA channel, a DMA interrupt request is generated when a block transfer is complete. Alternatively, an interrupt can be generated when half of the block has been filled.

TABLE 21-2:   CONFIGURATION BITS DESCRIPTION (CONTINUED)

Bit Field	Register	RTSP Effect	Description
FPWRT<2:0>	FPOR	Immediate	Power-on Reset Timer Value Select bits `111` = PWRT = 128 ms `110` = PWRT = 64 ms `101` = PWRT = 32 ms `100` = PWRT = 16 ms `011` = PWRT = 8 ms `010` = PWRT = 4 ms `001` = PWRT = 2 ms `000` = PWRT = Disabled
JTAGEN	FICD	Immediate	JTAG Enable bits `1` = JTAG enabled `0` = JTAG disabled
ICS<1:0>	FICD	Immediate	ICD Communication Channel Select bits `11` = Communicate on PGEC1 and PGED1 `10` = Communicate on PGEC2 and PGED2 `01` = Communicate on PGEC3 and PGED3 `00` = Reserved

TABLE 22-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax		Description	# of Words	# of Cycles	Status Flags Affected
66	TBLRDL	TBLRDL	Ws,Wd	Read Prog<15:0> to Wd	1	2	None
67	TBLWTH	TBLWTH	Ws,Wd	Write Ws<7:0> to Prog<23:16>	1	2	None
68	TBLWTL	TBLWTL	Ws,Wd	Write Ws to Prog<15:0>	1	2	None
69	ULNK	ULNK		Unlink Frame Pointer	1	1	None
70	XOR	XOR	f	f = f .XOR. WREG	1	1	N,Z
		XOR	f,WREG	WREG = f .XOR. WREG	1	1	N,Z
		XOR	#lit10,Wn	Wd = lit10 .XOR. Wd	1	1	N,Z
		XOR	Wb,Ws,Wd	Wd = Wb .XOR. Ws	1	1	N,Z
		XOR	Wb,#lit5,Wd	Wd = Wb .XOR. lit5	1	1	N,Z
71	ZE	ZE	Ws,Wnd	Wnd = Zero-extend Ws	1	1	C,Z,N

23.2 MPLAB C Compilers for Various Device Families

The MPLAB C Compiler code development systems are complete ANSI C compilers for Microchip's PIC18, PIC24 and PIC32 families of microcontrollers and the dsPIC30 and dsPIC33 families of digital signal controllers. These compilers provide powerful integration capabilities, superior code optimization and ease of use.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

23.3 HI-TECH C for Various Device Families

The HI-TECH C Compiler code development systems are complete ANSI C compilers for Microchip's PIC family of microcontrollers and the dsPIC family of digital signal controllers. These compilers provide powerful integration capabilities, omniscient code generation and ease of use.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

The compilers include a macro assembler, linker, pre-processor, and one-step driver, and can run on multiple platforms.

23.4 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multi-purpose source files
- Directives that allow complete control over the assembly process

23.5 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler and the MPLAB C18 C Compiler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

23.6 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC devices. MPLAB C Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command line interface
- Rich directive set
- Flexible macro language
- MPLAB IDE compatibility

24.2 AC Characteristics and Timing Parameters

This section defines PIC24HJXXXGPX06A/X08A/X10A AC characteristics and timing parameters.

TABLE 24-14: TEMPERATURE AND VOLTAGE SPECIFICATIONS – AC

AC CHARACTERISTICS	Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended Operating voltage VDD range as described in Table 24-1.

FIGURE 24-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS

Load Condition 1 – for all pins except OSC2

Load Condition 2 – for OSC2

VDD/2

RL

Pin

CL

Vss

Pin

CL

Vss

RL = 464Ω
CL = 50 pF for all pins except OSC2
     15 pF for OSC2 output
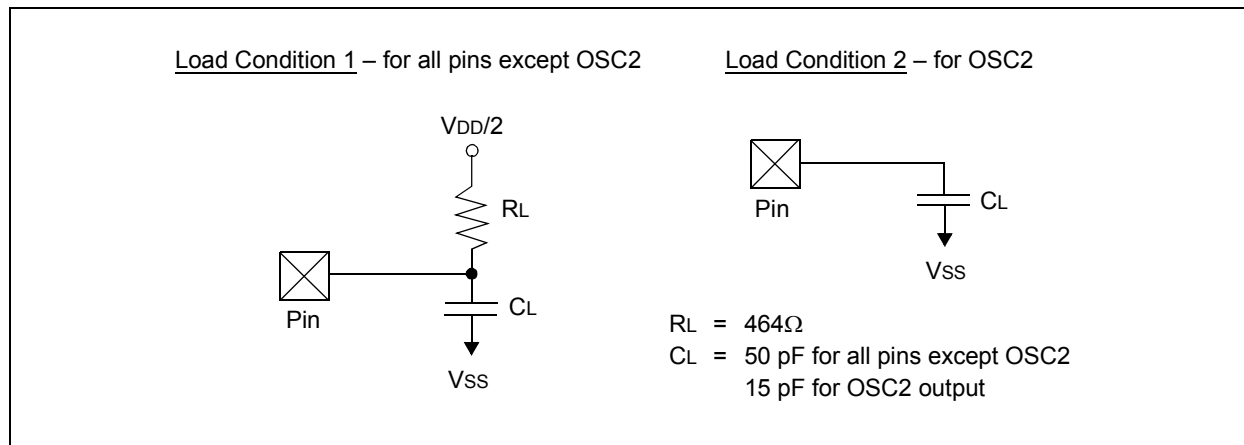
TABLE 24-15: CAPACITIVE LOADING REQUIREMENTS ON OUTPUT PINS

Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
DO50	C_{OSCO}	OSC2/SOSCO pin	—	—	15	pF	In XT and HS modes when external clock is used to drive OSC1
DO56	C_{IO}	All I/O pins and OSC2	—	—	50	pF	EC mode
DO58	C_B	SCLx, SDAx	—	—	400	pF	In I^{2}C™ mode

FIGURE 24-8: **OC/PWM MODULE TIMING CHARACTERISTICS**
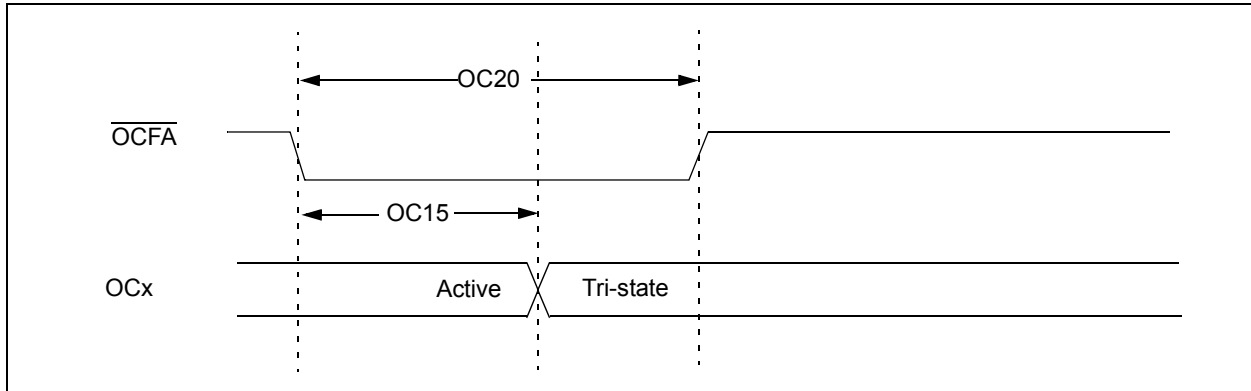
TABLE 24-27: **SIMPLE OC/PWM MODE TIMING REQUIREMENTS**

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic[1]	Min	Typ	Max	Units	Conditions
OC15	T_{FD}	Fault Input to PWM I/O Change	—	—	T_{CY}+20	ns	—
OC20	T_{FLT}	Fault Input Pulse-Width	T_{CY}+20	—	—	ns	—

Note 1:   These parameters are characterized but not tested in manufacturing.

TABLE 24-34: SPIx SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.4V to 3.6V (unless otherwise stated)					
			Operating temperature -40°C $\leq$ TA $\leq$ +85°C for Industrial -40°C $\leq$ TA $\leq$ +125°C for Extended					
Param No.	Symbol	Characteristic[1]	Min	Typ[2]	Max	Units	Conditions	
SP70	TscP	Maximum SCK Input Frequency	—	—	15	MHz	See **Note 3**	
SP72	TscF	SCKx Input Fall Time	—	—	—	ns	See parameter DO32 and **Note 4**	
SP73	TscR	SCKx Input Rise Time	—	—	—	ns	See parameter DO31 and **Note 4**	
SP30	TdoF	SDOx Data Output Fall Time	—	—	—	ns	See parameter DO32 and **Note 4**	
SP31	TdoR	SDOx Data Output Rise Time	—	—	—	ns	See parameter DO31 and **Note 4**	
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	6	20	ns	—	
SP36	TdoV2scH, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	—	ns	—	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	—	—	ns	—	
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	—	—	ns	—	
SP50	TssL2scH, TssL2scL	$\overline{SSx}$ ↓ to SCKx ↑ or SCKx Input	120	—	—	ns	—	
SP51	TssH2doZ	$\overline{SSx}$ ↑ to SDOx Output High-Impedance[4]	10	—	50	ns	—	
SP52	TscH2ssH TscL2ssH	$\overline{SSx}$ after SCKx Edge	1.5 TCY + 40	—	—	ns	See **Note 4**	

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated.

3: The minimum clock period for SCKx is 66.7 ns. Therefore, the SCK clock generated by the Master must not violate this specificiation.

4: Assumes 50 pF load on all SPIx pins.

TABLE 24-35: SPIx SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.4V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic[1]	Min	Typ[2]	Max	Units	Conditions
SP70	TscP	Maximum SCK Input Frequency	—	—	11	MHz	See **Note 3**
SP72	TscF	SCKx Input Fall Time	—	—	—	ns	See parameter DO32 and **Note 4**
SP73	TscR	SCKx Input Rise Time	—	—	—	ns	See parameter DO31 and **Note 4**
SP30	TdoF	SDOx Data Output Fall Time	—	—	—	ns	See parameter DO32 and **Note 4**
SP31	TdoR	SDOx Data Output Rise Time	—	—	—	ns	See parameter DO31 and **Note 4**
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	6	20	ns	—
SP36	TdoV2scH, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	—	ns	—
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	—	—	ns	—
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	—	—	ns	—
SP50	TssL2scH, TssL2scL	$\overline{SSx}$ ↓ to SCKx ↑ or SCKx Input	120	—	—	ns	—
SP51	TssH2doZ	$\overline{SSx}$ ↑ to SDOx Output High-Impedance[4]	10	—	50	ns	—
SP52	TscH2ssH TscL2ssH	$\overline{SSx}$ after SCKx Edge	1.5 TCY + 40	—	—	ns	See **Note 4**

Note 1: These parameters are characterized, but are not tested in manufacturing.
   2: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated.
   3: The minimum clock period for SCKx is 91 ns. Therefore, the SCK clock generated by the Master must not violate this specificiation.
   4: Assumes 50 pF load on all SPIx pins.

FIGURE 24-19: **I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (SLAVE MODE)**
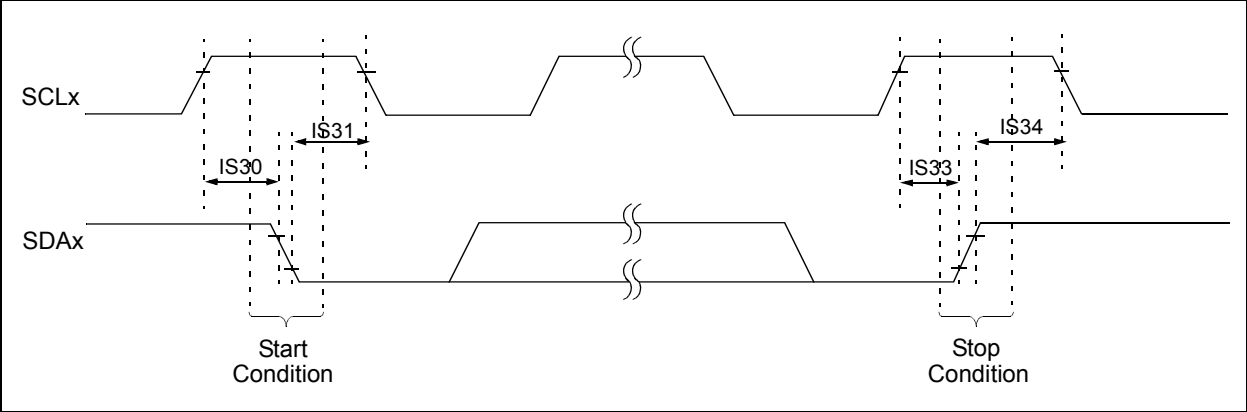
FIGURE 24-20: **I2Cx BUS DATA TIMING CHARACTERISTICS (SLAVE MODE)**
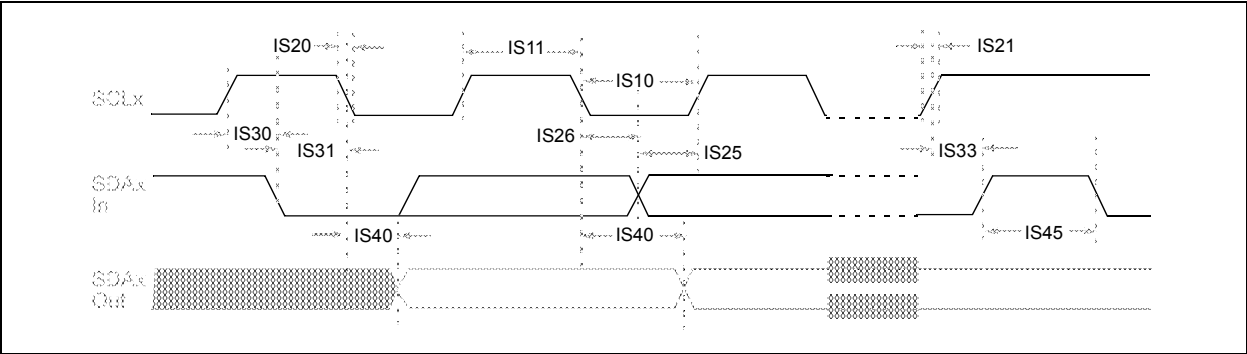
25.0 HIGH TEMPERATURE ELECTRICAL CHARACTERISTICS

This section provides an overview of PIC24HJXXXGPX06A/X08A/X10A electrical characteristics for devices operating in an ambient temperature range of -40°C to +150°C.

The specifications between -40°C to +150°C are identical to those shown in **Section 24.0 "Electrical Characteristics"** for operation between -40°C to +125°C, with the exception of the parameters listed in this section.

Parameters in this section begin with an H, which denotes High temperature. For example, parameter DC10 in **Section 24.0 "Electrical Characteristics"** is the Industrial and Extended temperature equivalent of HDC10.

Absolute maximum ratings for the PIC24HJXXXGPX06A/X08A/X10A high temperature devices are listed below. Exposure to these maximum rating conditions for extended periods can affect device reliability. Functional operation of the device at these or any other conditions above the parameters indicated in the operation listings of this specification is not implied.

Absolute Maximum Ratings
(See Note 1)

Ambient temperature under bias[4] ....-40°C to +150°C
Storage temperature .... -65°C to +160°C
Voltage on V_{DD} with respect to V_{SS} .... -0.3V to +4.0V
Voltage on any pin that is not 5V tolerant with respect to V_{SS}[5] .... -0.3V to (V_{DD} + 0.3V)
Voltage on any 5V tolerant pin with respect to V_{SS} when V_{DD} < 3.0V[5] .... -0.3V to (V_{DD} + 0.3V)
Voltage on any 5V tolerant pin with respect to V_{SS} when $V_{DD} \geq 3.0V$[5] .... -0.3V to 5.6V
Voltage on V_{CAP} with respect to V_{SS} .... 2.25V to 2.75V
Maximum current out of V_{SS} pin ....60 mA
Maximum current into V_{DD} pin[2] ....60 mA
Maximum junction temperature.. +155°C
Maximum current sourced/sunk by any 2x I/O pin[3] ....2 mA
Maximum current sourced/sunk by any 4x I/O pin[3] ....4 mA
Maximum current sourced/sunk by any 8x I/O pin[3] ....8 mA
Maximum current sunk by all ports combined ....10 mA
Maximum current sourced by all ports combined[2] ....10 mA

> **Note 1:** Stresses above those listed under "Absolute Maximum Ratings" can cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods can affect device reliability.
>
> **2:** Maximum allowable current is a function of device maximum power dissipation (see Table 25-2).
>
> **3:** Unlike devices at 125°C and below, the specifications in this section also apply to the CLKOUT, V_{REF}+, V_{REF}-, SCLx, SDAx, PGECx, and PGEDx pins.
>
> **4:** AEC-Q100 reliability testing for devices intended to operate at 150°C is 1,000 hours. Any design in which the total operating time from 125°C to 150°C will be greater than 1,000 hours is not warranted without prior written approval from Microchip Technology Inc.
>
> **5:** Refer to the **"Pin Diagrams"** section for 5V tolerant pins.

TABLE B-2: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
Section 24.0 "Electrical Characteristics"	Removed Note 4 from the DC Temperature and Voltage Specifications (see Table 24-4).
	Updated the maximum value for parameter DI19 and added parameters DI28, DI29, DI60a, DI60b, and DI60c to the I/O Pin Input Specifications (see Table 24-9).
	Removed Note 2 from the AC Characteristics: Internal RC Accuracy (see Table 24-18).
	Updated the characteristic description for parameter DI35 in the I/O Timing Requirements (see Table 24-20).
	Updated the ADC Module Specification minimum values for parameters AD05 and AD07, and updated the maximum value for parameter AD06 (see Table 24-39).
	Added Note 1 to the ADC Module Specifications (12-bit Mode) (see Table 24-40).
	Added Note 1 to the ADC Module Specifications (10-bit Mode) (see Table 24-41).
	Added DMA Read/Write Timing Requirements (see Table 24-44).
Section 25.0 "High Temperature Electrical Characteristics"	Updated all ambient temperature end range values to +150ºC throughout the chapter.
	Updated the storage temperature end range to +160ºC.
	Updated the maximum junction temperature from +145ºC to +155ºC.
	Updated the maximum values for High Temperature Devices in the Thermal Operating Conditions (see Table 25-2).
	Added Note 3 and updated the ADC Module Specifications (12-bit Mode), removing all parameters with the exception of HAD33a (see Table 25-15).
	Added Note 3 and updated the ADC Module Specifications (10-bit Mode), removing all parameters with the exception of HAD33b (see Table 25-16).

PIC24HJXXXGPX06A/X08A/X10A

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