

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	40 MIPs
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	85
Program Memory Size	64KB (22K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 32x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24hj64gp510a-e-pt

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Pin Diagrams (Continued)



3.4 Arithmetic Logic Unit (ALU)

The PIC24HJXXXGPX06A/X08A/X10A ALU is 16 bits wide and is capable of addition, subtraction, bit shifts and logic operations. Unless otherwise mentioned, arithmetic operations are 2's complement in nature. Depending on the operation, the ALU may affect the values of the Carry (C), Zero (Z), Negative (N), Overflow (OV) and Digit Carry (DC) Status bits in the <u>SR register</u>. The <u>C and DC</u> Status bits operate as Borrow and Digit Borrow bits, respectively, for subtraction operations.

The ALU can perform 8-bit or 16-bit operations, depending on the mode of the instruction that is used. Data for the ALU operation can come from the W register array, or data memory, depending on the addressing mode of the instruction. Likewise, output data from the ALU can be written to the W register array or a data memory location.

Refer to the "16-bit MCU and DSC Programmer's Reference Manual" (DS70157) for information on the SR bits affected by each instruction.

The PIC24HJXXXGPX06A/X08A/X10A CPU incorporates hardware support for both multiplication and division. This includes a dedicated hardware multiplier and support hardware for 16-bit divisor division.

3.4.1 MULTIPLIER

Using the high-speed 17-bit x 17-bit multiplier, the ALU supports unsigned, signed or mixed-sign operation in several multiplication modes:

- 16-bit x 16-bit signed
- 16-bit x 16-bit unsigned
- 16-bit signed x 5-bit (literal) unsigned
- 16-bit unsigned x 16-bit unsigned
- 16-bit unsigned x 5-bit (literal) unsigned
- 16-bit unsigned x 16-bit signed
- 8-bit unsigned x 8-bit unsigned

3.4.2 DIVIDER

The divide block supports 32-bit/16-bit and 16-bit/16-bit signed and unsigned integer divide operations with the following data sizes:

- 32-bit signed/16-bit signed divide
- 32-bit unsigned/16-bit unsigned divide
- 16-bit signed/16-bit signed divide
- 16-bit unsigned/16-bit unsigned divide

The quotient for all divide instructions ends up in W0 and the remainder in W1. Sixteen-bit signed and unsigned DIV instructions can specify any W register for both the 16-bit divisor (Wn) and any W register (aligned) pair (W(m + 1):Wm) for the 32-bit dividend. The divide algorithm takes one cycle per bit of divisor, so both 32-bit/16-bit and 16-bit/16-bit instructions take the same number of cycles to execute.

3.4.3 MULTI-BIT DATA SHIFTER

The multi-bit data shifter is capable of performing up to 16-bit arithmetic or logic right shifts, or up to 16-bit left shifts in a single cycle. The source can be either a working register or a memory location.

The shifter requires a signed binary value to determine both the magnitude (number of bits) and direction of the shift operation. A positive value shifts the operand right. A negative value shifts the operand left. A value of '0' does not modify the operand.

IADLE 4	19.	ECAN	I KEGIS					$\mathbf{IN} = 0 \mathbf{F}$		24ПЈЛЛ	VGE 200	DAISIUF	VOIUAL					
File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
	0400- 041E							See	e definition	when WIN	= x							
C1RXFUL1	0420	RXFUL15	RXFUL14	RXFUL13	RXFUL12	RXFUL11	RXFUL10	RXFUL9	RXFUL8	RXFUL7	RXFUL6	RXFUL5	RXFUL4	RXFUL3	RXFUL2	RXFUL1	RXFUL0	0000
C1RXFUL2	0422	RXFUL31	RXFUL30	RXFUL29	RXFUL28	RXFUL27	RXFUL26	RXFUL25	RXFUL24	RXFUL23	RXFUL22	RXFUL21	RXFUL20	RXFUL19	RXFUL18	RXFUL17	RXFUL16	0000
C1RXOVF1	0428	RXOVF15	RXOVF14	RXOVF13	RXOVF12	RXOVF11	RXOVF10	RXOVF9	RXOVF8	RXOVF7	RXOVF6	RXOVF5	RXOVF4	RXOVF3	RXOVF2	RXOVF1	RXOVF0	0000
C1RXOVF2	042A	RXOVF31	RXOVF30	RXOVF29	RXOVF28	RXOVF27	RXOVF26	RXOVF25	RXOVF24	RXOVF23	RXOVF22	RXOVF21	RXOVF20	RXOVF19	RXOVF18	RXOVF17	RXOVF16	0000
C1TR01CO N	0430	TXEN1	TX ABT1	TX LARB1	TX ERR1	TX REQ1	RTREN1	TX1PF	RI<1:0>	TXEN0	TX ABAT0	TX LARB0	TX ERR0	TX REQ0	RTREN0	TX0PF	રા<1:0>	0000
C1TR23CO N	0432	TXEN3	TX ABT3	TX LARB3	TX ERR3	TX REQ3	RTREN3	TX3PF	RI<1:0>	TXEN2	TX ABAT2	TX LARB2	TX ERR2	TX REQ2	RTREN2	TX2PF	રા<1:0>	0000
C1TR45CO N	0434	TXEN5	TX ABT5	TX LARB5	TX ERR5	TX REQ5	RTREN5	TX5PF	RI<1:0>	TXEN4	TX ABAT4	TX LARB4	TX ERR4	TX REQ4	RTREN4	TX4PF	રા<1:0>	0000
C1TR67CO N	0436	TXEN7	TX ABT7	TX LARB7	TX ERR7	TX REQ7	RTREN7	TX7PF	રા<1:0>	TXEN6	TX ABAT6	TX LARB6	TX ERR6	TX REQ6	RTREN6	TX6PF	२।<1:0>	XXXX
C1RXD	0440		Recieved Data Word xxxx								xxxx							
C1TXD	0442		Transmit Data Word xxxx															

TABLE 4-19: ECAN1 REGISTER MAP WHEN C1CTRL1.WIN = 0 FOR PIC24HJXXXGP506A/510A/610A DEVICES ONLY

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal for PinHigh devices.

TABLE 4-20: ECAN1 REGISTER MAP WHEN C1CTRL1.WIN = 1 FOR PIC24HJXXXGP506A/510A/610A DEVICES ONLY

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
	0400- 041E								See definit	ition when WIN = x								
C1BUFPNT1	0420		F3BF	°<3:0>			F2BF	P<3:0>			F1BP	<3:0>		F0BP<3:0>				
C1BUFPNT2	0422		F7BP<3:0> F6BP<3:0>					F5BP<3:0>				F4BP<3:0>				0000		
C1BUFPNT3	0424		F11BI	P<3:0>			F10B	P<3:0>			F9BP	<3:0>			F8BP	<3:0>		0000
C1BUFPNT4	0426		F15BP<3:0> F14BP<3:0>					F13BP<3:0> F12BP<3:0>					0000					
C1RXM0SID	0430				SID<	10:3>					SID<2:0>		_	MIDE	—	EID<1	7:16>	xxxx
C1RXM0EID	0432		EID<15:8> EID<7:0>					xxxx										
C1RXM1SID	0434		SID<10:3>					SID<2:0>		_	MIDE	_	EID<1	7:16>	xxxx			
C1RXM1EID	0436				EID<	15:8>							EID<	7:0>				xxxx
C1RXM2SID	0438		SID<10:3> SID<2:0> —				_	MIDE	_	EID<1	7:16>	xxxx						
C1RXM2EID	043A				EID<	15:8>							EID<	7:0>				xxxx
C1RXF0SID	0440		SID<10:3> SID<2:0> —		SID<2:0> — EXIDE — EID<17:				7:16>	xxxx								
C1RXF0EID	0442	EID<15:8>							EID<	7:0>				xxxx				
C1RXF1SID	0444	SID<10:3> SID<2:0> — EXIDE					EXIDE	_	EID<1	7:16>	xxxx							

© 2009-2012 Microchip Technology Inc.

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal for PinHigh devices.

7.0 INTERRUPT CONTROLLER

- **Note 1:** This data sheet summarizes the features of the PIC24HJXXXGPX06A/X08A/X10A family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 6. "Interrupts" (DS70184) of the "dsPIC33F/PIC24H Familv Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The PIC24HJXXXGPX06A/X08A/X10A interrupt controller reduces the numerous peripheral interrupt request signals to a single interrupt request signal to the PIC24HJXXXGPX06A/X08A/X10A CPU. It has the following features:

- · Up to 8 processor exceptions and software traps
- 7 user-selectable priority levels
- Interrupt Vector Table (IVT) with up to 118 vectors
- A unique vector for each interrupt or exception source
- · Fixed priority within a specified user priority level
- Alternate Interrupt Vector Table (AIVT) for debug support
- Fixed interrupt entry and return latencies

7.1 Interrupt Vector Table

The Interrupt Vector Table (IVT) is shown in Figure 7-1. The IVT resides in program memory, starting at location 000004h. The IVT contains 126 vectors consisting of 8 nonmaskable trap vectors plus up to 118 sources of interrupt. In general, each interrupt source has its own vector. Each interrupt vector contains a 24-bit wide address. The value programmed into each interrupt vector location is the starting address of the associated Interrupt Service Routine (ISR).

Interrupt vectors are prioritized in terms of their natural priority; this priority is linked to their position in the vector table. All other things being equal, lower addresses have a higher natural priority. For example, the interrupt associated with vector 0 will take priority over interrupts at any other vector address.

PIC24HJXXXGPX06A/X08A/X10A devices implement up to 61 unique interrupts and 5 nonmaskable traps. These are summarized in Table 7-1 and Table 7-2.

7.1.1 ALTERNATE VECTOR TABLE

The Alternate Interrupt Vector Table (AIVT) is located after the IVT, as shown in Figure 7-1. Access to the AIVT is provided by the ALTIVT control bit (INTCON2<15>). If the ALTIVT bit is set, all interrupt and exception processes use the alternate vectors instead of the default vectors. The alternate vectors are organized in the same manner as the default vectors.

The AIVT supports debugging by providing a means to switch between an application and a support environment without requiring the interrupt vectors to be reprogrammed. This feature also enables switching between applications for evaluation of different software algorithms at run time. If the AIVT is not needed, the AIVT should be programmed with the same addresses used in the IVT.

7.2 Reset Sequence

A device Reset is not a true exception because the interrupt controller is not involved in the Reset process. The PIC24HJXXXGPX06A/X08A/X10A device clears its registers in response to a Reset which forces the PC to zero. The digital signal controller then begins program execution at location 0x000000. The user programs a GOTO instruction at the Reset address which redirects program execution to the appropriate start-up routine.

Note: Any unimplemented or unused vector locations in the IVT and AIVT should be programmed with the address of a default interrupt handler routine that contains a RESET instruction.

REGISTER 7-1: SR: CPU STATUS REGISTER⁽¹⁾

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	DC
bit 15							bit 8

R/W-0 ⁽³⁾	R/W-0 ⁽³⁾	R/W-0 ⁽³⁾	R-0	R/W-0	R/W-0	R/W-0	R/W-0
IPL2 ⁽²⁾	IPL1 ⁽²⁾	IPL0 ⁽²⁾	RA	Ν	OV	Z	С
bit 7							bit 0

Legend:		
C = Clear only bit	R = Readable bit	U = Unimplemented bit, read as '0'
S = Set only bit	W = Writable bit	-n = Value at POR
'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 IPL<2:0>: CPU Interrupt Priority Level Status bits⁽²⁾

111 = CPU Interrupt Priority Level is 7 (15), user interrupts disabled

- 110 = CPU Interrupt Priority Level is 6 (14)
- 101 = CPU Interrupt Priority Level is 5 (13) 100 = CPU Interrupt Priority Level is 4 (12)
- 011 = CPU Interrupt Priority Level is 3 (11)
- 010 = CPU Interrupt Priority Level is 2 (10)
- 001 = CPU Interrupt Priority Level is 1 (9)
- 000 = CPU Interrupt Priority Level is 0 (8)
- **Note 1:** For complete register details, see Register 3-1.
 - 2: The IPL<2:0> bits are concatenated with the IPL<3> bit (CORCON<3>) to form the CPU Interrupt Priority Level. The value in parentheses indicates the IPL if IPL<3> = 1. User interrupts are disabled when IPL<3> = 1.
 - **3:** The IPL<2:0> Status bits are read-only when NSTDIS (INTCON1<15>) = 1.

REGISTER 7-2: CORCON: CORE CONTROL REGISTER⁽¹⁾

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
		_	_	_		_	
bit 15							bit 8
U-0	U-0	U-0	U-0	R/C-0	R/W-0	U-0	U-0
		—	—	IPL3 ⁽²⁾	PSV	—	
bit 7							bit 0
Legend:		C = Clear only	/ bit				
R = Readable b	oit	W = Writable	bit	-n = Value at	POR	'1' = Bit is set	
0' = Bit is clear	ed	ʻx = Bit is unki	nown	U = Unimpler	nented bit, read	as '0'	
bit 3	IPL3: CPU Int 1 = CPU inter 0 = CPU inter	terrupt Priority rupt priority lev rupt priority lev	Level Status b rel is greater th rel is 7 or less	_{it 3} (2) nan 7			

Note 1: For complete register details, see Register 3-2.

2: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.

REGISTER 7-3: INTCON1: INTERRUPT CONTROL REGISTER 1

R/W-0	U-0						
NSTDIS	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
—	DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFAIL	—
bit 7							bit 0

Legend:								
R = Readable	bit	W = Writable bit	U = Unimplemented bit,	read as '0'				
-n = Value at F	POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown				
bit 15	NSTDIS:	nterrupt Nesting Disable bit	t					
	1 = Interru	pt nesting is disabled						
	0 = Interru	ipt nesting is enabled						
bit 14-7	14-7 Unimplemented: Read as '0'							
bit 6	bit 6 DIV0ERR: Arithmetic Error Status bit							
1 = Math error trap was caused by a divide by zero								
bit 5	DMACER	R: DMA Controller Error Sta	atus bit					
	1 = DMA controller error trap has occurred							
	0 = DMA c	controller error trap has not	occurred					
bit 4	MATHERF	R: Arithmetic Error Status bi	t					
	1 = Math e	error trap has occurred						
	0 = Math e	error trap has not occurred						
bit 3	ADDRER	R: Address Error Trap Statu	is bit					
	1 = Addres	ss error trap has occurred	a d					
1.11.0		ss error trap has not occurre	ea					
bit 2	SIKERR:	Stack Error Trap Status bit						
	$\perp = Stack$	error trap has occurred						
hit 1		Chor trap has not occurred	tue hit					
DIL		tor failure trap has occurred	d					
	1 = Oscillar0 = Oscillar	ator failure trap has occurre	urred					
bit 0	Unimplem	nented: Read as '0'						
	-							

REGISTER 7-13: IEC3: INTERRUPT ENABLE CONTROL REGISTER 3

U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	R/W-0
_	—	DMA5IE	_	—		—	C2IE
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
C2RXIE	INT4IE	INT3IE	T9IE	T8IE	MI2C2IE	SI2C2IE	T7IE
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	nented bit, read	l as '0'	
-n = Value at I	POR	'1' = Bit is set		0' = Bit is cle	ared	x = Bit is unkn	iown
bit 15 11	Unimplomen	ted. Dood oo (<u>,</u> ,				
DIL 10-14		A Channel 5 D	J ata Transfor (Complete Inter	unt Enable bit		
DIL 13	1 = Interrupt r						
	0 = Interrupt r	request not enabled	ibled				
bit 12-9	Unimplemen	ted: Read as ') '				
bit 8	C2IE: ECAN2	2 Event Interrup	t Enable bit				
	1 = Interrupt r	request enable	b				
	0 = Interrupt r	request not ena	bled				
bit 7	C2RXIE: ECA	AN2 Receive D	ata Ready Inte	errupt Enable I	bit		
	1 = Interrupt r	request enable	d 				
	0 = Interrupt r	request not ena					
bit 6	INT4IE: Exter	nal Interrupt 4	Enable bit				
	1 = Interrupt r	request enable	d Ibled				
bit 5	INT3IE: Exter	nal Interrunt 3	Enable hit				
bit 0	1 = Interrupt r	request enable					
	0 = Interrupt r	request not ena	ibled				
bit 4	T9IE: Timer9	Interrupt Enab	e bit				
	1 = Interrupt r	request enable	d				
	0 = Interrupt r	request not ena	bled				
bit 3	T8IE: Timer8	Interrupt Enab	e bit				
	1 = Interrupt r	request enable	d blod				
h it 0				abla bit			
DIL Z	1 = Interrupt r	2 Master Even	is interrupt Er ⊣	lable bit			
	0 = Interrupt r	request enabled	ibled				
bit 1	SI2C2IE: 12C	2 Slave Events	Interrupt Ena	ıble bit			
	1 = Interrupt r	request enable	d				
	0 = Interrupt r	request not ena	bled				
bit 0	T7IE: Timer7	Interrupt Enab	e bit				
	1 = Interrupt r	request enable	d .				
	0 = Interrupt r	request not ena	Ibled				

REGISTER 7-27: IPC12: INTERRUPT PRIORITY CONTROL REGISTER 12

	- • • • •	D	D 4 • / •		B	D/11/2	D 444 A					
U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0					
		T8IP<2:0>		—		MI2C2IP<2:0>						
bit 15							bit 8					
							ī					
U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0					
		SI2C2IP<2:0>		—		T7IP<2:0>						
bit 7							bit 0					
Legend:												
R = Readable	e bit	W = Writable	bit	U = Unimplei	mented bit, rea	ad as '0'						
-n = Value at	POR	'1' = Bit is set		'0' = Bit is cle	Bit is cleared x = Bit is unknown							
bit 15	Unimplem	ented: Read as ')'									
bit 14-12	T8IP<2:0>:	Timer8 Interrupt	Priority bits									
	111 = Inter	rupt is priority 7 (I	nighest priorif	ty interrupt)								
	•											
	•											
	• 001 = Inter	runt is priority 1										
	000 = Inter	rupt source is dis	abled									
bit 11	Unimplem	ented: Read as ')'									
bit 10-8	MI2C2IP<2	MI2C2IP<2:0>: I2C2 Master Events Interrupt Priority bits										
	111 = Inter	rupt is priority 7 (I	nighest priorit	ty interrupt)								
	•		0	, i ,								
	•											
	• 001 - Inter	rupt is priority 1										
	000 = Inter	rupt source is dis	abled									
bit 7	Unimplem	ented: Read as ')'									
bit 6-4	SI2C2IP<2	:0>: I2C2 Slave E	vents Interru	ot Priority bits								
	111 = Inter	rupt is priority 7 (I	niahest priorit	v interrupt)								
	•		J	· · · · · · · · · · · · · · · · · · ·								
	•											
	•	rupt is priority 1										
	001 = Inter	rupt is priority i rupt source is dis	abled									
bit 3	Unimplem	ented: Read as '(מגייט מ ז'									
bit 2-0		Timer7 Interrunt	Priority hits									
Dit 2 0	111 = Inter	runt is priority 7 (l	niahest priorit	v interrunt)								
	•		ingricot priori									
	•											
	•	munt in priority 4										
	001 = Inter	rupt is priority 1	abled									

REGISTER 8-2: DMAxREQ: DMA CHANNEL x IRQ SELECT REGISTER

R/W-0	U-0						
FORCE ⁽¹⁾	—	—	-	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	IRQSEL6 ⁽²⁾	IRQSEL5(2)	IRQSEL4(2)	IRQSEL3(2)	IRQSEL2 ⁽²⁾	IRQSEL1(2)	IRQSEL0(2)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **FORCE:** Force DMA Transfer bit⁽¹⁾

1 = Force a single DMA transfer (Manual mode)

0 = Automatic DMA transfer initiation by DMA request

bit 14-7 Unimplemented: Read as '0'

- bit 6-0 IRQSEL<6:0>: DMA Peripheral IRQ Number Select bits⁽²⁾ 0000000-1111111 = DMAIRQ0-DMAIRQ127 selected to be Channel DMAREQ
- **Note 1:** The FORCE bit cannot be cleared by the user. The FORCE bit is cleared by hardware when the forced DMA transfer is complete.

2: Please see Table 8-1 for a complete listing of IRQ numbers for all interrupt sources.

NOTES:

16.3 SPI Control Registers

REGISTER 16-1: SPIxSTAT: SPIx STATUS AND CONTROL REGISTER

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0			
SPIEN	—	SPISIDL	—		—		—			
bit 15	bit 15 bit 8									
U-0	R/C-0	U-0	U-0	U-0	U-0	R-0	R-0			
—	SPIROV	—	—	_	—	SPITBF	SPIRBF			
bit 7							bit 0			

Legend:	C = Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15	SPIEN: SPIx Enable bit
	1 = Enables module and configures SCKx, SDOx, SDIx and \overline{SSx} as serial port pins 0 = Disables module
bit 14	Unimplemented: Read as '0'
bit 13	SPISIDL: Stop in Idle Mode bit
	1 = Discontinue module operation when device enters Idle mode0 = Continue module operation in Idle mode
bit 12-7	Unimplemented: Read as '0'
bit 6	 SPIROV: Receive Overflow Flag bit 1 = A new byte/word is completely received and discarded. The user software has not read the previous data in the SPIxBUF register 0 = No overflow has occurred
bit 5-2	Unimplemented: Read as '0'
bit 1	SPITBF: SPIx Transmit Buffer Full Status bit
	 1 = Transmit not yet started, SPIxTXB is full 0 = Transmit started, SPIxTXB is empty Automatically set in hardware when CPU writes SPIxBUF location, loading SPIxTXB. Automatically cleared in hardware when SPIx module transfers data from SPIxTXB to SPIxSR.
bit 0	SPIRBF: SPIx Receive Buffer Full Status bit
	 1 = Receive complete, SPIxRXB is full 0 = Receive is not complete, SPIxRXB is empty Automatically set in hardware when SPIx transfers data from SPIxSR to SPIxRXB. Automatically cleared in hardware when core reads SPIxBUF location, reading SPIxRXB.

REGISTER 19-26: CiTRmnCON: ECAN[™] MODULE TX/RX BUFFER m CONTROL REGISTER (m = 0.2.4.6: n = 1.3.5.7)

	(11 – 0,2	2, 4 ,0, 11 = 1,3,	5,1)				
R/W-0	R-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
TXENn	TXABTn	TXLARBn	TXERRn	TXREQn	RTRENn	TXnPF	RI<1:0>
bit 15							bit 8

R/W-0	R-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
TXENm	TXABTm ⁽¹⁾	TXLARBm ⁽¹⁾	TXERRm ⁽¹⁾	TXREQm	RTRENm	TXmPF	RI<1:0>
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8	See Definition for Bits 7-0, Controls Buffer n
bit 7	TXENm: TX/RX Buffer Selection bit
	 1 = Buffer TRBn is a transmit buffer 0 = Buffer TRBn is a receive buffer
bit 6	TXABTm: Message Aborted bit ⁽¹⁾
	1 = Message was aborted0 = Message completed transmission successfully
bit 5	TXLARBm: Message Lost Arbitration bit ⁽¹⁾
	 1 = Message lost arbitration while being sent 0 = Message did not lose arbitration while being sent
bit 4	TXERRm: Error Detected During Transmission bit ⁽¹⁾
	 1 = A bus error occurred while the message was being sent 0 = A bus error did not occur while the message was being sent
bit 3	TXREQm: Message Send Request bit
	Setting this bit to '1' requests sending a message. The bit will automatically clear when the message is successfully sent. Clearing the bit to '0' while set will request a message abort.
bit 2	RTRENm: Auto-Remote Transmit Enable bit
	 1 = When a remote transmit is received, TXREQ will be set 0 = When a remote transmit is received, TXREQ will be unaffected
bit 1-0	TXmPRI<1:0>: Message Transmission Priority bits
	 11 = Highest message priority 10 = High intermediate message priority 01 = Low intermediate message priority 00 = Lowest message priority

Note 1: This bit is cleared when TXREQ is set.





21.0 SPECIAL FEATURES

- **Note 1:** This data sheet summarizes the features of the PIC24HJXXXGPX06A/X08A/X10A families of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section "CodeGuard™ Security" 23. (DS70199), Section 24. "Programming and Diagnostics" (DS70207), and Section 25. "Device Configuration" (DS70194) in the "dsPIC33F/PIC24H Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

PIC24HJXXXGPX06A/X08A/X10A devices include several features intended to maximize application flexibility and reliability, and minimize cost through elimination of external components. These are:

- Flexible Configuration
- Watchdog Timer (WDT)
- Code Protection and CodeGuard[™] Security
- JTAG Boundary Scan Interface
- In-Circuit Serial Programming™ (ICSP™) programming capability
- In-Circuit Emulation

Address Name Bit 7 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0 Bit 6 Bit 5 RBS<1:0> BSS<2:0> BWRP 0xF80000 FBS SSS<2:0> 0xF80002 FSS RSS<1:0> SWRP 0xF80004 FGS GSS<1:0> GWRP 0xF80006 FOSCSEL Reserved⁽²⁾ FNOSC<2:0> **IESO** 0xF80008 FOSC FCKSM<1:0> OSCIOFNC POSCMD<1:0> ____ PLLKEN(3) WDTPOST<3:0> 0xF8000A FWDT FWDTEN WINDIS **WDTPRE** Reserved⁽⁴⁾ 0xF8000C FPOR FPWRT<2:0> ____ Reserved⁽¹⁾ 0xF8000E FICD **JTAGEN** ICS<1:0> 0xF80010 FUID0 User Unit ID Byte 0 0xF80012 FUID1 User Unit ID Byte 1 0xF80014 FUID2 User Unit ID Byte 2 0xF80016 FUID3 User Unit ID Byte 3

TABLE 21-1: DEVICE CONFIGURATION REGISTER MAP

Legend: — = unimplemented bits, read as '0'.

Note 1: These bits are reserved for use by development tools and must be programmed as '1'.

- 2: When read, this bit returns the current programmed value.
- **3:** This bit is unimplemented on PIC24HJ64GPX06A/X08A/X10A and PIC24HJ128GPX06A/X08A/X10A devices and reads as '0'.
- 4: These bits are reserved and always read as '1'.

21.1 Configuration Bits

PIC24HJXXXGPX06A/X08A/X10A devices provide nonvolatile memory implementation for device configuration bits. Refer to **Section 25. "Device Configuration"** (DS70194) of the *"dsPIC33F/PIC24H Family Reference Manual"*, for more information on this implementation.

The Configuration bits can be programmed (read as '0'), or left unprogrammed (read as '1'), to select various device configurations. These bits are mapped starting at program memory location 0xF80000.

The device Configuration register map is shown in Table 21-1.

The individual Configuration bit descriptions for the Configuration registers are shown in Table 21-2.

Note that address 0xF80000 is beyond the user program memory space. In fact, it belongs to the configuration memory space (0x800000-0xFFFFFF), which can only be accessed using table reads and table writes.

Base Instr #	Assembly Mnemonic		Assembly Syntax	Description	# of Words	# of Cycles	Status Flags Affected
1	ADD	ADD	f	f = f + WREG	1	1	C,DC,N,OV,Z
		ADD f,WREG		WREG = f + WREG	1	1	C,DC,N,OV,Z
		ADD	#lit10,Wn	Wd = lit10 + Wd	1	1	C,DC,N,OV,Z
		ADD	Wb,Ws,Wd	Wd = Wb + Ws	1	1	C,DC,N,OV,Z
		ADD	Wb,#lit5,Wd	Wd = Wb + lit5	1	1	C,DC,N,OV,Z
2	ADDC	ADDC	f	f = f + WREG + (C)	1	1	C,DC,N,OV,Z
		ADDC	f,WREG	I = I + WKEG + (C) EG WREG = f + WREG + (C)			
		ADDC	#lit10,Wn	Wd = Iit10 + Wd + (C)	1	1	C,DC,N,OV,Z
		ADDC	Wb,Ws,Wd	Wd = Wb + Ws + (C)	1	1	C,DC,N,OV,Z
		ADDC	Wb,#lit5,Wd	Wd = Wb + lit5 + (C)	1	1	C,DC,N,OV,Z
3	AND	AND	f	f = f .AND. WREG	1	1	N,Z
		AND	f,WREG	WREG = f .AND. WREG	1	1	N,Z
		AND	#lit10,Wn	Wd = lit10 .AND. Wd	1	1	N,Z
		AND	Wb,Ws,Wd	Wd = Wb .AND. Ws	1	1	N,Z
		AND	Wb,#lit5,Wd	Wd = Wb .AND. lit5	1	1	N,Z
4	ASR	ASR	f	f = Arithmetic Right Shift f	1	1	C,N,OV,Z
		ASR	f,WREG	WREG = Arithmetic Right Shift f	1	1	C,N,OV,Z
		ASR	Ws,Wd	Wd = Arithmetic Right Shift Ws	1	1	C,N,OV,Z
		ASR	Wb,Wns,Wnd	Wnd = Arithmetic Right Shift Wb by Wns	1	1	N,Z
		ASR	Wb,#lit5,Wnd	Wnd = Arithmetic Right Shift Wb by lit5	1	1	N,Z
5	BCLR	BCLR	f,#bit4	Bit Clear f	1	1	None
		BCLR	Ws,#bit4	Bit Clear Ws	1	1	None
6	BRA	BRA	C,Expr	Branch if Carry	1	1 (2)	None
		BRA	GE,Expr	Branch if greater than or equal	1	1 (2)	None
		BRA	GEU,Expr	Branch if unsigned greater than or equal	1	1 (2)	None
		BRA	GT,Expr	Branch if greater than	1	1 (2)	None
		BRA	GTU,Expr	Branch if unsigned greater than	1	1 (2)	None
		BRA	LE,Expr	Branch if less than or equal	1	1 (2)	None
		BRA	LEU,Expr	Branch if unsigned less than or equal	1	1 (2)	None
		BRA	LT,Expr	Branch if less than	1	1 (2)	None
		BRA	LTU,Expr	Branch if unsigned less than	1	1 (2)	None
		BRA	N,Expr	Branch if Negative	1	1 (2)	None
		BRA	NC,Expr	Branch if Not Carry	1	1 (2)	None
		BRA	NN,Expr	Branch if Not Negative	1	1 (2)	None
		BRA	NZ,Expr	Branch if Not Zero	1	1 (2)	None
		BRA	Expr	Branch Unconditionally	1	2	None
		BRA	Z,Expr	Branch if Zero	1	1 (2)	None
		BRA	Wn	Computed Branch	1	2	None
7	BSET	BSET	f,#bit4	Bit Set f	1	1	None
		BSET	Ws,#bit4	Bit Set Ws	1	1	None
8	BSW	BSW.C	Ws,Wb	Write C bit to Ws <wb></wb>	1	1	None
		BSW.Z	Ws,Wb	Write Z bit to Ws <wb></wb>	1	1	None
9	BTG	BTG	f,#bit4	Bit Toggle f	1	1	None
		BTG	Ws,#bit4	Bit Toggle Ws	1	1	None
10	BTSC	BTSC	f,#bit4	Bit Test f, Skip if Clear	1	1 (2 or 3)	None
		BTSC	Ws,#bit4	Bit Test Ws, Skip if Clear	1	1 (2 or 3)	None
11	BTSS	BTSS	f,#bit4	Bit Test f, Skip if Set	1	1 (2 or 3)	None
		BTSS	Ws,#bit4	Bit Test Ws, Skip if Set	1	1 (2 or 3)	None

TABLE 22-2: INSTRUCTION SET OVERVIEW

© 2009-2012 Microchip Technology Inc.



FIGURE 24-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING CHARACTERISTICS

TABLE 24-21: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER TIMING REQUIREMENTS

AC CHARACTERISTICS			$\begin{array}{llllllllllllllllllllllllllllllllllll$					
Param No.	Symbol	Characteristic ⁽¹⁾	Min	Тур ⁽²⁾	Мах	Units	Conditions	
SY10	TMCL	MCLR Pulse Width (low)	2	—	_	μS	-40°C to +85°C	
SY11	Tpwrt	Power-up Timer Period	_	2 4 16 32 64 128	_	ms	-40°C to +85°C User programmable	
SY12	TPOR	Power-on Reset Delay	3	10	30	μS	-40°C to +85°C	
SY13	Tioz	I/O High-Impedance from MCLR Low or Watchdog Timer Reset	0.68	0.72	1.2	μS	_	
SY20	Twdt1	Watchdog Timer Time-out Period	_	_	_	_	See Section 21.4 "Watchdog Timer (WDT)" and LPRC specification F21 (Table 24-19)	
SY30	Tost	Oscillator Start-up Timer Period	_	1024 Tosc	_	_	Tosc = OSC1 period	
SY35	TFSCM	Fail-Safe Clock Monitor Delay	—	500	900	μS	-40°C to +85°C	

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated.

FIGURE 24-19: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (SLAVE MODE)









25.1 High Temperature DC Characteristics

TABLE 25-1: OPERATING MIPS VS. VOLTAGE

Charactoristic	VDD Range	Temperature Range	Max MIPS		
Characteristic	(in Volts)	(in °C)	PIC24HJXXXGPX06A/X08A/X10A		
HDC5	VBOR to 3.6V ⁽¹⁾	-40°C to +150°C	20		

Note 1: Device is functional at VBORMIN < VDD < VDDMIN. Analog modules such as the ADC will have degraded performance. Device functionality is tested but not characterized. Refer to parameter BO10 in Table 24-11 for the minimum and maximum BOR values.

TABLE 25-2: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min	Тур	Max	Unit		
High Temperature Devices							
Operating Junction Temperature Range	TJ	-40	—	+155	°C		
Operating Ambient Temperature Range	TA	-40	—	+150	°C		
Power Dissipation: Internal chip power dissipation: $PINT = VDD x (IDD - \Sigma IOH)$ I/O Pin Power Dissipation: $I/O = \Sigma ({VDD - VOH} x IOH) + \Sigma (VOL x IOL)$	PD	PINT + PI/O			W		
Maximum Allowed Power Dissipation	PDMAX	(ТЈ - ТА)/ӨЈА			W		

TABLE 25-3: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS

DC CHARACTERISTICS			$\begin{tabular}{lllllllllllllllllllllllllllllllllll$				
Parameter No.	Symbol	Characteristic	Min	Тур	Мах	Units	Conditions
Operating Voltage							
HDC10	Supply Voltage						
	VDD		3.0	3.3	3.6	V	-40°C to +150°C

TABLE 25-4: DC CHARACTERISTICS: POWER-DOWN CURRENT (IPD)

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +150^{\circ}C$ for High Temperature			
Parameter No.	Typical	Мах	Units	Conditions		
Power-Down Current (IPD)						
HDC60e	250	2000	μA	+150°C	3.3V	Base Power-Down Current ^(1,3)
Note 1. Base IPD is measured with all peripherals and clocks shut down. All I/Os are configured as inputs and						

Note 1: Base IPD is measured with all peripherals and clocks shut down. All I/Os are configured as inputs and pulled to Vss. WDT, etc., are all switched off, and VREGS (RCON<8>) = 1.

2: The ∆ current is the additional current consumed when the module is enabled. This current should be added to the base IPD current.

3: These currents are measured on the device containing the most memory in this family.

4: These parameters are characterized, but are not tested in manufacturing.