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Details

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	40 MIPs
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	85
Program Memory Size	64KB (22K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 32x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24hj64gp510at-i-pt

TABLE 4-17: DMA REGISTER MAP (CONTINUED)

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets	
DMA5PAD	03C4	PAD<15:0>																0000	
DMA5CNT	03C6	—	—	—	—	—	—	CNT<9:0>										0000	
DMA6CON	03C8	CHEN	SIZE	DIR	HALF	NULLW	—	—	—	—	—	AMODE<1:0>		—	—	MODE<1:0>		0000	
DMA6REQ	03CA	FORCE	—	—	—	—	—	—	—	—	IRQSEL<6:0>								0000
DMA6STA	03CC	STA<15:0>																0000	
DMA6STB	03CE	STB<15:0>																0000	
DMA6PAD	03D0	PAD<15:0>																0000	
DMA6CNT	03D2	—	—	—	—	—	—	CNT<9:0>										0000	
DMA7CON	03D4	CHEN	SIZE	DIR	HALF	NULLW	—	—	—	—	—	AMODE<1:0>		—	—	MODE<1:0>		0000	
DMA7REQ	03D6	FORCE	—	—	—	—	—	—	—	—	IRQSEL<6:0>								0000
DMA7STA	03D8	STA<15:0>																0000	
DMA7STB	03DA	STB<15:0>																0000	
DMA7PAD	03DC	PAD<15:0>																0000	
DMA7CNT	03DE	—	—	—	—	—	—	CNT<9:0>										0000	
DMACS0	03E0	PWCOL7	PWCOL6	PWCOL5	PWCOL4	PWCOL3	PWCOL2	PWCOL1	PWCOL0	XWCOL7	XWCOL6	XWCOL5	XWCOL4	XWCOL3	XWCOL2	XWCOL1	XWCOL0	0000	
DMACS1	03E2	—	—	—	—	LSTCH<3:0>				PPST7	PPST6	PPST5	PPST4	PPST3	PPST2	PPST1	PPST0	0000	
DSADR	03E4	DSADR<15:0>																0000	

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal for PinHigh devices.

TABLE 4-18: ECAN1 REGISTER MAP WHEN C1CTRL1.WIN = 0 OR 1 FOR PIC24HJXXXGP506A/510A/610A DEVICES ONLY

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
C1CTRL1	0400	—	—	CSIDL	ABAT	—	REQOP<2:0>			OPMODE<2:0>			—	CANCAP	—	—	WIN	0480
C1CTRL2	0402	—	—	—	—	—	—	—	—	—	—	—	DNCNT<4:0>					0000
C1VEC	0404	—	—	—	FILHIT<4:0>					—	ICODE<6:0>						0000	
C1FCTRL	0406	DMABS<2:0>			—	—	—	—	—	—	—	—	FSA<4:0>					0000
C1FIFO	0408	—	—	FBP<5:0>						—	—	FNRB<5:0>					0000	
C1INTF	040A	—	—	TXBO	TXBP	RXBP	TXWAR	RXWAR	EWARN	IVRIF	WAKIF	ERRIF	—	FIFOIF	RBOVIF	RBIF	TBIF	0000
C1INTE	040C	—	—	—	—	—	—	—	—	IVRIE	WAKIE	ERRIE	—	FIFOIE	RBOVIE	RBIE	TBIE	0000
C1EC	040E	TERRCNT<7:0>								RERRCNT<7:0>								0000
C1CFG1	0410	—	—	—	—	—	—	—	—	SJW<1:0>		BRP<5:0>						0000
C1CFG2	0412	—	WAKFIL	—	—	—	SEG2PH<2:0>			SEG2PHTS	SAM	SEG1PH<2:0>			PRSEG<2:0>			0000
C1FEN1	0414	FLTEN15	FLTEN14	FLTEN13	FLTEN12	FLTEN11	FLTEN10	FLTEN9	FLTEN8	FLTEN7	FLTEN6	FLTEN5	FLTEN4	FLTEN3	FLTEN2	FLTEN1	FLTEN0	FFFF
C1FMSKSEL1	0418	F7MSK<1:0>		F6MSK<1:0>		F5MSK<1:0>		F4MSK<1:0>		F3MSK<1:0>		F2MSK<1:0>		F1MSK<1:0>		F0MSK<1:0>		0000
C1FMSKSEL2	041A	F15MSK<1:0>		F14MSK<1:0>		F13MSK<1:0>		F12MSK<1:0>		F11MSK<1:0>		F10MSK<1:0>		F9MSK<1:0>		F8MSK<1:0>		0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal for PinHigh devices.

PIC24HJXXXGPX06A/X08A/X10A

6.0 RESET

Note 1: This data sheet summarizes the features of the PIC24HJXXXGPX06A/X08A/X10A family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 8. “Reset”** (DS70192) of the “dsPIC33F/PIC24H Family Reference Manual”, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The Reset module combines all Reset sources and controls the device Master Reset Signal, $\overline{\text{SYSRST}}$. The following is a list of device Reset sources:

- POR: Power-on Reset
- BOR: Brown-out Reset
- MCLR: Master Clear Pin Reset
- SWR: RESET Instruction
- WDT: Watchdog Timer Reset
- TRAPR: Trap Conflict Reset
- IOPUWR: Illegal Opcode and Uninitialized W Register Reset

A simplified block diagram of the Reset module is shown in Figure 6-1.

Any active source of Reset will make the $\overline{\text{SYSRST}}$ signal active. Many registers associated with the CPU and peripherals are forced to a known Reset state. Most registers are unaffected by a Reset; their status is unknown on POR and unchanged by all other Resets.

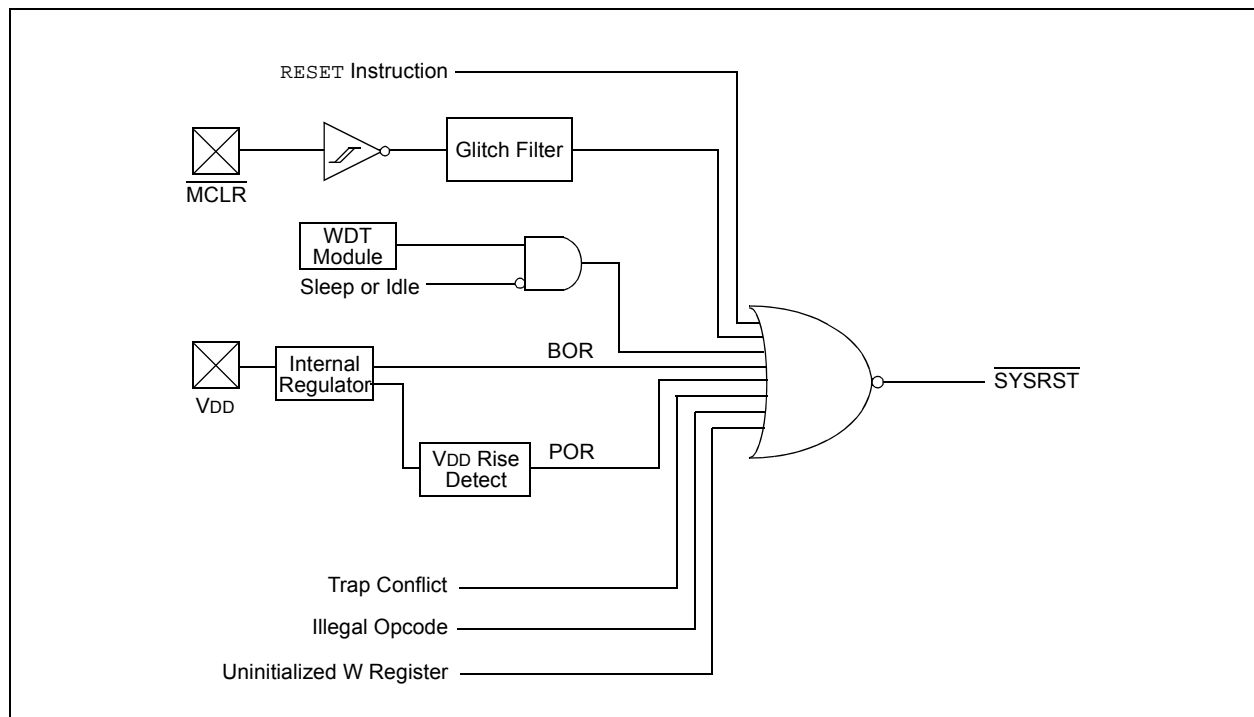
Note: Refer to the specific peripheral or CPU section of this data sheet for register Reset states.

All types of device Reset will set a corresponding status bit in the RCON register to indicate the type of Reset (see Register 6-1). A POR will clear all bits, except for the POR bit ($\text{RCON}<0>$), that are set. The user can set or clear any bit at any time during code execution. The RCON bits only serve as status bits. Setting a particular Reset status bit in software does not cause a device Reset to occur.

The RCON register also has other bits associated with the Watchdog Timer and device power-saving states. The function of these bits is discussed in other sections of this manual.

Note: The status bits in the RCON register should be cleared after they are read so that the next RCON register value after a device Reset will be meaningful.

FIGURE 6-1: RESET SYSTEM BLOCK DIAGRAM



PIC24HJXXXGPX06A/X08A/X10A

REGISTER 7-4: INTCON2: INTERRUPT CONTROL REGISTER 2

R/W-0	R-0	U-0	U-0	U-0	U-0	U-0	U-0
ALTIVT	DISI	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **ALTIVT:** Enable Alternate Interrupt Vector Table bit

1 = Use alternate vector table

0 = Use standard (default) vector table

bit 14 **DISI:** DISI Instruction Status bit

1 = DISI instruction is active

0 = DISI instruction is not active

bit 13-5 **Unimplemented:** Read as '0'

bit 4 **INT4EP:** External Interrupt 4 Edge Detect Polarity Select bit

1 = Interrupt on negative edge

0 = Interrupt on positive edge

bit 3 **INT3EP:** External Interrupt 3 Edge Detect Polarity Select bit

1 = Interrupt on negative edge

0 = Interrupt on positive edge

bit 2 **INT2EP:** External Interrupt 2 Edge Detect Polarity Select bit

1 = Interrupt on negative edge

0 = Interrupt on positive edge

bit 1 **INT1EP:** External Interrupt 1 Edge Detect Polarity Select bit

1 = Interrupt on negative edge

0 = Interrupt on positive edge

bit 0 **INT0EP:** External Interrupt 0 Edge Detect Polarity Select bit

1 = Interrupt on negative edge

0 = Interrupt on positive edge

PIC24HJXXXGPX06A/X08A/X10A

NOTES:

PIC24HJXXXGPX06A/X08A/X10A

REGISTER 9-1: OSCCON: OSCILLATOR CONTROL REGISTER^(1,3) (CONTINUED)

- bit 1 **LPOSCEN**: Secondary (LP) Oscillator Enable bit
 1 = Enable secondary oscillator
 0 = Disable secondary oscillator
- bit 0 **OSWEN**: Oscillator Switch Enable bit
 1 = Request oscillator switch to selection specified by NOSC<2:0> bits
 0 = Oscillator switch is complete

- Note 1:** Writes to this register require an unlock sequence. Refer to **Section 7. “Oscillator”** (DS70186) in the *dsPIC33F/PIC24H Family Reference Manual* for details.
- 2:** Direct clock switches between any primary oscillator mode with PLL and FRCPLL mode are not permitted. This applies to clock switches in either direction. In these instances, the application must switch to FRC mode as a transition clock source between the two PLL modes.
- 3:** This register is reset only on a Power-on Reset (POR).

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REGISTER 19-1: CiCTRL1: ECAN™ MODULE CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	r-0	R/W-1	R/W-0	R/W-0
—	—	CSIDL	ABAT	—	REQOP<2:0>		
bit 15						bit 8	

R-1	R-0	R-0	U-0	R/W-0	U-0	U-0	R/W-0
OPMODE<2:0>			—	CANCAP	—	—	WIN
bit 7							bit 0

Legend:	r = Bit is Reserved		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15-14 **Unimplemented:** Read as '0'
- bit 13 **CSIDL:** Stop in Idle Mode bit
1 = Discontinue module operation when device enters Idle mode
0 = Continue module operation in Idle mode
- bit 12 **ABAT:** Abort All Pending Transmissions bit
1 = Signal all transmit buffers to abort transmission
0 = Module will clear this bit when all transmissions are aborted
- bit 11 **Reserved:** Do not use
- bit 10-8 **REQOP<2:0>:** Request Operation Mode bits
111 = Set Listen All Messages mode
110 = Reserved – do not use
101 = Reserved – do not use
100 = Set Configuration mode
011 = Set Listen Only Mode
010 = Set Loopback mode
001 = Set Disable mode
000 = Set Normal Operation mode
- bit 7-5 **OPMODE<2:0>:** Operation Mode bits
111 = Module is in Listen All Messages mode
110 = Reserved
101 = Reserved
100 = Module is in Configuration mode
011 = Module is in Listen Only mode
010 = Module is in Loopback mode
001 = Module is in Disable mode
000 = Module is in Normal Operation mode
- bit 4 **Unimplemented:** Read as '0'
- bit 3 **CANCAP:** CAN Message Receive Timer Capture Event Enable bit
1 = Enable input capture based on CAN message receive
0 = Disable CAN capture
- bit 2-1 **Unimplemented:** Read as '0'
- bit 0 **WIN:** SFR Map Window Select bit
1 = Use filter window
0 = Use buffer window

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REGISTER 19-11: CiFEN1: ECAN™ MODULE ACCEPTANCE FILTER ENABLE REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
FLTEN15	FLTEN14	FLTEN13	FLTEN12	FLTEN11	FLTEN10	FLTEN9	FLTEN8
bit 15						bit 8	

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
FLTEN7	FLTEN6	FLTEN5	FLTEN4	FLTEN3	FLTEN2	FLTEN1	FLTEN0
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0

FLTENn: Enable Filter n (0-15) to Accept Messages bits

1 = Enable Filter n

0 = Disable Filter n

PIC24HJXXXGPX06A/X08A/X10A

REGISTER 19-12: CiBUPNT1: ECAN™ MODULE FILTER 0-3 BUFFER POINTER REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F3BP<3:0>				F2BP<3:0>			
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F1BP<3:0>				F0BP<3:0>			
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-12 **F3BP<3:0>**: RX Buffer Written when Filter 3 Hits bits

1111 = Filter hits received in RX FIFO buffer

1110 = Filter hits received in RX Buffer 14

•

•

•

0001 = Filter hits received in RX Buffer 1

0000 = Filter hits received in RX Buffer 0

bit 11-8 **F2BP<3:0>**: RX Buffer Written when Filter 2 Hits bits

1111 = Filter hits received in RX FIFO buffer

1110 = Filter hits received in RX Buffer 14

•

•

•

0001 = Filter hits received in RX Buffer 1

0000 = Filter hits received in RX Buffer 0

bit 7-4 **F1BP<3:0>**: RX Buffer Written when Filter 1 Hits bits

1111 = Filter hits received in RX FIFO buffer

1110 = Filter hits received in RX Buffer 14

•

•

•

0001 = Filter hits received in RX Buffer 1

0000 = Filter hits received in RX Buffer 0

bit 3-0 **F0BP<3:0>**: RX Buffer Written when Filter 0 Hits bits

1111 = Filter hits received in RX FIFO buffer

1110 = Filter hits received in RX Buffer 14

•

•

•

0001 = Filter hits received in RX Buffer 1

0000 = Filter hits received in RX Buffer 0

PIC24HJXXXGPX06A/X08A/X10A

REGISTER 19-18: CiFMSKSEL1: ECAN™ MODULE FILTER 7-0 MASK SELECTION REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F7MSK<1:0>		F6MSK<1:0>		F5MSK<1:0>		F4MSK<1:0>	
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F3MSK<1:0>		F2MSK<1:0>		F1MSK<1:0>		F0MSK<1:0>	
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15-14 **F7MSK<1:0>**: Mask Source for Filter 7 bit
11 = Reserved; do not use
10 = Acceptance Mask 2 registers contain mask
01 = Acceptance Mask 1 registers contain mask
00 = Acceptance Mask 0 registers contain mask
- bit 13-12 **F6MSK<1:0>**: Mask Source for Filter 6 bit
11 = Reserved; do not use
10 = Acceptance Mask 2 registers contain mask
01 = Acceptance Mask 1 registers contain mask
00 = Acceptance Mask 0 registers contain mask
- bit 11-10 **F5MSK<1:0>**: Mask Source for Filter 5 bit
11 = Reserved; do not use
10 = Acceptance Mask 2 registers contain mask
01 = Acceptance Mask 1 registers contain mask
00 = Acceptance Mask 0 registers contain mask
- bit 9-8 **F4MSK<1:0>**: Mask Source for Filter 4 bit
11 = Reserved; do not use
10 = Acceptance Mask 2 registers contain mask
01 = Acceptance Mask 1 registers contain mask
00 = Acceptance Mask 0 registers contain mask
- bit 7-6 **F3MSK<1:0>**: Mask Source for Filter 3 bit
11 = Reserved; do not use
10 = Acceptance Mask 2 registers contain mask
01 = Acceptance Mask 1 registers contain mask
00 = Acceptance Mask 0 registers contain mask
- bit 5-4 **F2MSK<1:0>**: Mask Source for Filter 2 bit
11 = Reserved; do not use
10 = Acceptance Mask 2 registers contain mask
01 = Acceptance Mask 1 registers contain mask
00 = Acceptance Mask 0 registers contain mask
- bit 3-2 **F1MSK<1:0>**: Mask Source for Filter 1 bit
11 = Reserved; do not use
10 = Acceptance Mask 2 registers contain mask
01 = Acceptance Mask 1 registers contain mask
00 = Acceptance Mask 0 registers contain mask
- bit 1-0 **F0MSK<1:0>**: Mask Source for Filter 0 bit
11 = Reserved; do not use
10 = Acceptance Mask 2 registers contain mask
01 = Acceptance Mask 1 registers contain mask
00 = Acceptance Mask 0 registers contain mask

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REGISTER 19-19: CifMSKSEL2: ECAN™ FILTER 15-8 MASK SELECTION REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F15MSK<1:0>		F14MSK<1:0>		F13MSK<1:0>		F12MSK<1:0>	
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F11MSK<1:0>		F10MSK<1:0>		F9MSK<1:0>		F8MSK<1:0>	
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15-14 **F15MSK<1:0>**: Mask Source for Filter 15 bit
11 = Reserved; do not use
10 = Acceptance Mask 2 registers contain mask
01 = Acceptance Mask 1 registers contain mask
00 = Acceptance Mask 0 registers contain mask
- bit 13-12 **F14MSK<1:0>**: Mask Source for Filter 14 bit
11 = Reserved; do not use
10 = Acceptance Mask 2 registers contain mask
01 = Acceptance Mask 1 registers contain mask
00 = Acceptance Mask 0 registers contain mask
- bit 11-10 **F13MSK<1:0>**: Mask Source for Filter 13 bit
11 = Reserved; do not use
10 = Acceptance Mask 2 registers contain mask
01 = Acceptance Mask 1 registers contain mask
00 = Acceptance Mask 0 registers contain mask
- bit 9-8 **F12MSK<1:0>**: Mask Source for Filter 12 bit
11 = Reserved; do not use
10 = Acceptance Mask 2 registers contain mask
01 = Acceptance Mask 1 registers contain mask
00 = Acceptance Mask 0 registers contain mask
- bit 7-6 **F11MSK<1:0>**: Mask Source for Filter 11 bit
11 = Reserved; do not use
10 = Acceptance Mask 2 registers contain mask
01 = Acceptance Mask 1 registers contain mask
00 = Acceptance Mask 0 registers contain mask
- bit 5-4 **F10MSK<1:0>**: Mask Source for Filter 10 bit
11 = Reserved; do not use
10 = Acceptance Mask 2 registers contain mask
01 = Acceptance Mask 1 registers contain mask
00 = Acceptance Mask 0 registers contain mask
- bit 3-2 **F9MSK<1:0>**: Mask Source for Filter 9 bit
11 = Reserved; do not use
10 = Acceptance Mask 2 registers contain mask
01 = Acceptance Mask 1 registers contain mask
00 = Acceptance Mask 0 registers contain mask
- bit 1-0 **F8MSK<1:0>**: Mask Source for Filter 8 bit
11 = Reserved; do not use
10 = Acceptance Mask 2 registers contain mask
01 = Acceptance Mask 1 registers contain mask
00 = Acceptance Mask 0 registers contain mask

PIC24HJXXXGPX06A/X08A/X10A

REGISTER 19-31: CiTRBnSTAT: ECAN™ MODULE RECEIVE BUFFER n STATUS
(n = 0, 1, ..., 31)

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	FILHIT<4:0>				
bit 15			bit 8				
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7			bit 0				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15-13 **Unimplemented:** Read as '0'
- bit 12-8 **FILHIT<4:0>:** Filter Hit Code bits (only written by module for receive buffers, unused for transmit buffers)
Encodes number of filter that resulted in writing this buffer.
- bit 7-0 **Unimplemented:** Read as '0'

20.0 10-BIT/12-BIT ANALOG-TO-DIGITAL CONVERTER (ADC)

Note 1: This data sheet summarizes the features of the PIC24HJXXXGPX06A/X08A/X10A family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *“dsPIC33F/PIC24H Family Reference Manual”*, **Section 16. “Analog-to-Digital Converter (ADC)”** (DS70183), which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The PIC24HJXXXGPX06A/X08A/X10A devices have up to 32 Analog-to-Digital input channels. These devices also have up to 2 Analog-to-Digital converter modules (ADCx, where ‘x’ = 1 or 2), each with its own set of Special Function Registers.

The AD12B bit (ADxCON1<10>) allows each of the ADC modules to be configured by the user as either a 10-bit, 4-sample/hold ADC (default configuration) or a 12-bit, 1-sample/hold ADC.

Note: The ADC module needs to be disabled before modifying the AD12B bit.

20.1 Key Features

The 10-bit ADC configuration has the following key features:

- Successive Approximation (SAR) conversion
- Conversion speeds of up to 1.1 Msps
- Up to 32 analog input pins
- External voltage reference input pins
- Simultaneous sampling of up to four analog input pins
- Automatic Channel Scan mode
- Selectable conversion trigger source
- Selectable Buffer Fill modes
- Two result alignment options (signed/unsigned)
- Operation during CPU Sleep and Idle modes

The 12-bit ADC configuration supports all the above features, except:

- In the 12-bit configuration, conversion speeds of up to 500 ksps are supported
- There is only 1 sample/hold amplifier in the 12-bit configuration, so simultaneous sampling of multiple channels is not supported.

Depending on the particular device pinout, the Analog-to-Digital Converter can have up to 32 analog input pins, designated AN0 through AN31. In addition, there are two analog input pins for external voltage reference connections. These voltage reference inputs may be shared with other analog input pins. The actual number of analog input pins and external voltage reference input configuration will depend on the specific device.

A block diagram of the Analog-to-Digital Converter is shown in Figure 20-1.

20.2 Analog-to-Digital Initialization

The following configuration steps should be performed.

1. Configure the ADC module:
 - a) Select port pins as analog inputs (ADxPCFGH<15:0> or ADxPCFGL<15:0>)
 - b) Select voltage reference source to match expected range on analog inputs (ADxCON2<15:13>)
 - c) Select the analog conversion clock to match desired data rate with processor clock (ADxCON3<7:0>)
 - d) Determine how many S/H channels will be used (ADxCON2<9:8> and ADxPCFGH<15:0> or ADxPCFGL<15:0>)
 - e) Select the appropriate sample/conversion sequence (ADxCON1<7:5> and ADxCON3<12:8>)
 - f) Select how conversion results are presented in the buffer (ADxCON1<9:8>)
 - g) Turn on the ADC module (ADxCON1<15>)
2. Configure ADC interrupt (if required):
 - a) Clear the ADxIF bit
 - b) Select ADC interrupt priority

20.3 ADC and DMA

If more than one conversion result needs to be buffered before triggering an interrupt, DMA data transfers can be used. Both ADC1 and ADC2 can trigger a DMA data transfer. If ADC1 or ADC2 is selected as the DMA IRQ source, a DMA transfer occurs when the AD1IF or AD2IF bit gets set as a result of an ADC1 or ADC2 sample conversion sequence.

The SMPI<3:0> bits (ADxCON2<5:2>) are used to select how often the DMA RAM buffer pointer is incremented.

The ADDMABM bit (ADxCON1<12>) determines how the conversion results are filled in the DMA RAM buffer area being used for ADC. If this bit is set, DMA buffers are written in the order of conversion. The module will provide an address to the DMA channel that is the same as the address used for the non-DMA stand-alone buffer. If the ADDMABM bit is cleared, the DMA buffers are written in Scatter/Gather mode. The module will provide a scatter/gather address to the DMA channel, based on the index of the analog input and the size of the DMA buffer.

21.4 Watchdog Timer (WDT)

For PIC24HJXXXGPX06A/X08A/X10A devices, the WDT is driven by the LPRC oscillator. When the WDT is enabled, the clock source is also enabled.

The nominal WDT clock source from LPRC is 32 kHz. This feeds a prescaler that can be configured for either 5-bit (divide-by-32) or 7-bit (divide-by-128) operation. The prescaler is set by the WDTPRE Configuration bit. With a 32 kHz input, the prescaler yields a nominal WDT time-out period (TWDT) of 1 ms in 5-bit mode, or 4 ms in 7-bit mode.

A variable postscaler divides down the WDT prescaler output and allows for a wide range of time-out periods. The postscaler is controlled by the WDTPOST<3:0> Configuration bits (FWDT<3:0>) which allow the selection of a total of 16 settings, from 1:1 to 1:32,768. Using the prescaler and postscaler, time-out periods ranging from 1 ms to 131 seconds can be achieved.

The WDT, prescaler and postscaler are reset:

- On any device Reset
- On the completion of a clock switch, whether invoked by software (i.e., setting the OSWEN bit after changing the NOSC bits) or by hardware (i.e., Fail-Safe Clock Monitor)
- When a PWRSAV instruction is executed (i.e., Sleep or Idle mode is entered)
- When the device exits Sleep or Idle mode to resume normal operation
- By a CLRWDT instruction during normal execution

If the WDT is enabled, it will continue to run during Sleep or Idle modes. When the WDT time-out occurs, the device will wake the device and code execution will continue from where the PWRSAV instruction was executed. The corresponding SLEEP or IDLE bits (RCON<3,2>) will need to be cleared in software after the device wakes up.

The WDT flag bit, WDTO (RCON<4>), is not automatically cleared following a WDT time-out. To detect subsequent WDT events, the flag must be cleared in software.

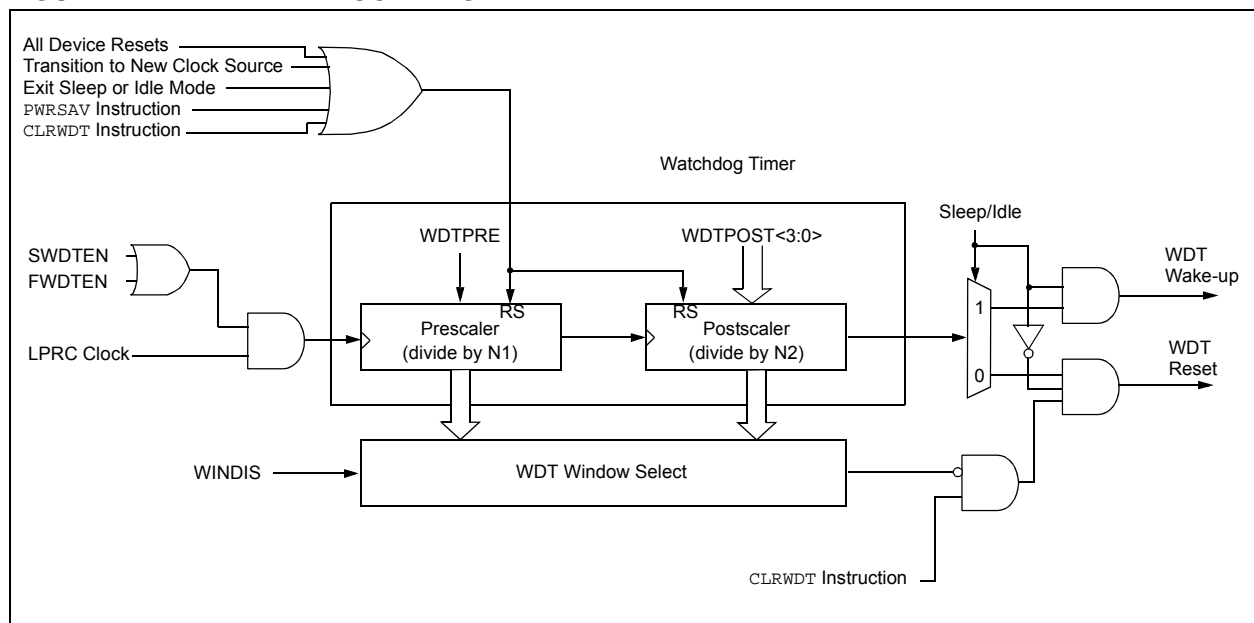
Note: The CLRWDT and PWRSAV instructions clear the prescaler and postscaler counts when executed.

The WDT is enabled or disabled by the FWDTEN Configuration bit in the FWDT Configuration register. When the FWDTEN Configuration bit is set, the WDT is always enabled.

The WDT can be optionally controlled in software when the FWDTEN Configuration bit has been programmed to '0'. The WDT is enabled in software by setting the SWDTEN control bit (RCON<5>). The SWDTEN control bit is cleared on any device Reset. The software WDT option allows the user to enable the WDT for critical code segments and disable the WDT during non-critical segments for maximum power savings.

Note: If the WINDIS bit (FWDT<6>) is cleared, the CLRWDT instruction should be executed by the application software only during the last 1/4 of the WDT period. This CLRWDT window can be determined by using a timer. If a CLRWDT instruction is executed before this window, a WDT Reset occurs.

FIGURE 21-2: WDT BLOCK DIAGRAM



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TABLE 22-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles	Status Flags Affected
47	RCALL	RCALL Expr	Relative Call	1	2	None
		RCALL Wn	Computed Call	1	2	None
48	REPEAT	REPEAT #lit14	Repeat Next Instruction lit14 + 1 times	1	1	None
		REPEAT Wn	Repeat Next Instruction (Wn) + 1 times	1	1	None
49	RESET	RESET	Software device Reset	1	1	None
50	RETFIE	RETFIE	Return from interrupt	1	3 (2)	None
51	RETLW	RETLW #lit10, Wn	Return with literal in Wn	1	3 (2)	None
52	RETURN	RETURN	Return from Subroutine	1	3 (2)	None
53	RLC	RLC f	f = Rotate Left through Carry f	1	1	C,N,Z
		RLC f, WREG	WREG = Rotate Left through Carry f	1	1	C,N,Z
		RLC Ws, Wd	Wd = Rotate Left through Carry Ws	1	1	C,N,Z
54	RLNC	RLNC f	f = Rotate Left (No Carry) f	1	1	N,Z
		RLNC f, WREG	WREG = Rotate Left (No Carry) f	1	1	N,Z
		RLNC Ws, Wd	Wd = Rotate Left (No Carry) Ws	1	1	N,Z
55	RRC	RRC f	f = Rotate Right through Carry f	1	1	C,N,Z
		RRC f, WREG	WREG = Rotate Right through Carry f	1	1	C,N,Z
		RRC Ws, Wd	Wd = Rotate Right through Carry Ws	1	1	C,N,Z
56	RRNC	RRNC f	f = Rotate Right (No Carry) f	1	1	N,Z
		RRNC f, WREG	WREG = Rotate Right (No Carry) f	1	1	N,Z
		RRNC Ws, Wd	Wd = Rotate Right (No Carry) Ws	1	1	N,Z
57	SE	SE Ws, Wnd	Wnd = sign-extended Ws	1	1	C,N,Z
58	SETM	SETM f	f = 0xFFFF	1	1	None
		SETM WREG	WREG = 0xFFFF	1	1	None
		SETM Ws	Ws = 0xFFFF	1	1	None
59	SL	SL f	f = Left Shift f	1	1	C,N,OV,Z
		SL f, WREG	WREG = Left Shift f	1	1	C,N,OV,Z
		SL Ws, Wd	Wd = Left Shift Ws	1	1	C,N,OV,Z
		SL Wb, Wns, Wnd	Wnd = Left Shift Wb by Wns	1	1	N,Z
		SL Wb, #lit5, Wnd	Wnd = Left Shift Wb by lit5	1	1	N,Z
60	SUB	SUB f	f = f – WREG	1	1	C,DC,N,OV,Z
		SUB f, WREG	WREG = f – WREG	1	1	C,DC,N,OV,Z
		SUB #lit10, Wn	Wn = Wn – lit10	1	1	C,DC,N,OV,Z
		SUB Wb, Ws, Wd	Wd = Wb – Ws	1	1	C,DC,N,OV,Z
		SUB Wb, #lit5, Wd	Wd = Wb – lit5	1	1	C,DC,N,OV,Z
61	SUBB	SUBB f	f = f – WREG – (\overline{C})	1	1	C,DC,N,OV,Z
		SUBB f, WREG	WREG = f – WREG – (\overline{C})	1	1	C,DC,N,OV,Z
		SUBB #lit10, Wn	Wn = Wn – lit10 – (\overline{C})	1	1	C,DC,N,OV,Z
		SUBB Wb, Ws, Wd	Wd = Wb – Ws – (\overline{C})	1	1	C,DC,N,OV,Z
		SUBB Wb, #lit5, Wd	Wd = Wb – lit5 – (\overline{C})	1	1	C,DC,N,OV,Z
62	SUBR	SUBR f	f = WREG – f	1	1	C,DC,N,OV,Z
		SUBR f, WREG	WREG = WREG – f	1	1	C,DC,N,OV,Z
		SUBR Wb, Ws, Wd	Wd = Ws – Wb	1	1	C,DC,N,OV,Z
		SUBR Wb, #lit5, Wd	Wd = lit5 – Wb	1	1	C,DC,N,OV,Z
63	SUBBR	SUBBR f	f = WREG – f – (\overline{C})	1	1	C,DC,N,OV,Z
		SUBBR f, WREG	WREG = WREG – f – (\overline{C})	1	1	C,DC,N,OV,Z
		SUBBR Wb, Ws, Wd	Wd = Ws – Wb – (\overline{C})	1	1	C,DC,N,OV,Z
		SUBBR Wb, #lit5, Wd	Wd = lit5 – Wb – (\overline{C})	1	1	C,DC,N,OV,Z
64	SWAP	SWAP.b Wn	Wn = nibble swap Wn	1	1	None
		SWAP Wn	Wn = byte swap Wn	1	1	None
65	TBLRDH	TBLRDH Ws, Wd	Read Prog<23:16> to Wd<7:0>	1	2	None

23.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers and dsPIC® digital signal controllers are supported with a full range of software and hardware development tools:

- Integrated Development Environment
 - MPLAB® IDE Software
- Compilers/Assemblers/Linkers
 - MPLAB C Compiler for Various Device Families
 - HI-TECH C® for Various Device Families
 - MPASM™ Assembler
 - MPLINK™ Object Linker/
MPLIB™ Object Librarian
 - MPLAB Assembler/Linker/Librarian for Various Device Families
- Simulators
 - MPLAB SIM Software Simulator
- Emulators
 - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers
 - MPLAB ICD 3
 - PICKit™ 3 Debug Express
- Device Programmers
 - PICKit™ 2 Programmer
 - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards, Evaluation Kits, and Starter Kits

23.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8/16/32-bit microcontroller market. The MPLAB IDE is a Windows® operating system-based application that contains:

- A single graphical interface to all debugging tools
 - Simulator
 - Programmer (sold separately)
 - In-Circuit Emulator (sold separately)
 - In-Circuit Debugger (sold separately)
- A full-featured editor with color-coded context
- A multiple project manager
- Customizable data windows with direct edit of contents
- High-level source code debugging
- Mouse over variable inspection
- Drag and drop variables from source to watch windows
- Extensive on-line help
- Integration of select third party tools, such as IAR C Compilers

The MPLAB IDE allows you to:

- Edit your source files (either C or assembly)
- One-touch compile or assemble, and download to emulator and simulator tools (automatically updates all project information)
- Debug using:
 - Source files (C or assembly)
 - Mixed C and assembly
 - Machine code

MPLAB IDE supports multiple debugging tools in a single development paradigm, from the cost-effective simulators, through low-cost in-circuit debuggers, to full-featured emulators. This eliminates the learning curve when upgrading to tools with increased flexibility and power.

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23.11 PICkit 2 Development Programmer/Debugger and PICkit 2 Debug Express

The PICkit™ 2 Development Programmer/Debugger is a low-cost development tool with an easy to use interface for programming and debugging Microchip's Flash families of microcontrollers. The full featured Windows® programming interface supports baseline (PIC10F, PIC12F5xx, PIC16F5xx), midrange (PIC12F6xx, PIC16F), PIC18F, PIC24, dsPIC30, dsPIC33, and PIC32 families of 8-bit, 16-bit, and 32-bit microcontrollers, and many Microchip Serial EEPROM products. With Microchip's powerful MPLAB Integrated Development Environment (IDE) the PICkit™ 2 enables in-circuit debugging on most PIC® microcontrollers. In-Circuit-Debugging runs, halts and single steps the program while the PIC microcontroller is embedded in the application. When halted at a breakpoint, the file registers can be examined and modified.

The PICkit 2 Debug Express include the PICkit 2, demo board and microcontroller, hookup cables and CDROM with user's guide, lessons, tutorial, compiler and MPLAB IDE software.

23.12 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages and a modular, detachable socket assembly to support various package types. The ICSP™ cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices and incorporates an MMC card for file storage and data applications.

23.13 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

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TABLE 24-11: ELECTRICAL CHARACTERISTICS: BOR

DC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended					
Param.	Symbol	Characteristic ⁽¹⁾	Min ⁽¹⁾	Typ	Max ⁽¹⁾	Units	Conditions
BO10	VBOR	BOR Event on VDD transition high-to-low	2.40	—	2.55	V	VDD

Note 1: Parameters are for design guidance only and are not tested in manufacturing.

TABLE 24-12: DC CHARACTERISTICS: PROGRAM MEMORY

DC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended					
Param No.	Symbol	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Conditions
D130	EP	Program Flash Memory Cell Endurance	10,000	—	—	E/W	VMIN = Minimum operating voltage VMIN = Minimum operating voltage Provided no other specifications are violated TRW = 11064 FRC cycles, TA = +85°C, See Note 2 TRW = 11064 FRC cycles, TA = +150°C, See Note 2 TPE = 168517 FRC cycles, TA = +85°C, See Note 2 TPE = 168517 FRC cycles, TA = +150°C, See Note 2 TWW = 355 FRC cycles, TA = +85°C, See Note 2 TWW = 355 FRC cycles, TA = +150°C, See Note 2
D131	VPR	VDD for Read	VMIN	—	3.6	V	
D132b	VPEW	VDD for Self-Timed Write	VMIN	—	3.6	V	
D134	TRETD	Characteristic Retention	20	—	—	Year	
D135	IDDP	Supply Current during Programming	—	10	—	mA	
D136a	TRW	Row Write Time	1.32	—	1.74	ms	
D136b	TRW	Row Write Time	1.28	—	1.79	ms	
D137a	TPE	Page Erase Time	20.1	—	26.5	ms	
D137b	TPE	Page Erase Time	19.5	—	27.3	ms	
D138a	TWW	Word Write Cycle Time	42.3	—	55.9	μs	
D138b	TWW	Word Write Cycle Time	41.1	—	57.6	μs	

Note 1: Data in “Typ” column is at 3.3V, 25°C unless otherwise stated.

2: Other conditions: FRC = 7.37 MHz, TUN<5:0> = b'011111 (for Min), TUN<5:0> = b'100000 (for Max). This parameter depends on the FRC accuracy (see Table 24-19) and the value of the FRC Oscillator Tuning register (see Register 9-4). For complete details on calculating the Minimum and Maximum time see Section 5.3 “Programming Operations”.

TABLE 24-13: INTERNAL VOLTAGE REGULATOR SPECIFICATIONS

Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended							
Param.	Symbol	Characteristics	Min	Typ	Max	Units	Comments
	CEFC	External Filter Capacitor Value	4.7	10	—	μF	Capacitor must be low series resistance (< 5 Ohms)

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DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$ for High Temperature			
Parameter No.	Typical	Max	Units	Conditions		
Power-Down Current (IPD)						
HDC61c	3	5	μA	+150°C	3.3V	Watchdog Timer Current: ΔI_{WDT} ^(2,4)

- Note 1:** Base IPD is measured with all peripherals and clocks shut down. All I/Os are configured as inputs and pulled to VSS. WDT, etc., are all switched off, and VREGS (RCON<8>) = 1.
- 2:** The Δ current is the additional current consumed when the module is enabled. This current should be added to the base IPD current.
- 3:** These currents are measured on the device containing the most memory in this family.
- 4:** These parameters are characterized, but are not tested in manufacturing.

TABLE 25-5: DC CHARACTERISTICS: DOZE CURRENT (IDOE)

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$ for High Temperature			
Parameter No.	Typical ⁽¹⁾	Max	Doze Ratio	Units	Conditions	
HDC72a	39	45	1:2	mA	+150°C	3.3V
HDC72f	18	25	1:64	mA		
HDC72g	18	25	1:128	mA		

- Note 1:** Parameters with Doze ratios of 1:2 and 1:64 are characterized, but are not tested in manufacturing.

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NOTES:

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