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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	32-Bit Single-Core
Speed	84MHz
Connectivity	CANbus, EBI/EMI, Microwire, SPI, SSI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	76
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lh75401n0q100c0-55

LH75401/LH75411
System-on-Chip

Product data sheet

DESCRIPTION

The NXP BlueStreak LH75401/LH75411 family consists of two low-cost 16/32-bit System-on-Chip (SoC) devices.

- LH75401 — contains the superset of features.
- LH75411 — similar to LH75401, without CAN 2.0B.

COMMON FEATURES

- Highly Integrated System-on-Chip
- ARM7TDMI-S™ Core
- High Performance (84 MHz CPU Speed)
  - Internal PLL Driven or External Clock Driven
  - Crystal Oscillator/Internal PLL Can Operate with Input Frequency Range of 14 MHz to 20 MHz
- 32 kB On-chip SRAM
  - 16 kB Tightly Coupled Memory (TCM) SRAM
  - 16 kB Internal SRAM
- Clock and Power Management
  - Low Power Modes: Standby, Sleep, Stop
- Eight Channel, 10-bit Analog-to-Digital Converter
- Integrated Touch Screen Controller
- Serial interfaces
  - Two 16C550-type UARTs supporting baud rates up to 921,600 baud (requires crystal frequency of 14.756 MHz).
  - One 82510-type UART supporting baud rates up to 3,225,600 baud (requires a system clock of 70 MHz).
- Synchronous Serial Port
  - Motorola SPI™
  - National Semiconductor Microwire™
  - Texas Instruments SSI
- Real-Time Clock (RTC)
- Three Counter/Timers
  - Capture/Compare/PWM Compatibility
  - Watchdog Timer (WDT)
- Low-Voltage Detector
- JTAG Debug Interface and Boundary Scan
- Single 3.3 V Supply
- 5 V Tolerant Digital I/O
  - XTALIN and XTAL32IN inputs are 1.8 V ± 10 %
- 144-pin LQFP Package
- –40°C to +85°C Operating Temperature

Unique Features of the LH75401

- Color and Grayscale Liquid Crystal Display (LCD) Controller
  - 12-bit (4,096) Direct Mode Color, up to VGA
  - 8-bit (256) Direct or Palettized Color, up to SVGA
  - 4-bit (16) Direct Mode Color/Grayscale, up to XGA
  - 12-bit Video Bus
  - Supports STN, TFT, HR-TFT, and AD-TFT Displays.
- CAN Controller that supports CAN version 2.0B.

Unique Features of the LH75411

- Color and Grayscale LCD Controller (LCDC)
  - 12-bit (4,096) Direct Mode Color, up to VGA
  - 8-bit (256) Direct or Palettized Color, up to SVGA
  - 4-bit (16) Direct Mode Color/Grayscale, up to XGA
  - 12-bit Video Bus
  - Supports STN, TFT, HR-TFT, and AD-TFT Displays.

LH75401 BLOCK DIAGRAM

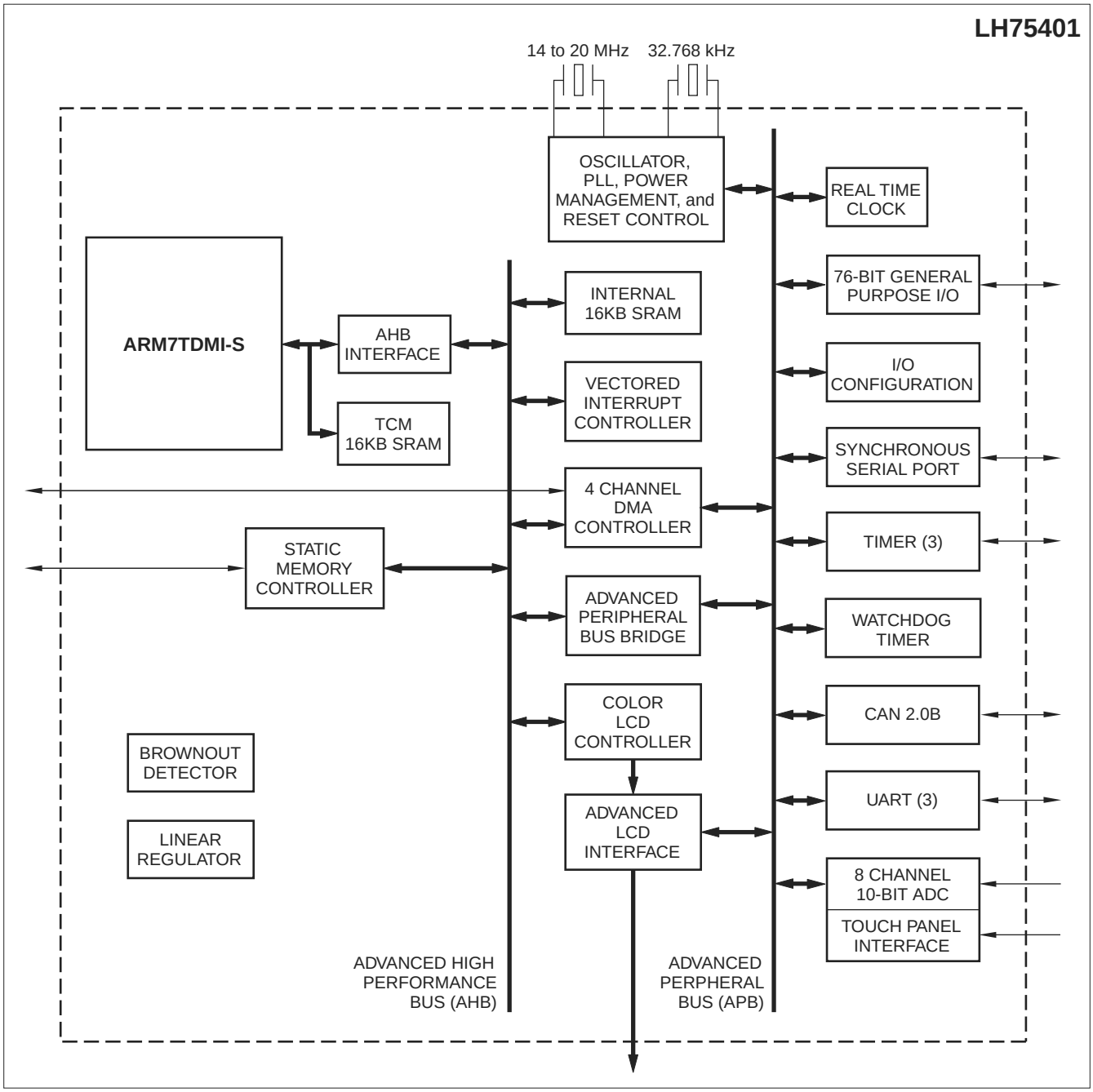


Figure 1. LH75401 Block Diagram

LH75411 BLOCK DIAGRAM

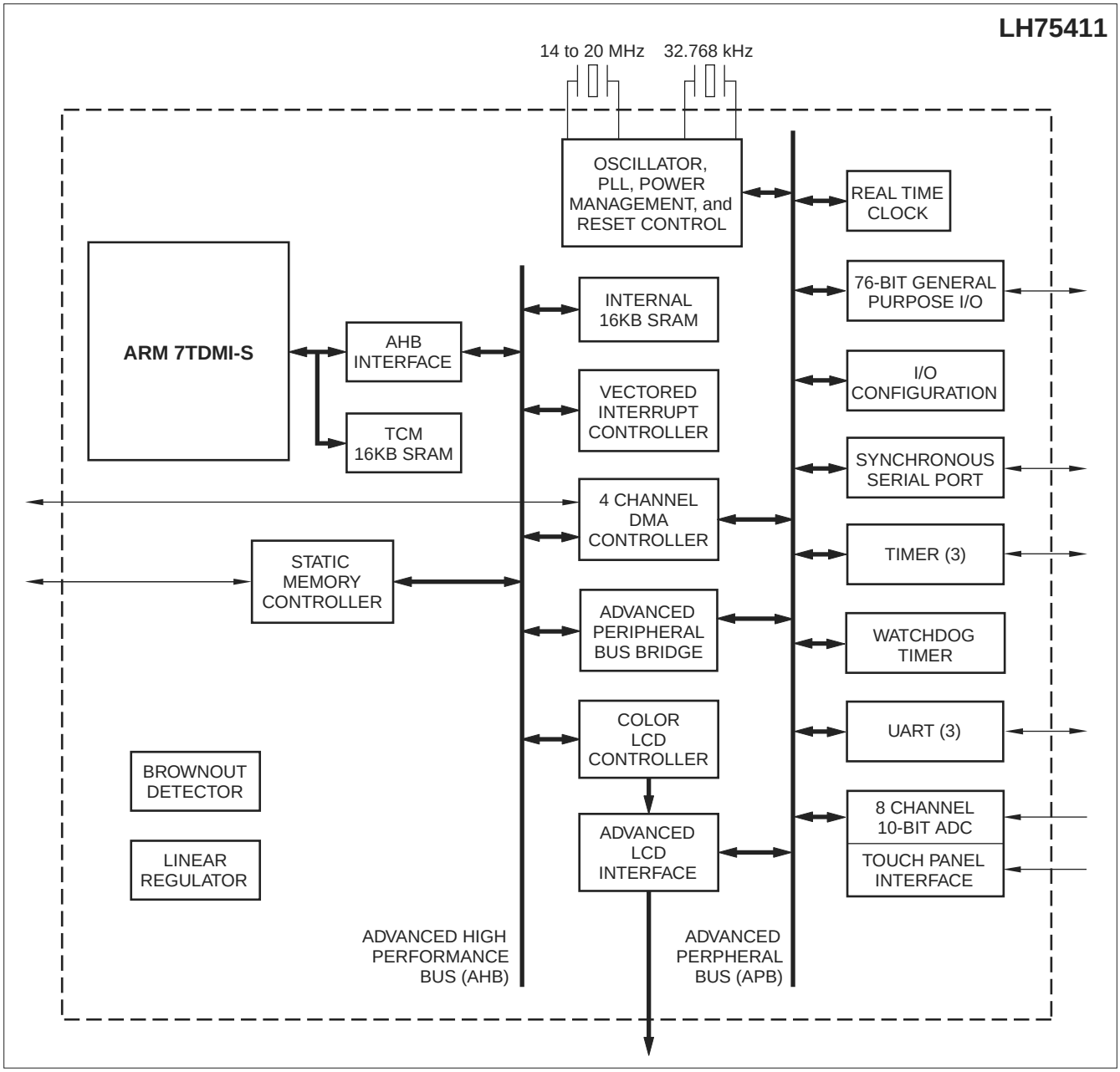


Figure 2. LH75411 Block Diagram

LH75401 Numerical Pin Listing

Table 2. LH75401 Numerical Pin List

PIN NO.	FUNCTION AT RESET	FUNCTION 2	FUNCTION 3	FUNCTION TYPE	OUTPUT DRIVE	BUFFER TYPE	BEHAVIOR DURING RESET	NOTES
1	PA7	D15		I/O	8 mA	Bidirectional	Pull-up	1
2	PA6	D14		I/O	8 mA	Bidirectional	Pull-up	1
3	VDD			Power	None			
4	PA5	D13		I/O	8 mA	Bidirectional	Pull-up	1
5	PA4	D12		I/O	8 mA	Bidirectional	Pull-up	1
6	PA3	D11		I/O	8 mA	Bidirectional	Pull-up	1
7	PA2	D10		I/O	8 mA	Bidirectional	Pull-up	1
8	VSS			Ground	None			
9	PA1	D9		I/O	8 mA	Bidirectional	Pull-up	1
10	PA0	D8		I/O	8 mA	Bidirectional	Pull-up	1
11	VDDC			Power	None			
12	D7			I/O	8 mA	Bidirectional	Pull-up	
13	D6			I/O	8 mA	Bidirectional	Pull-up	
14	VSSC			Ground	None			
15	D5			I/O	8 mA	Bidirectional	Pull-up	
16	D4			I/O	8 mA	Bidirectional	Pull-up	
17	VDD			Power	None			
18	D3			I/O	8 mA	Bidirectional	Pull-up	
19	D2			I/O	8 mA	Bidirectional	Pull-up	
20	D1			I/O	8 mA	Bidirectional	Pull-up	
21	D0			I/O	8 mA	Bidirectional	Pull-up	
22	nWE				8 mA	Output	HIGH	3
23	nOE				8 mA	Output	HIGH	3
24	PB5	nWAIT			8 mA	Bidirectional	Pull-up	1, 3
25	PB4	nBLE1			8 mA	Bidirectional	Pull-up	1, 3
26	VSS			Ground	None			
27	PB3	nBLE0			8 mA	Bidirectional	Pull-up	1, 3
28	PB2	nCS3			8 mA	Bidirectional	Pull-up	1, 3
29	PB1	nCS2			8 mA	Bidirectional	Pull-up	1, 3
30	PB0	nCS1			8 mA	Bidirectional	Pull-up	1, 3
31	nCS0				8 mA	Output	Pull-up	3
32	PC7	A23			8 mA	Bidirectional	Pull-down	1
33	PC6	A22			8 mA	Bidirectional	Pull-down	1
34	VDD			Power	None			
35	PC5	A21			8 mA	Bidirectional	Pull-down	1
36	PC4	A20			8 mA	Bidirectional	Pull-down	1
37	PC3	A19			8 mA	Bidirectional	Pull-down	1
38	PC2	A18			8 mA	Bidirectional	Pull-down	1

Table 2. LH75401 Numerical Pin List (Cont'd)

PIN NO.	FUNCTION AT RESET	FUNCTION 2	FUNCTION 3	FUNCTION TYPE	OUTPUT DRIVE	BUFFER TYPE	BEHAVIOR DURING RESET	NOTES
39	PC1	A17			8 mA	Bidirectional	Pull-down	1
40	PC0	A16			8 mA	Bidirectional	Pull-down	1
41	VSS			Ground	None			
42	VDD			Power	None			
43	A15				8 mA	Output	LOW	
44	A14				8 mA	Output	LOW	
45	A13				8 mA	Output	LOW	
46	A12				8 mA	Output	LOW	
47	A11				8 mA	Output	LOW	
48	VSS			Ground	None			
49	A10				8 mA	Output	LOW	
50	A9				8 mA	Output	LOW	
51	A8				8 mA	Output	LOW	
52	A7				8 mA	Output	LOW	
53	A6				8 mA	Output	LOW	
54	VDD			Power	None			
55	A5				8 mA	Output	LOW	
56	A4				8 mA	Output	LOW	
57	A3				8 mA	Output	LOW	
58	A2				8 mA	Output	LOW	
59	VSS			Ground	None			
60	A1				8 mA	Output	LOW	
61	A0				8 mA	Output	LOW	
62	nRESETIN				None	Input	Pull-up	2, 3
63	TEST2				None	Input	Pull-up	2
64	TEST1				None	Input	Pull-up	2
65	TMS				None	Input	Pull-up	2
66	RTCK				8 mA	Output		
67	TCK				None	Input		
68	TDI				None	Input	Pull-up	2
69	TDO				4 mA	Output		
70	LINREGEN				None	Input		5
71	nRESETOUT				8 mA	Output		3
72	PD6	INT6	DREQ		6 mA	Bidirectional	Pull-down	1
73	PD5	INT5	DACK		6 mA	Bidirectional		1, 2
74	PD4	INT4	UARTRX1		8 mA	Bidirectional	Pull-up	1
75	VDDC			Power	None			
76	PD3	INT3	UARTTX1		8 mA	Bidirectional	Pull-up	1
77	PD2	INT2			2 mA	Bidirectional	Pull-up	1
78	PD1	INT1			6 mA	Bidirectional		1, 2
79	PD0	INT0			2 mA	Bidirectional		1
80	VSSC			Ground	None			

Table 2. LH75401 Numerical Pin List (Cont'd)

PIN NO.	FUNCTION AT RESET	FUNCTION 2	FUNCTION 3	FUNCTION TYPE	OUTPUT DRIVE	BUFFER TYPE	BEHAVIOR DURING RESET	NOTES
81	nPOR				None	Input	Pull-up	2, 3
82	XTAL32IN				None	Input		4
83	XTAL32OUT				None	Output		
84	VSSA_PLL			Ground	None			
85	VDDA_PLL			Power	None			
86	XTALIN				None	Input		4
87	XTALOUT				None	Output		
88	VSSA_ADC			Ground	None			
89	AN3 (LR/Y-)	PJ7			None	Input		
90	AN4 (Wiper)	PJ6			None	Input		
91	AN9	PJ5			None	Input		
92	AN2 (LL/Y+)	PJ4			None	Input		
93	AN8	PJ3			None	Input		
94	AN1 (UR/X-)	PJ2			None	Input		
95	AN6	PJ1			None	Input		
96	AN0 (UL/X+)	PJ0			None	Input		
97	VDDA_ADC			Power	None			
98	VDD			Power	None			
99	PE7	SSPFRM			4 mA	Bidirectional	Pull-up	1
100	PE6	SSPCLK			4 mA	Bidirectional	Pull-down	1
101	PE5	SSPRX			4 mA	Bidirectional	Pull-up	1
102	PE4	SSPTX			4 mA	Bidirectional	Pull-down	1
103	PE3	CANTX	UARTTX0		8 mA	Bidirectional	Pull-up	1
104	PE2	CANRX	UARTRX0		2 mA	Bidirectional	Pull-up	1
105	PE1	UARTTX2			4 mA	Bidirectional	Pull-up	1
106	VSS			Ground	None			
107	PE0	UARTRX2			4 mA	Bidirectional	Pull-up	1
108	PF6	CTCAP2B	CTCMP2B		4 mA	Bidirectional		2
109	PF5	CTCAP2A	CTCMP2A		4 mA	Bidirectional		
110	PF4	CTCAP1B	CACMP1B		4 mA	Bidirectional		2
111	PF3	CTCAP1A	CTCMP1A		4 mA	Bidirectional		
112	VDD			Power	None			
113	PF2	CTCAP0E			4 mA	Bidirectional		2
114	PF1	CTCAP0D			4 mA	Bidirectional		
115	PF0	CTCAP0C			4 mA	Bidirectional		2
116	PG7	CTCAP0B	CTCMP0B		4 mA	Bidirectional		
117	PG6	CTCAP0A	CTCMP0A		4 mA	Bidirectional		2
118	PG5	CTCLK			4 mA	Bidirectional		
119	VSS			Ground	None			
120	PG4	LCDVEEEN	LCDMOD		8 mA	Bidirectional		
121	PG3	LCDVDDEN			8 mA	Bidirectional		
122	PG2	LCDDSPLEN	LCDREV		8 mA	Bidirectional		

LH75401 Signal Descriptions

Table 3. LH75401 Signal Descriptions

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION	NOTES
MEMORY INTERFACE (MI)				
1 2 4 5 6 7 9 10 12 13 15 16 18 19 20 21	D[15:0]	Input/Output	Data Input/Output Signals	1
22	nWE	Output	Static Memory Controller Write Enable	2
23	nOE	Output	Static Memory Controller Output Enable	2
24	nWAIT	Input	Static Memory Controller External Wait Control	1, 2
25	nBLE1	Output	Static Memory Controller Byte Lane Strobe	1, 2
27	nBLE0	Output	Static Memory Controller Byte Lane Strobe	1, 2
28	nCS3	Output	Static Memory Controller Chip Select	1, 2
29	nCS2	Output	Static Memory Controller Chip Select	1, 2
30	nCS1	Output	Static Memory Controller Chip Select	1, 2
31	nCS0	Output	Static Memory Controller Chip Select	2
32 33 35 36 37 38 39 40 43 44 45 46 47 49 50 51 52 53 55 56 57 58 60 61	A[23:0]	Output	Address Signals	1
DMA CONTROLLER (DMAC)				
72	DREQ	Input	DMA Request	1
73	DACK	Output	DMA Acknowledge	1

Table 3. LH75401 Signal Descriptions (Cont'd)

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION	NOTES
72 73 74 76 77 78 79	PD6 PD5 PD4 PD3 PD2 PD1 PD0	Input/Output	General Purpose I/O Signals - Port D	1
89 90 91 92 93 94 95 96	PJ7 PJ6 PJ5 PJ4 PJ3 PJ2 PJ1 PJ0	Input	General Purpose I/O Signals - Port J	1
99 100 101 102 103 104 105 107	PE7 PE6 PE5 PE4 PE3 PE2 PE1 PE0	Input/Output	General Purpose I/O Signals - Port E	1
108 109 110 111 113 114 115	PF6 PF5 PF4 PF3 PF2 PF1 PF0	Input/Output	General Purpose I/O Signals - Port F	1
116 117 118 120 121 122 123 124	PG7 PG6 PG5 PG4 PG3 PG2 PG1 PG0	Input/Output	General Purpose I/O Signals - Port G	1
125 128 129 130 131 132 133 135	PH7 PH6 PH5 PH4 PH3 PH2 PH1 PH0	Input/Output	General Purpose I/O Signals - Port H	1
136 137 138 139 141 142 143 144	PI7 PI6 PI5 PI4 PI3 PI2 PI1 PI0	Input/Output	General Purpose I/O Signals - Port I	1
RESET, CLOCK, AND POWER CONTROLLER (RCPC)				
62	nRESETIN	Input	User Reset Input	2
71	nRESETOUT	Output	System Reset Output	2
72	INT6	Input	External Interrupt Input 6	1

LH75411 Numerical Pin Listing

Table 4. LH75411 Numerical Pin List

PIN NO.	FUNCTION AT RESET	FUNCTION 2	FUNCTION 3	FUNCTION TYPE	OUTPUT DRIVE	BUFFER TYPE	BEHAVIOR DURING RESET	NOTES
1	PA7	D15		I/O	8 mA	Bidirectional	Pull-up	1
2	PA6	D14		I/O	8 mA	Bidirectional	Pull-up	1
3	VDD			Power	None			
4	PA5	D13		I/O	8 mA	Bidirectional	Pull-up	1
5	PA4	D12		I/O	8 mA	Bidirectional	Pull-up	1
6	PA3	D11		I/O	8 mA	Bidirectional	Pull-up	1
7	PA2	D10		I/O	8 mA	Bidirectional	Pull-up	1
8	VSS			Ground	None			
9	PA1	D9		I/O	8 mA	Bidirectional	Pull-up	1
10	PA0	D8		I/O	8 mA	Bidirectional	Pull-up	1
11	VDDC			Power	None			
12	D7			I/O	8 mA	Bidirectional	Pull-up	
13	D6			I/O	8 mA	Bidirectional	Pull-up	
14	VSSC			Ground	None			
15	D5			I/O	8 mA	Bidirectional	Pull-up	
16	D4			I/O	8 mA	Bidirectional	Pull-up	
17	VDD			Power	None			
18	D3			I/O	8 mA	Bidirectional	Pull-up	
19	D2			I/O	8 mA	Bidirectional	Pull-up	
20	D1			I/O	8 mA	Bidirectional	Pull-up	
21	D0			I/O	8 mA	Bidirectional	Pull-up	
22	nWE				8 mA	Output	HIGH	3
23	nOE				8 mA	Output	HIGH	3
24	PB5	nWAIT			8 mA	Bidirectional	Pull-up	1, 3
25	PB4	nBLE1			8 mA	Bidirectional	Pull-up	1, 3
26	VSS			Ground	None			
27	PB3	nBLE0			8 mA	Bidirectional	Pull-up	1, 3
28	PB2	nCS3			8 mA	Bidirectional	Pull-up	1, 3
29	PB1	nCS2			8 mA	Bidirectional	Pull-up	1, 3
30	PB0	nCS1			8 mA	Bidirectional	Pull-up	1, 3
31	nCS0				8 mA	Output	Pull-up	3
32	PC7	A23			8 mA	Bidirectional	Pull-down	1
33	PC6	A22			8 mA	Bidirectional	Pull-down	1
34	VDD			Power	None			
35	PC5	A21			8 mA	Bidirectional	Pull-down	1
36	PC4	A20			8 mA	Bidirectional	Pull-down	1
37	PC3	A19			8 mA	Bidirectional	Pull-down	1
38	PC2	A18			8 mA	Bidirectional	Pull-down	1
39	PC1	A17			8 mA	Bidirectional	Pull-down	1
40	PC0	A16			8 mA	Bidirectional	Pull-down	1
41	VSS			Ground	None			

Table 4. LH75411 Numerical Pin List (Cont'd)

PIN NO.	FUNCTION AT RESET	FUNCTION 2	FUNCTION 3	FUNCTION TYPE	OUTPUT DRIVE	BUFFER TYPE	BEHAVIOR DURING RESET	NOTES
42	VDD			Power	None			
43	A15				8 mA	Output	LOW	
44	A14				8 mA	Output	LOW	
45	A13				8 mA	Output	LOW	
46	A12				8 mA	Output	LOW	
47	A11				8 mA	Output	LOW	
48	VSS			Ground	None			
49	A10				8 mA	Output	LOW	
50	A9				8 mA	Output	LOW	
51	A8				8 mA	Output	LOW	
52	A7				8 mA	Output	LOW	
53	A6				8 mA	Output	LOW	
54	VDD			Power	None			
55	A5				8 mA	Output	LOW	
56	A4				8 mA	Output	LOW	
57	A3				8 mA	Output	LOW	
58	A2				8 mA	Output	LOW	
59	VSS			Ground	None			
60	A1				8 mA	Output	LOW	
61	A0				8 mA	Output	LOW	
62	nRESETIN				None	Input	Pull-up	2, 3
63	TEST2				None	Input	Pull-up	2
64	TEST1				None	Input	Pull-up	2
65	TMS				None	Input	Pull-up	2
66	RTCK				8 mA	Output		
67	TCK				None	Input		
68	TDI				None	Input	Pull-up	2
69	TDO				4 mA	Output		
70	LINREGEN				None	Input		5
71	nRESETOUT				8 mA	Output		3
72	PD6	INT6	DREQ		6 mA	Bidirectional	Pull-down	1
73	PD5	INT5	DACK		6 mA	Bidirectional		1, 2
74	PD4	INT4	UARTRX1		8 mA	Bidirectional	Pull-up	1
75	VDDC			Power	None			
76	PD3	INT3	UARTTX1		8 mA	Bidirectional	Pull-up	1
77	PD2	INT2			2 mA	Bidirectional	Pull-up	1
78	PD1	INT1			6 mA	Bidirectional		1, 2
79	PD0	INT0			2 mA	Bidirectional		1
80	VSSC			Ground	None			
81	nPOR				None	Input	Pull-up	2, 3
82	XTAL32IN				None	Input		4
83	XTAL32OUT				None	Output		

Table 4. LH75411 Numerical Pin List (Cont'd)

PIN NO.	FUNCTION AT RESET	FUNCTION 2	FUNCTION 3	FUNCTION TYPE	OUTPUT DRIVE	BUFFER TYPE	BEHAVIOR DURING RESET	NOTES
84	VSSA_PLL			Ground	None			
85	VDDA_PLL			Power	None			
86	XTALIN				None	Input		4
87	XTALOUT				None	Output		
88	VSSA_ADC			Ground	None			
89	AN3 (LR/Y-)	PJ7			None	Input		
90	AN4 (Wiper)	PJ6			None	Input		
91	AN9	PJ5			None	Input		
92	AN2 (LL/Y+)	PJ4			None	Input		
93	AN8	PJ3			None	Input		
94	AN1 (UR/X-)	PJ2			None	Input		
95	AN6	PJ1			None	Input		
96	AN0 (UL/X+)	PJ0			None	Input		
97	VDDA_ADC			Power	None			
98	VDD			Power	None			
99	PE7	SSPFRM			4 mA	Bidirectional	Pull-up	1
100	PE6	SSPCLK			4 mA	Bidirectional	Pull-down	1
101	PE5	SSPRX			4 mA	Bidirectional	Pull-up	1
102	PE4	SSPTX			4 mA	Bidirectional	Pull-down	1
103	PE3	UARTTX0			8 mA	Bidirectional	Pull-up	1
104	PE2	UARTRX0			2 mA	Bidirectional	Pull-up	1
105	PE1	UARTTX2			4 mA	Bidirectional	Pull-up	1
106	VSS			Ground	None			
107	PE0	UARTRX2			4 mA	Bidirectional	Pull-up	1
108	PF6	CTCAP2B	CTCMP2B		4 mA	Bidirectional		2
109	PF5	CTCAP2A	CTCMP2A		4 mA	Bidirectional		
110	PF4	CTCAP1B	CACMP1B		4 mA	Bidirectional		2
111	PF3	CTCAP1A	CTCMP1A		4 mA	Bidirectional		
112	VDD			Power	None			
113	PF2	CTCAP0E			4 mA	Bidirectional		2
114	PF1	CTCAP0D			4 mA	Bidirectional		
115	PF0	CTCAP0C			4 mA	Bidirectional		2
116	PG7	CTCAP0B	CTCMP0B		4 mA	Bidirectional		
117	PG6	CTCAP0A	CTCMP0A		4 mA	Bidirectional		2
118	PG5	CTCLK			4 mA	Bidirectional		
119	VSS			Ground	None			
120	PG4	LCDVEEEN	LCDMOD		8 mA	Bidirectional		
121	PG3	LCDVDDEN			8 mA	Bidirectional		
122	PG2	LCDDSPLEN	LCDREV		8 mA	Bidirectional		
123	PG1	LCDCLS			8 mA	Bidirectional		
124	PG0	LCDPS			8 mA	Bidirectional		
125	PH7	LCDDCLK			8 mA	Bidirectional		

Table 5. LH75411 Signal Descriptions (Cont'd)

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION	NOTES
81	nPOR	Input	Power-on Reset Input	2
82	XTAL32IN	Input	32.768 kHz Crystal Clock Input	
83	XTAL32OUT	Output	32.768 kHz Crystal Clock Output	
86	XTALIN	Input	Crystal Clock Input	
87	XTALOUT	Output	Crystal Clock Output	
TEST INTERFACE				
63	TEST2	Input	Test Mode Pin 2	
64	TEST1	Input	Test Mode Pin 1	
65	TMS	Input	JTAG Test Mode Select Input	
66	RTCK	Output	Returned JTAG Test Clock Output	
67	TCK	Input	JTAG Test Clock Input	
68	TDI	Input	JTAG Test Serial Data Input	
69	TDO	Output	JTAG Test Data Serial Output	
POWER AND GROUND (GND)				
3 17 34 42 54 98 112 126 134	VDD	Power	I/O Ring VDD	
8 26 41 48 59 106 119 127 140	VSS	Power	I/O Ring VSS	
11 75	VDDC	Power	Core VDD supply (Output if Linear Regulator Enabled, Otherwise Input)	
14 80	VSSC	Power	Core VSS	
70	LINREGEN	Input	Linear Regulator Enable	
84	VSSA_PLL	Power	PLL Analog VSS	
85	VDDA_PLL	Power	PLL Analog VDD Supply	
88	VSSA_ADC	Power	A-to-D converter Analog VSS	
97	VDDA_ADC	Power	A-to-D converter Analog VDD Supply	

NOTES:
1. These pin numbers have multiplexed functions.
2. Signals preceded with 'n' are active LOW.

Color LCD Controller (CLCDC)

The CLCDC is an AMBA master-slave module that connects to the AHB. It translates pixel-coded data into the required formats and timings to drive single/dual monochrome and color LCD panels. Packets of pixel-coded data are fed, via the AHB interface, to two independently programmable, 32-bit-wide DMA FIFOs. Each FIFO is 16 words deep by 32 bits wide.

The CLCDC generates a single combined interrupt to the Vectored Interrupt Controller (VIC) when an interrupt condition becomes true for upper/lower panel DMA FIFO underflow, base address update signification, vertical compare, or bus error.

NOTE: LH75401 and LH75411 microcontrollers support full-color operation.

CLCDC FEATURES

- STN, Color STN, TFT, HR-TFT, and AD-TFT
  - Fully Programmable Timing Controls
  - Advanced LCD Interface for displays with a low level of integration, such as HR-TFT and AD-TFT
- Programmable Resolution
  - Up to VGA (640 × 480 DPI), 12-bit Direct Mode Color
  - Up to SVGA (800 × 600 DPI), 8-bit Direct/Palettized Color
  - Up to XGA (1,024 × 768 DPI), 4-bit Direct Color/Grayscale
  - Direct or Palettized Colors
- Single and Dual Panels
- Supports Sharp and non-Sharp Panels
- CLCDC Outputs Available as General Purpose Inputs/Outputs (GPIOs) if LCDC is Not Needed
- Additional Features
  - Fully programmable horizontal and vertical timing for different display panels
  - 256-entry, 16-bit palette RAM physically arranged as a 128 × 32-bit RAM
  - AC bias signal for STN panels and a data-enable signal for TFT panels.
- Programmable Panel-related Parameters
  - STN mono/color or TFT display
  - Bits-per-pixel
  - STN 4- or 8-bit Interface Mode
  - STN Dual or Single Panel Mode
  - AC panel bias
  - Panel clock frequency
  - Number of panel clocks per line
  - Signal polarity, active HIGH or LOW
  - Little Endian data format
  - Interrupt-generation event.

ADVANCED LCD INTERFACE

The Advanced LCD Interface (ALI) allows for direct connection to ultra-thin panels that do not include a timing ASIC. It converts TFT signals from the Color LCD controller to provide the proper signals, timing and levels for direct connection to a panel's Row and Column drivers for AD-TFT, HR-TFT, or any technology of panel that allows for a connection of this type. The ALI also provides a bypass mode that allows interfacing to the built-in timing ASIC in standard TFT and STN panels.

NOTES:
1. The Advanced LCD Interface pertains to the LH75401 and LH75411 microcontrollers.
2. VGA and XGA modes require 66 MHz core speed.

Universal Asynchronous Receiver Transmitters (UARTs)

The LH75401/LH75411 microcontrollers incorporate three UARTs, designated UART0, UART1, and UART2.

UART 0 AND 1 FEATURES

- Similar functionality to the industry-standard 16C550
- Supported baud rates up to 921,600 baud (given an external crystal frequency of 14.756 MHz)
- Supported character formats:
  - Data bits per character: 5, 6, 7, or 8
  - Parity generation and detection: Even, odd, stick, or none
  - Stop bit generation: 1 or 2
- Full-duplex operation
- Separate transmit and receive FIFOs, with:
  - Programmable depth (1 to 16)
  - Programmable-service 'trigger levels' (1/8, 1/4, 1/2, 3/4, and 7/8)
  - Overrun protection.
- Programmable baud-rate generator that:
  - Enables the UART input clock to be divided by 16 to 65,535 × 16
  - Generates an internal clock common to both transmit and receive portions of the UART.
- DMA support
- Support for generating and detecting breaks during UART transactions
- Loopback testing.

Vectored Interrupt Controller (VIC)

All internal and external interrupts are routed to the VIC, where hardware determines the interrupt priority (see Table 11). The VIC is also where the appropriate signal to the processor (IRQ or FIQ) is generated. The processor services the interrupt as either a vectored interrupt or a default-vectored interrupt.

The VIC accepts inputs from 32 interrupt source lines:

- Seven external
- Twenty-three internal
- Two used as software interrupts.

All 32 interrupt source lines can be enabled, disabled, and cleared individually, and individual status can be determined. On reset, all interrupts are disabled.

The VIC also accepts software-generated interrupts. Software-generated interrupts use the same enabling control as hardware-generated interrupts.

The VIC provides 32 interrupts:

- 16 vectored interrupts
- 16 or more default-vectored interrupts.

Any of the 32 interrupt source lines can be assigned to any of the 16 interrupt vectors. Any line not explicitly assigned to an interrupt vector is processed as a default-vectored interrupt. At reset, all 32 lines become default-vectored interrupts.

Each interrupt line can be explicitly identified as an IRQ (default) or FIQ interrupt. Vectored-interrupt servicing is only available for IRQ interrupts.

Table 11. Interrupt Channels

POSITION	DESCRIPTION	SOURCE
0	WDT	Watchdog Timer
1	Not Used	Available as a software interrupt
2	ARM7 DBGCOMMRX	Sourced by the ARM7TDMI-S Core
3	ARM7 DBGCOMMTX	Sourced by the ARM7TDMI-S Core
4	Timer0 Combined	Timer0
5	Timer1 Combined	Timer1
6	Timer2 Combined	Timer2
7	External Interrupt 0	Sourced by the GPIO Block
8	External Interrupt 1	Sourced by the GPIO Block
9	External Interrupt 2	Sourced by the GPIO Block
10	External Interrupt 3	Sourced by the GPIO Block
11	External Interrupt 4	Sourced by the GPIO Block
12	External Interrupt 5	Sourced by the GPIO Block
13	External Interrupt 6	Sourced by the GPIO Block
14	Not Used	Available as a software interrupt
15	RTC_ALARM	Real Time Clock
16	ADC TSCIRQ (combined)	Analog-to-Digital Converter
17	ADC BrownOutINTR	Brown Out Detector
18	ADC PenIRQ	Analog-to-Digital Converter
19	LCD	LCD Controller
20	SSPTXINTR	Synchronous Serial Port
21	SSPRXINTR	Synchronous Serial Port
22	SSPRORINTR	Synchronous Serial Port
23	SSPRXTOINTR	Synchronous Serial Port
24	SSPINTR	Synchronous Serial Port
25	UART1 UARTRXINTR	UART1
26	UART1 UARTTXINTR	UART1
27	UART1 UARTINTR	UART1
28	UART0 UARTINTR	UART0
29	UART2 Interrupt	UART2
30	DMA	DMA
31	CAN	CAN (LH75401) Reserved (LH75411)

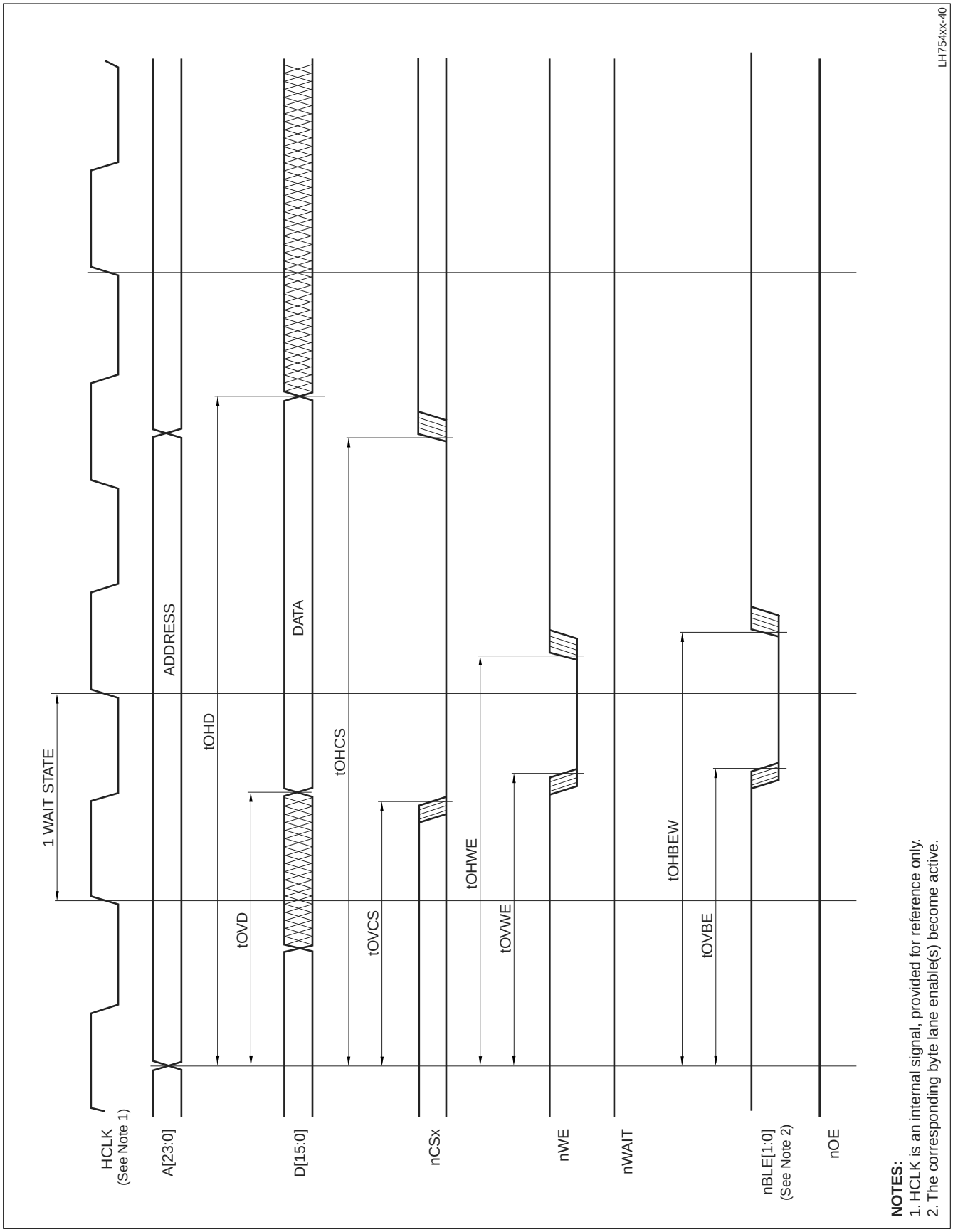


Figure 8. External Static Memory Write, One Wait State

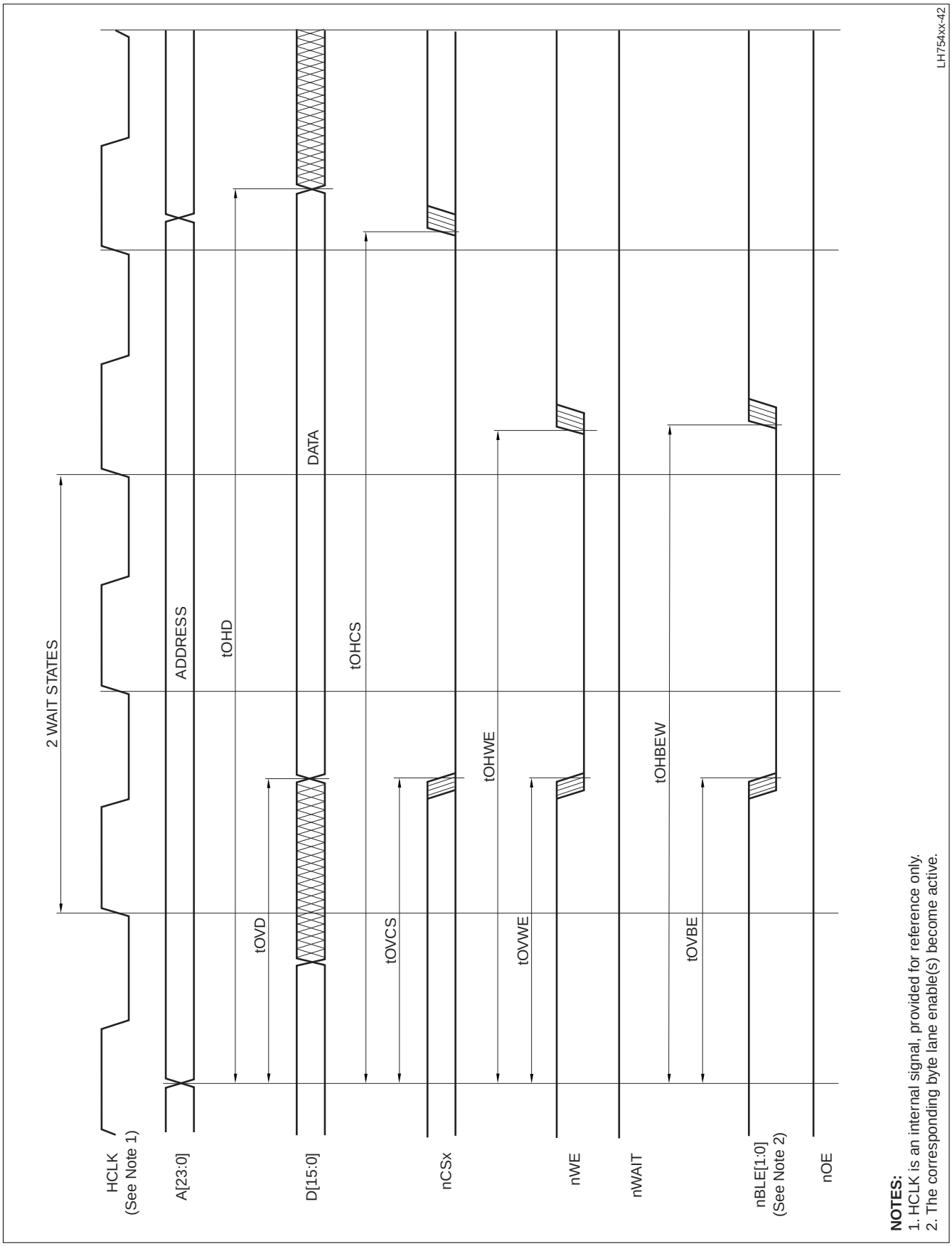


Figure 9. External Static Memory Write, Two Wait States

DMA Controller Timing Diagrams

Figure 13 and Figure 14 show examples of DMA timing diagrams.

- Figure 13 shows the timing for a peripheral-to-memory data transfer, where SoSize = DeSize and SoBurst = 4.
- Figure 14 shows the timing for a memory-to-peripheral data transfer, where SoSize = DeSize and SoBurst = 4.

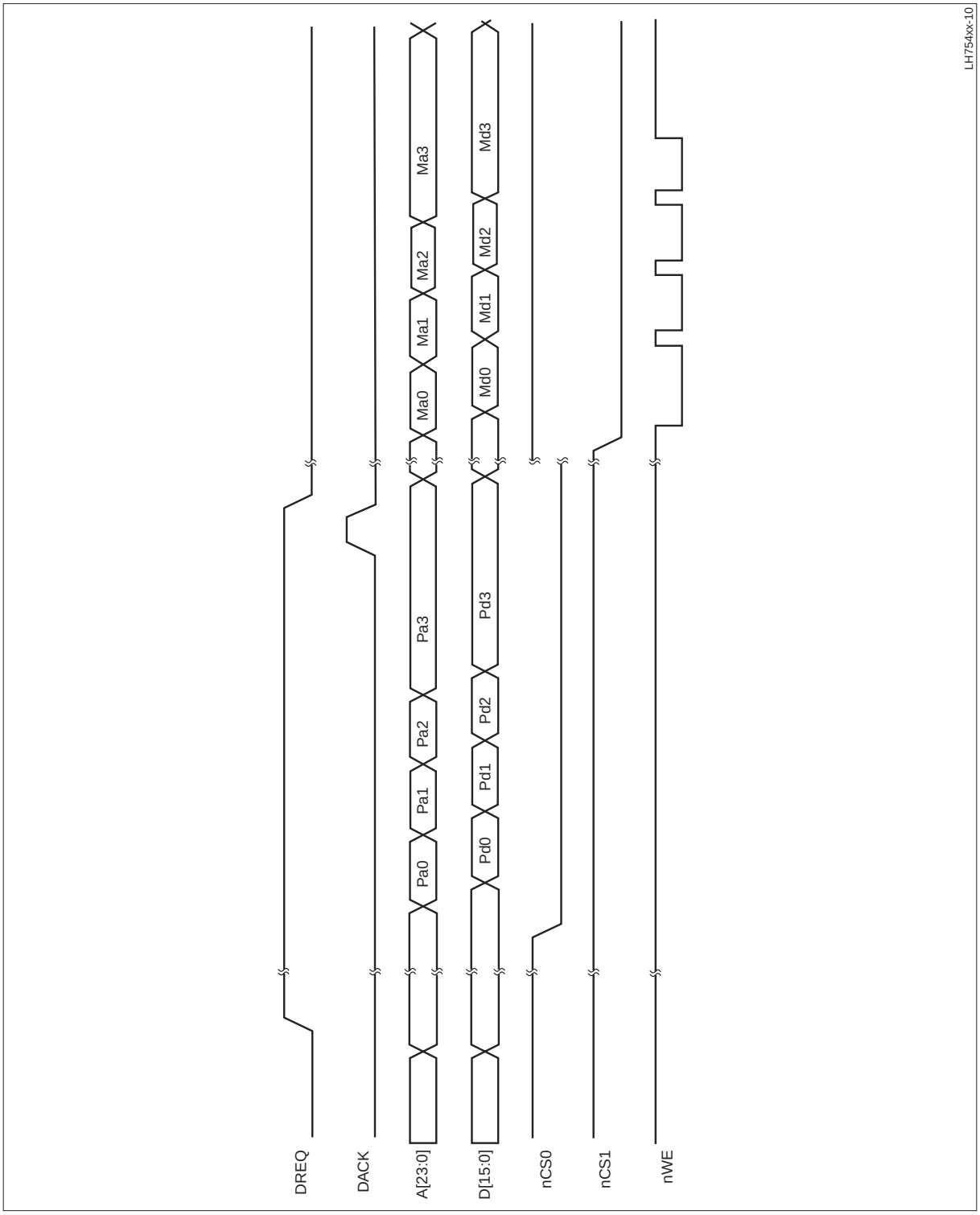


Figure 13. Peripheral-to-Memory Data-Transfer Timing

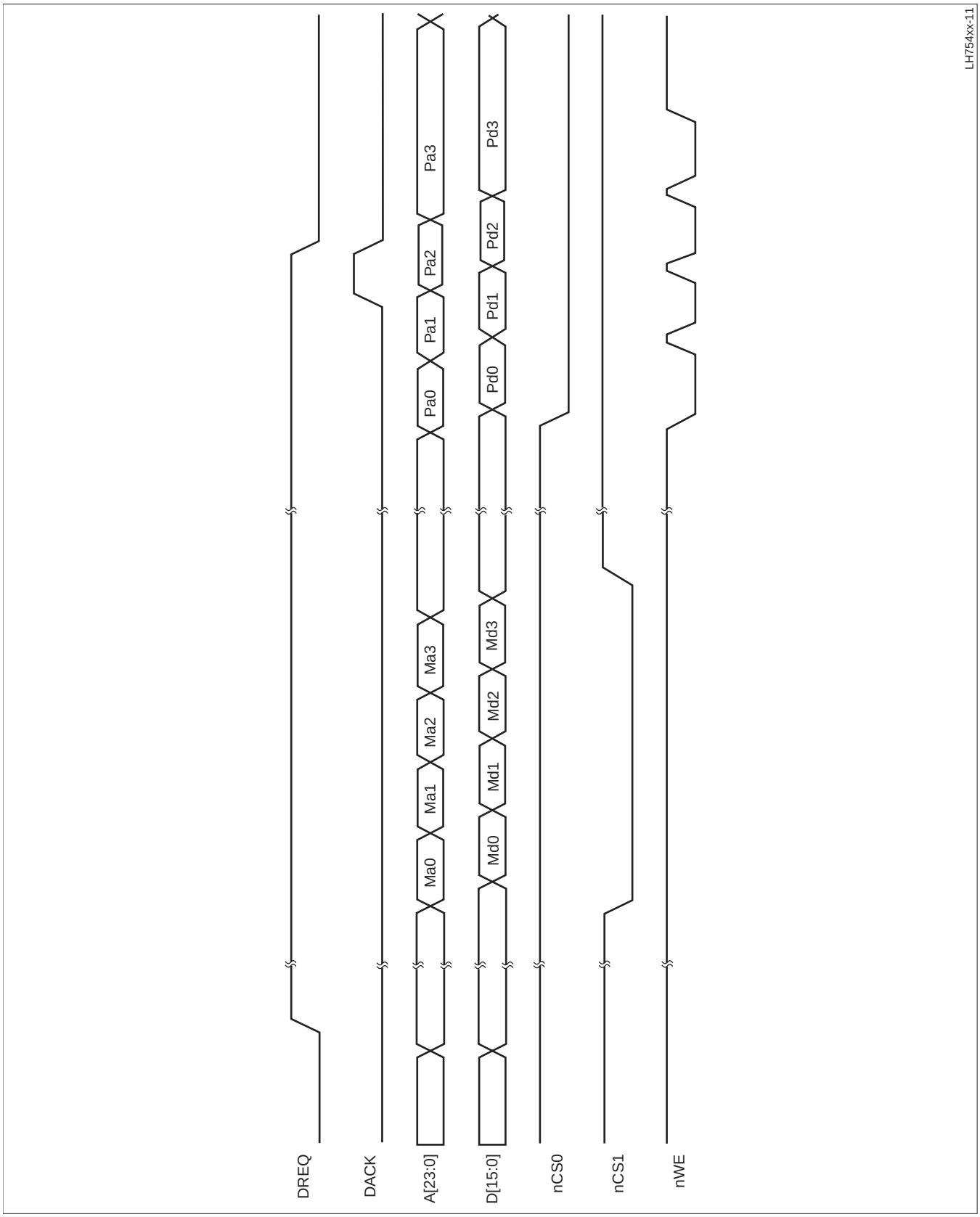


Figure 14. Memory-to-Peripheral Data-Transfer Timing

Color LCD Controller Timing Waveforms

This section describes typical output waveform diagrams for the CLCDC and the Advanced LCD Interface.

STN HORIZONTAL TIMING

Figure 15 shows typical horizontal timing waveforms for STN panels. In this figure, the CLCDC Clock (an input to the CLCDC) is scaled within the CLCDC and used to produce the LCDDCLK output. Programmable registers in the CLCDC set the timings (in terms of LCDDCLK pulses) to produce the other signals that control an STN display.

For example, Figure 15 shows that the duration of the LCDLP signal is controlled by Timing0:HSW (the HSW bit field in the Timing0 Register). Figure 15 also shows that the polarity of the LCDLP signal is set by Timing2:IHS.

STN VERTICAL TIMING

Figure 16 shows typical vertical timing waveforms for STN panels.

TFT HORIZONTAL TIMING

Figure 17 shows typical horizontal timing waveforms for TFT panels.

TFT VERTICAL TIMING

Figure 18 shows typical vertical timing waveforms for TFT panels.

AD-TFT/HR-TFT HORIZONTAL TIMING WAVEFORMS

Figure 19 shows typical horizontal timing waveforms for AD-TFT and HR-TFT panels. The ALI adjusts the normal TFT timing to accommodate these panels.

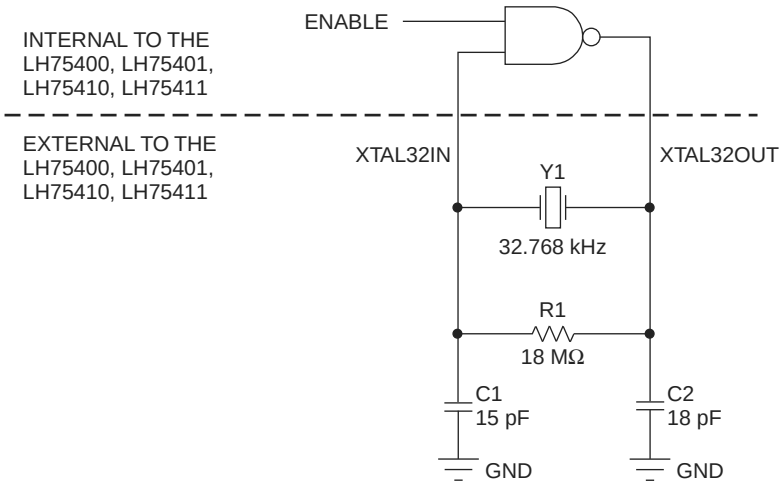
AD-TFT/HR-TFT VERTICAL TIMING WAVEFORMS

Figure 20 shows typical vertical timing waveforms for AD-TFT and HR-TFT panels. The power sequencing and register information is the same as for TFT vertical timing.

SUGGESTED EXTERNAL COMPONENTS

Figure 21 shows the suggested external components for the 32.768 kHz crystal circuit to be used with the NXP LH75401/LH75411. The NAND gate represents the logic inside the SoC. See the chart for crystal specifics.

Figure 22 shows the suggested external components for the 14.7456 MHz crystal circuit to be used with the NXP LH75401/LH75411. The NAND gate represents the logic inside the SoC. See the chart for crystal specifics.



NOTES:
1. Y1 is a parallel-resonant type crystal. (See table)
2. The nominal values for C1 and C2 shown are for a crystal specified at 12.5 pF load capacitance (CL).
3. The values for C1 and C2 are dependent upon the cystal's specified load capacitance and PCB stray capacitance.
4. R1 must be in the circuit.
5. Ground connections should be short and return to the ground plane which is connected to the processor's core ground pins.
6. Tolerance for R1, C1, C2 is ≤ 5%.

RECOMMENDED CRYSTAL SPECIFICATIONS

PARAMETER	DESCRIPTION
32.768 kHz Crystal	Parallel Mode
Tolerance	±30 ppm
Aging	±3 ppm
Load Capacitance	12.5 pF
ESR (MAX.)	50 kΩ
Drive Level	1.0 μW (MAX.)
Recommended Part	MTRON SX1555 or equivalent

LH754xx-101

Figure 21. Suggested External Components, 32.768 kHz Oscillator