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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	32-Bit Single-Core
Speed	84MHz
Connectivity	EBI/EMI, SPI, SSI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	76
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lh75411n0q100c0-55

LH75401/LH75411
System-on-Chip

Product data sheet

DESCRIPTION

The NXP BlueStreak LH75401/LH75411 family consists of two low-cost 16/32-bit System-on-Chip (SoC) devices.

- LH75401 — contains the superset of features.
- LH75411 — similar to LH75401, without CAN 2.0B.

COMMON FEATURES

- Highly Integrated System-on-Chip
- ARM7TDMI-S™ Core
- High Performance (84 MHz CPU Speed)
  - Internal PLL Driven or External Clock Driven
  - Crystal Oscillator/Internal PLL Can Operate with Input Frequency Range of 14 MHz to 20 MHz
- 32 kB On-chip SRAM
  - 16 kB Tightly Coupled Memory (TCM) SRAM
  - 16 kB Internal SRAM
- Clock and Power Management
  - Low Power Modes: Standby, Sleep, Stop
- Eight Channel, 10-bit Analog-to-Digital Converter
- Integrated Touch Screen Controller
- Serial interfaces
  - Two 16C550-type UARTs supporting baud rates up to 921,600 baud (requires crystal frequency of 14.756 MHz).
  - One 82510-type UART supporting baud rates up to 3,225,600 baud (requires a system clock of 70 MHz).
- Synchronous Serial Port
  - Motorola SPI™
  - National Semiconductor Microwire™
  - Texas Instruments SSI
- Real-Time Clock (RTC)
- Three Counter/Timers
  - Capture/Compare/PWM Compatibility
  - Watchdog Timer (WDT)
- Low-Voltage Detector
- JTAG Debug Interface and Boundary Scan
- Single 3.3 V Supply
- 5 V Tolerant Digital I/O
  - XTALIN and XTAL32IN inputs are 1.8 V ± 10 %
- 144-pin LQFP Package
- –40°C to +85°C Operating Temperature

Unique Features of the LH75401

- Color and Grayscale Liquid Crystal Display (LCD) Controller
  - 12-bit (4,096) Direct Mode Color, up to VGA
  - 8-bit (256) Direct or Palettized Color, up to SVGA
  - 4-bit (16) Direct Mode Color/Grayscale, up to XGA
  - 12-bit Video Bus
  - Supports STN, TFT, HR-TFT, and AD-TFT Displays.
- CAN Controller that supports CAN version 2.0B.

Unique Features of the LH75411

- Color and Grayscale LCD Controller (LCDC)
  - 12-bit (4,096) Direct Mode Color, up to VGA
  - 8-bit (256) Direct or Palettized Color, up to SVGA
  - 4-bit (16) Direct Mode Color/Grayscale, up to XGA
  - 12-bit Video Bus
  - Supports STN, TFT, HR-TFT, and AD-TFT Displays.

PIN CONFIGURATION

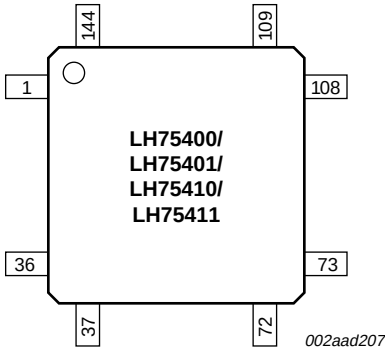


Figure 3. LH75401/LH75411 pin configuration

Table 3. LH75401 Signal Descriptions (Cont'd)

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION	NOTES
ANALOG-TO-DIGITAL CONVERTER (ADC)				
89 90 91 92 93 94 95 96	AN3 (LR/Y-) AN4 (Wiper) AN9 AN2 (LL/Y+) AN8 AN1 (UR/X-) AN6 AN0 (UL/X+)	Input	ADC Inputs	1
TIMER 0				
117 116 115 114 113	CTCAP0[A:E]	Input	Timer 0 Capture Inputs	1
117 116	CTCMP0[A:B]	Output	Timer 0 Compare Outputs	1
118	CTCLK	Input	Common External Clock	1
TIMER 1				
111 110	CTCAP1[A:B]	Input	Timer 1 Capture Inputs	1
111 110	CTCMP1[A:B]	Output	Timer 1 Compare Outputs	1
118	CTCLK	Input	Common External Clock	1
TIMER 2				
109 108	CTCAP2[A:B]	Input	Timer 2 Capture Inputs	1
109 108	CTCMP2[A:B]	Input	Timer 2 Compare Outputs	1
118	CTCLK	Input	Common External Clock	1
GENERAL PURPOSE INPUT/OUTPUT (GPIO)				
1 2 4 5 6 7 9 10	PA7 PA6 PA5 PA4 PA3 PA2 PA1 PA0	Input/Output	General Purpose I/O Signals - Port A	1
24 25 27 28 29 30	PB5 PB4 PB3 PB2 PB1 PB0	Input/Output	General Purpose I/O Signals - Port B	1
32 33 35 36 37 38 39 40	PC7 PC6 PC5 PC4 PC3 PC2 PC1 PC0	Input/Output	General Purpose I/O Signals - Port C	1

Table 3. LH75401 Signal Descriptions (Cont'd)

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION	NOTES
72 73 74 76 77 78 79	PD6 PD5 PD4 PD3 PD2 PD1 PD0	Input/Output	General Purpose I/O Signals - Port D	1
89 90 91 92 93 94 95 96	PJ7 PJ6 PJ5 PJ4 PJ3 PJ2 PJ1 PJ0	Input	General Purpose I/O Signals - Port J	1
99 100 101 102 103 104 105 107	PE7 PE6 PE5 PE4 PE3 PE2 PE1 PE0	Input/Output	General Purpose I/O Signals - Port E	1
108 109 110 111 113 114 115	PF6 PF5 PF4 PF3 PF2 PF1 PF0	Input/Output	General Purpose I/O Signals - Port F	1
116 117 118 120 121 122 123 124	PG7 PG6 PG5 PG4 PG3 PG2 PG1 PG0	Input/Output	General Purpose I/O Signals - Port G	1
125 128 129 130 131 132 133 135	PH7 PH6 PH5 PH4 PH3 PH2 PH1 PH0	Input/Output	General Purpose I/O Signals - Port H	1
136 137 138 139 141 142 143 144	PI7 PI6 PI5 PI4 PI3 PI2 PI1 PI0	Input/Output	General Purpose I/O Signals - Port I	1
RESET, CLOCK, AND POWER CONTROLLER (RCPC)				
62	nRESETIN	Input	User Reset Input	2
71	nRESETOUT	Output	System Reset Output	2
72	INT6	Input	External Interrupt Input 6	1

Table 4. LH75411 Numerical Pin List (Cont'd)

PIN NO.	FUNCTION AT RESET	FUNCTION 2	FUNCTION 3	FUNCTION TYPE	OUTPUT DRIVE	BUFFER TYPE	BEHAVIOR DURING RESET	NOTES
126	VDD			Power	None			
127	VSS			Ground	None			
128	PH6	LCDLP	LCDHRLP		8 mA	Bidirectional		
129	PH5	LCDFP	LCDSPS		8 mA	Bidirectional		
130	PH4	LCDEN	LCDSPL		8 mA	Bidirectional		
131	PH3	LCDVD11			8 mA	Bidirectional		
132	PH2	LCDVD10			8 mA	Bidirectional		
133	PH1	LCDVD9			8 mA	Bidirectional		
134	VDD			Power	None			
135	PH0	LCDVD8			8 mA	Bidirectional		
136	PI7	LCDVD7			8 mA	Bidirectional		
137	PI6	LCDVD6			8 mA	Bidirectional		
138	PI5	LCDVD5			8 mA	Bidirectional		
139	PI4	LCDVD4			8 mA	Bidirectional		
140	VSS			Ground	None			
141	PI3	LCDVD3			8 mA	Bidirectional		
142	PI2	LCDVD2			8 mA	Bidirectional		
143	PI1	LCDVD1			8 mA	Bidirectional		
144	PI0	LCDVD0			8 mA	Bidirectional		

NOTES:
1. Signal is selectable as pull-up, pull-down, or no pull-up/pull-down via the I/O Configuration peripheral.
2. CMOS Schmitt trigger input.
3. Signals preceded with 'n' are active LOW.
4. Crystal Oscillator Inputs should be driven to 1.8 V ±10 % (MAX.)
5. LINREGEN activation requires a 0 Ω pull-up to VDD.

LH75411 Signal Descriptions

Table 5. LH75411 Signal Descriptions

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION	NOTES
MEMORY INTERFACE (MI)				
1 2 4 5 6 7 9 10 12 13 15 16 18 19 20 21	D[15:0]	Input/Output	Data Input/Output Signals	1
22	nWE	Output	Static Memory Controller Write Enable	2
23	nOE	Output	Static Memory Controller Output Enable	2
24	nWAIT	Input	Static Memory Controller External Wait Control	1, 2
25	nBLE1	Output	Static Memory Controller Byte Lane Strobe	1, 2
27	nBLE0	Output	Static Memory Controller Byte Lane Strobe	1, 2
28	nCS3	Output	Static Memory Controller Chip Select	1, 2
29	nCS2	Output	Static Memory Controller Chip Select	1, 2
30	nCS1	Output	Static Memory Controller Chip Select	1, 2
31	nCS0	Output	Static Memory Controller Chip Select	2
32 33 35 36 37 38 39 40 43 44 45 46 47 49 50 51 52 53 55 56 57 58 60 61	A[23:0]	Output	Address Signals	1
DMA CONTROLLER (DMAC)				
72	DREQ	Input	DMA Request	1
73	DACK	Output	DMA Acknowledge	1

Table 5. LH75411 Signal Descriptions (Cont'd)

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION	NOTES
81	nPOR	Input	Power-on Reset Input	2
82	XTAL32IN	Input	32.768 kHz Crystal Clock Input	
83	XTAL32OUT	Output	32.768 kHz Crystal Clock Output	
86	XTALIN	Input	Crystal Clock Input	
87	XTALOUT	Output	Crystal Clock Output	
TEST INTERFACE				
63	TEST2	Input	Test Mode Pin 2	
64	TEST1	Input	Test Mode Pin 1	
65	TMS	Input	JTAG Test Mode Select Input	
66	RTCK	Output	Returned JTAG Test Clock Output	
67	TCK	Input	JTAG Test Clock Input	
68	TDI	Input	JTAG Test Serial Data Input	
69	TDO	Output	JTAG Test Data Serial Output	
POWER AND GROUND (GND)				
3 17 34 42 54 98 112 126 134	VDD	Power	I/O Ring VDD	
8 26 41 48 59 106 119 127 140	VSS	Power	I/O Ring VSS	
11 75	VDDC	Power	Core VDD supply (Output if Linear Regulator Enabled, Otherwise Input)	
14 80	VSSC	Power	Core VSS	
70	LINREGEN	Input	Linear Regulator Enable	
84	VSSA_PLL	Power	PLL Analog VSS	
85	VDDA_PLL	Power	PLL Analog VDD Supply	
88	VSSA_ADC	Power	A-to-D converter Analog VSS	
97	VDDA_ADC	Power	A-to-D converter Analog VDD Supply	

NOTES:
1. These pin numbers have multiplexed functions.
2. Signals preceded with 'n' are active LOW.

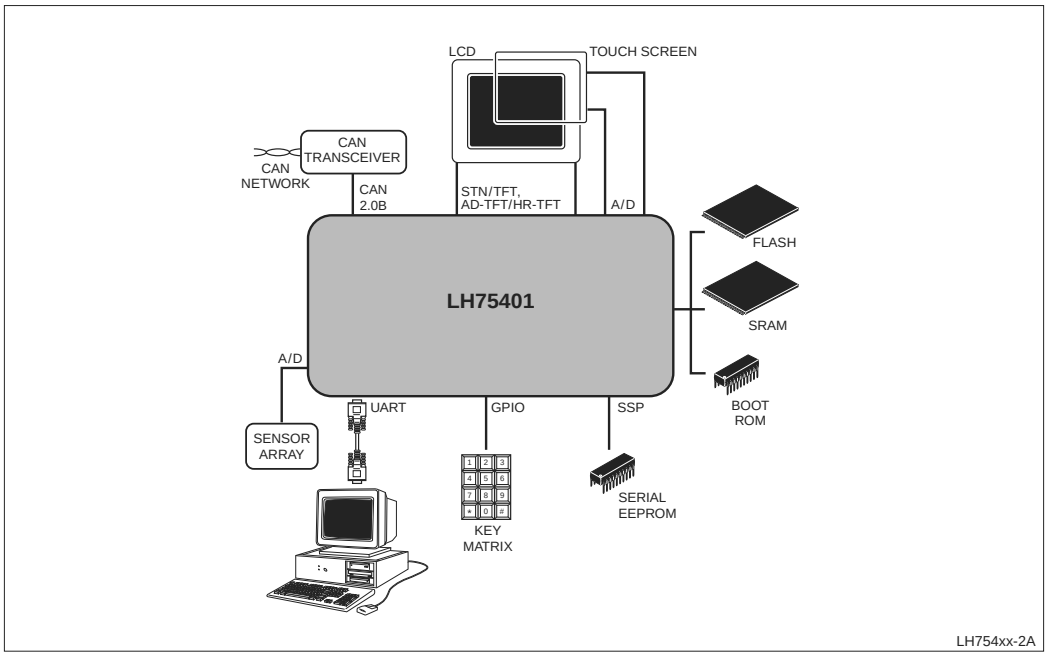


Figure 4. LH75401 System Application Example

FUNCTIONAL OVERVIEW

ARM7TDMI-S Processor

The LH75401/LH75411 microcontrollers feature the ARM7TDMI-S core with an Advanced High-Performance Bus (AHB) 2.0 interface. The ARM7TDMI-S is a 16/32-bit embedded RISC processor and a member of the ARM7 Thumb family of processors. For more information, visit the ARM Web site at www.arm.com.

Bus Architecture

The LH75401/LH75411 microcontrollers use the ARM Advanced Microcontroller Bus Architecture (AMBA) 2.0 internal bus protocol. Three AHB masters control access to external memory and on-chip peripherals:

- The ARM processor fetches instructions and transfers data
- The Direct Memory Access Controller (DMAC) transfers from memory to memory, from peripheral to memory, and from memory to peripheral
- The LCDC refreshes an LCD panel with data from the external memory or from internal memory if the frame buffer is 16 kB or less.

The ARM7TDMI-S processor is the default bus master. An Advanced Peripheral Bus (APB) bridge is provided to access to the various APB peripherals. Generally, APB peripherals are serviced by the ARM core. However, if they are DMA-enabled, they are also serviced by the DMAC to increase system performance while the ARM core runs from local internal memory.

Power Supplies

Five-Volt-tolerant 3.3 V I/Os are employed. The LH75401/LH75411 microcontrollers require a single 3.3 V supply. The core logic requires 1.8 V, supplied by an on-chip linear regulator. Core logic power may also be supplied externally to achieve higher system speeds. See the Electrical Specifications.

Clock Sources

The LH75401/LH75411 microcontrollers may use two crystal oscillators, or an externally supplied clock. There are two clock trees:

- One clock tree drives an internal Phase Lock Loop (PLL) and the three UARTs. It supports a crystal oscillator frequency range from 14 MHz to 20 MHz.
- The other is a 32.768 kHz oscillator that generates a 1 Hz clock for the RTC. (Use of the 32.768 kHz crystal for the Real Time Clock is optional. If not using the crystal, tie XTAL32IN to VSS and allow XTAL32OUT to float.)

The 14-to-20 MHz crystal oscillator drives the UART clocks, so an oscillator frequency of 14.7456 MHz is recommended to achieve modem baud rates.

The PLL may be bypassed and an external clock supplied at XTALIN; the SoC will operate to DC with the PLL disabled. When doing so, allow XTALOUT to float. The input clock with the PLL bypassed will be twice the desired system operating frequency, and care must be taken not to exceed the maximum input clock voltage. Maximum values for system speeds and input voltages are given in the Electrical Specifications.

Reset Generation

EXTERNAL RESETS

Two external signals generate resets to the ARM7TDMI-S core:

- nPOR sets all internal registers to their default state when asserted. It is used as a Power-On Reset.
- nRESETIN sets all internal registers, except the JTAG circuitry, to their default state when asserted.

When nPOR is asserted, nRESETIN defines the microcontroller Test Mode. When nPOR is released, nRESETIN behaves during Reset as described previously.

INTERNAL RESETS

There are two types of Internal Resets generated:

- System Reset
- RTC Reset.

System and RTC Resets are asserted by:

- An External Reset (a logic LOW signal on the external nRESETIN or nPOR input pin)
- A signal from the internal Watchdog Timer
- A Soft Reset.

The reset latency depends on the PLL lock state.

AHB Master Priority and Arbitration

The LH75401/LH75411 microcontrollers have three AHB masters:

- ARM processor
- DMAC
- LCD Controller.

Each AHB master has a priority level that is permanent and cannot change.

Table 6. Bus Master Priority

PRIORITY	BUS MASTER PRIORITY
1 (Highest)	Color LCDC (LH75401 and LH75411)
2	DMAC
3 (Lowest)	ARM7TDMI-S Core (Default)

Memory Interface Architecture

The LH75401/LH75411 microcontrollers provide the following data-path management resources on chip:

- AHB and APB data buses
- 16 kB of zero-wait-state TCM SRAM accessible via processor
- 16 kB of internal SRAM accessible via processor, DMAC, and LCDC
- A Static Memory Controller (SMC) that controls access to external memory
- A 4-stream general-purpose DMAC.

All external and internal system resources are memory-mapped. This memory map partition has three views, based on the setting of the REMAP bits in the Reset, Clock, and Power Controller (RCPC).

The second partitioning of memory space is the dividing of the segments into sections. The external memory segment is divided into eight 64 MB sections, of which the first four are used, each having a chip select associated with it. Access to any of the last four sections does not result in an external bus access and does not cause a memory abort. The peripheral register segment is divided into 4 kB peripheral sections, 21 of which are assigned to peripherals.

Table 7. Memory Mapping

ADDRESS	REMAP = 00 (DEFAULT)	REMAP = 01	REMAP = 10
0x00000000	External Memory	Internal SRAM	TCM SRAM
0x20000000	Reserved	Reserved	Reserved
0x40000000	External Memory	External Memory	External Memory
0x60000000	Internal SRAM	Internal SRAM	Internal SRAM
0x80000000	TCM SRAM	TCM SRAM	TCM SRAM
0xA0000000	Reserved	Reserved	Reserved
0xC0000000	Reserved	Reserved	Reserved
0xE0000000 - 0xFFFBFFFF	Reserved	Reserved	Reserved

Table 8. APB Peripheral Register Mapping

ADDRESS RANGE	DEVICE
0xFFFC0000 - 0xFFFC0FFF	UART0 (16550)
0xFFFC1000 - 0xFFFC1FFF	UART1 (16550)
0xFFFC2000 - 0xFFFC2FFF	UART2 (82510)
0xFFFC3000 - 0xFFFC3FFF	Analog-to-Digital Converter
0xFFFC4000 - 0xFFFC4FFF	Timer Module
0xFFFC5000 - 0xFFFC5FFF	CAN (LH75401) Reserved (LH75411)
0xFFFC6000 - 0xFFFC6FFF	Synchronous Serial Port
0xFFFC7000 - 0xFFFDAFFF	Reserved
0xFFFDB000 - 0xFFFDBFFF	GPIO4
0xFFFDC000 - 0xFFFDCFFF	GPIO3
0xFFFDD000 - 0xFFFDDFFF	GPIO2
0xFFFDE000 - 0xFFFDEFFF	GPIO1
0xFFFDF000 - 0xFFFDFFFF	GPIO0
0xFFFE0000 - 0xFFFE0FFF	Real Time Clock
0xFFFE1000 - 0xFFFE1FFF	DMAC
0xFFFE2000 - 0xFFFE2FFF	Reset Clock and Power Controller
0xFFFE3000 - 0xFFFE3FFF	Watchdog Timer
0xFFFE4000 - 0xFFFE4FFF	Advanced LCD Interface
0xFFFE5000 - 0xFFFE5FFF	I/O Configuration Peripheral
0xFFFE6000 - 0xFFFEFFFF	Reserved

Static Random Access Memory Controller

The LH75401/LH75411 microcontrollers have 32 kB of Static Random Access Memory (SRAM) organized into two 16 kB blocks:

- 16 kB of TCM 0 Wait State SRAM is available to the processor as an ARM7TDMI-S bus slave.
- 16 kB of internal SRAM is available as an AHB slave and accessible via processor, DMAC, and LCDC.

Each memory segment is 512 MB, though the TCM and internal SRAMs are 16 kB each in size. Any access beyond the first 16 kB is mapped to the lower 16 kB, but does not cause a data or prefetch abort.

Static Memory Controller (SMC)

The Static Memory Controller (SMC) is an AMBA AHB slave peripheral that provides the interface between the LH75401/LH75411 microcontrollers and external memory devices.

SMC FEATURES

- Provides four banks of external memory, each with a maximum size of 16 MB.
- Supports memory-mapped devices, including Random Access Memory (RAM), Read Only Memory (ROM), Flash, and burst ROM
- Supports external bus and external device widths of 8 and 16 bits
- Supports Asynchronous Burst Mode read access for Burst Mode ROM devices, with up to 32 independent wait states for read and write accesses
- Supports indefinite extended wait states via an external hardware pin (nWAIT)
- Supports varied bus turnaround cycles (1 to 16) between a read and write operation

Direct Memory Access Controller (DMAC)

One central DMAC services all peripheral DMA requirements for the DMA-capable peripherals listed in Table 9.

The DMA is controlled by the system clock. It has an APB slave port for programming of its registers and an AHB port for data transfers.

Table 9. DMAC Stream Assignments

DMA REQUEST SOURCE	DMA STREAM
UART1RX (highest priority)	Stream0
UART1TX	Stream1
UART0RX/External Request (DREQ)	Stream2
UART0TX (lowest priority)	Stream3

DMAC FEATURES

- Four data streams that can be used to service:
  - Four peripheral data streams (peripheral-to-memory or memory-to-peripheral)
  - Three peripheral data streams and one memory-to-memory data stream.
- Three transfer modes:
  - Memory to Memory (selectable on Stream3)
  - Peripheral to Memory (all streams)
  - Memory to Peripheral (all streams).
- Built-in data stream arbiter
- Seven programmable registers for each stream
- Ability for each stream to indicate a transfer error via an interrupt
- 16-word First-In, First Out (FIFO) array, with pack and unpack logic to handle all input/output combinations of byte, half-word, and word transfers
- APB slave port allows the ARM core to program DMAC registers
- AHB port for data transfers.

Table 10. SSP Modes

MODE	DESCRIPTION	DATA TRANSFERS
Motorola SPI	For communications with Motorola SPI-compatible devices. Clock polarity and phase are programmable.	Full-duplex, 4-wire synchronous
SSI	For communications with Texas Instruments DSP-compatible Serial Synchronous Interface devices.	Full-duplex, 4-wire synchronous
National Semiconductor Microwire	For communications with National Semiconductor Microwire-compatible devices.	Half-duplex synchronous, using 8-bit control messages

Watchdog Timer (WDT)

The WDT consists of a 32-bit down-counter that allows a selectable time-out interval to detect malfunctions. The timer must be reset by software periodically. Otherwise, a time-out occurs, interrupting the system. If the interrupt is not serviced within the timeout period, the WDT triggers the RCPC to generate a System Reset. If the WDT times out, it sets a bit in the RCPC Reset Status Register.

The WDT supports 16 selectable time intervals, for a time-out of 216 through 231 system clock cycles. All Control and Status Registers for the Watchdog Timer are accessed through the APB.

WDT FEATURES

- Counter generates an interrupt at a set interval and the count reloads from the pre-set value after reaching zero.
- Default timeout period is set to the minimum timeout of 216 system clock cycles.
- WDT is driven by the APB.
- Built-in protection mechanism guards against interrupt-service failure.
- WDT can be programmed to trigger a System Reset on a timeout.
- WDT can be programmed to trigger an interrupt on the first timeout; then, if the service routine fails to clear the interrupt, the next WDT timeout triggers a System Reset.

Reset, Clock, and Power Controller (RCPC)

The RCPC lets users control System Reset, clocks, power management, and external interrupt conditioning via the AMBA APB interface. This control includes:

- Enabling and disabling various clocks
- Managing power-down sequencing
- Selecting the sources for various clocks.

The RCPC provides for an orderly start-up until the crystal oscillator stabilizes and the PLL acquires lock. If users want to change the system clock frequency during normal operation, the RCPC ensures a seamless transition between the old and new frequencies.

RCPC FEATURES

- Manages five Power Modes for minimizing power consumption: Active, Standby, Sleep, Stop1, and Stop2
- Generates the system clock (HCLK) from either the PLL clock or the PLL-bypassed (oscillator) clock, divided by 2, 4, 6, 8, … 30
- Generates three UART clocks from oscillator clock
- Generates the 1 Hz RTC clock
- Generates the SSP and LCD clocks from HCLK, divided by 1, 2, 4, 8, 16, 32, or 64
- Provides a selectable external clock output
- Generates system and RTC Resets based on an external reset, Watchdog Timer reset, or soft reset
- Configures seven HIGH/LOW-level or rising/falling edge-trigger external interrupts and converts them to HIGH-level trigger interrupt outputs required by the VIC
- Generates remap outputs used by the memory map decoder
- Provides an identification register
- Supports external or watchdog reset status.

Operating Modes

The LH75401/LH75411 microcontrollers support three operating modes:

- Normal Mode
- PLL Bypass Mode, where the internal PLL is bypassed and an external clock source is used; otherwise the chip operates normally
- EmbeddedICE Mode, where the JTAG port accesses the TAP Controller in the core and the core is placed in Debug Mode.

The state of the TEST1, TEST2, and nRESETIN signals determines the operating mode entered at Power-on Reset (see Table 12).

Table 12. Device Operating Modes

OPERATING MODE	TEST2	TEST1	nRESETIN
Reserved	0	0	0
PLL Bypass	0	0	1
Reserved	0	1	x
Reserved	1	0	0
EmbeddedICE	1	0	1
Normal	1	1	x

NOTE: TEST1, TEST2, and nRESETIN are latched on the rising edge of nPOR. The microcontroller stays in that operating mode until power is removed or nPOR transitions from LOW to HIGH.

General Purpose Input/Output (GPIO)

The LH75401/LH75411 microcontrollers have 10 GPIO ports:

- Seven 8-bit ports
- Two 7-bit ports
- One 6-bit port.

The GPIO ports are designated A through J and provide 76 bits of programmable input/output (see Table 13). Pins of all ports, except Port J, can be configured as inputs or outputs. Port J is input only. Upon System Reset, all ports default to inputs.

Table 13. GPIO Ports

PORT	PROGRAMMABLE PINS
A	8 Input/Output Pins
B	6 Input/Output Pins
C	8 Input/Output Pins
D	7 Input/Output Pins
E	8 Input/Output Pins
F	7 Input/Output Pins
G	8 Input/Output Pins
H	8 Input/Output Pins
I	8 Input/Output Pins
J	8 Input Pins

Analog-To-Digital Converter Electrical Characteristics

Table 21 shows the derated specifications for extended temperature operation. See Figure 6 for the ADC transfer characteristics.

Table 21. ADC Electrical Characteristics at Industrial Operating Range

PARAMETER	MIN.	TYP.	MAX.	UNITS	NOTES
A/D Resolution	10		10	Bits	
Throughput Conversion	17			CLK Cycles	1
Acquisition Time	3			CLK Cycles	
Clk Period	500		5,000	ns	
Differential Non-Linearity	-0.99		4.5	LSB	
Integral Non-Linearity	-3.5		+3.5	LSB	
Offset Error	-35		+35	mV	
Gain Error	-4.0		4.0	LSB	
On-chip Voltage Reference (VREF)	1.85	2.0	2.15	V	
Negative Reference Input (VREF-)	VSSA	VSSA	(VREF+) -1.0	V	2
Positive Reference Input (VREF+)	(VREF-) +1.0	VREF	VDDA	V	2
Crosstalk between channels		-60		dB	
Analog Input Voltage Range	0		VDDA	V	3
Analog Input Current			5	μA	
Reference Input Current			5	μA	
Analog input capacitance			15	pF	
Operating Supply Voltage	3.0		3.6	V	
Operating Current, VDDA		590		μA	
Standby Current		180		μA	4
Stop Current, VDDA		< 1		μA	
Brown Out Trip Point		2.63		V	
Brown Out Hysterisis		120		mV	
Operating Temperature	–40		85	°C	

NOTES:

1. The analog section of the ADC takes 16 × A2DCLK cycles per conversion, plus 1 × A2DCLK cycles to be made available in the PCLK domain. An additional 3 × PCLK cycles are required before being available on the APB.
2. The internal voltage reference is driven to nominal value VREF = 2.0 V. Using the Reference Multiplexer, alternative low impedance (RS < 500) voltages can be selected as reference voltages. The range of voltages allowed are specified above. However, the on-chip reference cannot drive the ADC unless the reference buffer is switched on.
3. The analog input pins can be driven anywhere between the power supply rails. If the voltage at the input to the ADC exceeds VREF+ or is below VREF-, the A/D result will saturate appropriately at positive or negative full scale. Trying to pull the analog input pins above or below the power supply rails will cause protection diodes to be forward-biased, resulting in large current source/sink and possible damage to the ADC.
4. Bandgap and other low-bandwidth circuitry operating. All other ADC blocks shut down.

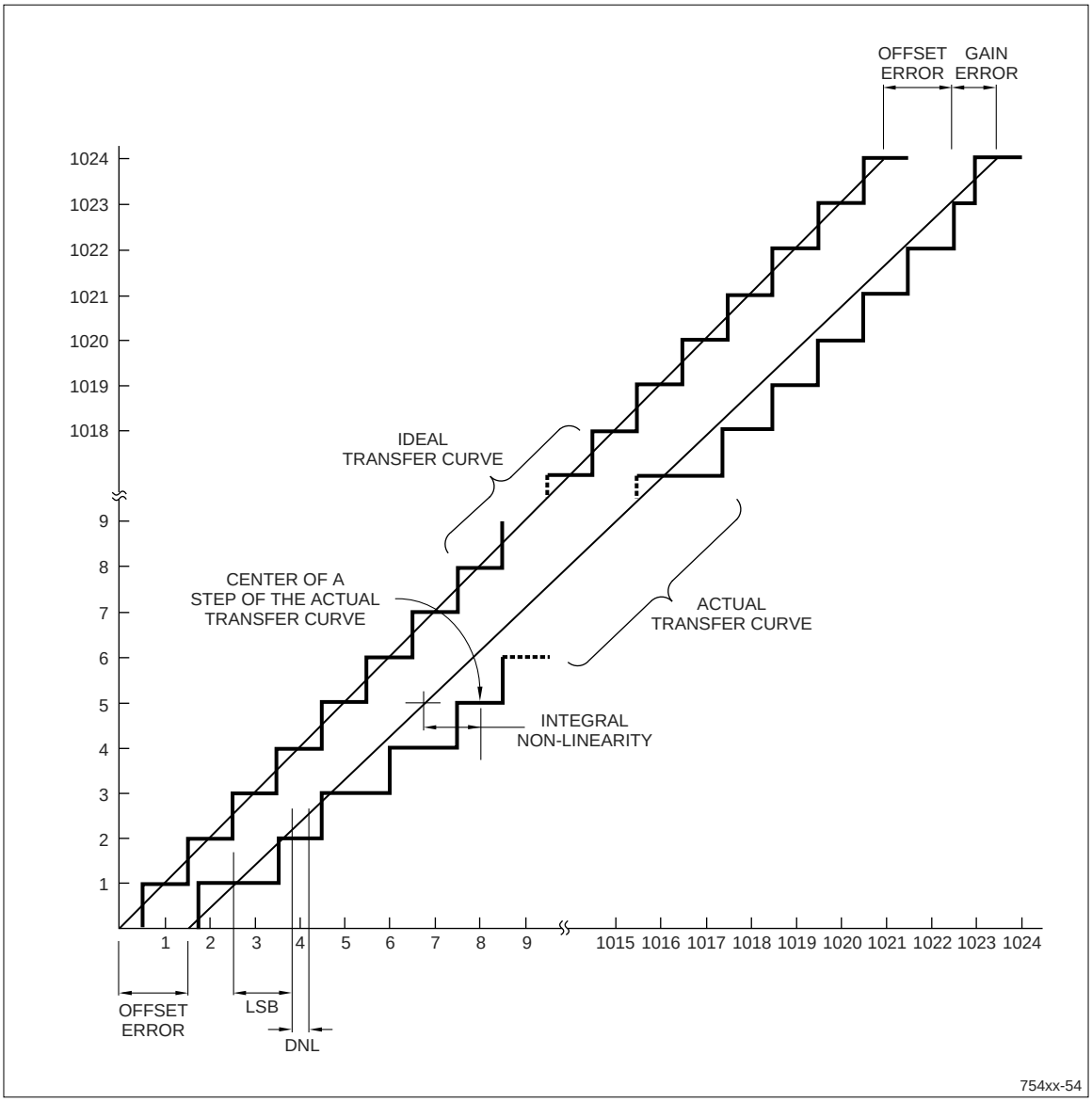


Figure 6. ADC Transfer Characteristics

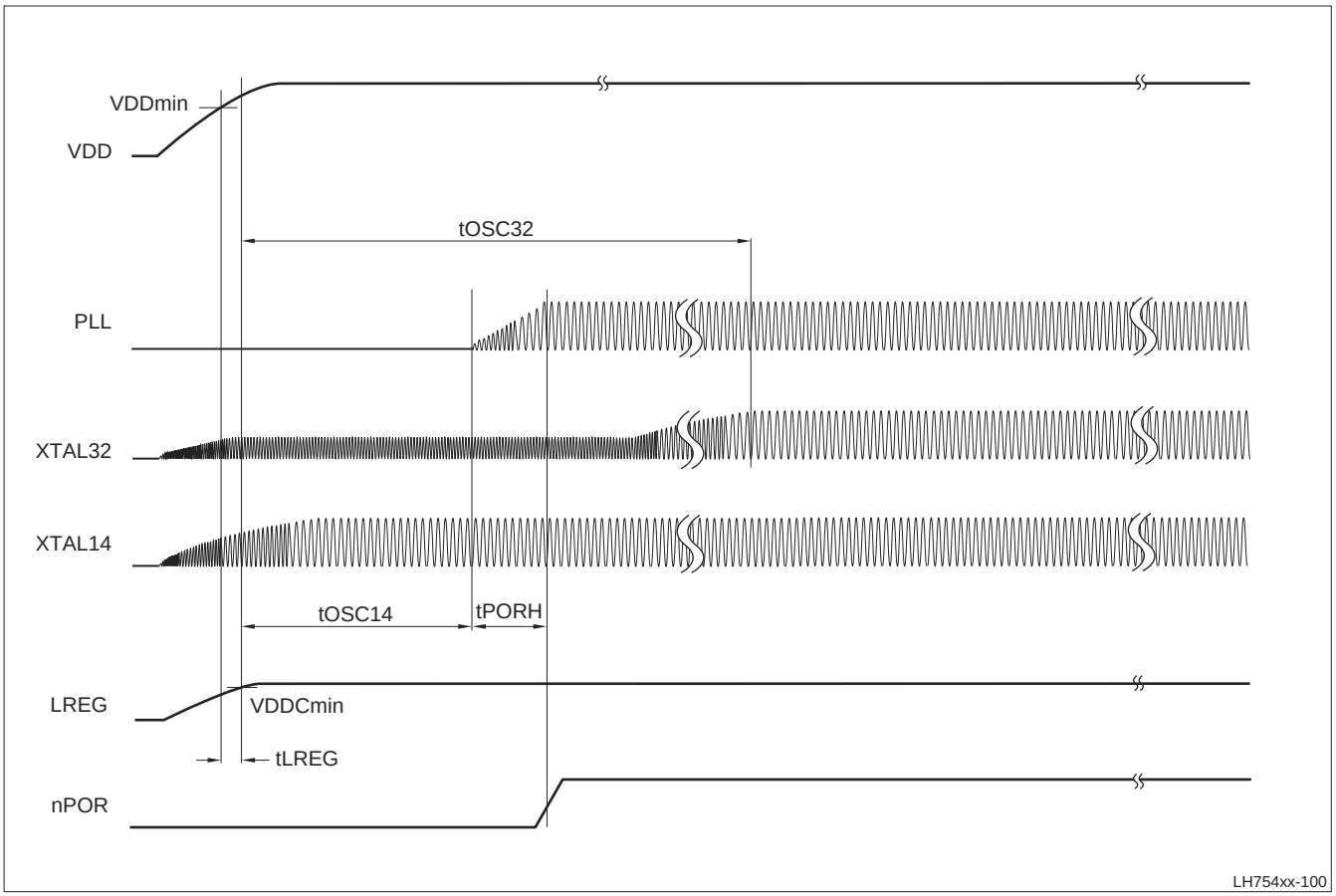


Figure 7. Power-up Stabilization

MEMORY CONTROLLER WAVEFORMS

Static Memory Controller Waveforms

Figure 8 shows the waveform and timing for an External Static Memory Write, with one Wait State. Figure 9 shows the waveform and timing for an External Static Memory Write, with two Wait States. Figure 10 shows the waveform and timing for an External Static Memory Read, with one Wait State.

The SMC supports an nWAIT input that can be used by an external device to extend the wait time during a memory access. The SMC samples nWAIT at the beginning of at the beginning of each system clock cycle. The system clock cycle in which the nCSx signal is asserted counts as the first wait state. See Figure 11. The SMC recognizes that nWAIT is active within 2 clock cycles after it has been asserted. To assure that the current access (read or write) will be extended by nWAIT, program at least two wait states for this bank of memory. If N wait states are programmed, the SMC holds this state for N system clocks or until the SMC detects that nWAIT is inactive, whichever occurs last. As the number of wait states programmed increases, the amount of delay before nWAIT must be asserted also increases. If only 2 wait states are programmed, nWAIT must be asserted in the clock cycle immediately following the clock cycle during which the nCSx signal is asserted. Once the SMC detects that the external device has deactivated nWAIT, the SMC completes its access in 3 system clock cycles.

The formula for the allowable delay between asserting nCSx and asserting nWAIT is:

tASSERT = (system clock period) × (Wait States - 1)
(where Wait States is from 2 to 31.)

The signal tIDD is shown without a setup time, as measurements are made from the Address Valid point and HCLK is an internal signal, shown for reference only.

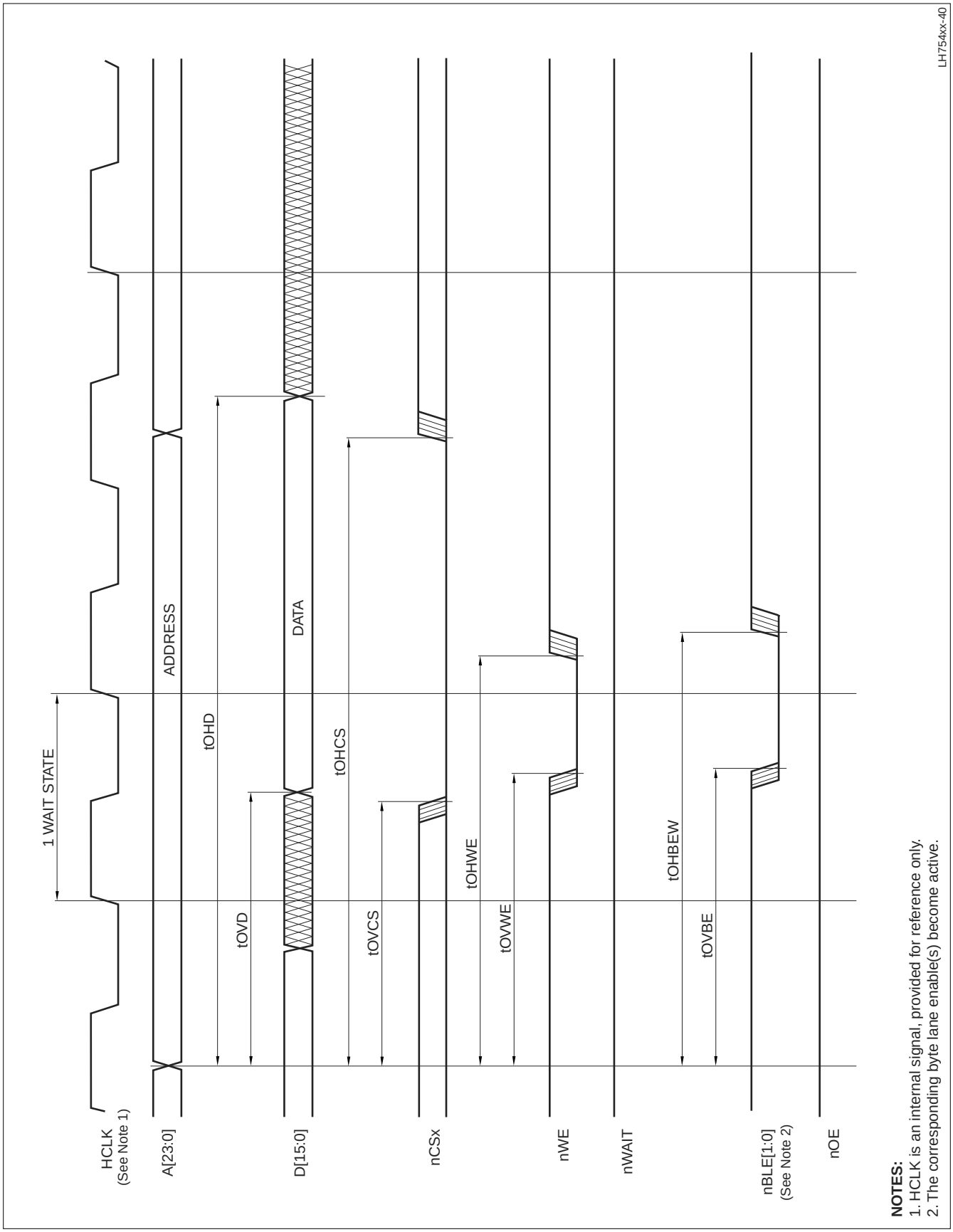


Figure 8. External Static Memory Write, One Wait State

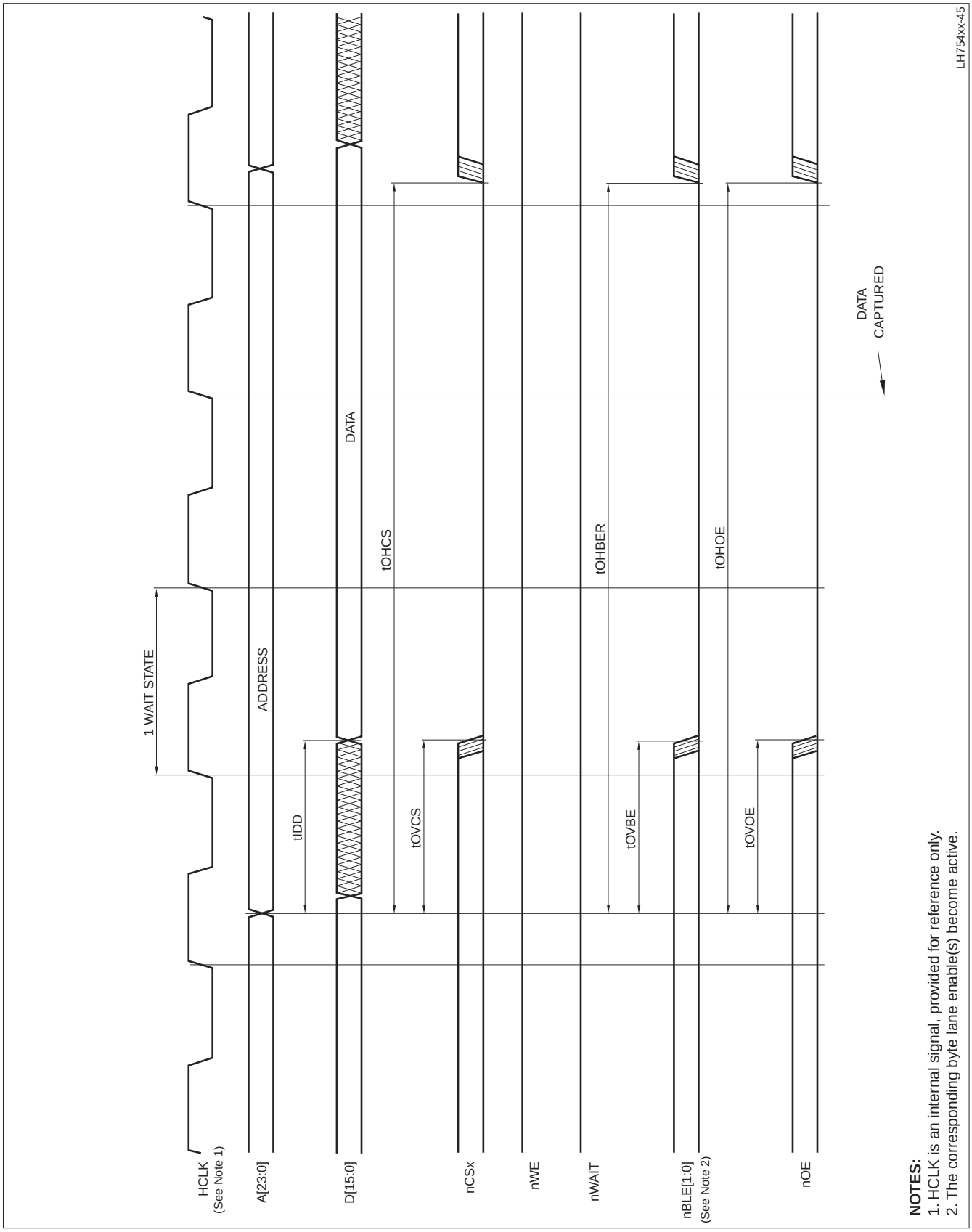


Figure 10. External Static Memory Read, One Wait State

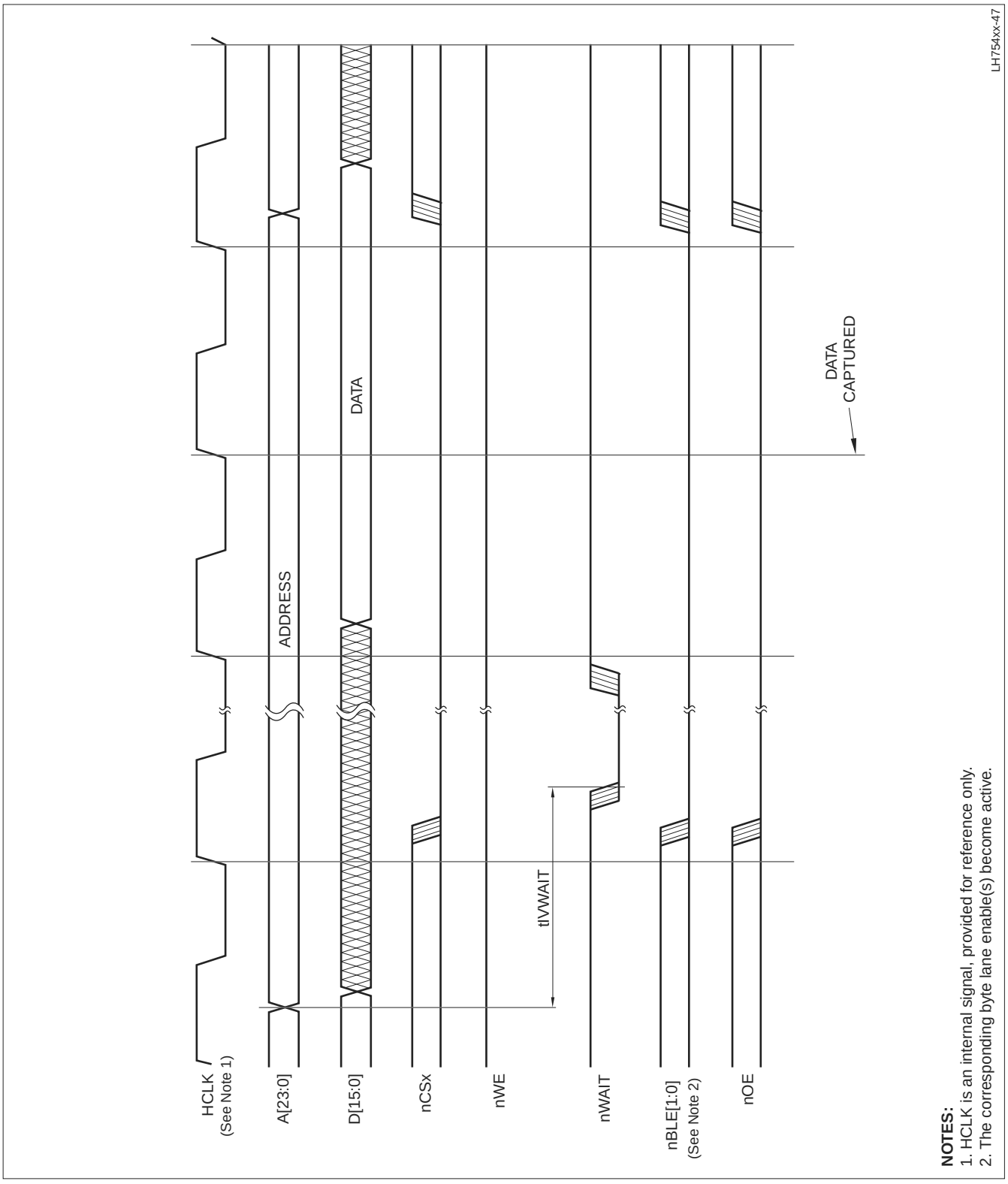


Figure 11. External Static Memory Read, nWAIT Active

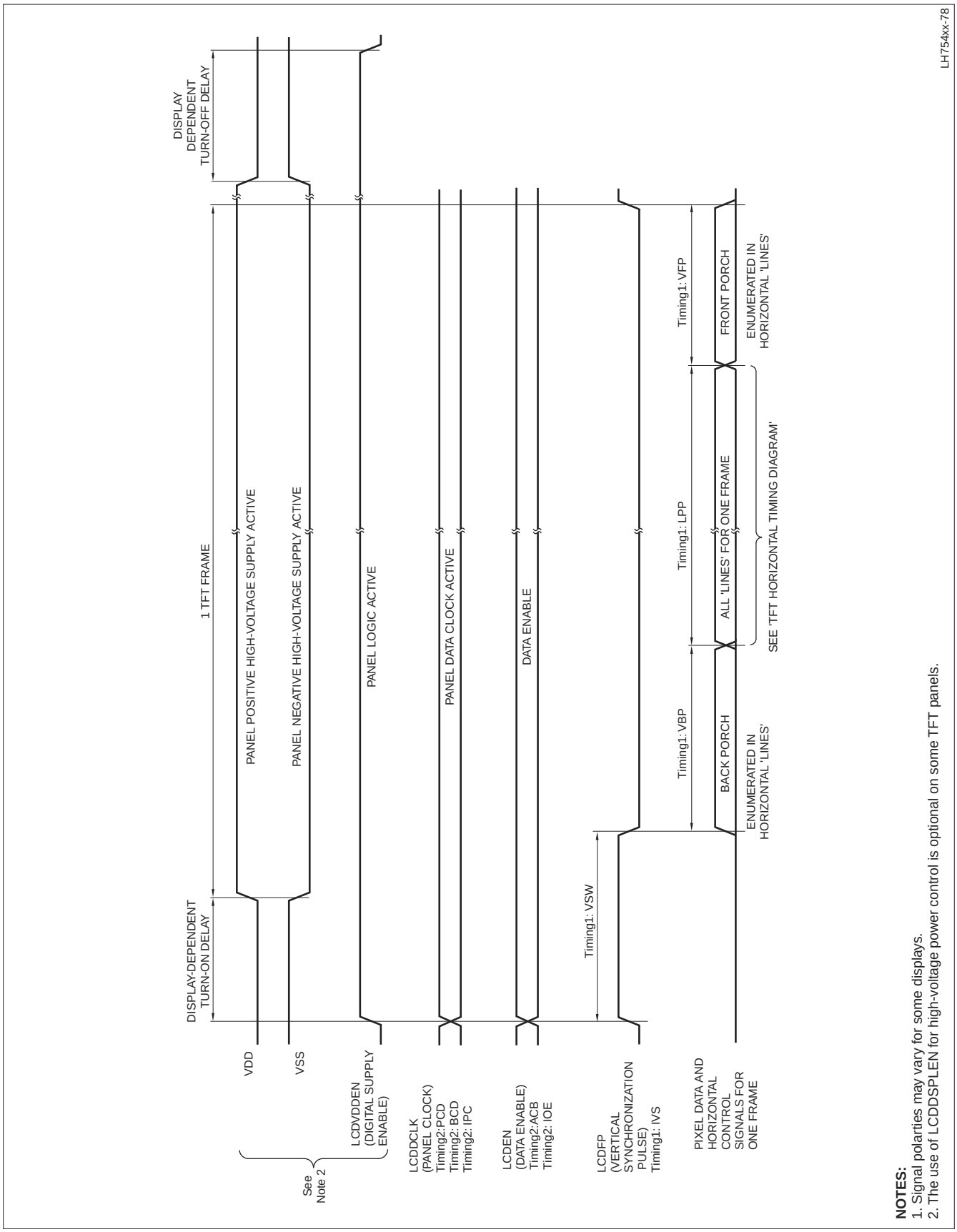
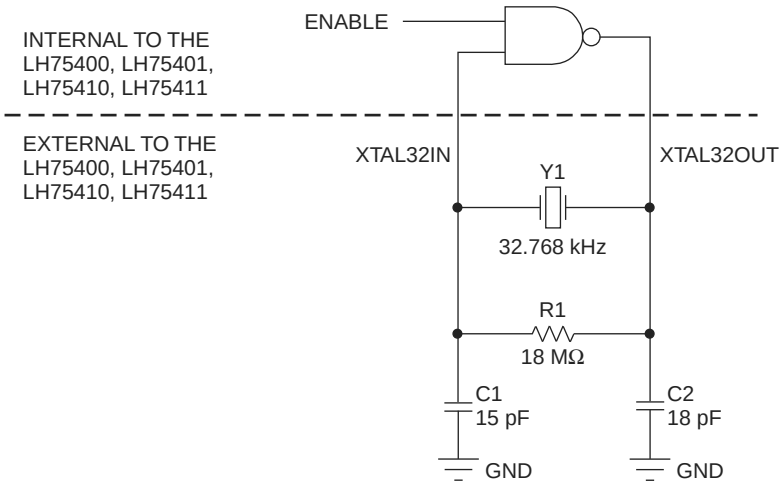


Figure 18. TFT Vertical Timing Diagram

SUGGESTED EXTERNAL COMPONENTS

Figure 21 shows the suggested external components for the 32.768 kHz crystal circuit to be used with the NXP LH75401/LH75411. The NAND gate represents the logic inside the SoC. See the chart for crystal specifics.

Figure 22 shows the suggested external components for the 14.7456 MHz crystal circuit to be used with the NXP LH75401/LH75411. The NAND gate represents the logic inside the SoC. See the chart for crystal specifics.



NOTES:
1. Y1 is a parallel-resonant type crystal. (See table)
2. The nominal values for C1 and C2 shown are for a crystal specified at 12.5 pF load capacitance (CL).
3. The values for C1 and C2 are dependent upon the cystal's specified load capacitance and PCB stray capacitance.
4. R1 must be in the circuit.
5. Ground connections should be short and return to the ground plane which is connected to the processor's core ground pins.
6. Tolerance for R1, C1, C2 is ≤ 5%.

RECOMMENDED CRYSTAL SPECIFICATIONS

PARAMETER	DESCRIPTION
32.768 kHz Crystal	Parallel Mode
Tolerance	±30 ppm
Aging	±3 ppm
Load Capacitance	12.5 pF
ESR (MAX.)	50 kΩ
Drive Level	1.0 μW (MAX.)
Recommended Part	MTRON SX1555 or equivalent

LH754xx-101

Figure 21. Suggested External Components, 32.768 kHz Oscillator