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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	740
Core Size	8-Bit
Speed	12.5MHz
Connectivity	SIO, UART/USART
Peripherals	PWM, WDT
Number of I/O	34
Program Memory Size	48KB (48K x 8)
Program Memory Type	QzROM
EEPROM Size	-
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 9x8b
Oscillator Type	External, Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	42-SOP (0.330", 8.40mm Width)
Supplier Device Package	42-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m38588gcfp-u0

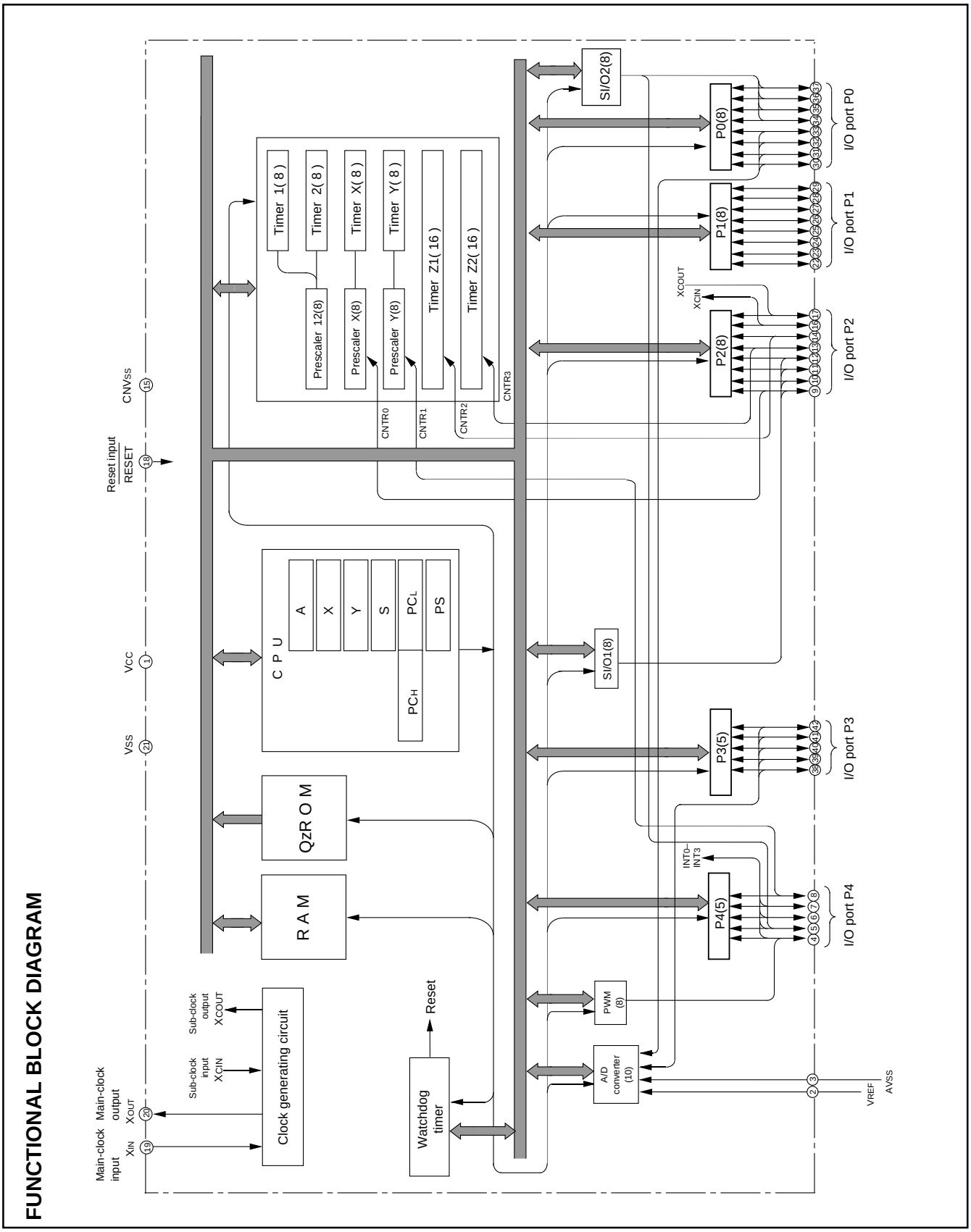


Fig. 2 Functional block diagram

PART NUMBERING

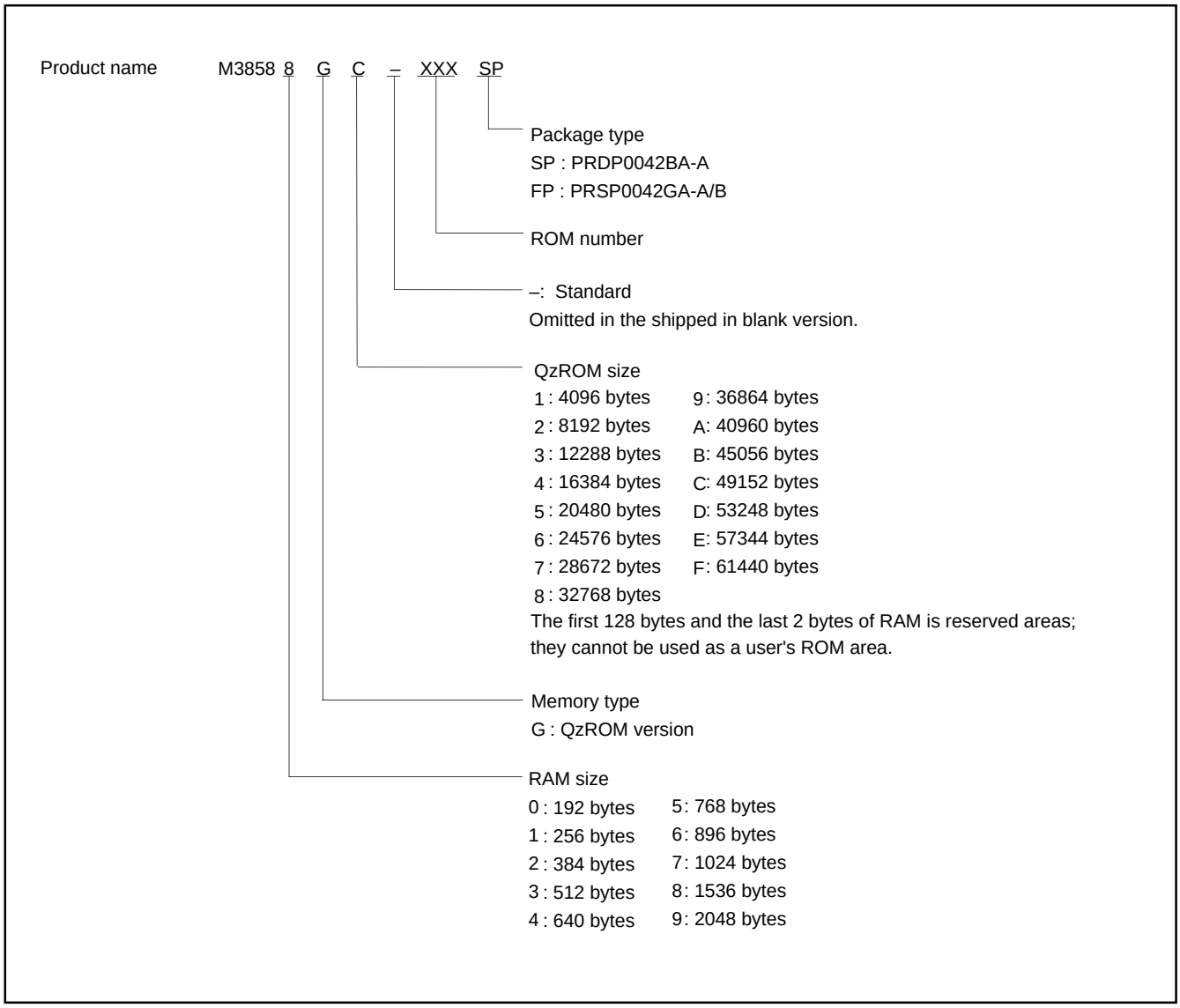


Fig. 3 Part numbering

GROUP EXPANSION

Renesas Technology plans to expand the 3858 group as follows.

Memory Type

Support for QzROM version.

Memory Size

QzROM size ..... 48 K bytes
RAM size ..... 1.5 K bytes

Packages

PRDP0042BA-A ..... 42-pin shrink plastic-molded SDIP
PRSP0042GA-A/B ..... 42-pin plastic-molded SSOP

Memory Expansion Plan

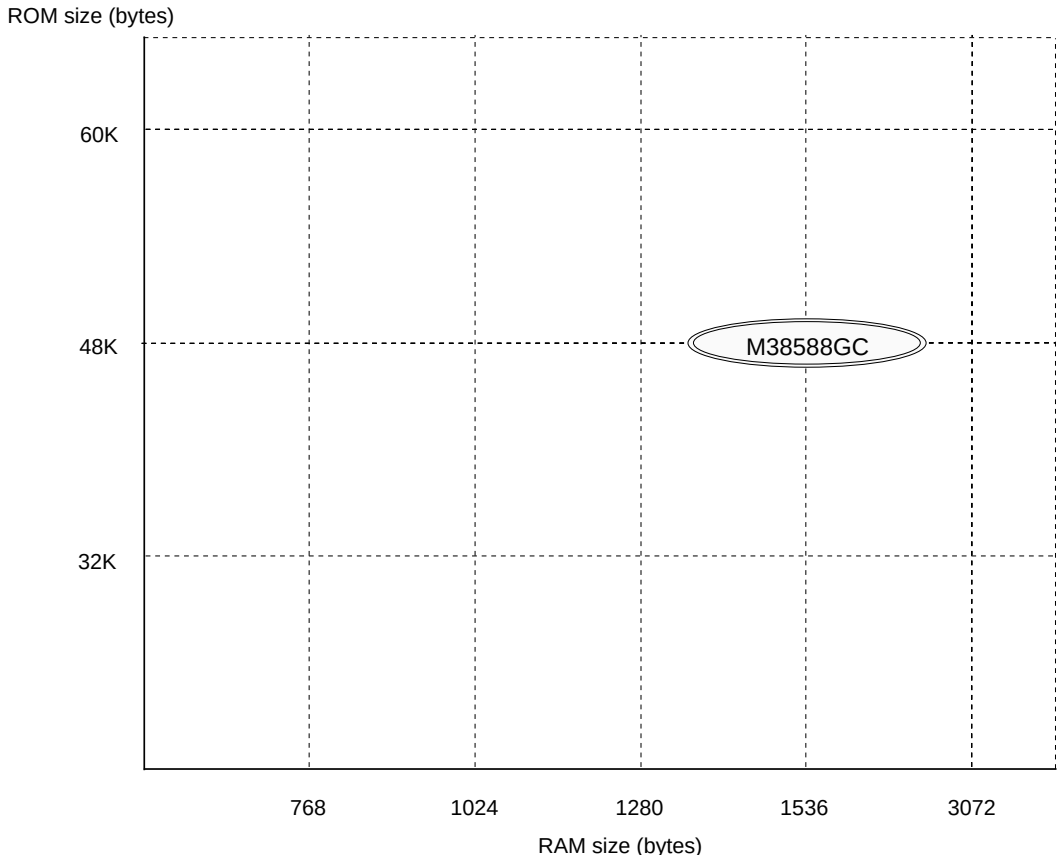


Fig. 4 Memory expansion plan

Table 2 List of products

Part number	ROM size (bytes) ROM size for User in ( )	RAM size (bytes)	Package	Remarks
M38588GC-XXXSP	49152 (49021)	1536	PRDP0042BA-A	
M38588GC-XXXFP			PRSP0042GA-A/B	
M38588GCSP	49152 (49021)	1536	PRDP0042BA-A	Blank
M38588GCFP			PRSP0042GA-A/B	

I/O PORTS

The I/O ports have direction registers which determine the input/output direction of each individual pin. Each bit in a direction register corresponds to one pin, and each pin can be set to be input port or output port.

When "0" is written to the bit corresponding to a pin, that pin becomes an input pin. When "1" is written to that bit, that pin becomes an output pin.

If data is read from a pin which is set to output, the value of the port output latch is read, not the value of the pin itself. Pins set to input are floating. If a pin set to input is written to, only the port output latch is written to and the pin remains floating.

By setting the port P0 pull-up control register (address 0010_{16}), the port P1 pull-up control register (address 0011_{16}), the port P2 pull-up control register (address 0012_{16}), the port P3 pull-up control register (address 0013_{16}), or the port P4 pull-up control register (address 0014_{16}), ports can control pull-up with a program. However, the contents of these registers do not affect ports programmed as the output ports.

Table 5 I/O port function

Pin	Name	Input/Output	I/O Structure	Non-Port Function	Related SFRs	Ref.No.
P0$_0$/SIN$_2$ P0$_1$/SOUT$_2$ P0$_2$/SCLK$_2$ P0$_3$/$\overline{\text{SRDY}_2}$	Port P0	Input/output, individual bits	CMOS compatible input level CMOS 3-state output	Serial I/O2 function I/O	Serial I/O2 control register	(1) (2) (3) (4)
P0$_4$/AN$_5$–P0$_7$AN$_8$				A/D converter input	AD control register AD input selection register	(13)
P1$_0$–P1$_7$	Port P1					(5)
P2$_0$/XCOUT P2$_1$/XCIN	Port P2			Sub-clock generating circuit	CPU mode register	(6) (7)
P2$_2$/CNTR$_2$				Timer Z1 function I/O	Timer Z1 mode register	(8)
P2$_3$/CNTR$_3$				Timer Z2 function I/O	Timer Z2 mode register	(8)
P2$_4$/RxD P2$_5$/TxD P2$_6$/SCLK$_1$				Serial I/O1 function I/O	Serial I/O1 control register	(9) (10) (11)
P2$_7$/CNTR$_0$/$\overline{\text{SRDY}_1}$				Timer X function I/O Serial I/O1 function I/O	Timer XY mode register Serial I/O1 control register	(12)
P3$_0$/AN$_0$– P3$_4$/AN$_4$	Port P3 **(Note)**			A/D converter input	AD control register AD input selection register	(13)
P4$_0$/CNTR$_1$	Port P4 **(Note)**			Timer Y function I/O	Timer XY mode register	(14)
P4$_1$/INT$_0$ P4$_2$/INT$_1$				External interrupt input	Interrupt edge selection register	(15)
P4$_3$/INT$_2$/SCMP$_2$				External interrupt input SCMP$_2$ output	Interrupt edge selection register Serial I/O2 control register	(16)
P4$_4$/INT$_3$/PWM				External interrupt input PWM output	Interrupt edge selection register PWM control register	(17)

Note: When bits 5 to 7 of Ports P3 and P4 are read out, the contents are undefined.

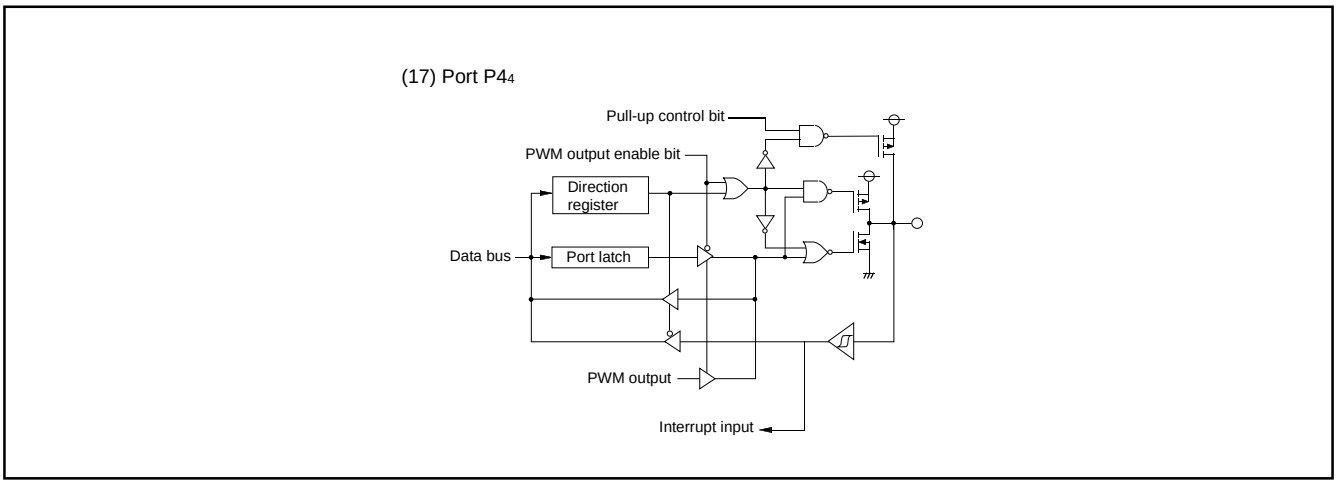
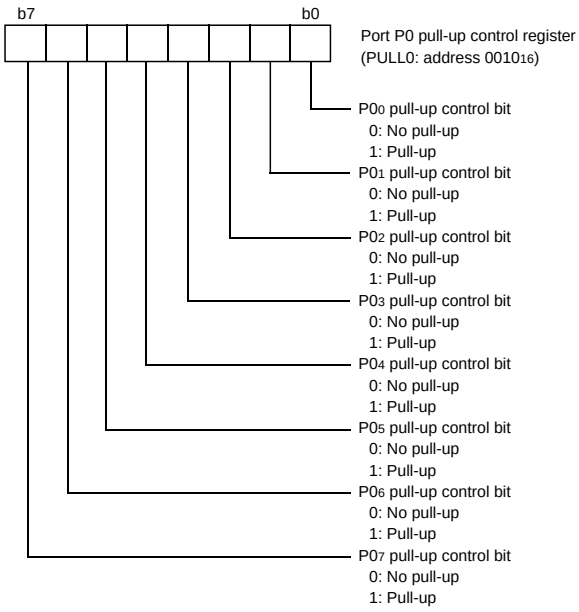
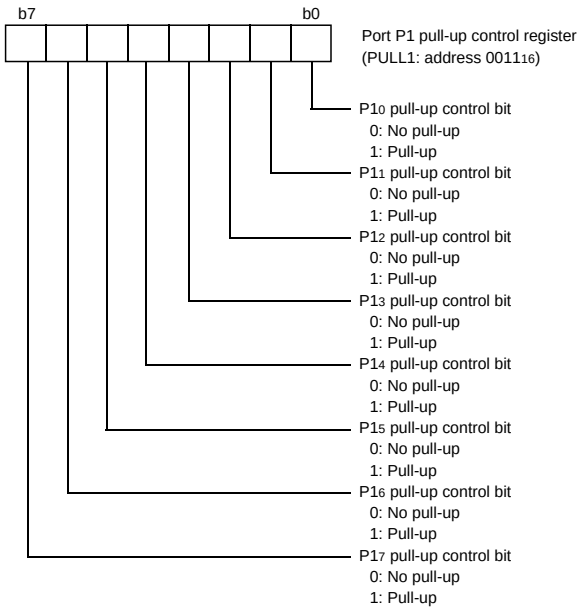


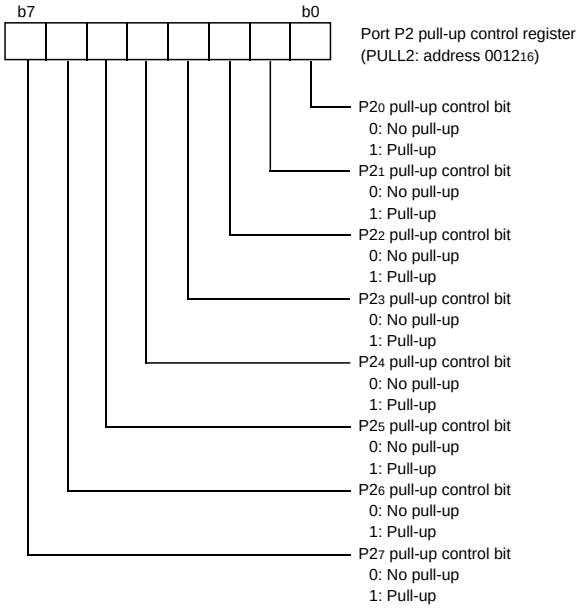
Fig. 12 Port block diagram (3)



Note: Pull-up control is valid when the corresponding bit of the port direction register is "0" (input).
When that bit is "1" (output), pull-up cannot be set to the port of which pull-up is selected.



Note: Pull-up control is valid when the corresponding bit of the port direction register is "0" (input).
When that bit is "1" (output), pull-up cannot be set to the port of which pull-up is selected.



Note: Pull-up control is valid when the corresponding bit of the port direction register is "0" (input).
When that bit is "1" (output), pull-up cannot be set to the port of which pull-up is selected.

Fig. 13 Structure of port registers (1)

TIMERS

●8-bit Timers

The 3858 group has four 8-bit timers: timer 1, timer 2, timer X, and timer Y.

The timer 1 and timer 2 use one prescaler in common, and the timer X and timer Y use each prescaler. Those are 8-bit prescalers. Each of the timers and prescalers has a timer latch or a prescaler latch.

The division ratio of each timer or prescaler is given by 1/(n + 1), where n is the value in the corresponding timer or prescaler latch.

All timers are down-counters. When the timer reaches "00_{16}", an underflow occurs at the next count pulse and the contents of the corresponding timer latch are reloaded into the timer and the count is continued. When the timer underflows, the interrupt request bit corresponding to that timer is set to "1".

●Timer divider

The divider count source is switched by the main clock division ratio selection bits of CPU mode register (bits 7 and 6 at address $003B_{16}$). When these bits are "00" (high-speed mode) or "01" (middle-speed mode), X_{IN} is selected. When these bits are "10" (low-speed mode), X_{CIN} is selected.

●Prescaler 12

The prescaler 12 counts the output of the timer divider. The count source is selected by the timer 12, X count source selection register (address $002E_{16}$) among 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512, 1/1024 of f(X_{IN}) or f(X_{CIN}).

Timer 1 and Timer 2

The timer 1 and timer 2 counts the output of prescaler 12 and periodically set the interrupt request bit.

●Prescaler X and prescaler Y

The prescaler X and prescaler Y count the output of the timer divider or f(X_{CIN}). The count source is selected by the timer 12, X count source selection register (address $002E_{16}$) and the timer Y, Z1 count source selection register (address $002F_{16}$) among 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512, and 1/1024 of f(X_{IN}) or f(X_{CIN}); and f(X_{CIN}).

Timer X and Timer Y

The timer X and timer Y can each select one of four operating modes by setting the timer XY mode register (address 0023_{16}).

(1) Timer mode

●Mode selection

This mode can be selected by setting "00" to the timer X operating mode bits (bits 1 and 0) and the timer Y operating mode bits (bits 5 and 4) of the timer XY mode register (address 0023_{16}).

●Explanation of operation

The timer count operation is started by setting "0" to the timer X count stop bit (bit 3) and the timer Y count stop bit (bit 7) of the timer XY mode register (address 0023_{16}).

When the timer reaches "00_{16}", an underflow occurs at the next count pulse and the contents of timer latch are reloaded into the timer and the count is continued.

(2) Pulse output mode

●Mode selection

This mode can be selected by setting "01" to the timer X operating mode bits (bits 1 and 0) and the timer Y operating mode bits (bits 5 and 4) of the timer XY mode register (address 0023_{16}).

●Explanation of operation

The operation is the same as the timer mode's. Moreover the pulse which is inverted each time the timer underflows is output from $CNTR_0$/$CNTR_1$ pin. Regardless of the timer counting or not the output of $CNTR_0$/$CNTR_1$ pin is initialized to the level of specified by their active edge switch bits when writing to the timer. When the $CNTR_0$ active edge switch bit (bit 2) and the $CNTR_1$ active edge switch bit (bit 6) of the timer XY mode register (address 0023_{16}) is "0", the output starts with "H" level. When it is "1", the output starts with "L" level.

Switching the $CNTR_0$ or $CNTR_1$ active edge switch bit will reverse the output level of the corresponding $CNTR_0$ or CNTR1 pin.

■Precautions

Set the double-function port of $CNTR_0$/$CNTR_1$ pin and port $P2_7$/$P4_0$ to output in this mode.

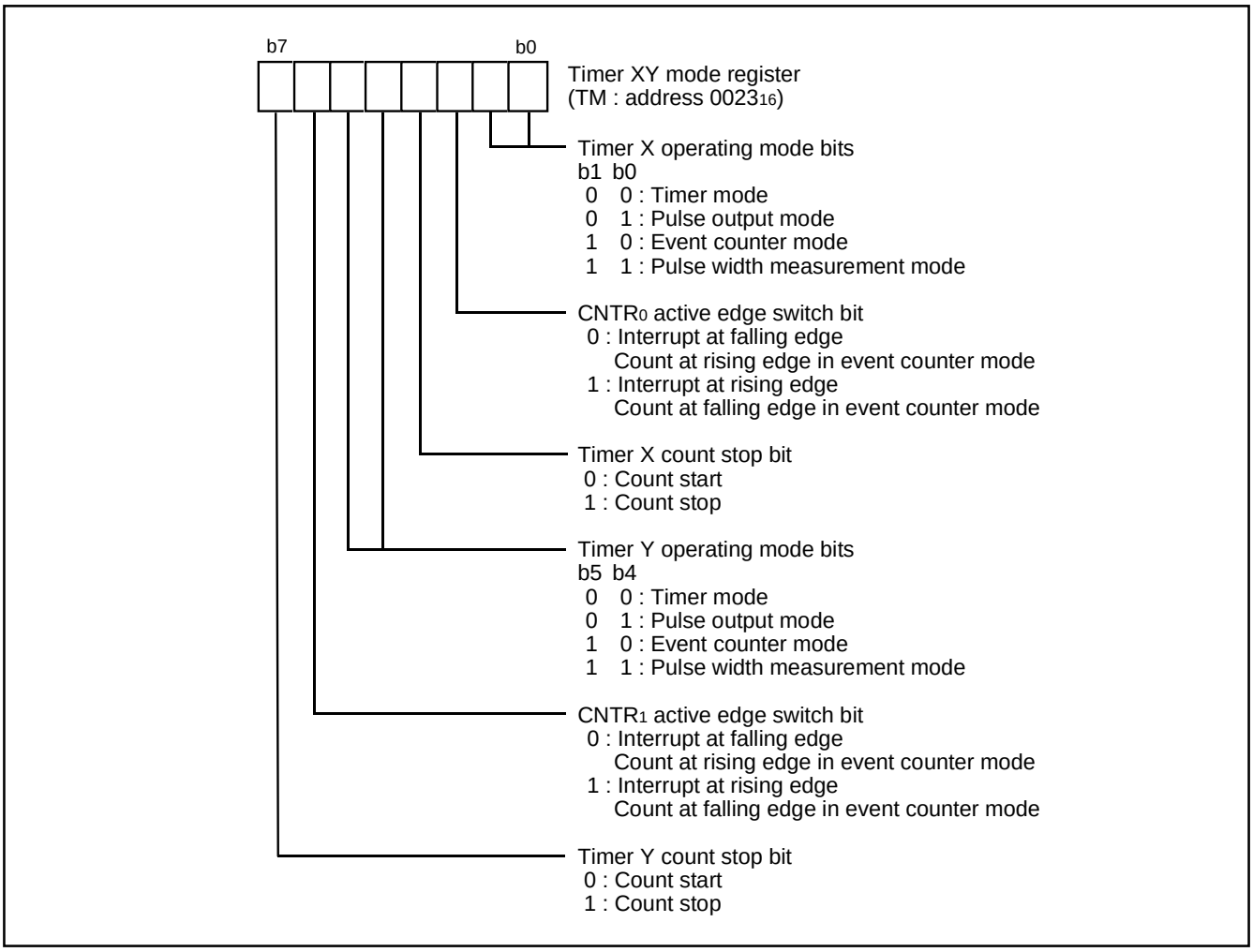


Fig. 18 Structure of timer XY mode register

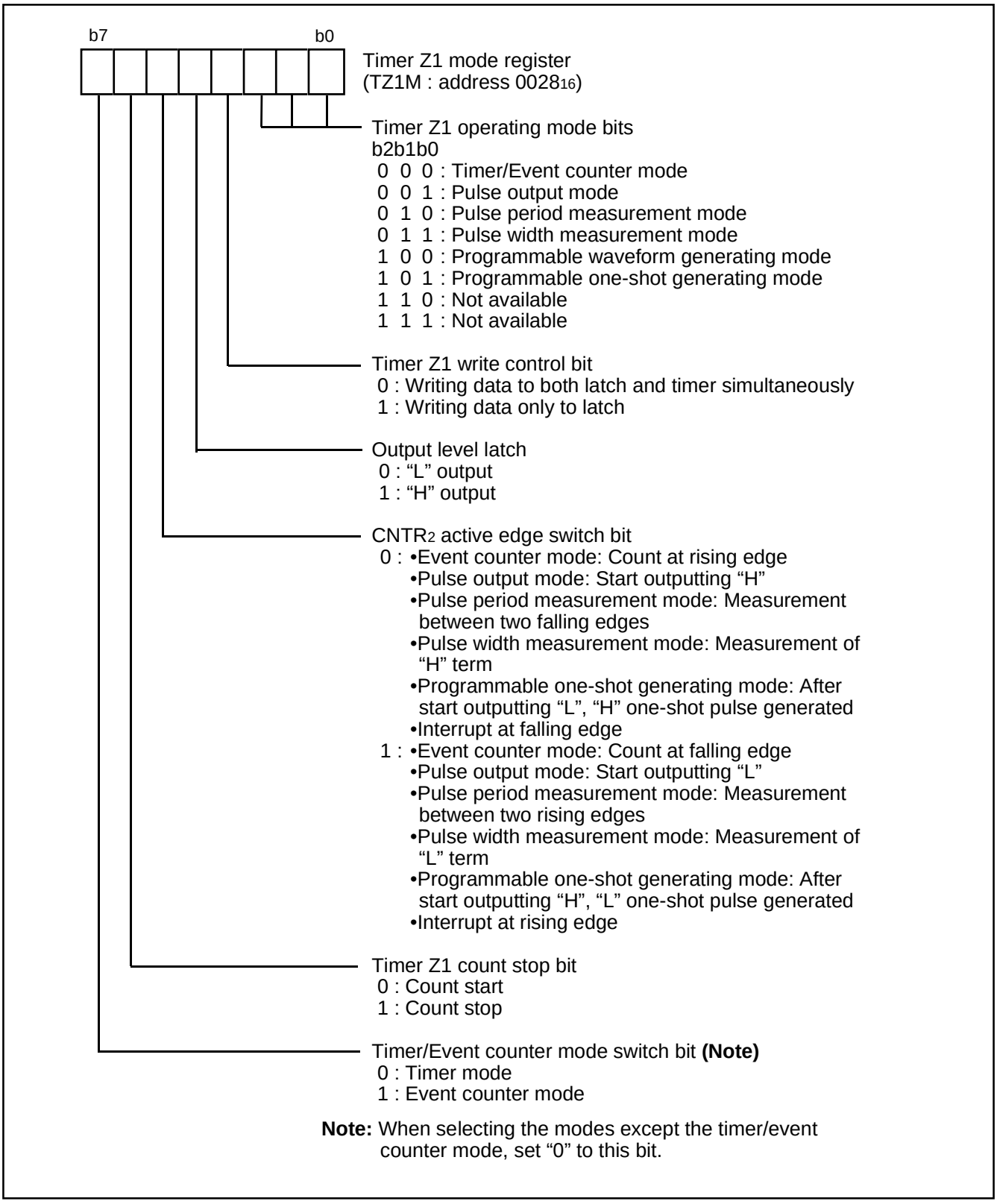
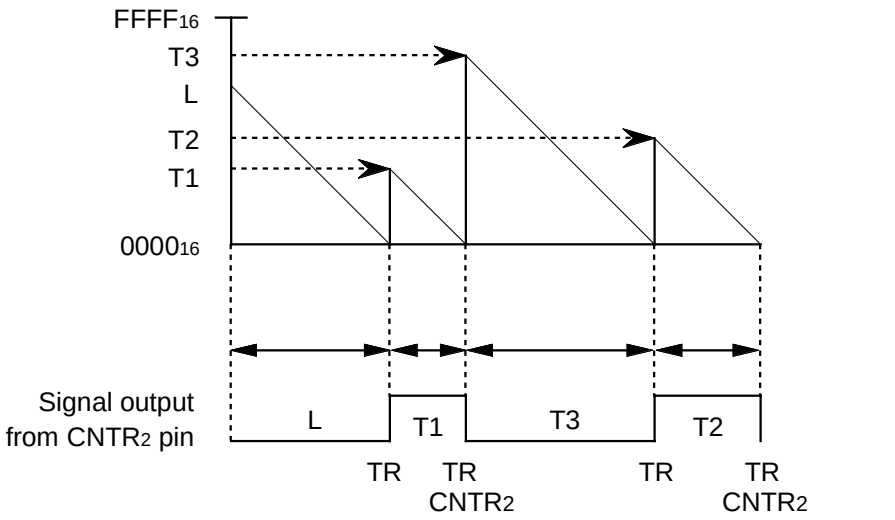
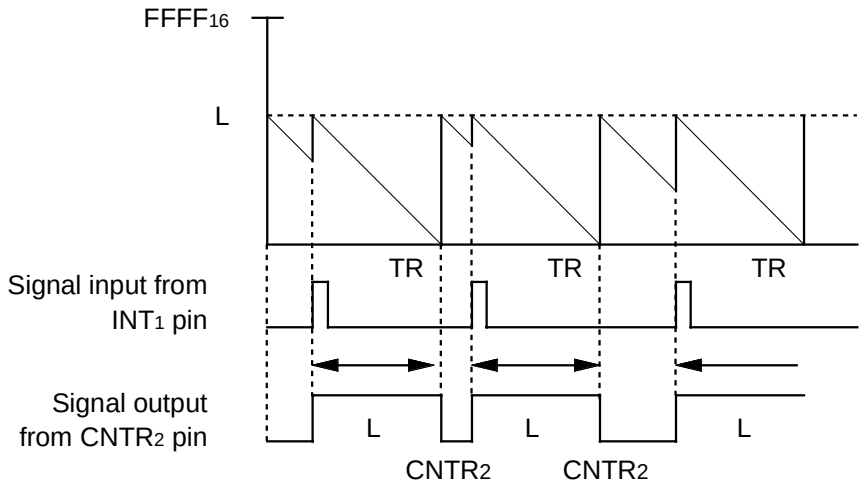


Fig. 21 Structure of timer Z1 mode register



L : Timer initial value
TR : Timer interrupt request
CNTR2 : CNTR2 interrupt request
(CNTR2 active edge switch bit = “0”; Falling edge active)

Fig. 26 Timing chart of programmable waveform generating mode



L : One-shot pulse width
TR : Timer interrupt request
CNTR2 : CNTR2 interrupt request
(CNTR2 active edge switch bit = “0”; Falling edge active)

Fig. 27 Timing chart of programmable one-shot generating mode (“H” one-shot pulse generating)

(4) Pulse period measurement mode

●Mode selection

This mode can be selected by setting “010” to the timer Z2 operating mode bits (bits 2 to 0) and setting “0” to the timer/event counter mode switch bit (b7) of the timer Z2 mode register (address $002B_{16}$).

●Count source selection

In high-, or middle-speed mode, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 or 1/1024 of f(XIN); or f(XCIN) can be selected as the count source.

In low-speed mode, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 or 1/1024 of f(XCIN); or f(XCIN) can be selected as the count source.

●Interrupt

The interrupt at an underflow is the same as the timer mode’s. When the pulse period measurement is completed, the timer Z2/CNTR3 interrupt request bit (bit 1) of the interrupt request register 1 (address $003C_{16}$) is set to “1”.

●Explanation of operation

The cycle of the pulse which is input from the CNTR3 pin is measured. When the CNTR3 active edge switch bit (bit 5) of the timer Z2 mode register (address $002B_{16}$) is “0”, the timer counts during the term from one falling edge of CNTR3 pin input to the next falling edge. When it is “1”, the timer counts during the term from one rising edge input to the next rising edge input.

When the valid edge of measurement completion/start is detected, the 1’s complement of the timer value is written to the timer latch and “$FFFF_{16}$” is set to the timer.

Furthermore when the timer underflows, the timer Z2 interrupt request occurs and “$FFFF_{16}$” is set to the timer. When reading the timer Z2, the value of the timer latch (measured value) is read. The measured value is retained until the next measurement completion.

■Precautions

Set the double-function port of CNTR3 pin and port P23 to input in this mode.

A read-out of timer value is impossible in this mode. The timer can be written to only during timer stop (no measurement of pulse period).

Since the timer latch in this mode is specialized for the read-out of measured values, do not perform any write operation during measurement.

“$FFFF_{16}$” is set to the timer when the timer underflows or when the valid edge of measurement start/completion is detected. Consequently, the timer value at start of pulse period measurement depends on the timer value just before measurement start.

Figure 32 shows the timing chart of the pulse period measurement mode.

(5) Pulse width measurement mode

●Mode selection

This mode can be selected by setting “011” to the timer Z2 operating mode bits (bits 2 to 0) and setting “0” to the timer/event counter mode switch bit (b7) of the timer Z2 mode register (address $002B_{16}$).

●Count source selection

In high-, or middle-speed mode, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 or 1/1024 of f(XIN); or f(XCIN) can be selected as the count source.

In low-speed mode, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 or 1/1024 of f(XCIN); or f(XCIN) can be selected as the count source.

●Interrupt

The interrupt at an underflow is the same as the timer mode’s. When the pulse widths measurement is completed, the timer Z2/CNTR3 interrupt request bit (bit 1) of the interrupt request register 1 (address $003C_{16}$) is set to “1”.

●Explanation of operation

The pulse width which is input from the CNTR3 pin is measured. When the CNTR3 active edge switch bit (bit 5) of the timer Z2 mode register (address $002B_{16}$) is “0”, the timer counts during the term from one rising edge input to the next falling edge input (“H” term). When it is “1”, the timer counts during the term from one falling edge of CNTR3 pin input to the next rising edge of input (“L” term).

When the valid edge of measurement completion is detected, the 1’s complement of the timer value is written to the timer latch.

When the valid edge of measurement completion/start is detected, “$FFFF_{16}$” is set to the timer.

When the timer Z2 underflows, the timer Z2 interrupt occurs and “$FFFF_{16}$” is set to the timer Z2. When reading the timer Z2, the value of the timer latch (measured value) is read. The measured value is retained until the next measurement completion.

■Precautions

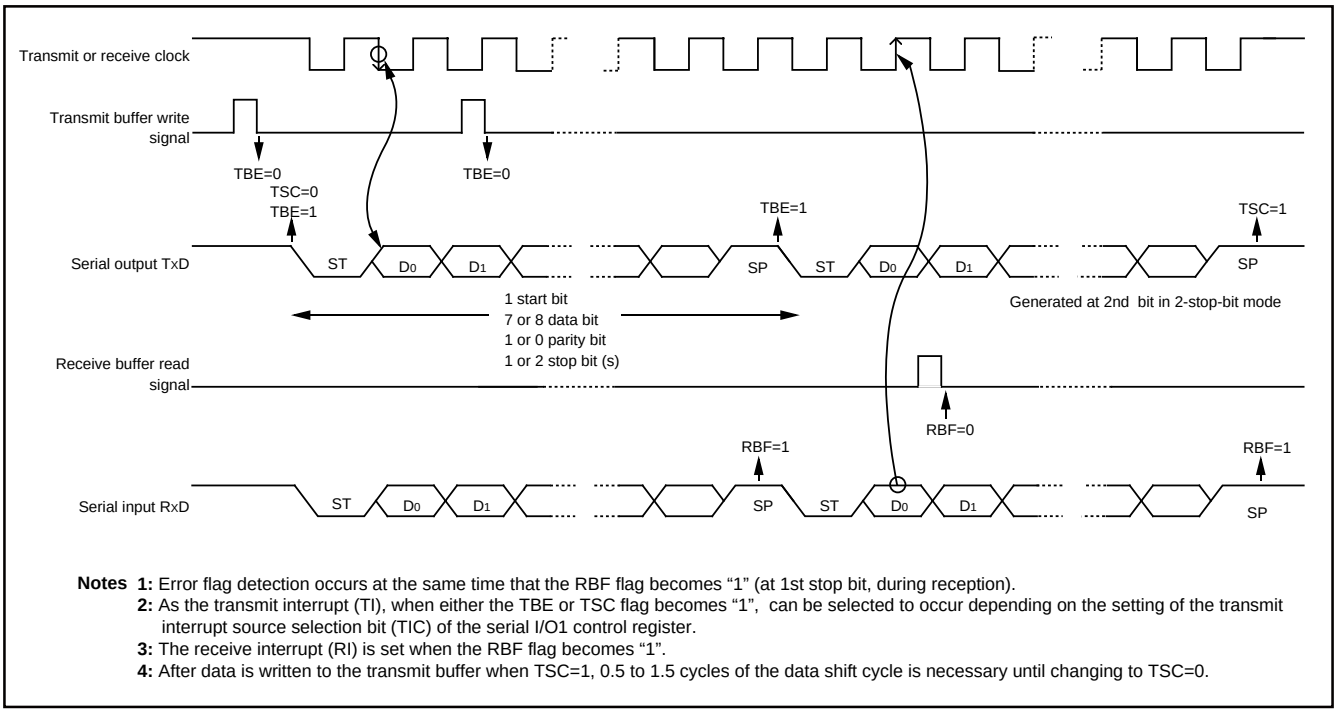
Set the double-function port of CNTR3 pin and port P23 to input in this mode.

A read-out of timer value is impossible in this mode. The timer can be written to only during timer stop (no measurement of pulse widths).

Since the timer latch in this mode is specialized for the read-out of measured values, do not perform any write operation during measurement.

“$FFFF_{16}$” is set to the timer when the timer underflows or when the valid edge of measurement start/completion is detected. Consequently, the timer value at start of pulse width measurement depends on the timer value just before measurement start.

Figure 33 shows the timing chart of the pulse width measurement mode.



Notes
1: Error flag detection occurs at the same time that the RBF flag becomes “1” (at 1st stop bit, during reception).
2: As the transmit interrupt (TI), when either the TBE or TSC flag becomes “1”, can be selected to occur depending on the setting of the transmit interrupt source selection bit (TIC) of the serial I/O1 control register.
3: The receive interrupt (RI) is set when the RBF flag becomes “1”.
4: After data is written to the transmit buffer when TSC=1, 0.5 to 1.5 cycles of the data shift cycle is necessary until changing to TSC=0.

Fig. 39 Operation of UART serial I/O1 function

[Transmit Buffer Register/Receive Buffer Register (TB/RB)] 0018$_{16}$

The transmit buffer register and the receive buffer register are located at the same address. The transmit buffer is write-only and the receive buffer is read-only. If a character bit length is 7 bits, the MSB of data stored in the receive buffer is “0”.

[Serial I/O1 Status Register (SIOSTS)] 0019$_{16}$

The read-only serial I/O1 status register consists of seven flags (bits 0 to 6) which indicate the operating status of the serial I/O1 function and various errors.

Three of the flags (bits 4 to 6) are valid only in UART mode.

The receive buffer full flag (bit 1) is cleared to “0” when the receive buffer register is read.

If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer register, and the receive buffer full flag is set. A write to the serial I/O1 status register clears all the error flags OE, PE, FE, and SE (bit 3 to bit 6, respectively). Writing “0” to the serial I/O1 enable bit SIOE (bit 7 of the serial I/O1 control register) also clears all the status flags, including the error flags.

Bits 0 to 6 of the serial I/O1 status register are initialized to “0” at reset, but if the transmit enable bit (bit 4) of the serial I/O1 control register has been set to “1”, the transmit shift completion flag (bit 2) and the transmit buffer empty flag (bit 0) become “1”.

[Serial I/O1 Control Register (SIOCON)] 001A$_{16}$

The serial I/O1 control register consists of eight control bits for the serial I/O1 function.

[UART Control Register (UARTCON)] 001B$_{16}$

The UART control register consists of four control bits (bits 0 to 3) which are valid when asynchronous serial I/O is selected and set the data format of an data transfer and one bit (bit 4) which is always valid and sets the output structure of the P25/TxD pin.

[Baud Rate Generator (BRG)] 001C$_{16}$

The baud rate generator determines the baud rate for serial transfer.

The baud rate generator divides the frequency of the count source by 1/(n + 1), where n is the value written to the baud rate generator.

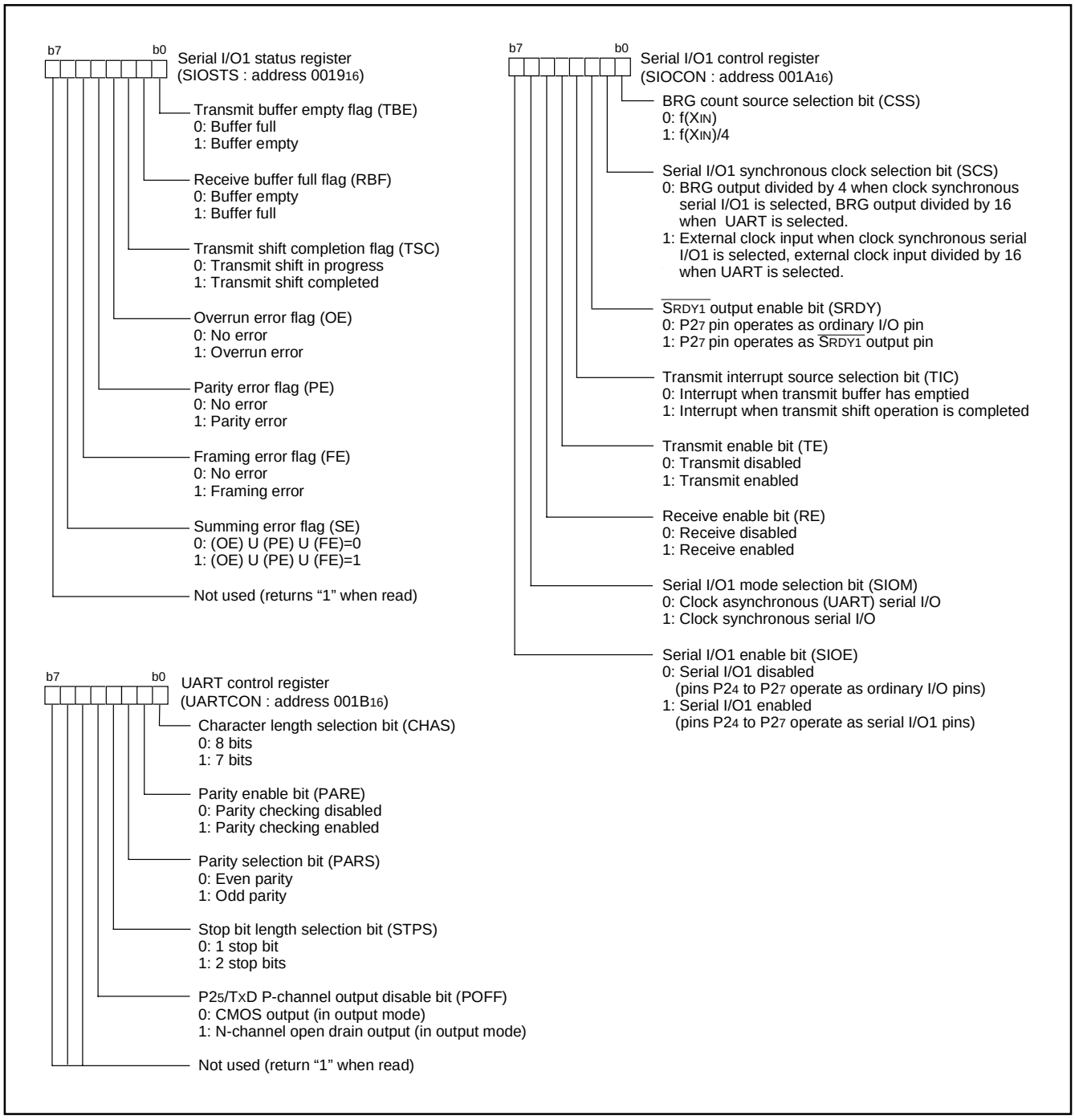
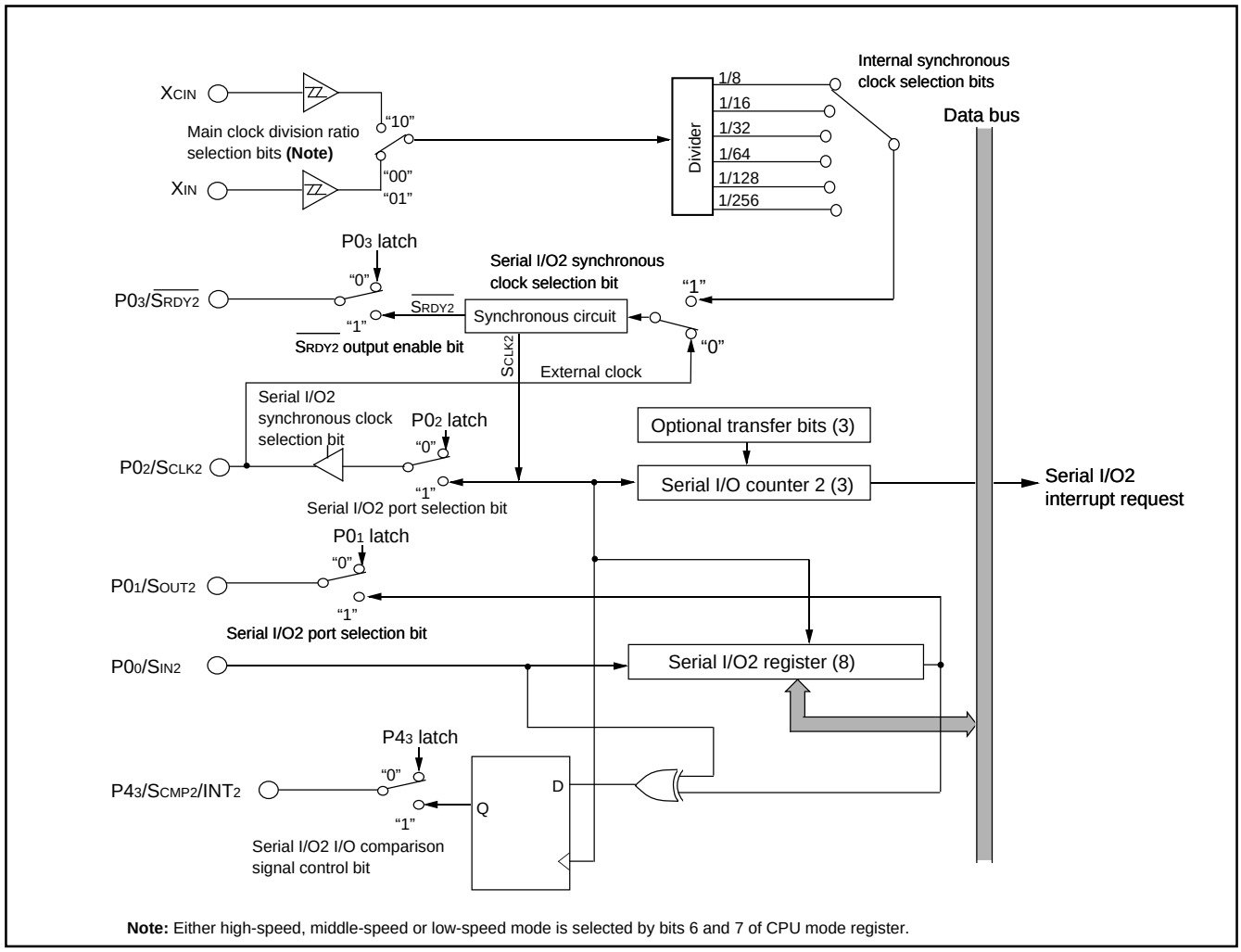


Fig. 40 Structure of serial I/O1 control registers

■Notes on serial interface

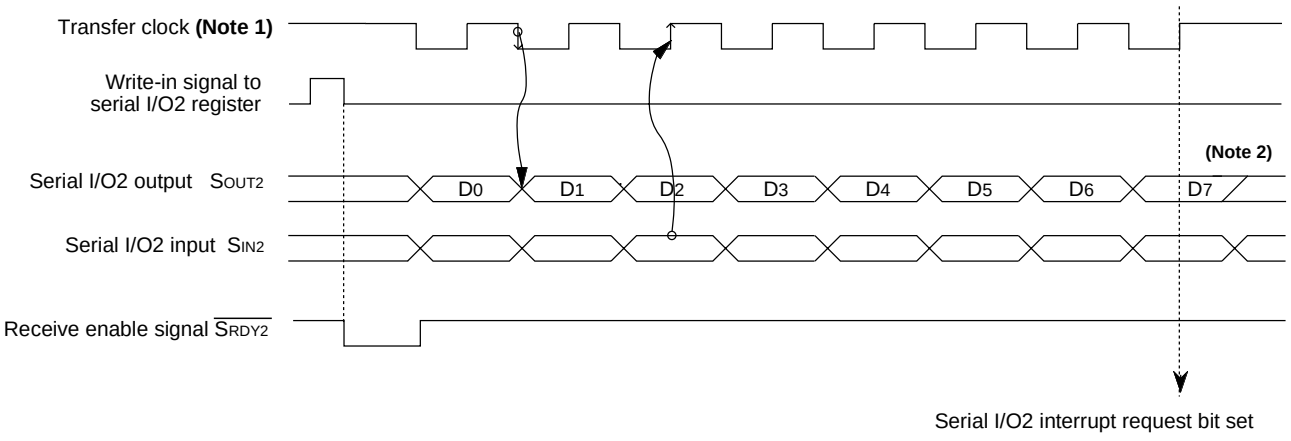
When setting the transmit enable bit of serial I/O1 to “1”, the serial I/O1 transmit interrupt request bit is automatically set to “1”. When not requiring the interrupt occurrence synchronized with the transmission enabled, take the following sequence.

(1) Set the serial I/O1 transmit interrupt enable bit to “0” (disabled).
(2) Set the transmit enable bit to “1”.
(3) Set the serial I/O1 transmit interrupt request bit to “0” after 1 or more instructions have been executed.
(4) Set the serial I/O1 transmit interrupt enable bit to “1” (enabled).



Note: Either high-speed, middle-speed or low-speed mode is selected by bits 6 and 7 of CPU mode register.

Fig. 42 Block diagram of Serial I/O2



Notes 1: When the internal clock is selected as a transfer clock, the f(XIN) clock division (f(XCIN) in low-speed mode) can be selected by setting bits 0 to 2 of serial I/O2 control register 1.
2: When the internal clock is selected as a transfer clock, the SOUT2 pin has high impedance after transfer completion.

Fig. 43 Timing chart of Serial I/O2

WATCHDOG TIMER

The watchdog timer gives a mean of returning to the reset status when a program cannot run on a normal loop (for example, because of a software run-away). The watchdog timer consists of an 8-bit watchdog timer L and an 8-bit watchdog timer H.

Initial Value of Watchdog Timer

At reset or writing to the watchdog timer control register (address 0039_{16}), each of watchdog timer H and L is set to "FF_{16}". Any instruction which generates a write signal such as the instructions of STA, LDM, CLB and others can be used to write. The data of bits 6 and 7 are only valid when writing to the watchdog timer control register. Each of watchdog timer is set to "FF_{16}" regardless of the written data of bits 0 to 5.

Bit 6 can be written to only once after reset release. After this bit is written, it cannot rewritten because it is locked.

Operation of Watchdog Timer

The watchdog timer stops at reset and starts to count down by writing to the watchdog timer control register. An internal reset occurs at an underflow of the watchdog timer H. The reset is released after waiting for a reset release time and the program is processed from the reset vector address. Accordingly, programming is usually performed so that writing to the watchdog timer control register may be started before an underflow of the watchdog timer H. If writing to the watchdog timer control register is not performed once, the watchdog timer does not function.

Bit 6 of Watchdog Timer Control Register

When bit 6 of the watchdog timer control register is "0", the MCU enters the stop mode by execution of STP instruction. Just after releasing the stop mode, the watchdog timer restarts counting (Note). When executing the WIT instruction, the watchdog timer does not stop.

When bit 6 is "1", execution of STP instruction causes an internal reset. When this bit is set to "1" once, it cannot be rewritten to "0" by program. Bit 6 is "0" at reset.

The necessary time after writing to the watchdog timer control register to an underflow of the watchdog timer H is shown as follows.

When bit 7 of the watchdog timer control register is "0":

32 s at X_{CIN} = 32.768 kHz frequency and

131.072 ms at X_{IN} = 8 MHz frequency.

When bit 7 of the watchdog timer control register is "1":

125 ms at X_{CIN} = 32.768 kHz frequency and

512 µs at X_{IN} = 8 MHz frequency.

Note: The watchdog timer continues to count for waiting for a stop mode release time. Do not generate an underflow of the watchdog timer H during that time.

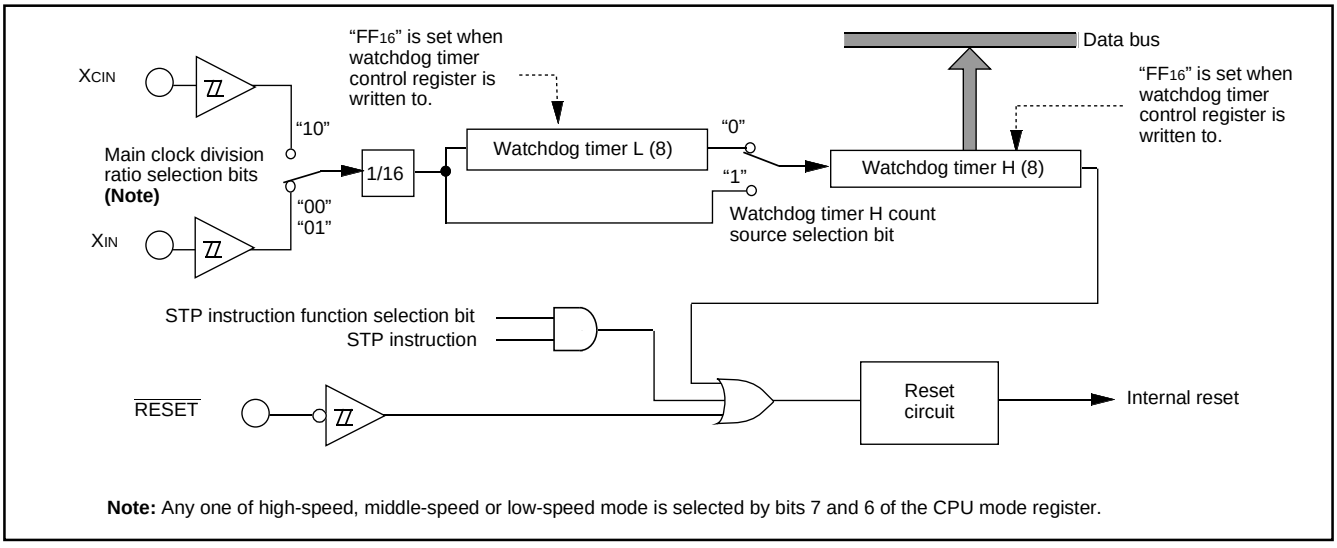


Fig. 51 Block diagram of Watchdog timer

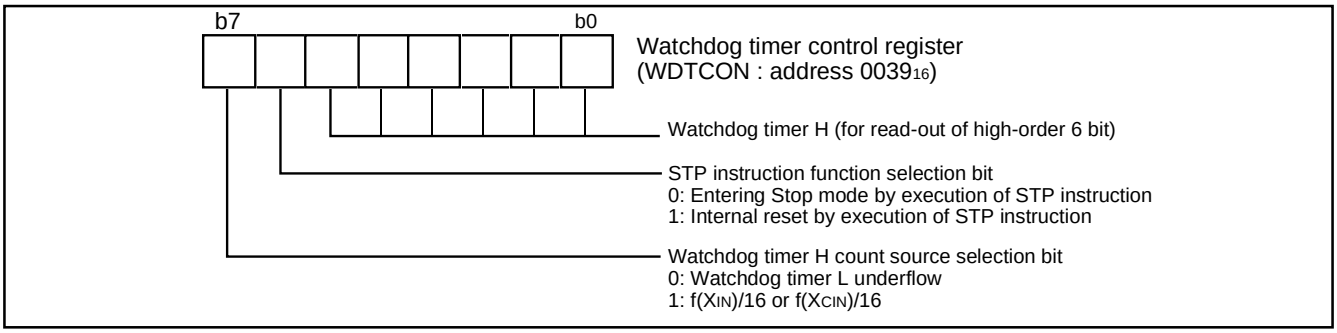


Fig. 52 Structure of Watchdog timer control register

		Address	Register contents
(1)	Port P0 (P0)	0000_{16}	00_{16}
(2)	Port P0 direction register (P0D)	0001_{16}	00_{16}
(3)	Port P1 (P1)	0002_{16}	00_{16}
(4)	Port P1 direction register (P1D)	0003_{16}	00_{16}
(5)	Port P2 (P2)	0004_{16}	00_{16}
(6)	Port P2 direction register (P2D)	0005_{16}	00_{16}
(7)	Port P3 (P3)	0006_{16}	00_{16}
(8)	Port P3 direction register (P3D)	0007_{16}	00_{16}
(9)	Port P4 (P4)	0008_{16}	00_{16}
(10)	Port P4 direction register (P4D)	0009_{16}	00_{16}
(11)	Port P0 pull-up control register (PULL0)	0010_{16}	00_{16}
(12)	Port P1 pull-up control register (PULL1)	0011_{16}	00_{16}
(13)	Port P2 pull-up control register (PULL2)	0012_{16}	00_{16}
(14)	Port P3 pull-up control register (PULL3)	0013_{16}	00_{16}
(15)	Port P4 pull-up control register (PULL4)	0014_{16}	00_{16}
(16)	Serial I/O2 control register 1 (SIO2CON1)	0015_{16}	00_{16}
(17)	Serial I/O2 control register 2 (SIO2CON2)	0016_{16}	0 0 0 0 0 1 1 1
(18)	Serial I/O2 register (SIO2)	0017_{16}	X X X X X X X X
(19)	Transmit/Receive buffer register (TB/RB)	0018_{16}	X X X X X X X X
(20)	Serial I/O1 status register (SIOSTS)	0019_{16}	1 0 0 0 0 0 0 0
(21)	Serial I/O1 control register (SIOCON)	$001A_{16}$	00_{16}
(22)	UART control register (UARTCON)	$001B_{16}$	1 1 1 0 0 0 0 0
(23)	Baud rate generator (BRG)	$001C_{16}$	X X X X X X X X
(24)	PWM control register (PWMCON)	$001D_{16}$	00_{16}
(25)	PWM prescaler (PREPWM)	$001E_{16}$	X X X X X X X X
(26)	PWM register (PWM)	$001F_{16}$	X X X X X X X X
(27)	Prescaler 12 (PRE12)	0020_{16}	FF_{16}
(28)	Timer 1 (T1)	0021_{16}	01_{16}
(29)	Timer 2 (T2)	0022_{16}	FF_{16}
(30)	Timer XY mode register (TM)	0023_{16}	00_{16}
(31)	Prescaler X (PREX)	0024_{16}	FF_{16}
(32)	Timer X (TX)	0025_{16}	FF_{16}
(33)	Prescaler Y (PREY)	0026_{16}	FF_{16}
(34)	Timer Y (TY)	0027_{16}	FF_{16}

		Address	Register contents
(35)	Timer Z1 mode register (TZ1M)	0028_{16}	00_{16}
(36)	Timer Z1 low-order (TZ1L)	0029_{16}	FF_{16}
(37)	Timer Z1 high-order (TZ1H)	$002A_{16}$	FF_{16}
(38)	Timer Z2 mode register (TZ2M)	$002B_{16}$	00_{16}
(39)	Timer Z2 low-order (TZ2L)	$002C_{16}$	FF_{16}
(40)	Timer Z2 high-order (TZ2H)	$002D_{16}$	FF_{16}
(41)	Timer 12, X count source selection register (T12XCSS)	$002E_{16}$	0 0 1 1 0 0 1 1
(42)	Timer Y, Z1 count source selection register (TYZ1CSS)	$002F_{16}$	0 0 1 1 0 0 1 1
(43)	Timer Z2 count source selection register (TZ2CSS)	0030_{16}	0 0 0 0 0 0 1 1
(44)	AD control register (ADCON)	0034_{16}	0 0 0 1 0 0 0 0
(45)	AD conversion register (AD)	0035_{16}	X X X X X X X X
(46)	Interrupt source selection register (INTSEL)	0036_{16}	00_{16}
(47)	MISRG	0038_{16}	00_{16}
(48)	Watchdog timer control register (WDTCON)	0039_{16}	0 0 1 1 1 1 1 1
(49)	Interrupt edge selection register (INTEDGE)	$003A_{16}$	00_{16}
(50)	CPU mode register (CPUM)	$003B_{16}$	0 1 0 0 1 0 0 0
(51)	Interrupt request register 1 (IREQ1)	$003C_{16}$	00_{16}
(52)	Interrupt request register 2 (IREQ2)	$003D_{16}$	00_{16}
(53)	Interrupt control register 1 (ICON1)	$003E_{16}$	00_{16}
(54)	Interrupt control register 2 (ICON2)	$003F_{16}$	00_{16}
	Processor status register	(PS)	X X X X X 1 X X
	Program counter	(PC_H)	$FFFD_{16}$ contents
		(PC_L)	$FFFC_{16}$ contents

Note : X : Not fixed
Since the initial values for other than above mentioned registers and RAM contents are indefinite at reset, they must be set.

Fig. 55 Internal status at reset

Electrical characteristics

Absolute maximum ratings

Table 7 Absolute maximum ratings

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power source voltage	All voltages are based on V_{SS}.	–0.3 to 6.5	V
V_I	Input voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$, $P2_1$, $P2_4$–$P2_7$, $P3_0$–$P3_4$, $P4_0$–$P4_4$, V_{REF}	When an input voltage is measured, output transistors are cut off.	–0.3 to V_{CC} +0.3	V
V_I	Input voltage $P2_2$, $P2_3$		–0.3 to V_{CC} +0.3	V
V_I	Input voltage $\overline{RESET}$, X_{IN}		–0.3 to V_{CC} +0.3	V
V_I	Input voltage CNV$_{SS}$		–0.3 to 8.0	V
V_O	Output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$, $P2_1$, $P2_4$–$P2_7$, $P3_0$–$P3_4$, $P4_0$–$P4_4$, X_{OUT}		–0.3 to V_{CC} +0.3	V
V_O	Output voltage $P2_2$, $P2_3$		–0.3 to 5.8	V
P_d	Power dissipation	T_a = 25 °C	1000 **(Note)**	mW
T_{opr}	Operating temperature	–	–20 to 85	°C
T_{stg}	Storage temperature	–	–40 to 125	°C

Note : The rating becomes 300mW at the PRSP0042GA-A/B (42P2R-A/E) package.

Timing requirements

Table 12 Timing requirements (1)

(Vcc = 4.0 to 5.5 V, Vss = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
tw($\overline{\text{RESET}}$)	Reset input “L” pulse width	20			XIN cycle
tc(XIN)	External clock input cycle time	80			ns
twH(XIN)	External clock input “H” pulse width	32			ns
twL(XIN)	External clock input “L” pulse width	32			ns
tc(CNTR)	CNTR0, CNTR1 input cycle time	200			ns
twH(CNTR)	CNTR0, CNTR1 input “H” pulse width	80			ns
twL(CNTR)	CNTR0, CNTR1 input “L” pulse width	80			ns
twH(INT)	INT0 to INT3 input “H” pulse width	80			ns
twL(INT)	INT0 to INT3 input “L” pulse width	80			ns
tc(SCLK1)	Serial I/O1 clock input cycle time **(Note)**	800			ns
twH(SCLK1)	Serial I/O1 clock input “H” pulse width **(Note)**	370			ns
twL(SCLK1)	Serial I/O1 clock input “L” pulse width **(Note)**	370			ns
tsu(RxD-SCLK1)	Serial I/O1 input setup time	220			ns
th(SCLK1-RxD)	Serial I/O1 input hold time	100			ns
tc(SCLK2)	Serial I/O2 clock input cycle time	1000			ns
twH(SCLK2)	Serial I/O2 clock input “H” pulse width	400			ns
twL(SCLK2)	Serial I/O2 clock input “L” pulse width	400			ns
tsu(SIN2-SCLK2)	Serial I/O2 clock input setup time	200			ns
th(SCLK2-SIN2)	Serial I/O2 clock input hold time	200			ns

Note : When f(XIN) = 8 MHz and bit 6 of address 001A16 is “1” (clock synchronous).
Divide this value by four when f(XIN) = 8 MHz and bit 6 of address 001A16 is “0” (UART).

Table13 Timing requirements (2)

(Vcc = 2.7 to 5.5 V, Vss = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
tw($\overline{\text{RESET}}$)	Reset input “L” pulse width	20			XIN cycle
tc(XIN)	External clock input cycle time	166			ns
twH(XIN)	External clock input “H” pulse width	66			ns
twL(XIN)	External clock input “L” pulse width	66			ns
tc(CNTR)	CNTR0, CNTR1 input cycle time	500			ns
twH(CNTR)	CNTR0, CNTR1 input “H” pulse width	230			ns
twL(CNTR)	CNTR0, CNTR1 input “L” pulse width	230			ns
twH(INT)	INT0 to INT3 input “H” pulse width	230			ns
twL(INT)	INT0 to INT3 input “L” pulse width	230			ns
tc(SCLK1)	Serial I/O1 clock input cycle time **(Note)**	2000			ns
twH(SCLK1)	Serial I/O1 clock input “H” pulse width **(Note)**	950			ns
twL(SCLK1)	Serial I/O1 clock input “L” pulse width **(Note)**	950			ns
tsu(RxD-SCLK1)	Serial I/O1 input setup time	400			ns
th(SCLK1-RxD)	Serial I/O1 input hold time	200			ns
tc(SCLK2)	Serial I/O2 clock input cycle time	2000			ns
twH(SCLK2)	Serial I/O2 clock input “H” pulse width	950			ns
twL(SCLK2)	Serial I/O2 clock input “L” pulse width	950			ns
tsu(SIN2-SCLK2)	Serial I/O2 clock input setup time	400			ns
th(SCLK2-SIN2)	Serial I/O2 clock input hold time	300			ns

Note : When f(XIN) = 4 MHz and bit 6 of address 001A16 is “1” (clock synchronous).
Divide this value by four when f(XIN) = 4 MHz and bit 6 of address 001A16 is “0” (UART).

Notes on Interrupts

1. Change of relevant register settings

When the setting of the following registers or bits is changed, the interrupt request bit may be set to “1”. When not requiring the interrupt occurrence synchronized with these setting, take the following sequence.

- Interrupt edge selection register (address 003A16)
- Timer XY mode register (address 002316)

Set the above listed registers or bits as the following sequence.

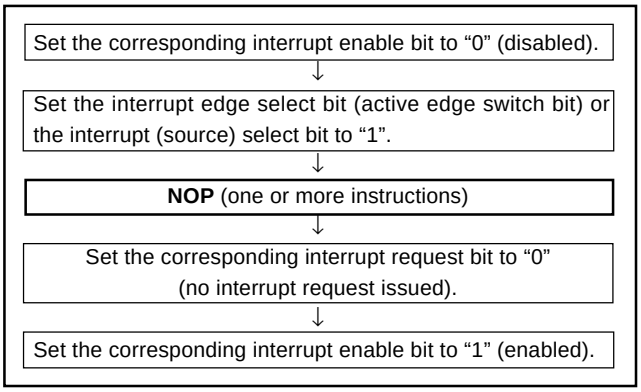


Fig 66. Sequence of changing relevant register

<Reason>
When setting the followings, the interrupt request bit may be set to “1”.

- When setting external interrupt active edge
  Concerned register: Interrupt edge selection register (address 003A16)
  Timer XY mode register (address 002316)
- When switching interrupt sources of an interrupt vector address where two or more interrupt sources are allocated.
  Concerned register: Interrupt edge selection register (address 003A16)

2. Check of interrupt request bit

When executing the BBC or BBS instruction to an interrupt request bit of an interrupt request register immediately after this bit is set to “0” by using a data transfer instruction, execute one or more instructions before executing the BBC or BBS instruction.

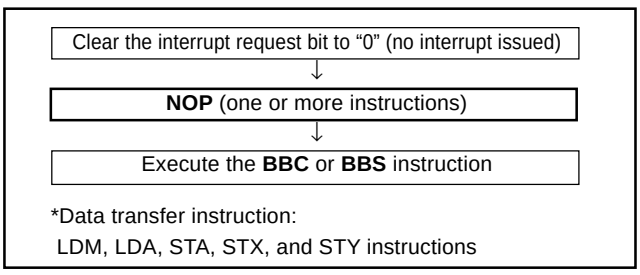


Fig 67. Sequence of check of interrupt request bit

<Reason>
If the BBC or BBS instruction is executed immediately after an interrupt request bit of an interrupt request register is cleared to “0”, the value of the interrupt request bit before being cleared to “0” is read.

Notes on Timer

- If a value n (between 0 and 255) is written to a timer latch, the frequency division ratio is 1/(n+1).
- When switching the count source by the timer 12, X and Y count source selection bits, the value of timer count is altered in unconsiderable amount owing to generating of thin pulses in the count input signals.
  Therefore, select the timer count source before set the value to the prescaler and the timer.

Notes on Serial Interface

1. Notes when selecting clock synchronous serial I/O (Serial I/O1)

(1) Stop of transmission operation
Clear the serial I/O1 enable bit and the transmit enable bit to “0” (Serial I/O1 and transmit disabled).
<Reason>
Since transmission is not stopped and the transmission circuit is not initialized even if only the serial I/O1 enable bit is cleared to “0” (Serial I/O1 disabled), the internal transmission is running (in this case, since pins TxD, RxD, SCLK1, and $\overline{\text{SRDY1}}$ function as I/O ports, the transmission data is not output). When data is written to the transmit buffer register in this state, data starts to be shifted to the transmit shift register. When the serial I/O1 enable bit is set to “1” at this time, the data during internally shifting is output to the TxD pin and an operation failure occurs.

(2) Stop of receive operation
Clear the receive enable bit to “0” (receive disabled), or clear the serial I/O1 enable bit to “0” (Serial I/O1 disabled).

(3) Stop of transmit/receive operation
Clear the transmit enable bit and receive enable bit to “0” simultaneously (transmit and receive disabled).
(when data is transmitted and received in the clock synchronous serial I/O mode, any one of data transmission and reception cannot be stopped.)
<Reason>
In the clock synchronous serial I/O mode, the same clock is used for transmission and reception. If any one of transmission and reception is disabled, a bit error occurs because transmission and reception cannot be synchronized.
In this mode, the clock circuit of the transmission circuit also operates for data reception. Accordingly, the transmission circuit does not stop by clearing only the transmit enable bit to “0” (transmit disabled). Also, the transmission circuit is not initialized by clearing the serial I/O1 enable bit to “0” (Serial I/O1 disabled) (refer to (1) in 1).

(4) $\overline{\text{SRDY1}}$ output of reception side (Serial I/O1)
When signals are output from the $\overline{\text{SRDY1}}$ pin on the reception side by using an external clock in the clock synchronous serial I/O mode, set all of the receive enable bit, the $\overline{\text{SRDY1}}$ output enable bit, and the transmit enable bit to “1” (transmit enabled).

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