Infineon Technologies - XC2786X96F66LACKXUMA1 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	C166SV2
Core Size	16/32-Bit
Speed	66MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I²S, POR, PWM, WDT
Number of I/O	116
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	51K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-144-4
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc2786x96f66lackxuma1

2 General Device Information

The XC2786X derivatives are high-performance members of the Infineon XC2000 Family of full-feature single-chip CMOS microcontrollers. These devices extend the functionality and performance of the C166 Family in terms of instructions (MAC unit), peripherals, and speed. They combine high CPU performance (up to 80 million instructions per second) with extended peripheral functionality and enhanced IO capabilities. Optimized peripherals can be adapted flexibly to meet the application requirements. These derivatives utilize clock generation via PLL and internal or external clock sources. On-chip memory modules include program Flash, program RAM, and data RAM.

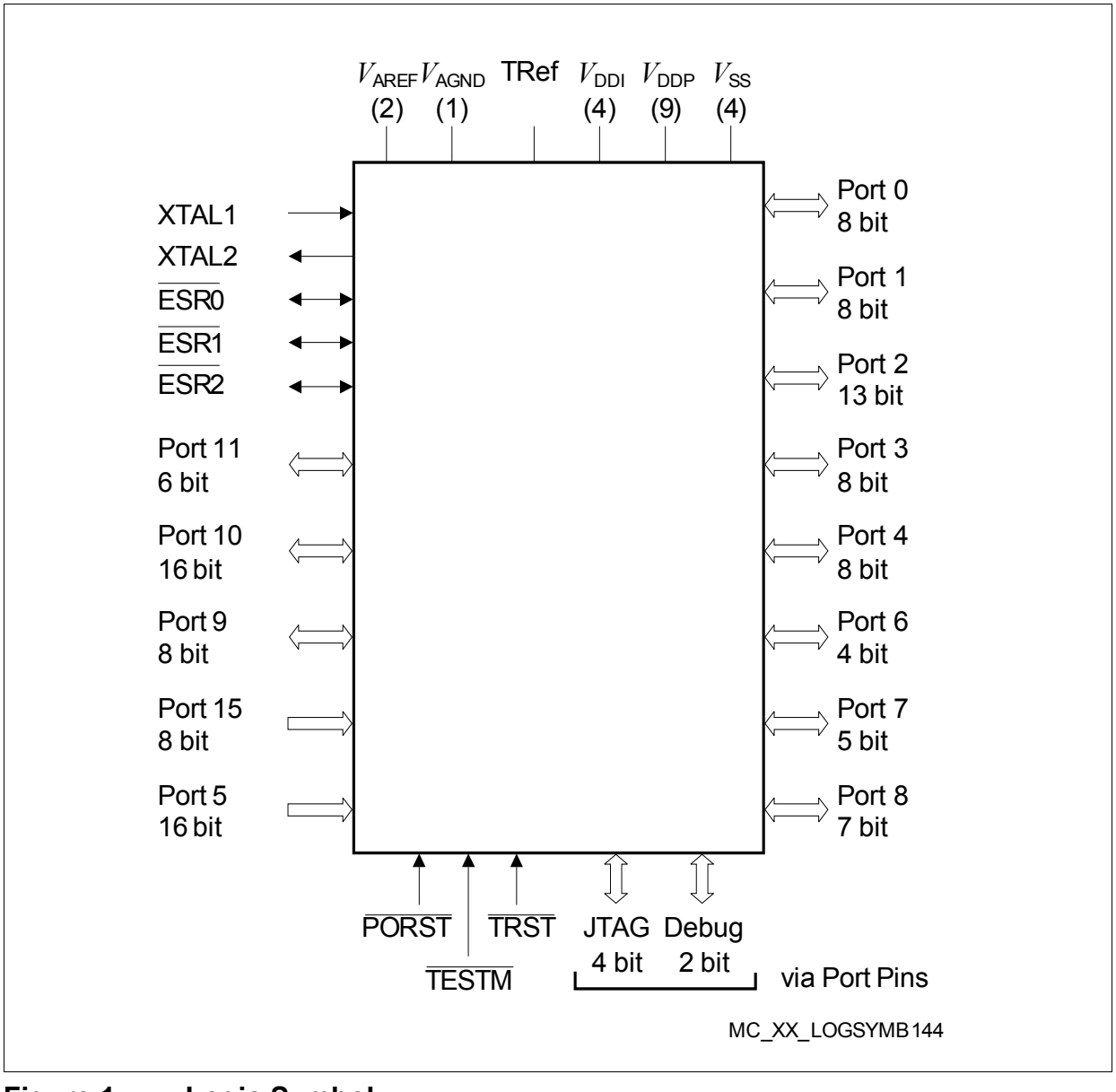

Figure 1 Logic Symbol

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
8	P7.0	O0 / I	St/B	**Bit 0 of Port 7, General Purpose Input/Output**
	T3OUT	O1	St/B	**GPT1 Timer T3 Toggle Latch Output**
	T6OUT	O2	St/B	**GPT2 Timer T6 Toggle Latch Output**
	TDO_A	OH	St/B	**JTAG Test Data Output**
	ESR2_1	I	St/B	**ESR2 Trigger Input 1**
9	P7.3	O0 / I	St/B	**Bit 3 of Port 7, General Purpose Input/Output**
	EMUX1	O1	St/B	**External Analog MUX Control Output 1 (ADC1)**
	U0C1_DOUT	O2	St/B	**USIC0 Channel 1 Shift Data Output**
	U0C0_DOUT	O3	St/B	**USIC0 Channel 0 Shift Data Output**
	CCU62_ CCPOS1A	I	St/B	**CCU62 Position Input 1**
	TMS_C	I	St/B	**JTAG Test Mode Selection Input**
	U0C1_DX0F	I	St/B	**USIC0 Channel 1 Shift Data Input**
10	P8.2	O0 / I	St/B	**Bit 2 of Port 8, General Purpose Input/Output**
	CCU60_ CC62	O1 / I	St/B	**CCU60 Channel 2 Input/Output**
11	P7.1	O0 / I	St/B	**Bit 1 of Port 7, General Purpose Input/Output**
	EXTCLK	O1	St/B	**Programmable Clock Signal Output**
	CCU62_ CTRAPA	I	St/B	**CCU62 Emergency Trap Input**
	$\overline{\text{BRKIN\_C}}$	I	St/B	**OCDS Break Signal Input**
12	P7.4	O0 / I	St/B	**Bit 4 of Port 7, General Purpose Input/Output**
	EMUX2	O1	St/B	**External Analog MUX Control Output 2 (ADC1)**
	U0C1_DOUT	O2	St/B	**USIC0 Channel 1 Shift Data Output**
	U0C1_ SCLKOUT	O3	St/B	**USIC0 Channel 1 Shift Clock Output**
	CCU62_ CCPOS2A	I	St/B	**CCU62 Position Input 2**
	TCK_C	I	St/B	**JTAG Clock Input**
	U0C0_DX0D	I	St/B	**USIC0 Channel 0 Shift Data Input**
	U0C1_DX1E	I	St/B	**USIC0 Channel 1 Shift Clock Input**

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
13	P8.1	O0 / I	St/B	**Bit 1 of Port 8, General Purpose Input/Output**
	CCU60_ CC61	O1 / I	St/B	**CCU60 Channel 1 Input/Output**
14	P8.0	O0 / I	St/B	**Bit 0 of Port 8, General Purpose Input/Output**
	CCU60_ CC60	O1 / I	St/B	**CCU60 Channel 0 Input/Output**
16	P6.0	O0 / I	St/A	**Bit 0 of Port 6, General Purpose Input/Output**
	EMUX0	O1	St/A	**External Analog MUX Control Output 0 (ADC0)**
	$\overline{\text{BRKOUT}}$	O3	St/A	**OCDS Break Signal Output**
	ADCx_ REQGTyC	I	St/A	**External Request Gate Input for ADC0/1**
	U1C1_DX0E	I	St/A	**USIC1 Channel 1 Shift Data Input**
17	P6.1	O0 / I	St/A	**Bit 1 of Port 6, General Purpose Input/Output**
	EMUX1	O1	St/A	**External Analog MUX Control Output 1 (ADC0)**
	T3OUT	O2	St/A	**GPT1 Timer T3 Toggle Latch Output**
	U1C1_DOUT	O3	St/A	**USIC1 Channel 1 Shift Data Output**
	ADCx_ REQTRyC	I	St/A	**External Request Trigger Input for ADC0/1**
18	P6.2	O0 / I	St/A	**Bit 2 of Port 6, General Purpose Input/Output**
	EMUX2	O1	St/A	**External Analog MUX Control Output 2 (ADC0)**
	T6OUT	O2	St/A	**GPT2 Timer T6 Toggle Latch Output**
	U1C1_ SCLKOUT	O3	St/A	**USIC1 Channel 1 Shift Clock Output**
	U1C1_DX1C	I	St/A	**USIC1 Channel 1 Shift Clock Input**
19	P6.3	O0 / I	St/A	**Bit 3 of Port 6, General Purpose Input/Output**
	T3OUT	O2	St/A	**GPT1 Timer T3 Toggle Latch Output**
	U1C1_ SELO0	O3	St/A	**USIC1 Channel 1 Select/Control 0 Output**
	U1C1_DX2D	I	St/A	**USIC1 Channel 1 Shift Control Input**
	ADCx_ REQTRyD	I	St/A	**External Request Trigger Input for ADC0/1**

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
21	P15.0	I	In/A	**Bit 0 of Port 15, General Purpose Input**
	ADC1_CH0	I	In/A	**Analog Input Channel 0 for ADC1**
22	P15.1	I	In/A	**Bit 1 of Port 15, General Purpose Input**
	ADC1_CH1	I	In/A	**Analog Input Channel 1 for ADC1**
23	P15.2	I	In/A	**Bit 2 of Port 15, General Purpose Input**
	ADC1_CH2	I	In/A	**Analog Input Channel 2 for ADC1**
	T5IN	I	In/A	**GPT2 Timer T5 Count/Gate Input**
24	P15.3	I	In/A	**Bit 3 of Port 15, General Purpose Input**
	ADC1_CH3	I	In/A	**Analog Input Channel 3 for ADC1**
	T5EUD	I	In/A	**GPT2 Timer T5 External Up/Down Control Input**
25	P15.4	I	In/A	**Bit 4 of Port 15, General Purpose Input**
	ADC1_CH4	I	In/A	**Analog Input Channel 4 for ADC1**
	T6IN	I	In/A	**GPT2 Timer T6 Count/Gate Input**
26	P15.5	I	In/A	**Bit 5 of Port 15, General Purpose Input**
	ADC1_CH5	I	In/A	**Analog Input Channel 5 for ADC1**
	T6EUD	I	In/A	**GPT2 Timer T6 External Up/Down Control Input**
27	P15.6	I	In/A	**Bit 6 of Port 15, General Purpose Input**
	ADC1_CH6	I	In/A	**Analog Input Channel 6 for ADC1**
28	P15.7	I	In/A	**Bit 7 of Port 15, General Purpose Input**
	ADC1_CH7	I	In/A	**Analog Input Channel 7 for ADC1**
29	V_{AREF1}	-	PS/A	**Reference Voltage for A/D Converter ADC1**
30	V_{AREF0}	-	PS/A	**Reference Voltage for A/D Converter ADC0**
31	V_{AGND}	-	PS/A	**Reference Ground for A/D Converters ADC0/1**
32	P5.0	I	In/A	**Bit 0 of Port 5, General Purpose Input**
	ADC0_CH0	I	In/A	**Analog Input Channel 0 for ADC0**
33	P5.1	I	In/A	**Bit 1 of Port 5, General Purpose Input**
	ADC0_CH1	I	In/A	**Analog Input Channel 1 for ADC0**
34	P5.2	I	In/A	**Bit 2 of Port 5, General Purpose Input**
	ADC0_CH2	I	In/A	**Analog Input Channel 2 for ADC0**
	TDI_A	I	In/A	**JTAG Test Data Input**

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
122	P9.3	O0 / I	St/B	**Bit 3 of Port 9, General Purpose Input/Output**
	CCU63_ COUT60	O1	St/B	**CCU63 Channel 0 Output**
	$\overline{\text{BRKOUT}}$	O2	St/B	**OCDS Break Signal Output**
123	P10.13	O0 / I	St/B	**Bit 13 of Port 10, General Purpose Input/Output**
	U1C0_DOUT	O1	St/B	**USIC1 Channel 0 Shift Data Output**
	U1C0_ SELO3	O3	St/B	**USIC1 Channel 0 Select/Control 3 Output**
	$\overline{\text{WR}}$/$\overline{\text{WRL}}$	OH	St/B	**External Bus Interface Write Strobe Output** Active for each external write access, when $\overline{\text{WR}}$, active for ext. writes to the low byte, when $\overline{\text{WRL}}$.
	U1C0_DX0D	I	St/B	**USIC1 Channel 0 Shift Data Input**
124	P1.3	O0 / I	St/B	**Bit 3 of Port 1, General Purpose Input/Output**
	CCU62_ COUT63	O1	St/B	**CCU62 Channel 3 Output**
	U1C0_ SELO7	O2	St/B	**USIC1 Channel 0 Select/Control 7 Output**
	U2C0_ SELO4	O3	St/B	**USIC2 Channel 0 Select/Control 4 Output**
	A11	OH	St/B	**External Bus Interface Address Line 11**
	ESR2_4	I	St/B	**ESR2 Trigger Input 4**
	CCU62_ T12HRB	I	St/B	**External Run Control Input for T12 of CCU62**
	EX3AINA	I	St/B	**External Interrupt Trigger Input**
125	P9.4	O0 / I	St/B	**Bit 4 of Port 9, General Purpose Input/Output**
	CCU63_ COUT61	O1	St/B	**CCU63 Channel 1 Output**
	U2C0_DOUT	O2	St/B	**USIC2 Channel 0 Shift Data Output**

3.1 Memory Subsystem and Organization

The memory space of the XC2786X is configured in the von Neumann architecture. In this architecture all internal and external resources, including code memory, data memory, registers and I/O ports, are organized in the same linear address space.

Table 5 XC2786X Memory Map

Address Area	Start Loc.	End Loc.	Area Size[1)]	Notes
IMB register space	$FF'FF00_H$	$FF'FFFF_H$	256 Bytes	–
Reserved (Access trap)	$F0'0000_H$	$FF'FEFF_H$	<1 Mbyte	Minus IMB registers
Reserved for EPSRAM	$E8'8000_H$	$EF'FFFF_H$	480 Kbytes	Mirrors EPSRAM
Emulated PSRAM	$E8'0000_H$	$E8'7FFF_H$	32 Kbytes	Flash timing
Reserved for PSRAM	$E0'8000_H$	$E7'FFFF_H$	480 Kbytes	Mirrors PSRAM
Program SRAM	$E0'0000_H$	$E0'7FFF_H$	32 Kbytes	Maximum speed
Reserved for pr. mem.	$CC'0000_H$	$DF'FFFF_H$	<1.25 Mbytes	–
Program Flash 2	$C8'0000_H$	$CB'FFFF_H$	256 Kbytes	–
Program Flash 1	$C4'0000_H$	$C7'FFFF_H$	256 Kbytes	–
Program Flash 0	$C0'0000_H$	$C3'FFFF_H$	256 Kbytes	2)
External memory area	$40'0000_H$	$BF'FFFF_H$	8 Mbytes	–
Available Ext. IO area[3)]	$20'5800_H$	$3F'FFFF_H$	< 2 Mbytes	Minus USIC/CAN
USIC registers	$20'4000_H$	$20'57FF_H$	6 Kbytes	Accessed via EBC
MultiCAN registers	$20'0000_H$	$20'3FFF_H$	16 Kbytes	Accessed via EBC
External memory area	$01'0000_H$	$1F'FFFF_H$	< 2 Mbytes	Minus segment 0
SFR area	$00'FE00_H$	$00'FFFF_H$	0.5 Kbyte	–
Dual-Port RAM	$00'F600_H$	$00'FDFF_H$	2 Kbytes	–
Reserved for DPRAM	$00'F200_H$	$00'F5FF_H$	1 Kbyte	–
ESFR area	$00'F000_H$	$00'F1FF_H$	0.5 Kbyte	–
XSFR area	$00'E000_H$	$00'EFFF_H$	4 Kbytes	–
Data SRAM	$00'A000_H$	$00'DFFF_H$	16 Kbytes	–
Reserved for DSRAM	$00'8000_H$	$00'9FFF_H$	8 Kbytes	–
External memory area	$00'0000_H$	$00'7FFF_H$	32 Kbytes	–

1) The areas marked with "<" are slightly smaller than indicated. See column "Notes".

2) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use ($C0'F000_H$ to $C0'FFFF_H$).

3) Several pipeline optimizations are not active within the external IO area. This is necessary to control external peripherals properly.

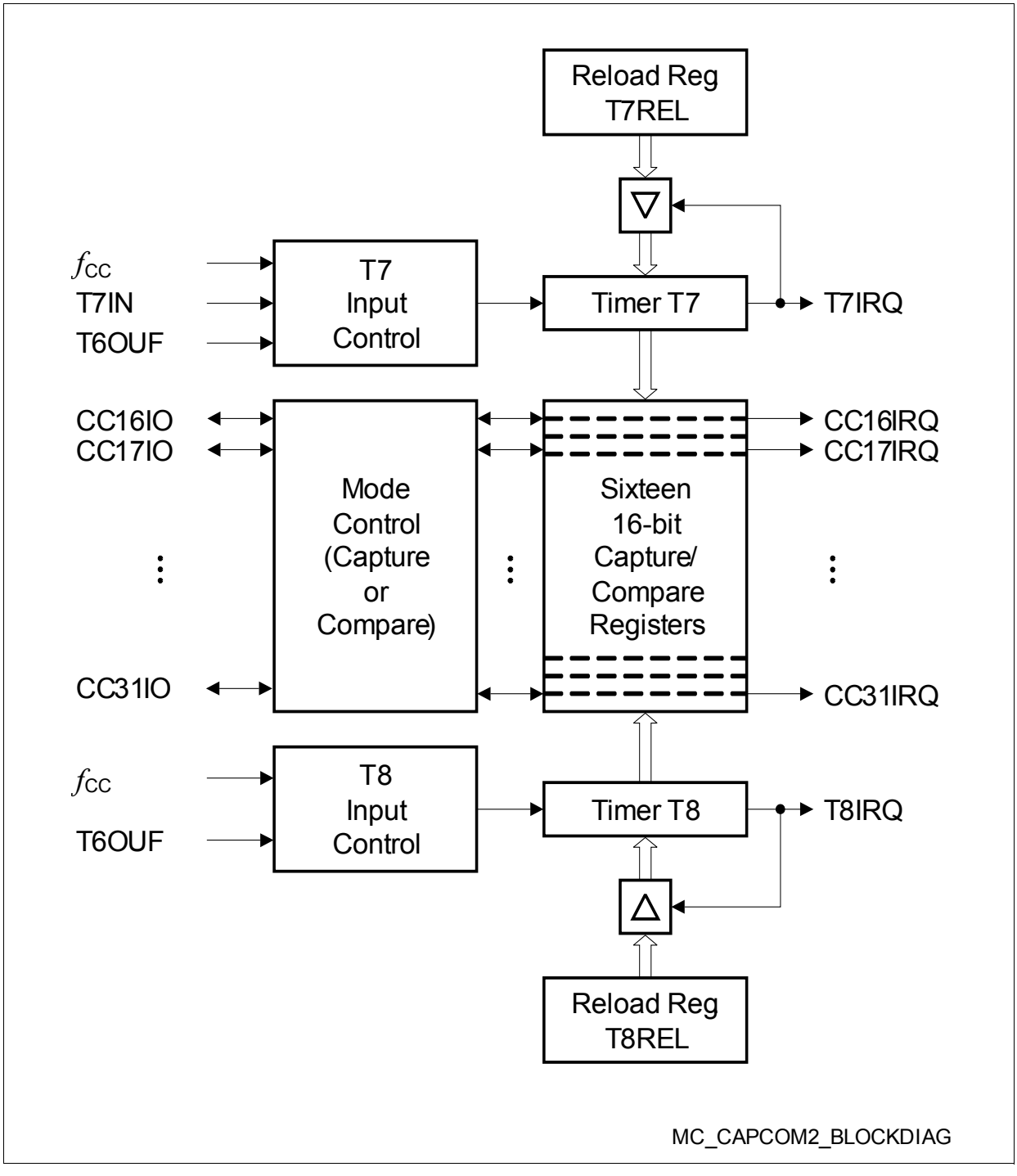

Figure 5 CAPCOM2 Unit Block Diagram

Target Protocols

Each USIC channel can receive and transmit data frames with a selectable data word width from 1 to 16 bits in each of the following protocols:

- **UART** (asynchronous serial channel)
  - maximum baud rate: f_{SYS} / 4
  - data frame length programmable from 1 to 63 bits
  - MSB or LSB first
- **LIN** Support (Local Interconnect Network)
  - maximum baud rate: f_{SYS} / 16
  - checksum generation under software control
  - baud rate detection possible by built-in capture event of baud rate generator
- **SSC/SPI/QSPI** (synchronous serial channel with or without data buffer)
  - maximum baud rate in slave mode: f_{SYS}
  - maximum baud rate in master mode: f_{SYS} / 2, limited by loop delay
  - number of data bits programmable from 1 to 63, more with explicit stop condition
  - MSB or LSB first
  - optional control of slave select signals
- **IIC** (Inter-IC Bus)
  - supports baud rates of 100 kbit/s and 400 kbit/s
- **IIS** (Inter-IC Sound Bus)
  - maximum baud rate: f_{SYS} / 2 for transmitter, f_{SYS} for receiver

Note: Depending on the selected functions (such as digital filters, input synchronization stages, sample point adjustment, etc.), the maximum achievable baud rate can be limited. Please note that there may be additional delays, such as internal or external propagation delays and driver delays (e.g. for collision detection in UART mode, for IIC, etc.).

3.12 MultiCAN Module

The MultiCAN module contains two independently operating CAN nodes with Full-CAN functionality which are able to exchange Data and Remote Frames using a gateway function. Transmission and reception of CAN frames is handled in accordance with CAN specification V2.0 B (active). Each CAN node can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers.

All CAN nodes share a common set of 64 message objects. Each message object can be individually allocated to one of the CAN nodes. Besides serving as a storage container for incoming and outgoing frames, message objects can be combined to build gateways between the CAN nodes or to set up a FIFO buffer.

The message objects are organized in double-chained linked lists, where each CAN node has its own list of message objects. A CAN node stores frames only into message objects that are allocated to its own message object list and it transmits only messages belonging to this message object list. A powerful, command-driven list controller performs all message object list operations.

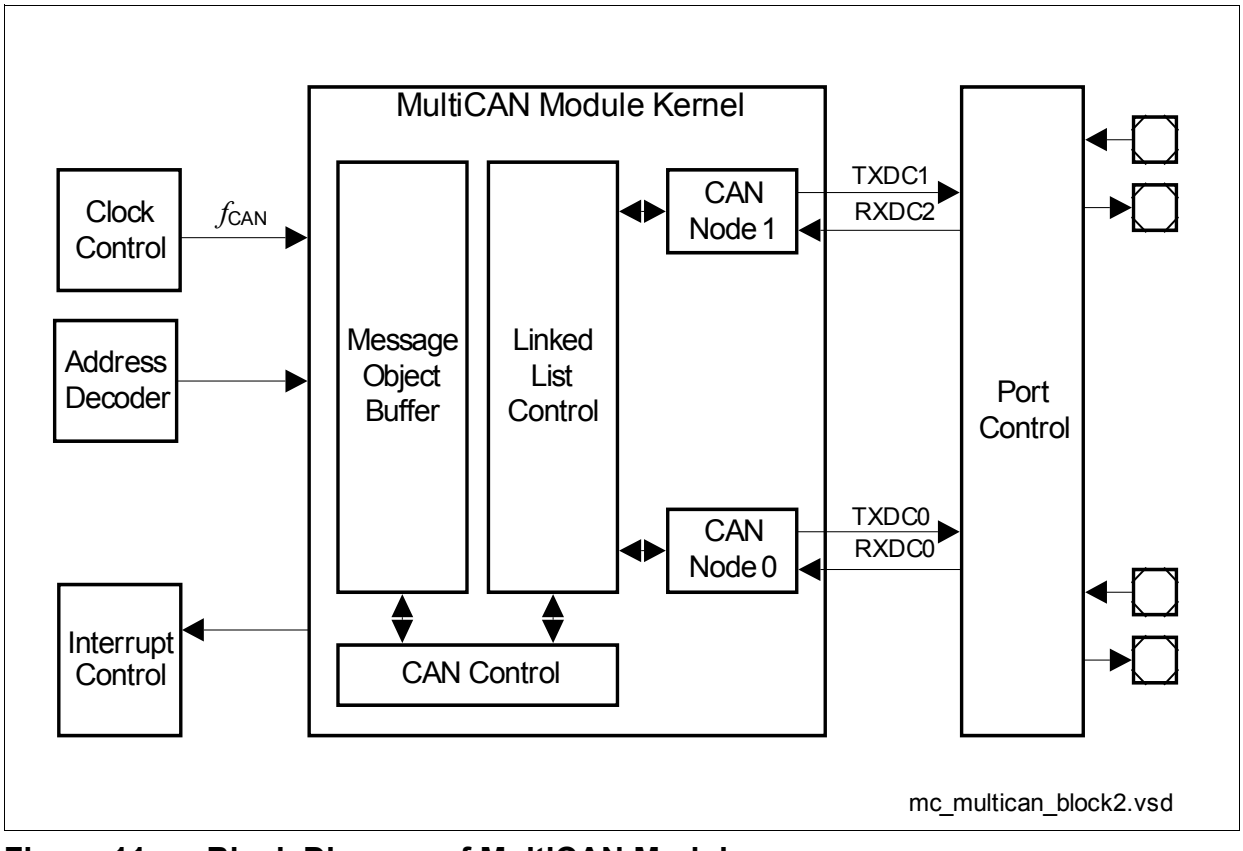

Figure 11 Block Diagram of MultiCAN Module

4.2.1 DC Parameters for Upper Voltage Area

These parameters apply to the upper IO voltage range, 4.5 V ≤ V_{DDP} ≤ 5.5 V.

Table 14 DC Characteristics for Upper Voltage Range (Operating Conditions apply)[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input low voltage (all except XTAL1)	V_{IL} SR	-0.3	–	0.3 × V_{DDP}	V	–
Input high voltage (all except XTAL1)	V_{IH} SR	0.7 × V_{DDP}	–	V_{DDP} + 0.3	V	–
Input Hysteresis[2)]	HYS CC	0.11 × V_{DDP}	–	–	V	V_{DDP} in [V], Series resistance = 0 Ω
Output low voltage	V_{OL} CC	–	–	1.0	V	$I_{OL} \le I_{OLmax}$[3)]
Output low voltage	V_{OL} CC	–	–	0.4	V	$I_{OL} \le I_{OLnom}$[3)4)]
Output high voltage[5)]	V_{OH} CC	V_{DDP} - 1.0	–	–	V	$I_{OH} \ge I_{OHmax}$[3)]
Output high voltage[5)]	V_{OH} CC	V_{DDP} - 0.4	–	–	V	$I_{OH} \ge I_{OHnom}$[3)4)]
Input leakage current (Port 5, Port 15)[6)]	I_{OZ1} CC	–	±10	±200	nA	0 V < V_{IN} < V_{DDP}
Input leakage current (all other)[6)7)]	I_{OZ2} CC	–	±0.2	±5	µA	$T_J \le$ 110°C, 0.45 V < V_{IN} < V_{DDP}
Input leakage current (all other)[6)7)]	I_{OZ2} CC	–	±0.2	±15	µA	$T_J \le$ 150°C, 0.45 V < V_{IN} < V_{DDP}
Pull level keep current	I_{PLK}	–	–	±30	µA	$V_{PIN} \ge V_{IH}$ (up)[8)] $V_{PIN} \le V_{IL}$ (dn)
Pull level force current	I_{PLF}	±250	–	–	µA	$V_{PIN} \le V_{IL}$ (up)[8)] $V_{PIN} \ge V_{IH}$ (dn)
Pin capacitance[9)] (digital inputs/outputs)	C_{IO} CC	–	–	10	pF	

1) Keeping signal levels within the limits specified in this table ensures operation without overload conditions. For signal levels outside these specifications, also refer to the specification of the overload current I_{OV}.

2) Not subject to production test - verified by design/characterization. Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It cannot suppress switching due to external system noise under all conditions.
3) The maximum deliverable output current of a port driver depends on the selected output driver mode, see **Table 13, Current Limits for Port Output Drivers**. The limit for pin groups must be respected.
4) As a rule, with decreasing output current the output levels approach the respective supply level ($V_{OL} \rightarrow V_{SS}$, $V_{OH} \rightarrow V_{DDP}$). However, only the levels for nominal output currents are verified.
5) This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage is determined by the external circuit.
6) An additional error current (I_{INJ}) will flow if an overload current flows through an adjacent pin. Please refer to the definition of the overload coupling factor K_{OV}.
   The leakage current value is not tested in the lower voltage range but only in the upper voltage range. This parameter is ensured by correlation.
7) The given values are worst-case values. In production test, this leakage current is only tested at 125°C; other values are ensured by correlation. For derating, please refer to the following descriptions:
   Leakage derating depending on temperature (T_J = junction temperature [°C]):
   I_{OZ} = 0.03 × $e^{(1.35 + 0.028 \times TJ)}$ [µA]. For example, at a temperature of 130°C the resulting leakage current is 4.41 µA.
   Leakage derating depending on voltage level (DV = V_{DDP} - V_{PIN} [V]):
   I_{OZ} = $I_{OZtempmax}$ - (1.3 × DV) [µA]
   This voltage derating formula is an approximation which applies for maximum temperature.
   Because pin P2.8 is connected to two pads (standard pad and high-speed clock pad), it has twice the normal leakage.
8) Keep current: Limit the current through this pin to the indicated value so that the enabled pull device can keep the default pin level: $V_{PIN} \geq V_{IH}$ for a pullup; $V_{PIN} \leq V_{IL}$ for a pulldown.
   Force current: Drive the indicated minimum current through this pin to change the default pin level driven by the enabled pull device: $V_{PIN} \leq V_{IL}$ for a pullup; $V_{PIN} \geq V_{IH}$ for a pulldown.
   These values apply to the fixed pull-devices in dedicated pins and to the user-selectable pull-devices in general purpose IO pins.
9) Not subject to production test - verified by design/characterization.
   Because pin P2.8 is connected to two pads (standard pad and high-speed clock pad), it has twice the normal capacitance.

4.3 Analog/Digital Converter Parameters

These parameters describe the conditions for optimum ADC performance.

Table 18 A/D Converter Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit	Test Condition
			Min.	Max.		
Analog reference supply	V_{AREF}	SR	V_{AGND} + 1.0	V_{DDPA} + 0.05	V	1)
Analog reference ground	V_{AGND}	SR	V_{SS} - 0.05	V_{AREF} - 1.0	V	–
Analog input voltage range	V_{AIN}	SR	V_{AGND}	V_{AREF}	V	2)
Analog clock frequency	f_{ADCI}		0.5	20	MHz	3)
Conversion time for 10-bit result[4)]	t_{C10}	CC	(13 + STC) × t_{ADCI} + 2 × t_{SYS}		–	–
Conversion time for 8-bit result[4)]	t_{C8}	CC	(11 + STC) × t_{ADCI} + 2 × t_{SYS}		–	–
Wakeup time from analog powerdown, fast mode	t_{WAF}	CC	–	1	µs	–
Wakeup time from analog powerdown, slow mode	t_{WAS}	CC	–	10	µs	–
Total unadjusted error[5)]	TUE	CC	–	±2	LSB	V_{AREF} = 5.0 V[1)]
DNL error	EA_{DNL}	CC	–	±1	LSB	
INL error	EA_{INL}	CC	–	±1.2	LSB	
Gain error	EA_{GAIN}	CC	–	±0.8	LSB	
Offset error	EA_{OFF}	CC	–	±0.8	LSB	
Total capacitance of an analog input	C_{AINT}	CC	–	10	pF	6)7)
Switched capacitance of an analog input	C_{AINS}	CC	–	4	pF	6)7)
Resistance of the analog input path	R_{AIN}	CC	–	1.5	kΩ	6)7)
Total capacitance of the reference input	C_{AREFT}	CC	–	15	pF	6)7)

4.4 System Parameters

The following parameters specify several aspects which are important when integrating the XC2786X into an application system.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Table 20 Various System Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply watchdog (SWD) supervision level (see Table 21)	V_{SWD} CC	V_{LV} - 0.150	V_{LV}	V_{LV} + 0.100	V	V_{LV} = selected voltage in upper voltage area
		V_{LV} - 0.125	V_{LV}	V_{LV} + 0.050	V	V_{LV} = selected voltage in lower voltage area
Core voltage (PVC) supervision level (see Table 22)	V_{PVC} CC	V_{LV} - 0.070	V_{LV}	V_{LV} + 0.030	V	V_{LV} = selected voltage
Current control limit	I_{CC} CC	13	–	30	mA	Power domain DMP_M
		90	–	150	mA	Power domain DMP_1
Wakeup clock source frequency	f_{WU} CC	400	500	600	kHz	FREQSEL = 00_B
Internal clock source frequency	f_{INT} CC	4.8	5.0	5.2	MHz	
Startup time from stopover mode	t_{SSO} CC	200	260	320	µs	User instruction from PSRAM

Table 21 Coding of Bitfields LEVxV in Register SWDCON0

Code	Default Voltage Level	Notes[1)]
0000_B	2.9 V	
0001_B	3.0 V	LEV1V: reset request
0010_B	3.1 V	
0011_B	3.2 V	
0100_B	3.3 V	
0101_B	3.4 V	
0110_B	3.6 V	
0111_B	4.0 V	
1000_B	4.2 V	
1001_B	4.5 V	LEV2V: no request
1010_B	4.6 V	
1011_B	4.7 V	
1100_B	4.8 V	
1101_B	4.9 V	
1110_B	5.0 V	
1111_B	5.5 V	

1) The indicated default levels are selected automatically after a power reset.

Table 22 Coding of Bitfields LEVxV in Registers PVCyCONz

Code	Default Voltage Level	Notes[1)]
000_B	0.9 V	
001_B	1.0 V	
010_B	1.1 V	
011_B	1.2 V	
100_B	1.3 V	LEV1V: reset request
101_B	1.4 V	LEV2V: interrupt request
110_B	1.5 V	
111_B	1.6 V	

1) The indicated default levels are selected automatically after a power reset.

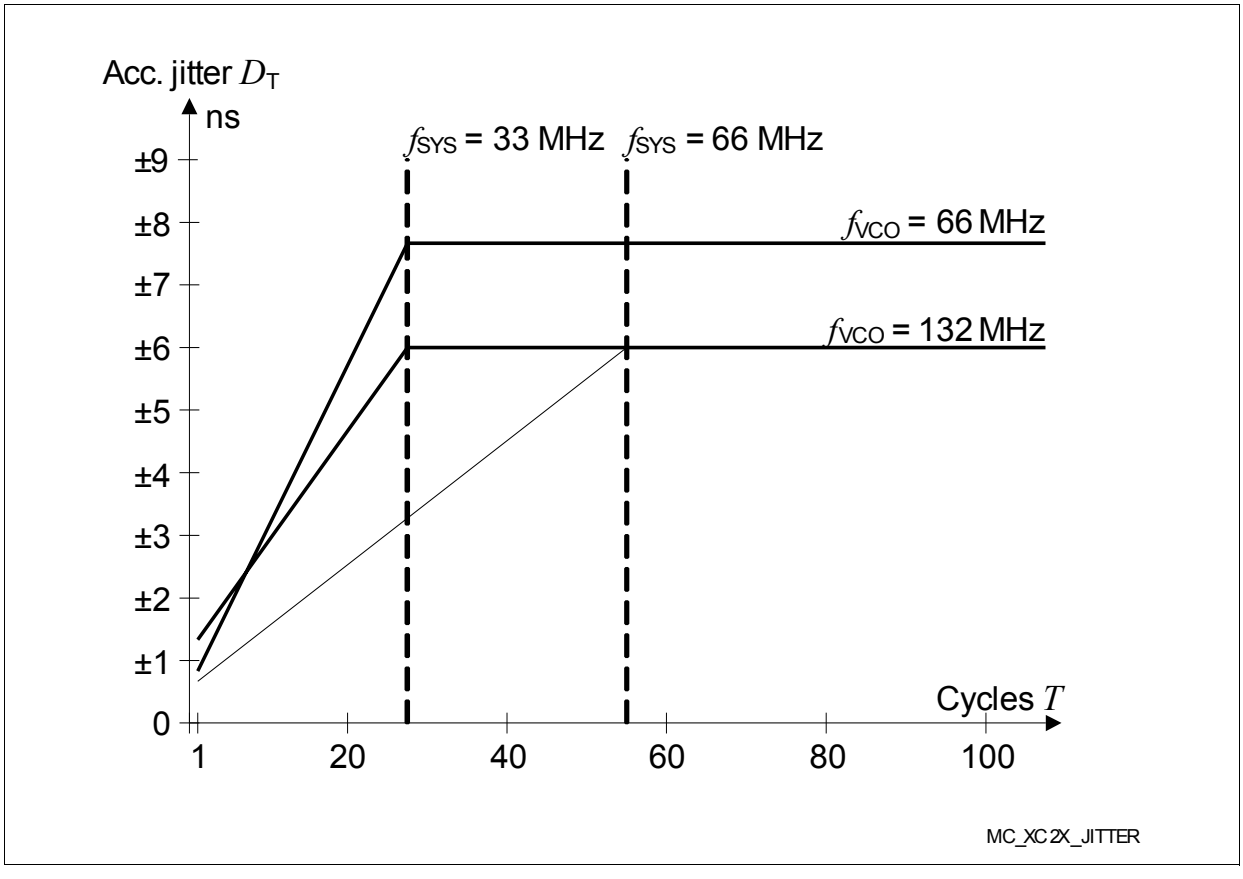

Figure 19 Approximated Accumulated PLL Jitter

*Note: The specified PLL jitter values are valid if the capacitive load per pin does not exceed C_L = 20 pF (see **Table 12**).*
The maximum peak-to-peak noise on the pad supply voltage (measured between V_{DDPB} pin 100/144 and V_{SS} pin 1) is limited to a peak-to-peak voltage of V_{PP} = 50 mV. This can be achieved by appropriate blocking of the supply voltage as close as possible to the supply pins and using PCB supply and ground planes.

Different frequency bands can be selected for the VCO so that the operation of the PLL can be adjusted to a wide range of input and output frequencies:

Table 25 VCO Bands for PLL Operation[1)]

PLLCON0.VCOSEL	VCO Frequency Range	Base Frequency Range
00	50 … 110 MHz	10 … 40 MHz
01	100 … 160 MHz	20 … 80 MHz
1X	Reserved	

1) Not subject to production test - verified by design/characterization.

External Bus Arbitration

If the arbitration signals are enabled, the XC2786X makes its external resources available in response to an arbitration request.

Table 31 Bus Arbitration Timing for Upper Voltage Range (Operating Conditions apply)

Parameter	Symbol	Limits			Unit	Note
		Min.	Typ.	Max.		
Input setup time for: HOLD input	t_{40} SR	18		–	ns	
Output delay rising edge for: HLDA, BREQ	t_{41} CC	0		13	ns	
Output delay falling edge for: HLDA	t_{42} CC	1		14	ns	

Table 32 Bus Arbitration Timing for Lower Voltage Range (Operating Conditions apply)

Parameter	Symbol	Limits			Unit	Note
		Min.	Typ.	Max.		
Input setup time for: HOLD input	t_{40} SR	28		–	ns	
Output delay rising edge for: HLDA, BREQ	t_{41} CC	0		19	ns	
Output delay falling edge for: HLDA	t_{42} CC	1		21	ns	

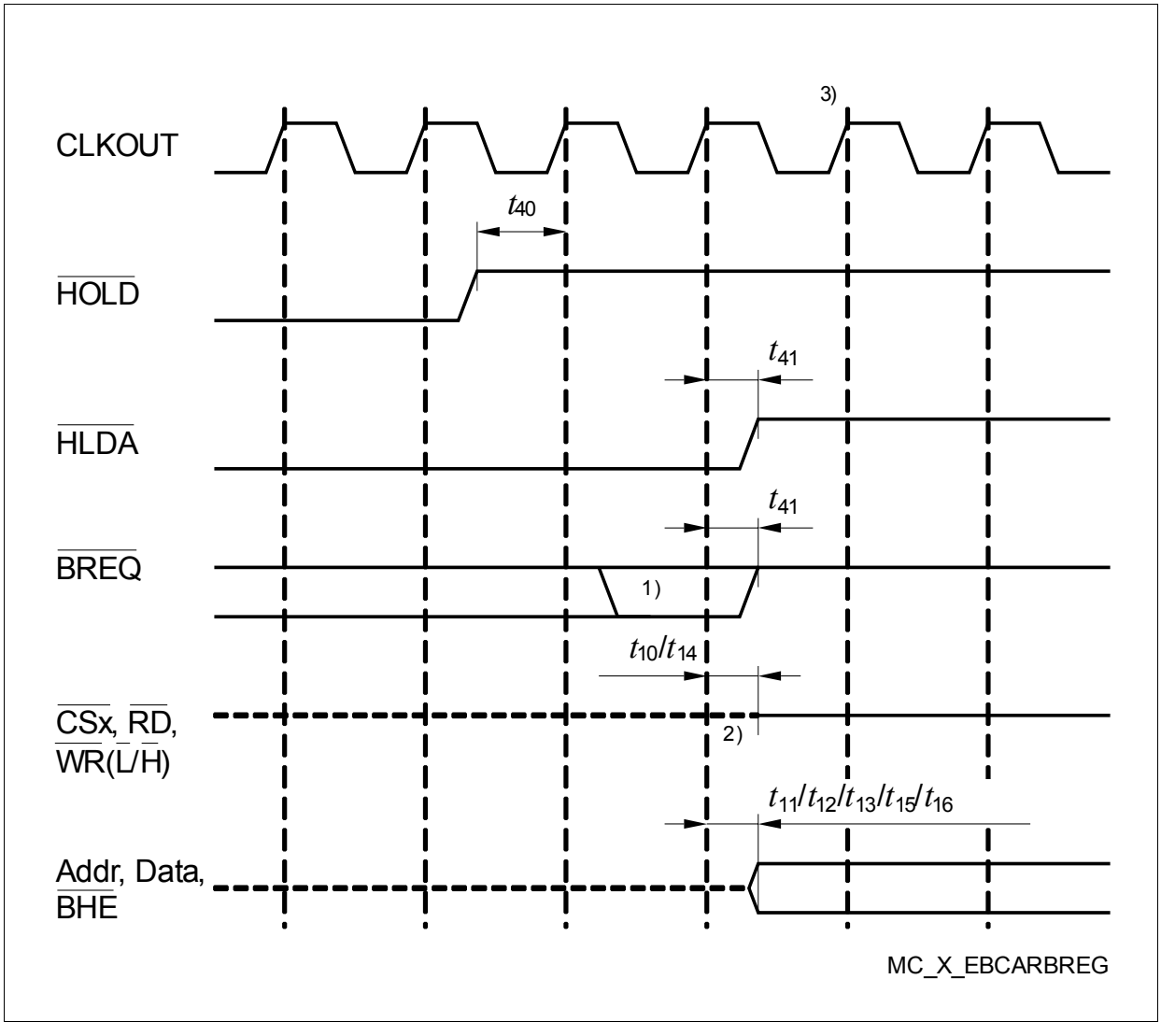

Figure 26 External Bus Arbitration, Regaining the Bus

Notes

1. *This is the last chance for $\overline{BREQ}$ to trigger the indicated regain sequence. Even if $\overline{BREQ}$ is activated earlier, the regain sequence is initiated by $\overline{HOLD}$ going high. Please note that $\overline{HOLD}$ may also be deactivated without the XC2786X requesting the bus.*
2. *The control outputs will be resistive high (pull-up) before being driven inactive (ALE will be low).*
3. *The next XC2786X-driven bus cycle may start here.*

4.6.5 Synchronous Serial Interface Timing

The following parameters are applicable for a USIC channel operated in SSC mode.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Table 33 SSC Master/Slave Mode Timing for Upper Voltage Range (Operating Conditions apply), C_L = 50 pF

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Master Mode Timing						
Slave select output SELO active to first SCLKOUT transmit edge	t_1 CC	0	–	1)	ns	2)
Slave select output SELO inactive after last SCLKOUT receive edge	t_2 CC	0.5 × t_{BIT}	–	3)	ns	
Transmit data output valid time	t_3 CC	-6	–	13	ns	
Receive data input setup time to SCLKOUT receive edge	t_4 SR	31	–	–	ns	
Data input DX0 hold time from SCLKOUT receive edge	t_5 SR	-7	–	–	ns	
Slave Mode Timing						
Select input DX2 setup to first clock input DX1 transmit edge	t_{10} SR	7	–	–	ns	4)
Select input DX2 hold after last clock input DX1 receive edge	t_{11} SR	5	–	–	ns	4)
Data input DX0 setup time to clock input DX1 receive edge	t_{12} SR	7	–	–	ns	4)
Data input DX0 hold time from clock input DX1 receive edge	t_{13} SR	5	–	–	ns	4)
Data output DOUT valid time	t_{14} CC	8	–	29	ns	4)

1) The maximum value further depends on the settings for the slave select output leading delay.

2) $t_{SYS} = 1/f_{SYS}$ (= 12.5 ns @ 80 MHz)

3) The maximum value depends on the settings for the slave select output trailing delay and for the shift clock output delay.

4) These input timings are valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).

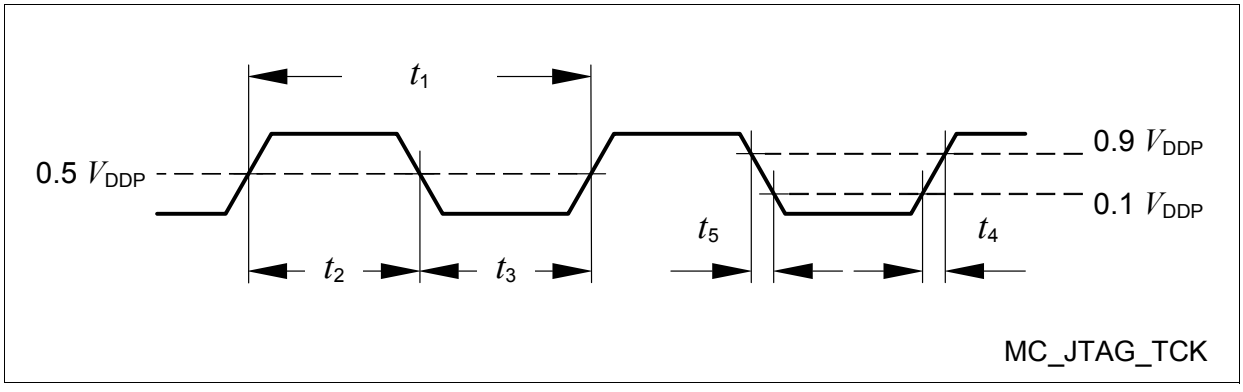

Figure 28 Test Clock Timing (TCK)

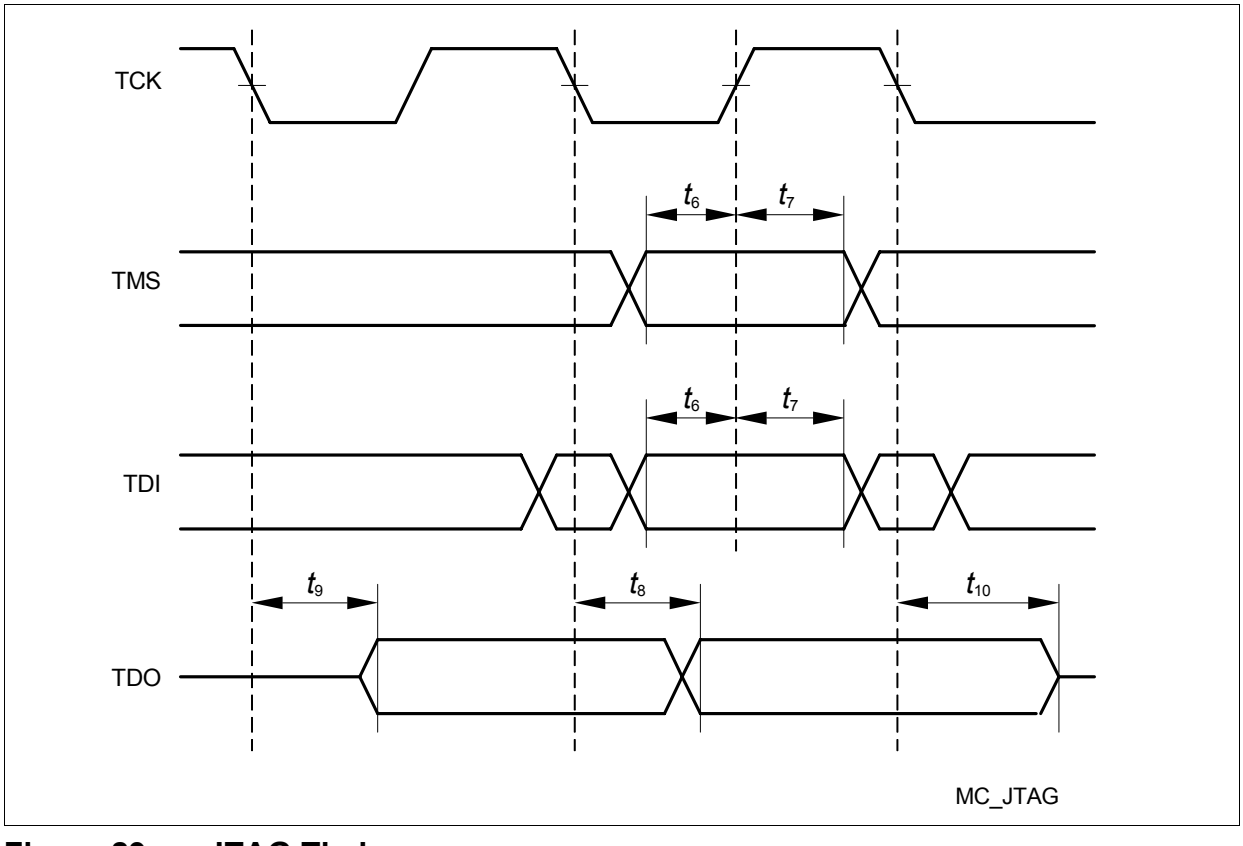

Figure 29 JTAG Timing

w w w . i n f i n e o n . c o m

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