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Details

Product Status	Obsolete
Module/Board Type	MPU Core
Core Processor	Zynq UltraScale+ XCZU9EG-1FFVC900E
Co-Processor	-
Speed	-
Flash Size	128MB
RAM Size	4GB
Connector Type	B2B
Size / Dimension	2.05" x 2.99" (52mm x 76mm)
Operating Temperature	-40°C ~ 85°C
Purchase URL	https://www.e-xfl.com/product-detail/trenz-electronic/te0808-04-09eg-2ie

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Bank	Type	B2B Connector	Count of MGT Lanes	Schematic Names / Connector Pins	MGT Bank's Reference Clock Inputs
505	GT R	J2	4 GTR lanes (4 RX / 4 TX)	B505_RX3_N, B505_RX3_P, pins J2-52, J2-54 B505_TX3_N, B505_TX3_P, pins J2-49, J2-51 B505_RX2_N, B505_RX2_P, pins J2-58, J2-60 B505_TX2_N, B505_TX2_P, pins J2-55, J2-57 B505_RX1_N, B505_RX1_P, pins J2-64, J2-66 B505_TX1_N, B505_TX1_P, pins J2-61, J2-63 B505_RX0_N, B505_RX0_P, pins J2-70, J2-72 B505_TX0_N, B505_TX0_P, pins J2-67, J2-69	2 reference clock signals (B505_CLK0, B505_CLK1) from B2B connector J2 (pins J2-10/J2-12, J2-16/J2-18) to bank's pins P25/P26, M25/M26 2 reference clock signal (B505_CLK2, B505_CLK3) from programmable PLL clock generator U5 to bank's pins K25/K26, H25/H26

Table 3: B2B connector pin-outs of available MGT lanes of the MPSoC.

3.3 JTAG Interface

JTAG access is provided through the MPSoC's PS configuration bank 503 with bank voltage PS_1V8.

JTAG Signal	B2B Connector Pin
TCK	J2-120
TDI	J2-122
TDO	J2-124
TMS	J2-126

Table 4: B2B connector pin-out of JTAG interface.

3.4 Configuration Bank Control Signals

The Xilinx Zynq UltraScale+ MPSoC's PS configuration bank 503 control signal pins are accessible through B2B connector J2.

For further information about the particular control signals and how to use and evaluate them, refer to the [Xilinx Zynq UltraScale+ MPSoC TRM](#) and [UltraScale Architecture Configuration - User Guide](#).

Signal	B2B Connector Pin	Function
DONE	J2-116	PL configuration completed.
PROG_B	J2-100	PL configuration reset signal.
INIT_B	J2-98	PS is initialized after a power-on reset.
SRST_B	J2-96	System reset.

Signal	B2B Connector Pin	Function
MODE0 ... MODE3	J2-109/J2-107/ J2-105/J2-103	4-bit boot mode pins. For further information about the boot modes refer to the Xilinx Zynq UltraScale+ MPSoC TRM section 'Boot and Configuration'.
ERR_STATU S/ ERR_OUT	J2-86 / J2-88	ERR_OUT signal is asserted for accidental loss of power, an error, or an exception in the MPSoC's Platform Management Unit (PMU). ERR_STATUS indicates a secure lock-down state.
PUDC_B	J2-127	Pull-up during configuration (pulled-up to PL_1V8).

Table 5: B2B connector pin-out of MPSoC's PS configuration bank.

3.5 Analog Input

The Xilinx Zynq UltraScale+ MPSoC provides differential pairs for analog input values. The pins are exposed to B2B-connector J2.

Signal	B2B Connector Pin	Function
V_P, V_N	J2-113, J2-115	System Monitor
DX_P, DX_N	J2-119, J2-121	Temperature-sensing diode pins

Table 6: B2B connector pin-out of analog input pins

3.6 Quad SPI Interface

Quad SPI Flash memory ICs U7 and U17 are connected to the Zynq MPSoC PS QSPI0 interface via PS MIO bank 500, pins MIO0 ... MIO5 and MIO7 ... MIO12.

MIO	Signal Name	U7 Pin	MIO	Signal Name	U17 Pin
0	SPI Flash CLK	B2	7	SPI Flash CS	C2
1	SPI Flash IO1	D2	8	SPI Flash IO0	D3
2	SPI Flash IO2	C4	9	SPI Flash IO1	D2
3	SPI Flash IO3	D4	10	SPI Flash IO2	C4
4	SPI Flash IO0	D3	11	SPI Flash IO3	D4
5	SPI Flash CS	C2	12	SPI Flash CLK	B2

Table 7: PS MIO pin assignment of the Quad SPI Flash memory ICs.

4 Boot Process

The boot device and mode of the Zynq UltraScale+ MPSoC can be selected via 4 dedicated pins accessible on B2B connector J2:

Boot Mode Pin	B2B Pin
PS_MODE0	J2-109
PS_MODE1	J2-107
PS_MODE2	J2-105
PS_MODE3	J2-103

Table 8: Boot mode pins on B2B connector J2.

Following boot modes are possible on the TE0808 UltraScale+ module by generating the corresponding 4-bit code by the pins PS_MODE0 ... PS_MODE3 (little-endian alignment):

Boot Mode	Mode Pins [3:0]	MIO Location	Description
JTAG	0x0	JTAG	Dedicated PS interface.
QSPI32	0x2	MIO[12:0]	Configured on module with dual QSPI Flash Memory. 32-bit addressing. Supports single and dual parallel configurations. Stack and dual stack is not supported.
SD0	0x3	MIO[25:13]	Supports SD 2.0.
SD1	0x5	MIO[51:38]	Supports SD 2.0.
eMMC_18	0x6	MIO[22:13]	Supports eMMC 4.5 at 1.8V.
USB 0	0x7	MIO[52:63]	Supports USB 2.0 and USB 3.0.
PJTAG_0	0x8	MIO[29:26]	PS JTAG connection 0 option.
SD1-LS	0xE	MIO[51:39]	Supports SD 3.0 with a required SD 3.0 compliant level shifter.

Table 9: Selectable boot modes by dedicated boot mode pins.

For functional details see [ug1085 - Zynq UltraScale+ TRM \(Boot Modes Section\)](#).

5 On-board Peripherals

5.1 Flash

The TE0808 SoM can be configured with max. 512 MByte Flash memory for configuration and operation.

Name	IC	Designat or	PS7	MIO	Notes
SPI Flash	N25Q256A1 1E1240E	U7	QSPI 0	MIO0 ... MIO5	dual parallel booting possible, 32 MByte memory per Flash IC at standard configuration
SPI Flash	N25Q256A1 1E1240E	U17	QSPI 0	MIO7 ... MIO12	as above

Table 10: Peripherals connected to the PS MIO pins.

5.2 DDR4 SDRAM

The TE0808-04 SoM is equipped with with four DDR4-2400 SDRAM modules with up to 8 GByte memory density. The SDRAM modules are connected to the Zynq MPSoC's PS DDR controller (bank 504) with a 64-bit data bus.

Refer to the Xilinx Zynq UltraScale+ datasheet [DS925](#) for more information on whether the specific package of the Zynq UltraScale+ MPSoC supports the maximum data transmission rate of 2400 MByte/s.

5.3 Programmable PLL Clock Generator

Following table illustrates on-board Si5345A programmable clock multiplier chip inputs and outputs:

Input	Connected to	Frequency	Notes
IN0	On-board Oscillator (U25)	25.000000 MHz	-
IN1	B2B Connector pins J2-4, J2-6 (differential pair)	User	AC decoupling required on base
IN2	B2B Connector pins J3-66, J3-68 (differential pair)	User	AC decoupling required on base
IN3	OUT9	User	Loop-back from OUT9
Output	Connected to	Frequency	Notes
OUT0	B2B Connector pins J2-3, J2-1 (differential pair)	User	Default off
OUT1	B230 CLK0	User	Default off
OUT2	B229 CLK1	User	Default off
OUT3	B228 CLK1	User	Default off
OUT4	B505 CLK2	User	Default off
OUT5	B505 CLK3	User	Default off
OUT6	B128 CLK0	User	Default off

OUT7	B2B Connector pins J2-7, J2-9 (differential pair)	User	Default off
OUT8	B2B Connector pins J2-13, J2-15 (differential pair)	User	Default off
OUT9	IN3 (Loop-back)	User	Default off
XA/XB	Quartz (Y1)	50.000 MHz	-

Table 11: Programmable PLL clock generator input/output.

The Si5345A programmable clock generator's control interface pins are exposed to B2B connector J2. For further information refer to the Si5345A data sheet.

Signal	B2B Connector Pin	Function
PLL_FINCL	J2-81	Frequency increment.
PLL_LOLN	J2-85	Loss of lock (active-low).
PLL_SEL0 / PLL_SEL1	J2-93 / J2-87	Manual input switching.
PLL_FDEC	J2-94	Frequency decrement.
PLL_RST	J2-59	Device reset (active-low)
PLL_SCL / PLL_SDA	J2-90 / J2-92	I ² C interface, external pull-ups needed for SCL / SDA lines. I ² C address in current configuration: 1101000b.

Table 12: B2B connector pin-out of Si5345A programmable clock generator.

⚠ Si5345 OTP ROM is not programmed by default at delivery, so it is customers responsibility to either configure Si5345 during FSBL or then use SiLabs programmer and program the OTP ROM with customer fixed clock setup.

Si5345 OTP can only be programmed two times, as different user configurations may required different setup TE0808 is normally shipped with blank OTP.

For more information refer to [Si5345 at SiLabs](#).

5.4 Oscillators

The TE0808-04 SoM is equipped with two on-board oscillators to provide the Zynq's MPSoC's PS configuration bank 503 with reference clock signals.

Clock	Frequency	Bank 503 Pin	Connected to
PS_CLK	33.333333 MHz	P20	MEMS Oscillator, U32
PS_PAD (RTC)	32.768 kHz	R22/R23	Quartz crystal, Y2

Table 13: Reference clock-signals to PS configuration bank 503.

5.5 On-board LEDs

LED Color		Connected to	Description and Notes
D1	Red	DONE signal (PS Configuration Bank 503)	This LED goes ON when power has been applied to the module and stays ON until MPSoC's programmable logic is configured properly.

Table 14: LED's description.

6 Power and Power-On Sequence

6.1 Power Consumption

The maximum power consumption of a module mainly depends on the design which is running on the FPGA.

Xilinx provide a power estimator excel sheets to calculate power consumption. It's also possible to evaluate the power consumption of the developed design with Vivado. See also Trenz Electronic Wiki FAQ.

Power Input Pin	Typical Current
DCDCIN	TBD*
LP_DCDC	TBD*
PL_DCIN	TBD*
PS_BATT	TBD*

Table 15: Maximum current of power supplies. *to be determined soon with reference design setup.

Power supply with minimum current capability of 3A for system startup is recommended. For the lowest power consumption and highest efficiency of on board DC/DC regulators it is recommended to powering the module from one single 3.3V supply. Except 'PS_BATT', all input power supplies have a nominal value of 3.3V. Although the input power supplies can be powered up in any order, it is recommended to power them up simultaneously.

The TE0808 module equipped with the Xilinx Zynq UltraScale+ MPSoC delivers a heterogeneous multi-processing system with integrated programmable logic and independently operable elements and is designed to meet embedded system power management requirement by advanced power management features. This features allow to offset the power and heat constraints against overall performance and operational efficiency.

This features allowing highly flexible power management are achieved by establishing Power Domains for power isolation. The Zynq UltraScale+ MPSoC has multiple power domains, whereby each power domain requires its own particular external DC-DC converters.

The Processing System contains three Power Domains:

- Battery Power Domain (BBRAM and RTC)
- Full-Power Domain (Application Processing Unit, DDR Controller, Graphics Processing Unit and High-Speed Connectivity)
- Low-Power Domain (Real-Time Processing Unit, Security and Configuration Unit, Platform Management Unit, System Monitor and General Connectivity)

The fourth Power Domain is for the Programmable Logic (PL). If individual Power Domain control is not required, power rails can be shared between domains.

On the TE0808-04 SoM, following power domains can be powered up individually with power rails available on the B2B connectors:

- Full-power domain, supplied by power rail **DCDCIN**
- Low-power domain, supplied by power rail **LP_DCDC**
- Programmable logic, supplied by power rail **PL_DCIN**
- Battery power domain, supplied by power rail **PS_BATT**

Each power domain has its own enable and power good signals. The power rail **GT_DCDC** is needed to generate the voltages for the Multi Gigabit Transceiver units of the Zynq UltraScale+ MPSoC.

6.2 Power Distribution Dependencies

The power rails DCDCIN, LP_DCDC, PL_DCIN, PS_BATT have to be powered up on the assigned pins of the B2B connectors as listed on the section "Power Rails". Except 'PS_BATT' (see section "Recommended Operation

Conditions"), all power-rails can be powered from 3.3V power sources (also share the same source, if power domain control is not required).

There are following dependencies how the initial voltages of the power rails on the B2B connectors are distributed to the on-board DC-DC converters, which power up further DC-DC converters and the particular on-board voltages:

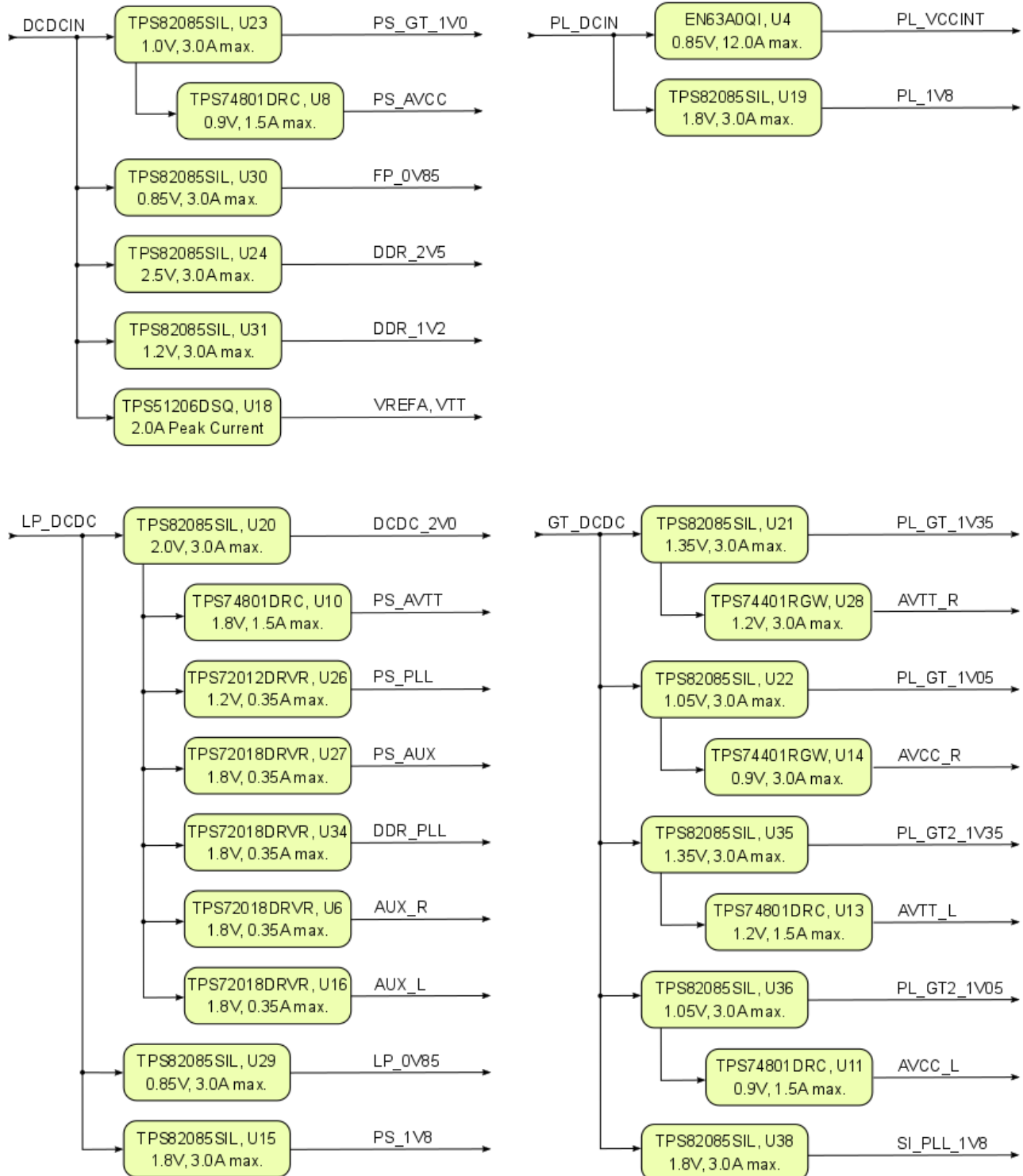



Figure 3: Power Distribution Diagram.

 Current rating of Samtec Razor Beam LP Terminal/Socket Strip ST5/SS5 B2B connectors is 1.5 A per pin (1 pin powered per row).

6.3 Power-On Sequence Diagram

The TE0808 SoM meets the recommended criteria to power up the Xilinx Zynq UltraScale+ MPSoC properly by keeping a specific sequence of enabling the on-board DC-DC converters dedicated to the particular Power Domains and powering up the on-board voltages.

The on-board voltages of the TE0808 SoM will be powered-up in order of a determined sequence by activating the above-mentioned power rails and the Enable-Signals of the DC-DC converters. The on-board voltages will be powered up at three steps.

1. Low-Power Domain (LPD) and on-board Si5345A programmable clock generator supply voltage
2. Programmable Logic (PL) and Full-Power Domain (FPD)
3. GTH, PS GTR transceiver and DDR memory

Hence, those three power instances will be powered up consecutively and the Power-Good-Signals of the previous instance has to be asserted.

Following diagram describes the sequence of enabling the three power instances utilizing the DC-DC converter control signals (Enable, Power-Good), which will power-up in descending order as listed in the blocks of the diagram.

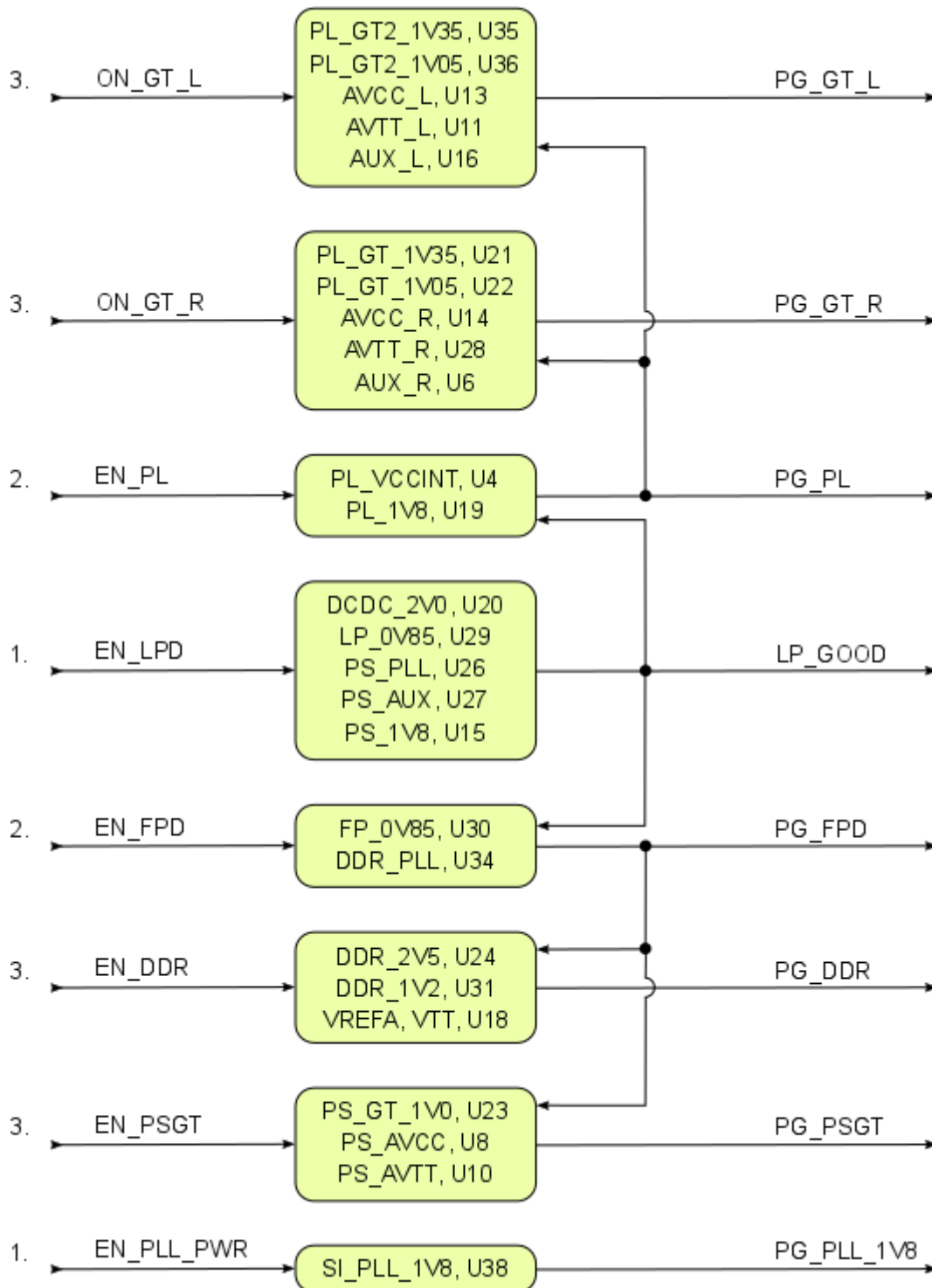



Figure 4: Power-On Sequence Utilizing DC-DC Converter Control Signals.

6.4 Operation Conditions of the DC-DC Converter Control Signals

The control signals have to be asserted on the B2B connector J2, whereby some of the Power-Good signals need external pull-up resistors.

Enable-Signal	B2B Connector Pin	Max. Voltage	Note	Power-Good-Signal	B2B Connector Pin	Pull-up Resistor	Note
EN_LPD	J2-108	6V	TPS82085SIL data sheet	LP_GOOD	J2-106	4K7, pulled up to LP_DCDC	-
EN_FPD	J2-102	DCDCIN	NC7S08P5X data sheet	PG_FPD	J2-110	4K7, pulled up to DCDCIN	-
EN_PL	J2-101	PL_DCIN	left floating for logic high (drive to GND for logic low)	PG_PL	J2-104	External pull-up needed (max. voltage GT_DCDC), max. sink current 1 mA	TPS82085SIL / NC7S08P5X data sheet
EN_DDR	J2-112	DCDCIN	NC7S08P5X data sheet	PG_DDR	J2-114	4K7, pulled up to DCDCIN	-
EN_PSGT	J2-84	DCDCIN	NC7S08P5X data sheet	PG_PSGT	J2-82	External pull-up needed (max. 5.5V), max. sink current 1 mA	TPS74801 data sheet
EN_GT_R	J2-95	GT_DCDC	NC7S08P5X data sheet	PG_GT_R	J2-91	External pull-up needed (max. 5.5V), max. sink current 1 mA	TPS74401 data sheet
EN_GT_L	J2-79	GT_DCDC	NC7S08P5X data sheet	PG_GT_L	J2-97	External pull-up needed (max. 5.5V), max. sink current 1 mA	TPS74801 data sheet
EN_PLL_PWR	J2-77	6V	TPS82085SIL data sheet	PG_PLL_1V8	J2-80	External pull-up needed (max. 5.5V), max. sink current 1 mA	TPS82085SIL data sheet

Table 16: Recommended operation conditions of DC-DC converter control signals.

 To avoid any damage to the MPSoC module, check for stabilized on-board voltages in steady state before powering up the MPSoC's I/O bank voltages VCCOx. All I/Os should be tri-stated during power-on sequence.

Core voltages and main supply voltages have to reach stable state and their "Power Good"-signals have to be asserted before other voltages like bank's I/O voltages (VCCOx) can be powered up.

It is important that all PS and PL I/Os are tri-stated at power-on until the "Power Good"-signals are high, meaning that all on-module voltages have become stable and module is properly powered up.

See Xilinx datasheet [DS925](#) for additional information. User should also check related base board documentation when intending base board design for TE0808 SoM.

6.5 Voltage Monitor Circuit

The voltages LP_DCDC and LP_0V85 are monitored by the voltage monitor circuit U41, which generates the POR_B reset signal at power-on. A manual reset is also possible by driving the MR-pin (J2-83) to GND. Leave this pin unconnected or connect to VDD (LP_DCDC) when unused.

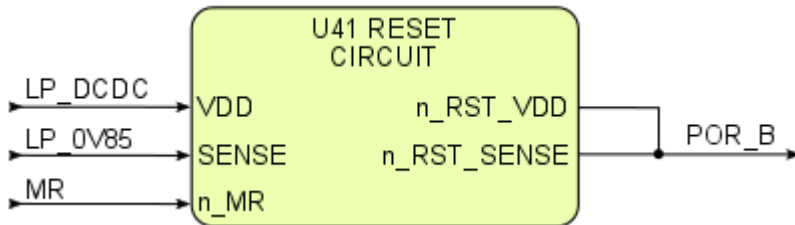


Figure 5: Voltage monitor circuit

6.6 Power Rails

Power Rail Name	B2B J1 Pins	B2B J2 Pins	B2B J3 Pins	Directions	Note
PL_DCIN	151, 153, 157, 159	-	-	Input	-
DCDCIN	-	154, 156, 158, 160, 153, 155, 157, 159	-	Input	-
LP_DCDC	-	138, 140, 142, 144	-	Input	-
PS_BATT	-	125	-	Input	-
GT_DCDC	-	-	157, 158, 159, 160	Input	-
PLL_3V3	-	-	152	Input	U5 (programmable PLL) 3.3V nominal input
SI_PLL_1V8	-	-	151	Output	Internal voltage level 1.8V nominal output
PS_1V8	-	99	147, 148	Output	Internal voltage level 1.8V nominal output
PL_1V8	91, 121	-	-	Output	Internal voltage level 1.8V nominal output

Power Rail Name	B2B J1 Pins	B2B J2 Pins	B2B J3 Pins	Directions	Note
DDR_1V2	-	135	-	Output	Internal voltage level 1.2V nominal output

Table 17: Power rails of the MPSoC module on accessible connectors.

6.7 Bank Voltages

Bank	Type	Schematic Name / B2B Connector Pins	Voltage	Reference Input Voltage	Voltage Range
47	HD	VCCO47, pins J3-43, J3-44	user	-	max. 3.3V
48	HD	VCCO48, pins J3-15, J3-16	user	-	max. 3.3V
64	HP	VCCO64, J4-58, J4-106	user	VREF_64, pin J4-88	max. 1.8V
65	HP	VCCO65, J4-69, J4-105	user	VREF_65, pin J4-15	max. 1.8V
66	HP	VCCO66, J1-90, J1-120	user	VREF_66, pin J1-108	max. 1.8V
500	MIO	PS_1V8	1.8V	-	-
501	MIO	PS_1V8	1.8V	-	-
502	MIO	PS_1V8	1.8V	-	-
503	CON FIG	PS_1V8	1.8V	-	-

Table 18: Range of MPSoC module's bank voltages.

7 B2B connectors

5.2 x 7.6 cm UltraSoM+ modules use four Samtec Razor Beam LP Terminal Strip (**ST5**) on the bottom side.

- 4x REF-192552-02 (160-pins)
 - ST5 Mates with SS5

5.2 x 7.6 cm UltraSoM+ carrier use four Samtec Razor Beam LP Socket Strip (**SS5**) on the top side.

- 4x REF192552-01 (160-pins)
 - SS5 Mates with ST5

7.1 Features

- Board-to-Board Connector 160-pins, 80 contacts per row
- Ultrafine .0197" (0.50 mm) pitch
- Narrow body design saves space on board
- Lead style -03.5
- Samtec 28+ Gbps Solution
- Mates with: ST5
- Insulator Material: Liquid Crystal Polymer, schwarz
- Operating Temperature Range: -55°C bis +125°C
- Lead-Free Solderable: Yes
- RoHS Konform: Yes

7.2 Connector Stacking height

When using the standard type on baseboard and module, the mating height is 5 mm.

Other mating heights are possible by using connectors with a different height:

Order number	REF number	Samtec Number	Type	Contribution to stacking height	Comment
27219	REF192552-01	SS5-80-3.50-L-D-K-TR	Baseboard connector	3.5mm	Standard connector used on modules
27018	REF-189545-02	SS5-80-3.00-L-D-K-TR	Baseboard connector	3 mm	Assembly option on request
27220	REF-192552-02	ST5-80-1.50-L-D-P-TR	Module connector	1.5 mm	Standard connector used on modules
27017	REF-189545-01	ST5-80-1.00-L-D-P-TR	Module connector	1 mm	Assembly option on request

The module can be manufactured using other connectors upon request.

7.3 Current Rating

Current rating of Samtec Razor Beam LP Terminal/Socket Strip ST5/SS5 B2B connectors is 1.5 A per pin (1 pin powered per row).

8 Variants Currently In Production

Module Variant	Zynq UltraScale+ MPSoC	DDR 4	Junction Temperature	Operating Temperature Range
TE0808-04-09EG-1 EA	XCZU9EG-1FFVC900E	2GB	0°C - 100°C	Extended Temperature Range
TE0808-04-09EG-1 EB	XCZU9EG-1FFVC900E	4GB	0°C - 100°C	Extended Temperature Range
TE0808-04-09EG-1 ED ⁽¹⁾	XCZU9EG-1FFVC900E	4GB	0°C - 100°C	Extended Temperature Range
TE0808-04-09EG-2 IB	XCZU9EG-2FFVC900I	4GB	-40°C - 100°C	Industrial Temperature Range

(1) Note: Lower B2B connector profile, check distance bolt of between module and carrier

Table 19: Differences between variants of Module TE0808-04

9 Technical Specifications

9.1 Absolute Maximum Ratings

Parameter	Min	Max	Unit	Notes / Reference Document
PL_DCIN	-0.3	7	V	TPS82085SIL / EN63A0QI data sheet
DCDCIN	-0.3	7	V	TPS82085SIL / TPS51206 data sheet
LP_DCDC	-0.3	4	V	TPS3106K33DBVR data sheet
GT_DCDC	-0.3	7	V	TPS82085SIL data sheet
PS_BATT	-0.5	2	V	Xilinx DS925 data sheet
PLL_3V3	-0.5	3.8	V	Si5345/44/42 data sheet
VCCO for HD I/O banks	-0.5	3.4	V	Xilinx DS925 data sheet
VCCO for HP I/O banks	-0.5	2	V	Xilinx DS925 data sheet
VREF	-0.5	2	V	Xilinx DS925 data sheet
I/O input voltage for HD I/O banks	-0.55	VCCO + 0.55	V	Xilinx DS925 data sheet
I/O input voltage for HP I/O banks	-0.55	VCCO + 0.55	V	Xilinx DS925 data sheet
PS I/O input voltage (MIO pins)	-0.5	VCCO_PSIO + 0.55	V	Xilinx DS925 data sheet, VCCO_PSIO 1.8V nominally
Receiver (RXP/RXN) and transmitter (TXP/TXN) absolute input voltage	-0.5	1.2	V	Xilinx DS925 data sheet
Voltage on input pins of NC7S08P5X 2-Input AND Gate	-0.5	VCC + 0.5	V	NC7S08P5X data sheet, see schematic for VCC
Voltage on input pins (nMR) of TPS3106K33DBVR Voltage Monitor, U41	-0.3	VDD + 0.3	V	TPS3106 data sheet, VDD = LP_DCDC
"Enable"-signals on TPS82085SIL (EN_PLL_PWR, EN_LPD)	-0.3	7	V	TPS82085SIL data sheet
Storage temperature (ambient)	-40	100	°C	ROHM Semiconductor SML-P11 Series data sheet

 Assembly variants for higher storage temperature range are available on request.

10 Revision History



10.1 Hardware Revision History

Date	Revision	Notes	Link to PCN	Documentation Link
-	04	First production silicon	-	TE0808-04
-	03	Second ES production release	-	TE0808-03
2016-03-09	02	First ES production release	-	TE0808-02
-	01	Prototypes	-	-

Hardware revision number is written on the PCB board together with the module model number separated by the dash.



10.2 Document Change History

Date	Revision	Contributors	Description
 2018-06-28	v.26	John Hartfiel	<ul style="list-style-type: none"> typo SI5348 B2B IOs + link correction
 13.11.2017	v.24	Ali Naseri	<ul style="list-style-type: none"> updated B2B connector max. current rating per pin
2017-11-13	v.22	John Hartfiel	<ul style="list-style-type: none"> rework B2B section
2017-10-20	v.21	Ali Naseri	<ul style="list-style-type: none"> Update links (pdf, documentation) to revision 4 ES silicon note removed
2017-08-28	v.15	John Hartfiel	<ul style="list-style-type: none"> Update section: Variants Currently In Production
2017-08-28	v.14	Jan Kumann	<ul style="list-style-type: none"> Block diagram changed. SPI flash section fixed. Few smaller improvements.
2017-08-15	v.12	Vitali Tsiukala	Changed signals count in the B2B connectors table
2017-08-15	v.11	John Hartfiel, Ali Naseri	<ul style="list-style-type: none"> PCB REV04 Initial release update boot mode section
2017-02-06	v.1	Jan Kumann	Initial document

any substance. For that, Trenz Electronic is obliged to neither register nor to provide safety data sheet. According to present knowledge and to best of our knowledge, no [SVHC \(Substances of Very High Concern\) on the Candidate List](#) are contained in our products. Furthermore, we will immediately and unsolicited inform our customers in compliance with REACH - Article 33 if any substance present in our goods (above a concentration of 0,1 % weight by weight) will be classified as SVHC by the [European Chemicals Agency \(ECHA\)](#).

RoHS

Trenz Electronic GmbH herewith declares that all its products are developed, manufactured and distributed RoHS compliant.

WEEE

Information for users within the European Union in accordance with Directive 2002/96/EC of the European Parliament and of the Council of 27 January 2003 on waste electrical and electronic equipment (WEEE).

Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.