Trenz Electronic GmbH - TE0808-04-15EG-1EE Datasheet

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Understanding Embedded - Microcontroller, Microprocessor, FPGA Modules

Embedded - Microcontroller, Microprocessor, and FPGA Modules are fundamental components in modern electronic systems, offering a wide range of functionalities and capabilities. Microcontrollers are compact integrated circuits designed to execute specific control tasks within an embedded system. They typically include a processor, memory, and input/output peripherals on a single chip. Microprocessors, on the other hand, are more powerful processing units used in complex computing tasks, often requiring external memory and peripherals. FPGAs (Field Programmable Gate Arrays) are highly flexible devices that can be configured by the user to perform specific logic functions, making them invaluable in applications requiring customization and adaptability.

Applications of Embedded - Microcontroller,

Details	
Product Status	Obsolete
Module/Board Type	MPU Core
Core Processor	Zynq UltraScale+ XCZU15EG-1FFVC900E
Co-Processor	-
Speed	-
Flash Size	128MB
RAM Size	2GB
Connector Type	B2B
Size / Dimension	2.05" x 2.99" (52mm x 76mm)
Operating Temperature	0°C ~ 85°C
Purchase URL	https://www.e-xfl.com/product-detail/trenz-electronic/te0808-04-15eg-1ee

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2.2 Block Diagram

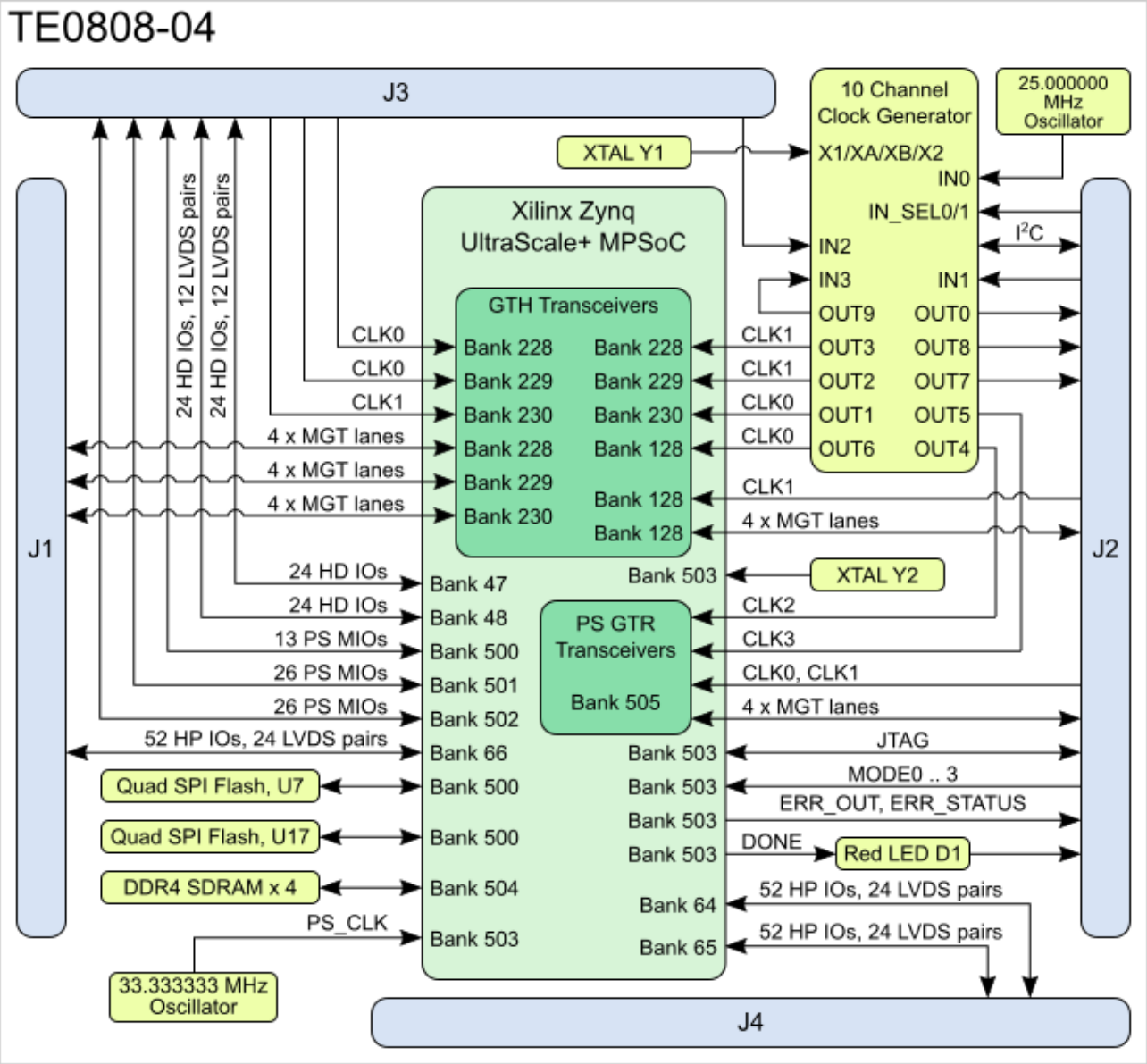

Figure 1: TE0808-04 Block Diagram.

2.3 Main Components

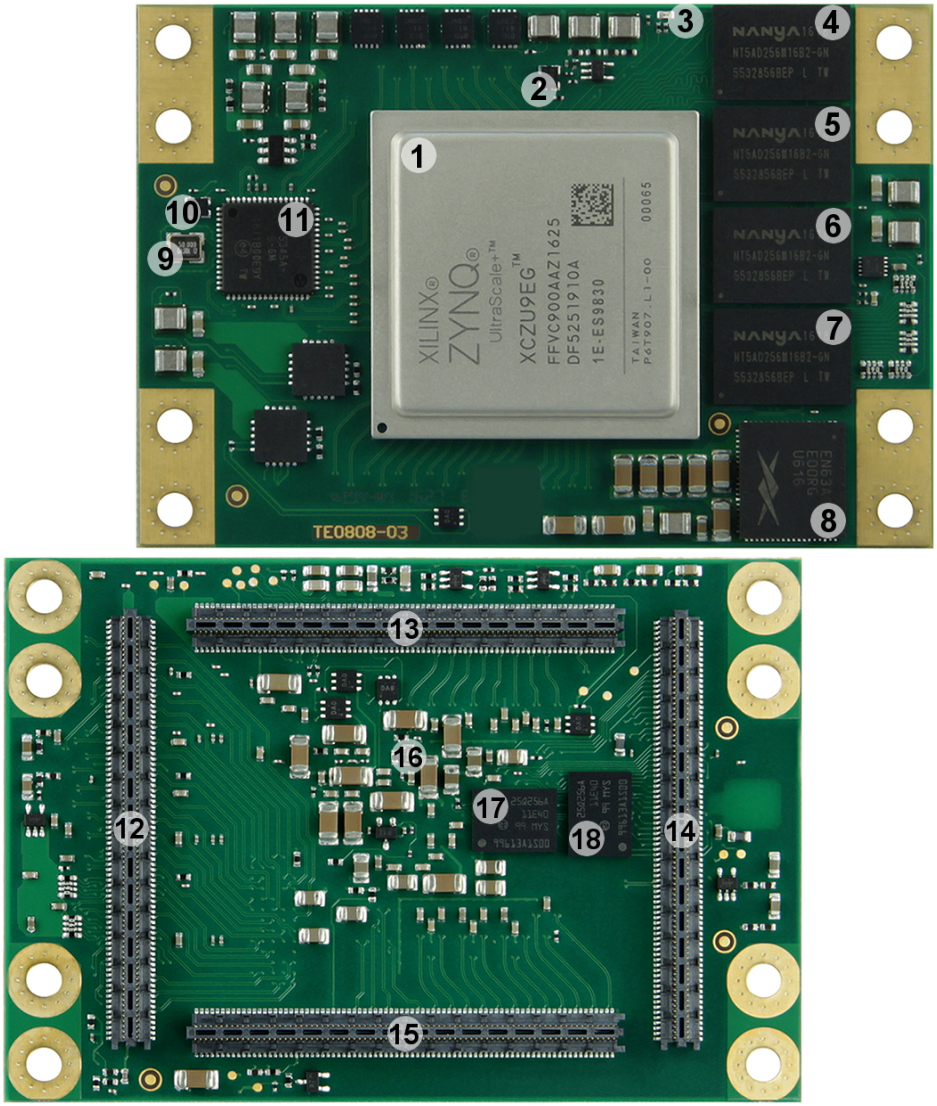

Figure 2: TE0808 MPSoC module.

1. Xilinx ZYNQ UltraScale+ XCZU9EG MPSoC, U1
2. Low-power programmable oscillator @ 33.333333 MHz (PS_CLK), U32
3. Red LED (DONE), D1
4. 256Mx16 DDR4-2400 SDRAM, U12
5. 256Mx16 DDR4-2400 SDRAM, U9
6. 256Mx16 DDR4-2400 SDRAM, U2
7. 256Mx16 DDR4-2400 SDRAM, U3
8. 12A PowerSoC DC-DC converter, U4
9. Quartz crystal, Y1
10. Low-power programmable oscillator @ 25.000000 MHz (IN0 for U5), U25
11. 10-channel programmable PLL clock generator, U5
12. Ultra fine 0.50 mm pitch, Razor Beam™ LP Slim Terminal Strip with 160 contacts, J4
13. Ultra fine 0.50 mm pitch, Razor Beam™ LP Slim Terminal Strip with 160 contacts, J2
14. Ultra fine 0.50 mm pitch, Razor Beam™ LP Slim Terminal Strip with 160 contacts, J3
15. Ultra fine 0.50 mm pitch, Razor Beam™ LP Slim Terminal Strip with 160 contacts, J1
16. Quartz crystal, Y2

3 Signals, Interfaces and Pins

3.1 Board to Board (B2B) connectors

The TE0808 MPSoC SoM has four Board to Board (B2B) connectors with 160 contacts per connector.

Each connector has a specific arrangement of the signal pins, which are grouped together in categories related to their functionalities and to their belonging to particular units of the Zynq UltraScale+ MPSoC like I/O banks, interfaces and Gigabit transceivers
or to the on-board peripherals.

Following table lists the I/O-bank signals, which are routed from the MPSoC's PL and PS banks as LVDS pairs or single ended I/O's to the B2B connectors.

Bank	Type	B2B Connector	Schematic Names / Connector Pins	I/O Signals	LVDS Pairs	VCCO Bank Voltage	Notes
47	HD	J3	B47_L1_P ... B47_L12_P B47_L1_N ... B47_L12_N	24 I/Os	12	VCCO47 pins J3-43, J3-44	VCCO max. 3.3V usable as single-ended I/Os
48	HD	J3	B48_L1_P ... B48_L12_P B48_L1_N ... B48_L12_N	24 I/Os	12	VCCO48 pins J3-15, J3-16	VCCO max. 3.3V usable as single-ended I/Os
64	HP	J4	B64_L1_P ... B64_L24_P B64_L1_N ... B64_L24_N B_64_T0 ... B_64_T3	52 I/O's	24	VCCO64 pins J4-58, J4-106	VCCO max. 1.8V usable as single-ended I/Os
65	HP	J4	B65_L1_P ... B65_L24_P B65_L1_N ... B65_L24_N B_65_T0 ... B_65_T3	52 I/Os	24	VCCO65 pins J4-69, J4-105	VCCO max. 1.8V usable as single-ended I/Os
66	HP	J1	B66_L1_P ... B66_L24_P B66_L1_N ... B66_L24_N B_66_T0 ... B_66_T3	48 I/Os	24	VCCO66 pins J1-90, J1-120	VCCO max. 1.8V usable as single-ended I/Os
500	MIO	J3	MIO13 ... MIO25	13 I/Os	-	PS_1V8	User configurable I/Os on B2B
501	MIO	J3	MIO26 ... MIO51	26 I/Os	-	PS_1V8	User configurable I/Os on B2B
502	MIO	J3	MIO52 ... MIO77	26 I/Os	-	PS_1V8	User configurable I/Os on B2B

Table 2: B2B connector pin-outs of available PL and PS banks of the TE0808-04 SoM.

All MIO banks are powered from on-module DC-DC power rail. All PL I/O Banks have separate VCCO pins in the B2B connectors, valid VCCO should be supplied from the baseboard.

For detailed information about the B2B pin-out, please refer to the Pin-out table.

The configuration of the I/O's MIO13 - MIO77 are depending on the base-board peripherals connected to these pins.

3.2 MGT Lanes

The B2B connector J1 and J2 provide also access to the MGT banks of the Zynq UltraScale+ MPSoC. There are 20 high-speed data lanes (Xilinx GTH / GTR transceiver) available composed as differential signaling pairs for both directions (RX/TX).

The MGT banks have also clock input-pins which are exposed to the B2B connectors J2 and J3. Following MGT lanes are available on the B2B connectors:

Bank	Type	B2B Connector	Count of MGT Lanes	Schematic Names / Connector Pins	MGT Bank's Reference Clock Inputs
228	GTH	J1	4 GTH lanes (4 RX / 4 TX)	B228_RX3_P, B228_RX3_N, pins J1-27, J1-29 B228_TX3_P, B228_TX3_N, pins J1-26, J1-28	1 reference clock signal (B228_CLK0) from B2B connector J3 (pins J3-60, J3-62) to bank's pins R8/R7
				B228_RX2_P, B228_RX2_N, pins J1-33, J1-35 B228_TX2_P, B228_TX2_N, pins J1-32, J1-34	1 reference clock signal (B228_CLK1) from programmable PLL clock generator U5 to bank's pins N8/N7
				B228_RX1_P, B228_RX1_N, pins J1-39, J1-41 B228_TX1_P, B228_TX1_N, pins J1-38, J1-40	
				B228_RX0_P, B228_RX0_N, pins J1-45, J1-47 B228_TX0_P, B228_TX0_N, pins J1-44, J1-46	
229	GTH	J1	4 GTH lanes (4 RX / 4 TX)	B229_RX3_P, B229_RX3_N, pins J1-27, J1-29 B229_TX3_P, B229_TX3_N, pins J1-26, J1-28	1 reference clock signal (B229_CLK0) from B2B connector J3 (pins J3-65, J3-67) to bank's pins L8/L7
				B229_RX2_P, B229_RX2_N, pins J1-33, J1-35 B229_TX2_P, B229_TX2_N, pins J1-32, J1-34	1 reference clock signal (B229_CLK1) from programmable PLL clock generator U5 to bank's pins J8/J7
				B229_RX1_P, B229_RX1_N, pins J1-39, J1-41 B229_TX1_P, B229_TX1_N, pins J1-38, J1-40	
				B229_RX0_P, B229_RX0_N, pins J1-45, J1-47 B229_TX0_P, B229_TX0_N, pins J1-44, J1-46	

5 On-board Peripherals

5.1 Flash

The TE0808 SoM can be configured with max. 512 MByte Flash memory for configuration and operation.

Name	IC	Designator	PS7	MIO	Notes
SPI Flash	N25Q256A11E1240E	U7	QSPI0	MIO0 ... MIO5	dual parallel booting possible, 32 MByte memory per Flash IC at standard configuration
SPI Flash	N25Q256A11E1240E	U17	QSPI0	MIO7 ... MIO12	as above

Table 10: Peripherals connected to the PS MIO pins.

5.2 DDR4 SDRAM

The TE0808-04 SoM is equipped with with four DDR4-2400 SDRAM modules with up to 8 GByte memory density. The SDRAM modules are connected to the Zynq MPSoC's PS DDR controller (bank 504) with a 64-bit data bus.

Refer to the Xilinx Zynq UltraScale+ datasheet DS925 for more information on whether the specific package of the Zynq UltraScale+ MPSoC supports the maximum data transmission rate of 2400 MByte/s.

5.3 Programmable PLL Clock Generator

Following table illustrates on-board Si5345A programmable clock multiplier chip inputs and outputs:

Input	Connected to	Frequency	Notes
IN0	On-board Oscillator (U25)	25.000000 MHz	-
IN1	B2B Connector pins J2-4, J2-6 (differential pair)	User	AC decoupling required on base
IN2	B2B Connector pins J3-66, J3-68 (differential pair)	User	AC decoupling required on base
IN3	OUT9	User	Loop-back from OUT9
Output	**Connected to**	**Frequency**	**Notes**
OUT0	B2B Connector pins J2-3, J2-1 (differential pair)	User	Default off
OUT1	B230 CLK0	User	Default off
OUT2	B229 CLK1	User	Default off
OUT3	B228 CLK1	User	Default off
OUT4	B505 CLK2	User	Default off
OUT5	B505 CLK3	User	Default off
OUT6	B128 CLK0	User	Default off

OUT7	B2B Connector pins J2-7, J2-9 (differential pair)	User	Default off
OUT8	B2B Connector pins J2-13, J2-15 (differential pair)	User	Default off
OUT9	IN3 (Loop-back)	User	Default off
XA/XB	Quartz (Y1)	50.000 MHz	-

Table 11: Programmable PLL clock generator input/output.

The Si5345A programmable clock generator's control interface pins are exposed to B2B connector J2. For further information refer to the Si5345A data sheet.

Signal	B2B Connector Pin	Function
PLL_FINC	J2-81	Frequency increment.
PLL_LOLN	J2-85	Loss of lock (active-low).
PLL_SEL0 / PLL_SEL1	J2-93 / J2-87	Manual input switching.
PLL_FDEC	J2-94	Frequency decrement.
PLL_RST	J2-59	Device reset (active-low)
PLL_SCL / PLL_SDA	J2-90 / J2-92	I^2C interface, external pull-ups needed for SCL / SDA lines. I^2C address in current configuration: 1101000b.

Table 12: B2B connector pin-out of Si5345A programmable clock generator.

⚠ Si5345 OTP ROM is not programmed by default at delivery, so it is customers responsibility to either configure Si5345 during FSBL or then use SiLabs programmer and program the OTP ROM with customer fixed clock setup.

Si5345 OTP can only be programmed two times, as different user configurations may required different setup TE0808 is normally shipped with blank OTP.
For more information refer to Si5345 at SiLabs.

5.4 Oscillators

The TE0808-04 SoM is equipped with two on-board oscillators to provide the Zynq's MPSoC's PS configuration bank 503 with reference clock signals.

Clock	Frequency	Bank 503 Pin	Connected to
PS_CLK	33.333333 MHz	P20	MEMS Oscillator, U32
PS_PAD (RTC)	32.768 kHz	R22/R23	Quartz crystal, Y2

Table 13: Reference clock-signals to PS configuration bank 503.

5.5 On-board LEDs

LED	Color	Connected to	Description and Notes
D1	Red	DONE signal (PS Configuration Bank 503)	This LED goes ON when power has been applied to the module and stays ON until MPSoC's programmable logic is configured properly.

Table 14: LED's description.

6 Power and Power-On Sequence

6.1 Power Consumption

The maximum power consumption of a module mainly depends on the design which is running on the FPGA.

Xilinx provide a power estimator excel sheets to calculate power consumption. It's also possible to evaluate the power consumption of the developed design with Vivado. See also Trenz Electronic Wiki FAQ.

Power Input Pin	Typical Current
DCDCIN	TBD*
LP_DCDC	TBD*
PL_DCIN	TBD*
PS_BATT	TBD*

Table 15: Maximum current of power supplies. *to be determined soon with reference design setup.

Power supply with minimum current capability of 3A for system startup is recommended. For the lowest power consumption and highest efficiency of on board DC/DC regulators it is recommended to powering the module from one single 3.3V supply. Except 'PS_BATT', all input power supplies have a nominal value of 3.3V. Although the input power supplies can be powered up in any order, it is recommended to power them up simultaneously.

The TE0808 module equipped with the Xilinx Zynq UltraScale+ MPSoC delivers a heterogeneous multi-processing system with integrated programmable logic and independently operable elements and is designed to meet embedded system power management requirement by advanced power management features. This features allow to offset the power and heat constraints against overall performance and operational efficiency.

This features allowing highly flexible power management are achieved by establishing Power Domains for power isolation. The Zynq UltraScale+ MPSoC has multiple power domains, whereby each power domain requires its own particular external DC-DC converters.

The Processing System contains three Power Domains:

- Battery Power Domain (BBRAM and RTC)
- Full-Power Domain (Application Processing Unit, DDR Controller, Graphics Processing Unit and High-Speed Connectivity)
- Low-Power Domain (Real-Time Processing Unit, Security and Configuration Unit, Platform Management Unit, System Monitor and General Connectivity)

The fourth Power Domain is for the Programmable Logic (PL). If individual Power Domain control is not required, power rails can be shared between domains.

On the TE0808-04 SoM, following power domains can be powered up individually with power rails available on the B2B connectors:

- Full-power domain, supplied by power rail **DCDCIN**
- Low-power domain, supplied by power rail **LP_DCDC**
- Programmable logic, supplied by power rail **PL_DCIN**
- Battery power domain, supplied by power rail **PS_BATT**

Each power domain has its own enable and power good signals. The power rail **GT_DCDC** is needed to generate the voltages for the Multi Gigabit Transceiver units of the Zynq UltraScale+ MPSoC.

6.2 Power Distribution Dependencies

The power rails DCDCIN, LP_DCDC, PL_DCIN, PS_BATT have to be powered up on the assigned pins of the B2B connectors as listed on the section "Power Rails". Except 'PS_BATT' (see section "Recommended Operation

Conditions"), all power-rails can be powered from 3.3V power sources (also share the same source, if power domain control is not required).

There are following dependencies how the initial voltages of the power rails on the B2B connectors are distributed to the on-board DC-DC converters, which power up further DC-DC converters and the particular on-board voltages:

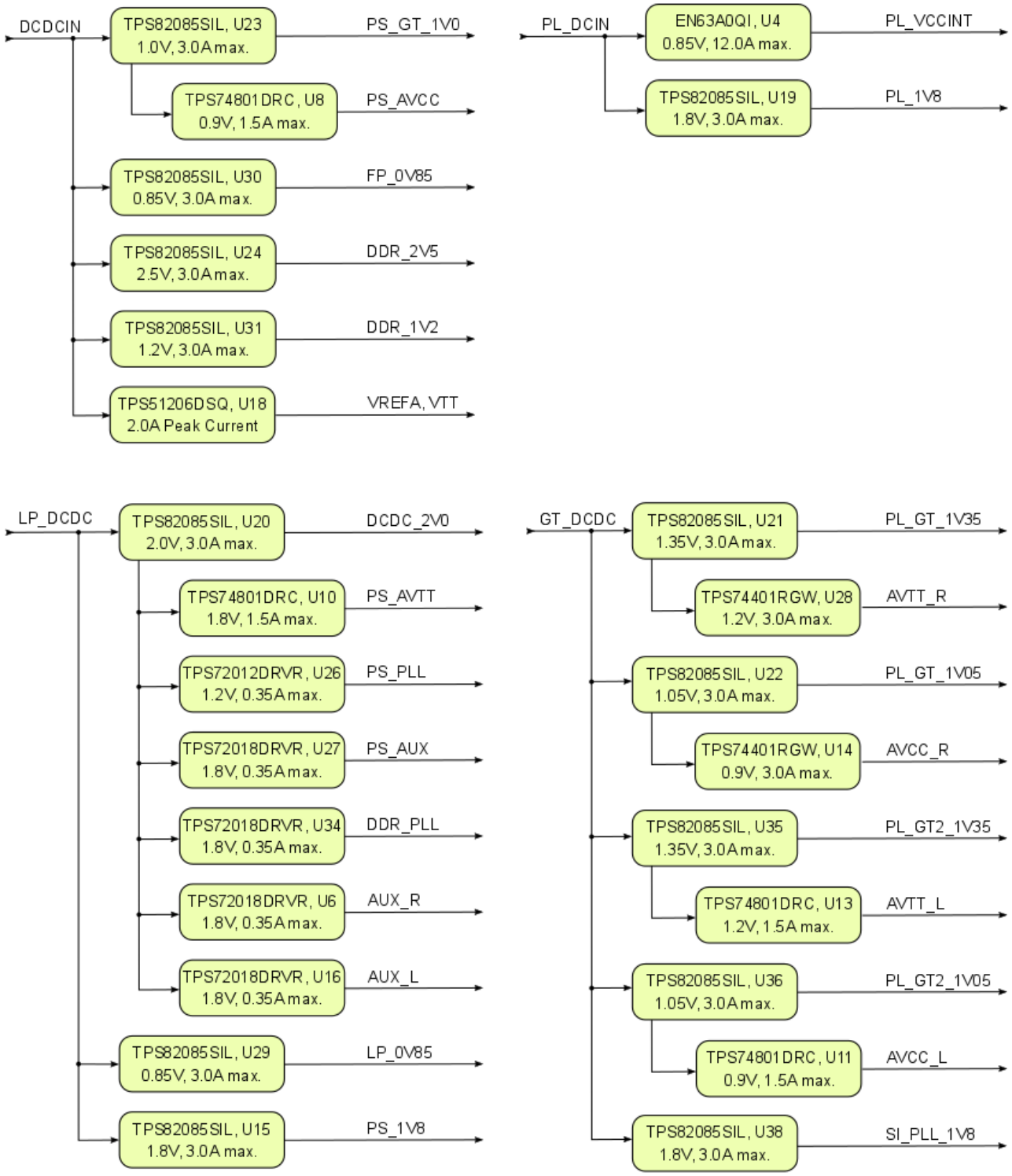

Figure 3: Power Distribution Diagram.

⚠ Current rating of Samtec Razor Beam LP Terminal/Socket Strip ST5/SS5 B2B connectors is 1.5 A per pin (1 pin powered per row).

6.3 Power-On Sequence Diagram

The TE0808 SoM meets the recommended criteria to power up the Xilinx Zynq UltraScale+ MPSoC properly by keeping a specific sequence of enabling the on-board DC-DC converters dedicated to the particular Power Domains and powering up the on-board voltages.

The on-board voltages of the TE0808 SoM will be powered-up in order of a determined sequence by activating the above-mentioned power rails and the Enable-Signals of the DC-DC converters. The on-board voltages will be powered up at three steps.

1. Low-Power Domain (LPD) and on-board Si5345A programmable clock generator supply voltage
2. Programmable Logic (PL) and Full-Power Domain (FPD)
3. GTH, PS GTR transceiver and DDR memory

Hence, those three power instances will be powered up consecutively and the Power-Good-Signals of the previous instance has to be asserted.

Following diagram describes the sequence of enabling the three power instances utilizing the DC-DC converter control signals (Enable, Power-Good), which will power-up in descending order as listed in the blocks of the diagram.

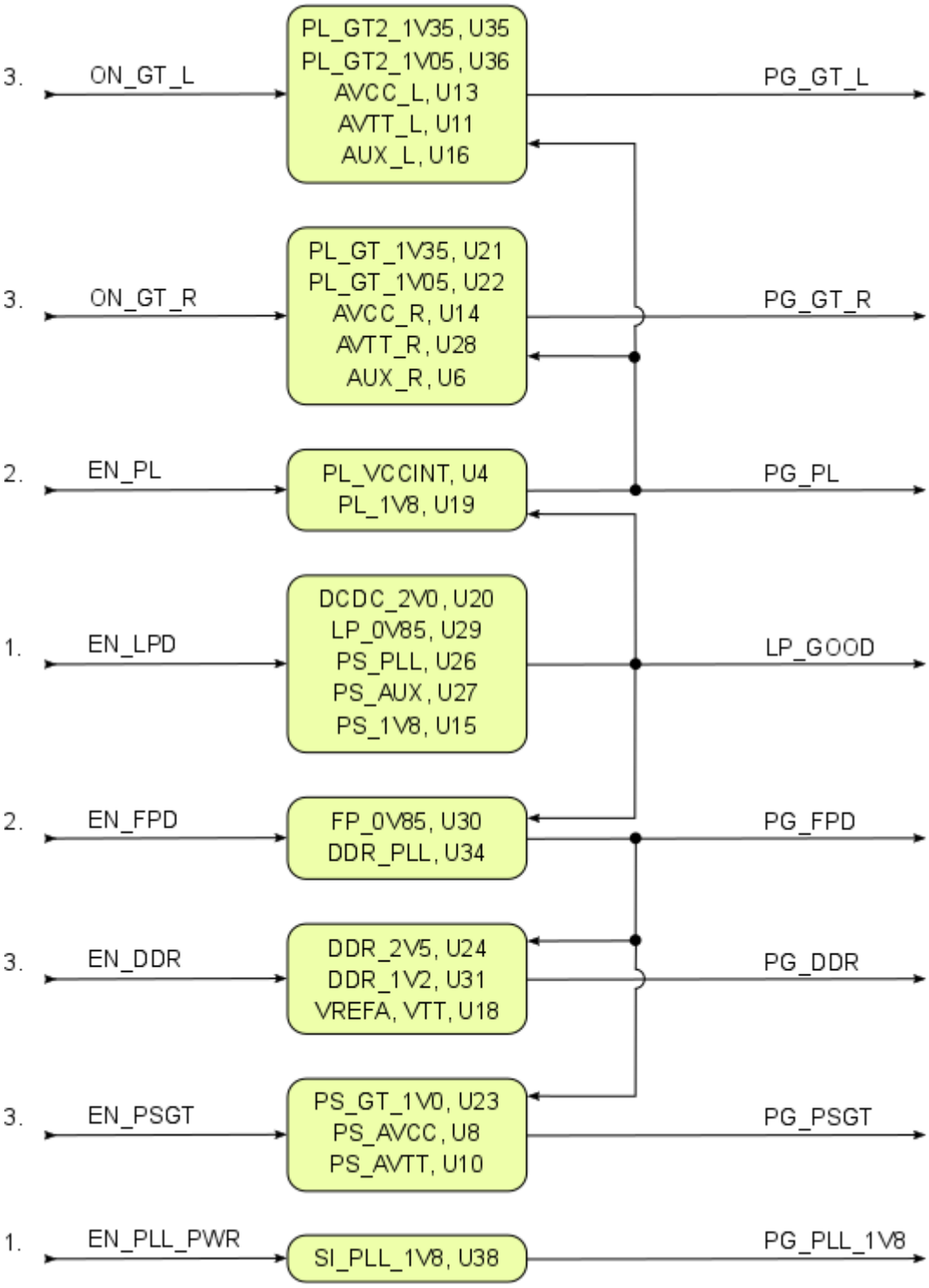

Figure 4: Power-On Sequence Utilizing DC-DC Converter Control Signals.

6.4 Operation Conditions of the DC-DC Converter Control Signals

The control signals have to be asserted on the B2B connector J2, whereby some of the Power-Good signals need external pull-up resistors.

Enable-Signal	B2B Connector Pin	Max. Voltage	Note	Power-Good-Signal	B2B Connector Pin	Pull-up Resistor	Note
EN_LPD	J2-108	6V	TPS82085SIL data sheet	LP_GOOD	J2-106	4K7, pulled up to LP_DCDC	-
EN_FPD	J2-102	DCDCIN	NC7S08P5X data sheet	PG_FPD	J2-110	4K7, pulled up to DCDCIN	-
EN_PL	J2-101	PL_DCIN	left floating for logic high (drive to GND for logic low)	PG_PL	J2-104	External pull-up needed (max. voltage GT_DCDC), max. sink current 1 mA	TPS82085SIL / NC7S08P5X data sheet
EN_DDR	J2-112	DCDCIN	NC7S08P5X data sheet	PG_DDR	J2-114	4K7, pulled up to DCDCIN	-
EN_PSGT	J2-84	DCDCIN	NC7S08P5X data sheet	PG_PSGT	J2-82	External pull-up needed (max. 5.5V), max. sink current 1 mA	TPS74801 data sheet
EN_GT_R	J2-95	GT_DCDC	NC7S08P5X data sheet	PG_GT_R	J2-91	External pull-up needed (max. 5.5V), max. sink current 1 mA	TPS74401 data sheet
EN_GT_L	J2-79	GT_DCDC	NC7S08P5X data sheet	PG_GT_L	J2-97	External pull-up needed (max. 5.5V), max. sink current 1 mA	TPS74801 data sheet
EN_PLL_PWR	J2-77	6V	TPS82085SIL data sheet	PG_PLL_1V8	J2-80	External pull-up needed (max. 5.5V), max. sink current 1 mA	TPS82085SIL data sheet

Table 16: Recommended operation conditions of DC-DC converter control signals.

To avoid any damage to the MPSoC module, check for stabilized on-board voltages in steady state before powering up the MPSoC's I/O bank voltages VCCOx. All I/Os should be tri-stated during power-on sequence.

Core voltages and main supply voltages have to reach stable state and their "Power Good"-signals have to be asserted before other voltages like bank's I/O voltages (VCCOx) can be powered up.

It is important that all PS and PL I/Os are tri-stated at power-on until the "Power Good"-signals are high, meaning that all on-module voltages have become stable and module is properly powered up.

See Xilinx datasheet DS925 for additional information. User should also check related base board documentation when intending base board design for TE0808 SoM.

7.4 Connector Speed Ratings

The connector speed rating depends on the stacking height:

Stacking height	Speed rating
4 mm, Single-Ended	13GHz/26Gbps
4 mm, Differential	13.5GHz/27Gbps
5 mm, Single-Ended	13.5GHz/27Gbps
5 mm, Differential	20GHz/40 Gbps

The SS5/ST5 series board-to-board spacing is currently available in 4mm (0.157"), 4.5mm (0.177") and 5mm (0.197") stack heights.

The data in the reports is applicable only to the 4mm and 5mm board-to-board mated connector stack height.

7.5 Manufacturer Documentation

Geändert
30 05, 2017 by Susanne Kunath
30 05, 2017 by Susanne Kunath
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13 11, 2017 by John Hartfiel
13 11, 2017 by John Hartfiel

8 Variants Currently In Production

Module Variant	Zynq UltraScale+ MPSoC	DDR 4	Junction Temperature	Operating Temperature Range
TE0808-04-09EG-1EA	XCZU9EG-1FFVC900E	2GB	0°C - 100°C	Extended Temperature Range
TE0808-04-09EG-1EB	XCZU9EG-1FFVC900E	4GB	0°C - 100°C	Extended Temperature Range
TE0808-04-09EG-1ED(1)	XCZU9EG-1FFVC900E	4GB	0°C - 100°C	Extended Temperature Range
TE0808-04-09EG-2IB	XCZU9EG-2FFVC900I	4GB	-40°C - 100°C	Industrial Temperature Range

(1) Note: Lower B2B connector profile,check distance bolt of between module and carrier

Table 19: Differences between variants of Module TE0808-04

9 Technical Specifications

9.1 Absolute Maximum Ratings

Parameter	Min	Max	Unit	Notes / Reference Document
PL_DCIN	-0.3	7	V	TPS82085SIL / EN63A0QI data sheet
DCDCIN	-0.3	7	V	TPS82085SIL / TPS51206 data sheet
LP_DCDC	-0.3	4	V	TPS3106K33DBVR data sheet
GT_DCDC	-0.3	7	V	TPS82085SIL data sheet
PS_BATT	-0.5	2	V	Xilinx DS925 data sheet
PLL_3V3	-0.5	3.8	V	Si5345/44/42 data sheet
VCCO for HD I/O banks	-0.5	3.4	V	Xilinx DS925 data sheet
VCCO for HP I/O banks	-0.5	2	V	Xilinx DS925 data sheet
VREF	-0.5	2	V	Xilinx DS925 data sheet
I/O input voltage for HD I/O banks	-0.55	VCCO + 0.55	V	Xilinx DS925 data sheet
I/O input voltage for HP I/O banks	-0.55	VCCO + 0.55	V	Xilinx DS925 data sheet
PS I/O input voltage (MIO pins)	-0.5	VCCO_PSIO + 0.55	V	Xilinx DS925 data sheet, VCCO_PSIO 1.8V nominally
Receiver (RXP/RXN) and transmitter (TXP/TXN) absolute input voltage	-0.5	1.2	V	Xilinx DS925 data sheet
Voltage on input pins of NC7S08P5X 2-Input AND Gate	-0.5	VCC + 0.5	V	NC7S08P5X data sheet, see schematic for VCC
Voltage on input pins (nMR) of TPS3106K33DBVR Voltage Monitor, U41	-0.3	VDD + 0.3	V	TPS3106 data sheet, VDD = LP_DCDC
"Enable"-signals on TPS82085SIL (EN_PLL_PWR, EN_LPD)	-0.3	7	V	TPS82085SIL data sheet
Storage temperature (ambient)	-40	100	°C	ROHM Semiconductor SML-P11 Series data sheet

⚠ Assembly variants for higher storage temperature range are available on request.

9.2 Recommended Operating Conditions

Parameter	Min	Max	Unit	Notes / Reference Document
PL_DCIN	2.5	6	V	EN63A0QI / TPS82085SIL data sheet
DCDCIN	3.1	6	V	TPS82085SIL / TPS51206PSQ data sheet
LP_DCDC	2.5	3.6	V	TPS82085SIL / TPS3106 data sheet
GT_DCDC	2.5	6	V	TPS82085SIL data sheet
PS_BATT	1.2	1.5	V	Xilinx DS925 data sheet
PLL_3V3	3.14	3.47	V	Si5345/44/42 data sheet 3.3V typical
VCCO for HD I/O banks	1.14	3.4	V	Xilinx DS925 data sheet
VCCO for HP I/O banks	0.95	1.9	V	Xilinx DS925 data sheet
I/O input voltage for HD I/O banks.	-0.2	VCCO + 0.2	V	Xilinx DS925 data sheet
I/O input voltage for HP I/O banks	-0.2	VCCO + 0.2	V	Xilinx DS925 data sheet
PS I/O input voltage (MIO pins)	-0.2	VCCO_PSIO + 0.2	V	Xilinx DS925 data sheet, VCCO_PSIO 1.8V nominally
Voltage on input pins of NC7S08P5X 2-Input AND Gate	0	VCC	V	NC7S08P5X data sheet, see schematic for VCC
Voltage on input pin 'MR' of TPS3106K33DBVR Voltage Monitor, U41	0	VDD	V	TPS3106 data sheet, VDD = LP_DCDC

⚠ Please check Xilinx datasheet DS925 for complete list of absolute maximum and recommended operating ratings.

9.3 Operating Temperature Ranges

Commercial grade: 0°C to +70°C.

Industrial grade: -40°C to +85°C.

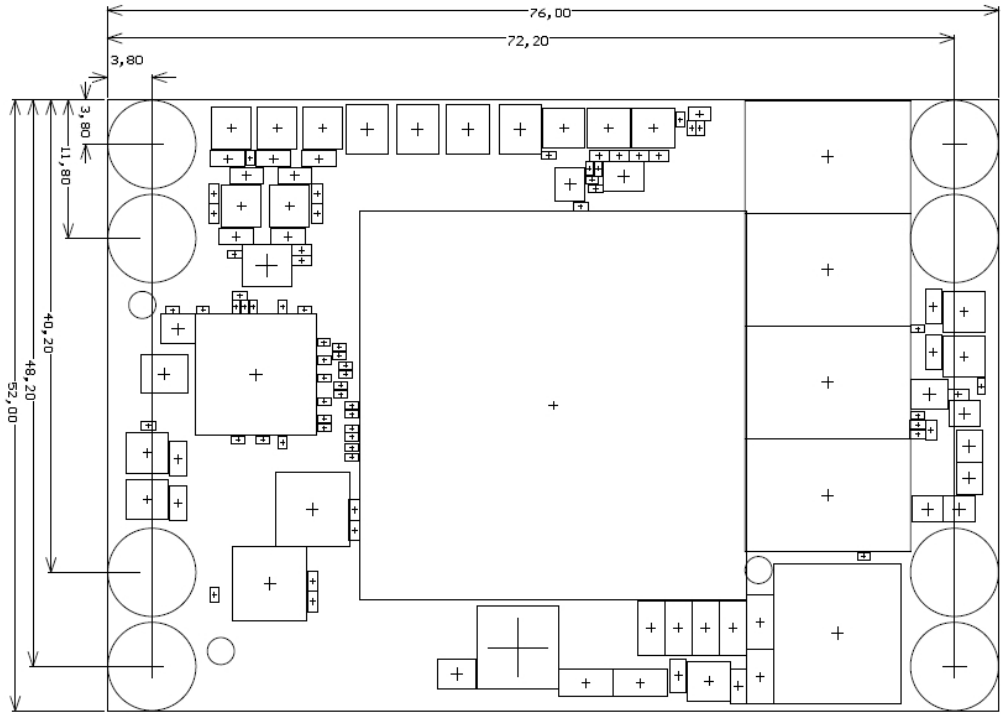
Extended grade: 0°C to +85°C.

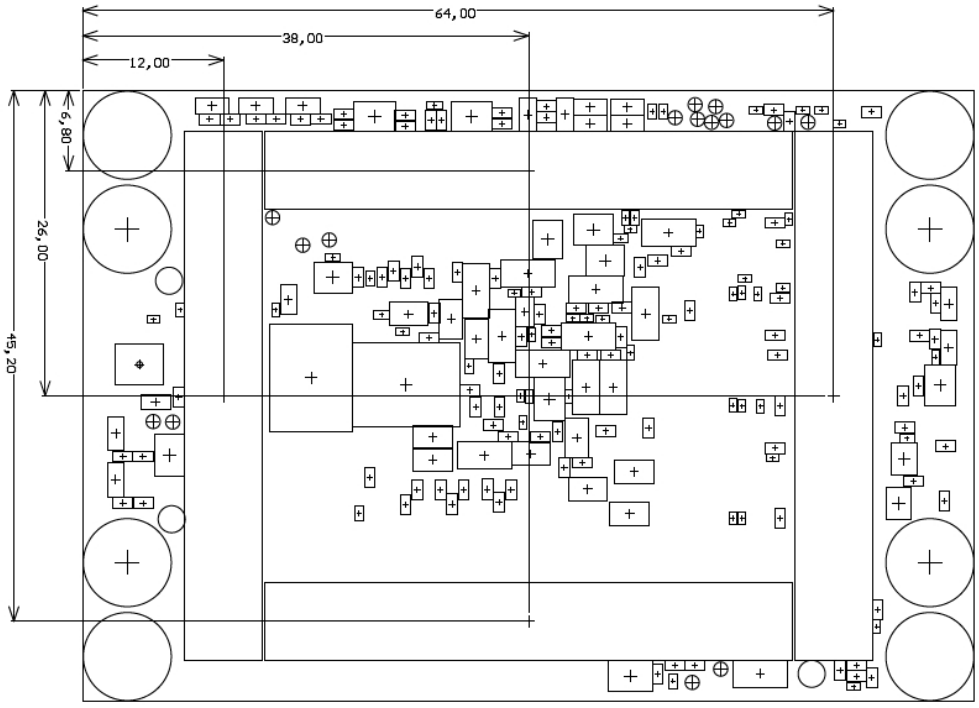
The module operating temperature range depends also on customer design and cooling solution. Please contact us for options.

9.4 Physical Dimensions

- Module size: 52 mm × 76 mm. Please download the assembly diagram for exact numbers
- Mating height with standard connectors: 4mm
- PCB thickness: 1.6mm
- Highest part on PCB: approx. 3mm. Please download the step model for exact numbers

All dimensions are given in millimeters.



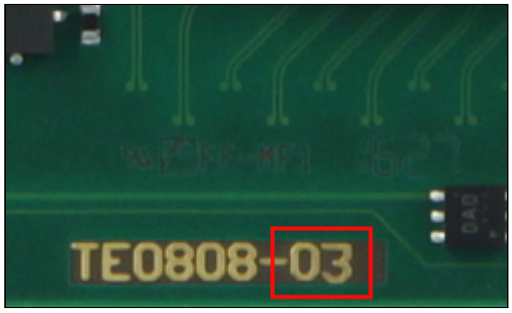


10 Revision History

10.1 Hardware Revision History

Date	Revision	Notes	Link to PCN	Documentation Link
-	04	First production silicon	-	TE0808-04
-	03	Second ES production release	-	TE0808-03
2016-03-09	02	First ES production release	-	TE0808-02
-	01	Prototypes	-	-

Hardware revision number is written on the PCB board together with the module model number separated by the dash.



10.2 Document Change History

Date	Revision	Contributors	Description
2018-06-28	v.26	John Hartfiel	• typo SI5348 B2B IOs + link correction
13.11.2017	v.24	Ali Naseri	• updated B2B connector max. current rating per pin
2017-11-13	v.22	John Hartfiel	• rework B2B section
2017-10-20	v.21	Ali Naseri	• Update links (pdf, documentation) to revision 4 • ES silicon note removed
2017-08-28	v.15	John Hartfiel	• Update section: Variants Currently In Production
2017-08-28	v.14	Jan Kumann	• Block diagram changed. • SPI flash section fixed. • Few smaller improvements.
2017-08-15	v.12	Vitali Tsiukala	Changed signals count in the B2B connectors table
2017-08-15	v.11	John Hartfiel, Ali Naseri	• PCB REV04 Initial release • update boot mode section
2017-02-06	v.1	Jan Kumann	Initial document

any substance. For that, Trenz Electronic is obliged to neither register nor to provide safety data sheet. According to present knowledge and to best of our knowledge, no SVHC (Substances of Very High Concern) on the Candidate List are contained in our products. Furthermore, we will immediately and unsolicited inform our customers in compliance with REACH - Article 33 if any substance present in our goods (above a concentration of 0,1 % weight by weight) will be classified as SVHC by the European Chemicals Agency (ECHA).

RoHS

Trenz Electronic GmbH herewith declares that all its products are developed, manufactured and distributed RoHS compliant.

WEEE

Information for users within the European Union in accordance with Directive 2002/96/EC of the European Parliament and of the Council of 27 January 2003 on waste electrical and electronic equipment (WEEE).

Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.