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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	Synchronous Serial Port (SSP)
Clock Rate	25MHz
Non-Volatile Memory	External
On-Chip RAM	6kB
Voltage - I/O	5.00V
Voltage - Core	5.00V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	68-LCC (J-Lead)
Supplier Device Package	68-PLCC (24.23x24.23)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-2101bp-100

Fabricated in a high speed, submicron, double-layer metal CMOS process, the highest-performance ADSP-21xx processors operate at 25 MHz with a 40 ns instruction cycle time. Every instruction can execute in a single cycle. Fabrication in CMOS results in low power dissipation.

The ADSP-2100 Family's flexible architecture and comprehensive instruction set support a high degree of parallelism. In one cycle the ADSP-21xx can perform all of the following operations:

- Generate the next program address
- Fetch the next instruction
- Perform one or two data moves
- Update one or two data address pointers
- Perform a computation
- Receive and transmit data via one or two serial ports
- Receive and/or transmit data via the host interface port (ADSP-2111 only)

The ADSP-2101, ADSP-2105, and ADSP-2115 comprise the basic set of processors of the family. Each of these three devices contains program and data memory RAM, an interval timer, and one or two serial ports. The ADSP-2103 is a 3.3 volt power supply version of the ADSP-2101; it is identical to the ADSP-2101 in all other characteristics. Table I shows the features of each ADSP-21xx processor.

The ADSP-2111 adds a 16-bit host interface port (HIP) to the basic set of ADSP-21xx integrated features. The host port provides a simple interface to host microprocessors or microcontrollers such as the 8031, 68000, or ISA bus.

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Flexible Framing—The SPORTs have independent framing for the transmit and receive functions; each function can run in a frameless mode or with frame synchronization signals internally generated or externally generated; frame sync signals may be active high or inverted, with either of two pulse widths and timings.

Different Word Lengths—Each SPORT supports serial data word lengths from 3 to 16 bits.

Companding in Hardware—Each SPORT provides optional A-law and μ-law companding according to CCITT recommendation G.711.

Flexible Interrupt Scheme—Receive and transmit functions can generate a unique interrupt upon completion of a data word transfer.

Autobuffering with Single-Cycle Overhead—Each SPORT can automatically receive or transmit the contents of an entire circular data buffer with only one overhead cycle per data word; an interrupt is generated after the transfer of the entire buffer is completed.

Multichannel Capability (SPORT0 Only)—SPORT0 provides a multichannel interface to selectively receive or transmit a 24-word or 32-word, time-division multiplexed serial bit stream; this feature is especially useful for T1 or CEPT interfaces, or as a network communication scheme for multiple processors. (Note that the ADSP-2105 includes only SPORT1, not SPORT0, and thus does not offer multichannel operation.)

Alternate Configuration—SPORT1 can be alternatively configured as two external interrupt inputs ($\overline{IRQ0}$, $\overline{IRQ1}$) and the Flag In and Flag Out signals (FI, FO).

Host Interface Port (ADSP-2111)

The ADSP-2111 includes a Host Interface Port (HIP), a parallel I/O port that allows easy connection to a host processor. Through the HIP, the ADSP-2111 can be accessed by the host processor as a memory-mapped peripheral. The host interface port can be thought of as an area of dual-ported memory, or mailbox registers, that allows communication between the computational core of the ADSP-2111 and the host computer. The host interface port is completely asynchronous. The host processor can write data into the HIP while the ADSP-2111 is operating at full speed.

Three pins configure the HIP for operation with different types of host processors. The HSIZE pin configures HIP for 8- or 16-bit communication with the host processor. HMD0 configures the bus strobes, selecting either separate read and write strobes or a single read/write select and a host data strobe. HMD1 selects either separate address (3-bit) and data (16-bit) buses or a multiplexed 16-bit address/data bus with address latch enable. Tying these pins to appropriate values configures the ADSP-2111 for straight-wire interface to a variety of industry-standard microprocessors and microcomputers.

The HIP contains six data registers (HDR5-0) and two status registers (HSR7-6) with an associated HMASK register for masking interrupts from individual HIP data registers. The HIP data registers are memory-mapped in the internal data memory of the ADSP-2111. The two status registers provide status information to both the ADSP-2111 and the host processor. HSR7 contains a software reset bit which can be set by both the ADSP-2111 and the host.

HIP transfers can be managed using either interrupts or polling. The HIP generates an interrupt whenever an HDR register receives data from a host processor write. It also generates an interrupt when the host processor has performed a successful read of any HDR. The read/write status of the HDRs is also stored in the HSR registers.

The HMASK register bits can be used to mask the generation of read or write interrupts from individual HDR registers. Bits in the IMASK register enable and disable all HIP read interrupts or all HIP write interrupts. So, for example, a write to HDR4 will cause an interrupt only if both the *HDR4 Write* bit in HMASK and the *HIP Write* interrupt enable bit in IMASK are set.

The HIP provides a second method of booting the ADSP-2111 in which the host processor loads instructions into the HIP. The ADSP-2111 automatically transfers the data, in this case opcodes, to internal program memory. The BMODE pin determines whether the ADSP-2111 boots from the host processor through the HIP or from external EPROM over the data bus.

Interrupts

The ADSP-21xx's interrupt controller lets the processor respond to interrupts with a minimum of overhead. Up to three external interrupt input pins, $\overline{IRQ0}$, $\overline{IRQ1}$, and $\overline{IRQ2}$, are provided. $\overline{IRQ2}$ is always available as a dedicated pin; $\overline{IRQ1}$ and $\overline{IRQ0}$ may be alternately configured as part of Serial Port 1. The ADSP-21xx also supports internal interrupts from the timer, the serial ports, and the host interface port (on the ADSP-2111). The interrupts are internally prioritized and individually maskable (except for $\overline{RESET}$ which is non-maskable). The $\overline{IRQx}$ input pins can be programmed for either level- or edge-sensitivity. The interrupt priorities for each ADSP-21xx processor are shown in Table III.

The ADSP-21xx uses a vectored interrupt scheme: when an interrupt is acknowledged, the processor shifts program control to the interrupt vector address corresponding to the interrupt received. Interrupts can be optionally nested so that a higher priority interrupt can preempt the currently executing interrupt service routine. Each interrupt vector location is four instructions in length so that simple service routines can be coded entirely in this space. Longer service routines require an additional JUMP or CALL instruction.

Individual interrupt requests are logically ANDed with the bits in the IMASK register; the highest-priority unmasked interrupt is then selected.

The interrupt control register, ICNTL, allows the external interrupts to be set as either edge- or level-sensitive. Depending on bit 4 in ICNTL, interrupt service routines can either be nested (with higher priority interrupts taking precedence) or be processed sequentially (with only one interrupt service active at a time).

The interrupt force and clear register, IFC, is a write-only register that contains a force bit and a clear bit for each interrupt (except for level-sensitive interrupts and the ADSP-2111 HIP interrupts—these cannot be forced or cleared in software).

When responding to an interrupt, the ASTAT, MSTAT, and IMASK status registers are pushed onto the status stack and the PC counter is loaded with the appropriate vector address. The status stack is seven levels deep (nine levels deep on the ADSP-2111) to allow interrupt nesting. The stack is automatically popped when a return from the interrupt instruction is executed.

Pin Definitions

Table IV (on next page) shows pin definitions for the ADSP-21xx processors. Any inputs not used must be tied to V_{DD}.

Table III. Interrupt Vector Addresses & Priority

ADSP-2105 Interrupt Source	**Interrupt Vector Address**
$\overline{\text{RESET}}$ Startup	0x0000
$\overline{\text{IRQ2}}$	0x0004 *(High Priority)*
SPORT1 Transmit *or* $\overline{\text{IRQ1}}$	0x0010
SPORT1 Receive *or* $\overline{\text{IRQ0}}$	0x0014
Timer	0x0018 *(Low Priority)*

ADSP-2101/2103/2115/216x Interrupt Source	**Interrupt Vector Address**
$\overline{\text{RESET}}$ Startup	0x0000
$\overline{\text{IRQ2}}$	0x0004 *(High Priority)*
SPORT0 Transmit	0x0008
SPORT0 Receive	0x000C
SPORT1 Transmit *or* $\overline{\text{IRQ1}}$	0x0010
SPORT1 Receive *or* $\overline{\text{IRQ0}}$	0x0014
Timer	0x0018 *(Low Priority)*

ADSP-2111 Interrupt Source	**Interrupt Vector Address**
$\overline{\text{RESET}}$ Startup	0x0000
$\overline{\text{IRQ2}}$	0x0004 *(High Priority)*
HIP Write from Host	0x0008
HIP Read to Host	0x000C
SPORT0 Transmit	0x0010
SPORT0 Receive	0x0014
SPORT1 Transmit *or* $\overline{\text{IRQ1}}$	0x0018
SPORT1 Receive *or* $\overline{\text{IRQ0}}$	0x001C
Timer	0x0020 *(Low Priority)*

SYSTEM INTERFACE

Figure 3 shows a typical system for the ADSP-2101, ADSP-2115, or ADSP-2103, with two serial I/O devices, a boot EPROM, and optional external program and data memory. A total of 15K words of data memory and 16K words of program memory is addressable for the ADSP-2101 and ADSP-2103. A total of 14.5K words of data memory and 15K words of program memory is addressable for the ADSP-2115.

Figure 4 shows a system diagram for the ADSP-2105, with one serial I/O device, a boot EPROM, and optional external program and data memory. A total of 14.5K words of data memory and 15K words of program memory is addressable for the ADSP-2105.

Figure 5 shows a system diagram for the ADSP-2111, with two serial I/O devices, a host processor, a boot EPROM, and optional external program and data memory. A total of 15K words of data memory and 16K words of program memory is addressable.

Programmable wait-state generation allows the processors to easily interface to slow external memories.

The ADSP-2101, ADSP-2103, ADSP-2115, and ADSP-2111 processors also provide either: one external interrupt ($\overline{\text{IRQ2}}$) and two serial ports (SPORT0, SPORT1), *or* three external interrupts ($\overline{\text{IRQ2}}$, $\overline{\text{IRQ1}}$, $\overline{\text{IRQ0}}$) and one serial port (SPORT0).

The ADSP-2105 provides either: one external interrupt ($\overline{\text{IRQ2}}$) and one serial port (SPORT1), *or* three external interrupts ($\overline{\text{IRQ2}}$, $\overline{\text{IRQ1}}$, $\overline{\text{IRQ0}}$) with no serial port.

Clock Signals

The ADSP-21xx processors' CLKIN input may be driven by a crystal or by a TTL-compatible external clock signal. The CLKIN input may not be halted or changed in frequency during operation, nor operated below the specified low frequency limit.

If an external clock is used, it should be a TTL-compatible signal running at the instruction rate. The signal should be connected to the processor's CLKIN input; in this case, the XTAL input must be left unconnected.

Because the ADSP-21xx processors include an on-chip oscillator circuit, an external crystal may also be used. The crystal should be connected across the CLKIN and XTAL pins, with two capacitors connected as shown in Figure 2. A parallel-resonant, fundamental frequency, microprocessor-grade crystal should be used.

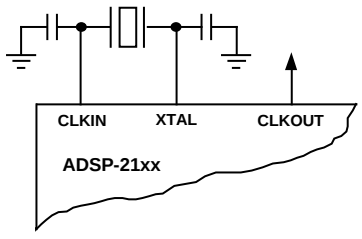


Figure 2. External Crystal Connections

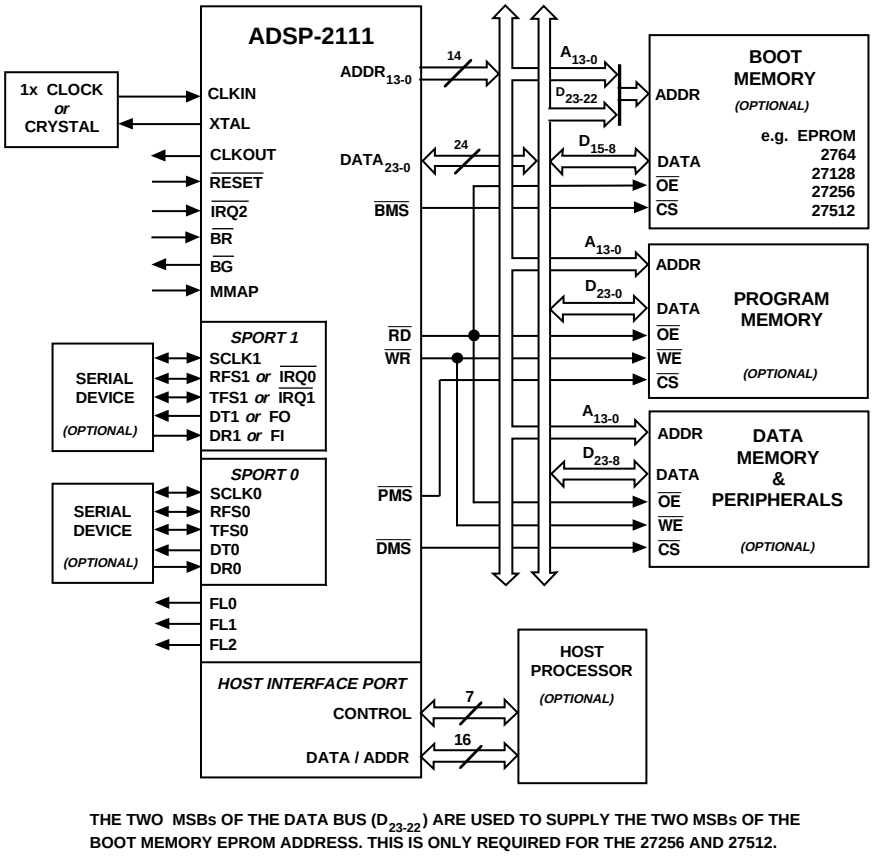


Figure 5. ADSP-2111 System

The $\overline{\text{RESET}}$ input resets all internal stack pointers to the empty stack condition, masks all interrupts, and clears the MSTAT register. When $\overline{\text{RESET}}$ is released, the boot loading sequence is performed (provided there is no pending bus request and the chip is configured for booting, with MMAP = 0). The first instruction is then fetched from internal program memory location 0x0000.

Program Memory Interface

The on-chip program memory address bus (PMA) and on-chip program memory data bus (PMD) are multiplexed with the on-chip data memory buses (DMA, DMD), creating a single external data bus and a single external address bus. The external data bus is bidirectional and is 24 bits wide to allow instruction fetches from external program memory. Program memory may contain code and data.

The external address bus is 14 bits wide. For the ADSP-2101, ADSP-2103, and ADSP-2111, these lines can directly address up to 16K words, of which 2K are on-chip. For the ADSP-2105 and ADSP-2115, the address lines can directly address up to 15K words, of which 1K is on-chip.

The data lines are bidirectional. The program memory select ($\overline{\text{PMS}}$) signal indicates accesses to program memory and can be used as a chip select signal. The write ($\overline{\text{WR}}$) signal indicates a write operation and is used as a write strobe. The read ($\overline{\text{RD}}$) signal indicates a read operation and is used as a read strobe or output enable signal.

The ADSP-21xx processors write data from their 16-bit registers to 24-bit program memory using the PX register to provide the lower eight bits. When the processor reads 16-bit data from 24-bit program memory to a 16-bit data register, the lower eight bits are placed in the PX register.

The program memory interface can generate 0 to 7 wait states for external memory devices; default is to 7 wait states after $\overline{\text{RESET}}$.

Program Memory Maps

Program memory can be mapped in two ways, depending on the state of the MMAP pin. Figure 6 shows the two program memory maps for the ADSP-2101, ADSP-2103, and ADSP-2111. Figure 8 shows the program memory maps for the ADSP-2105 and ADSP-2115. Figures 7 and 9 show the program memory maps for the ADSP-2161/62 and ADSP-2163/64, respectively.

Program Flow Instructions

DO <addr> [UNTIL term] ;	*Do Until Loop*
[IF cond] JUMP (Ix) ;	*Jump*
[IF cond] JUMP <addr>;	
[IF cond] CALL (Ix) ;	*Call Subroutine*
[IF cond] CALL <addr>;	
IF [NOT] FLAG_IN JUMP <addr>;	*Jump/Call on Flag In Pin*
IF [NOT] FLAG_IN CALL <addr>;	
[IF cond] SET|RESET|TOGGLE FLAG_OUT [, ...] ;	*Modify Flag Out Pin*
[IF cond] RTS ;	*Return from Subroutine*
[IF cond] RTI ;	*Return from Interrupt Service Routine*
IDLE [(n)] ;	*Idle*

Miscellaneous Instructions

NOP ;	*No Operation*
MODIFY (Ix , My);	*Modify Address Register*
[PUSH STS] [, POP CNTR] [, POP PC] [, POP LOOP] ;	*Stack Control*
ENA|DIS SEC_REG [, ...] ;	*Mode Control*
BIT_REV	
AV_LATCH	
AR_SAT	
M_MODE	
TIMER	
G_MODE	

Notation Conventions

Ix	Index registers for indirect addressing
My	Modify registers for indirect addressing
<data>	Immediate data value
<addr>	Immediate address value
<exp>	Exponent (shift value) in shift immediate instructions (8-bit signed number)
<ALU>	Any ALU instruction (except divide)
<MAC>	Any multiply-accumulate instruction
<SHIFT>	Any shift instruction (except shift immediate)
cond	Condition code for conditional instruction
term	Termination code for DO UNTIL loop
dreg	Data register (of ALU, MAC, or Shifter)
reg	Any register (including dregs)
;	A semicolon terminates the instruction
,	Commas separate multiple operations of a single instruction
[ ]	Optional part of instruction
[, ...]	Optional, multiple operations of an instruction
option1 | *option2*	List of options; choose one.

Assembly Code Example

The following example is a code fragment that performs the filter tap update for an adaptive filter based on a least-mean-squared algorithm. Notice that the computations in the instructions are written like algebraic equations.

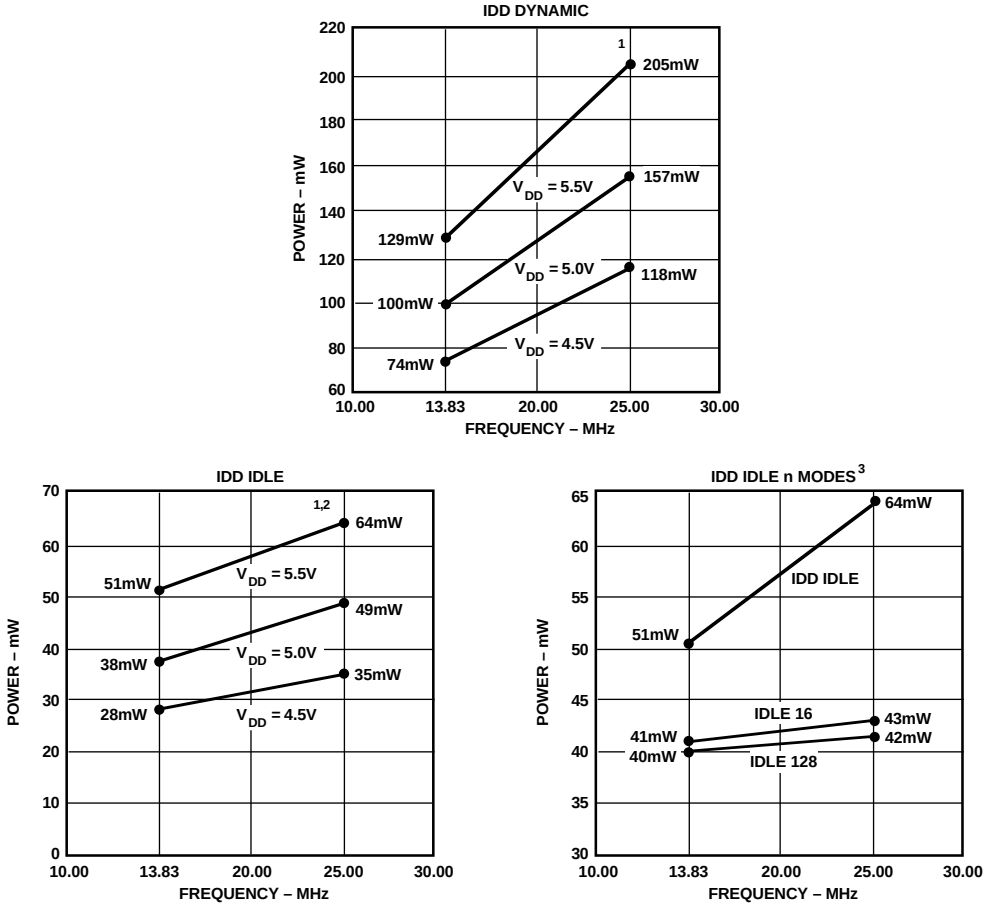
```
        MF=MX0*MY1(RND), MX0=DM(I2,M1);       {MF=error*beta}
        MR=MX0*MF(RND), AY0=PM(I6,M5);
        DO adapt UNTIL CE;
           AR=MR1+AY0, MX0=DM(I2,M1), AY0=PM(I6,M7);
adapt:     PM(I6,M6)=AR, MR=MX0*MF(RND);

        MODIFY(I2,M3);                        {Point to oldest data}
        MODIFY(I6,M7);                        {Point to start of data}
```

SPECIFICATIONS (ADSP-2101/2105/2115/2161/2163)

SUPPLY CURRENT & POWER (ADSP-2101/2105/2115/2161/2163)

Parameter		Test Conditions	Min	Max	Unit
I_{DD}	Supply Current (Dynamic)[1]	@ V_{DD} = max, t_{CK} = 40 ns[2]		38	mA
		@ V_{DD} = max, t_{CK} = 50 ns[2]		31	mA
		@ V_{DD} = max, t_{CK} = 72.3 ns[2]		24	mA
I_{DD}	Supply Current (Idle)[1, 3]	@ V_{DD} = max, t_{CK} = 40 ns[4]		12	mA
		@ V_{DD} = max, t_{CK} = 50 ns		11	mA
		@ V_{DD} = max, t_{CK} = 72.3 ns		10	mA

NOTES
[1]Current reflects device operating with no output loads.
[2]V_{IN} = 0.4 V and 2.4 V.
[3]Idle refers to ADSP-21xx state of operation during execution of IDLE instruction. Deasserted pins are driven to either V_{DD} or GND.
[4]ADSP-2105 is not available in a 25 MHz speed grade.
For typical supply current (internal power dissipation) figures, see Figure 11.



VALID FOR ALL TEMPERATURE GRADES.
1 POWER REFLECTS DEVICE OPERATING WITH NO OUTPUT LOADS.
2 IDLE REFERS TO ADSP-21xx OPERATION DURING EXECUTION OF IDLE INSTRUCTION. DEASSERTED PINS ARE DRIVEN TO EITHER V_{DD} OR GND.
3 MAXIMUM POWER DISSIPATION AT V_{DD} = 5.5V DURING EXECUTION OF *IDLE n* INSTRUCTION.

Figure 11. ADSP-2101 Power (Typical) vs. Frequency

SPECIFICATIONS (ADSP-2101/2105/2115/2161/2163)

TEST CONDITIONS

Figure 14 shows voltage reference levels for ac measurements.

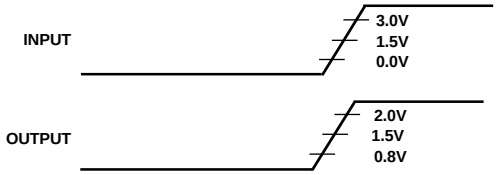


Figure 14. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Disable Time

Output pins are considered to be disabled when they have stopped driving and started a transition from the measured output high or low voltage to a high impedance state. The output disable time (t_{DIS}) is the difference of $t_{MEASURED}$ and t_{DECAY}, as shown in Figure 15. The time $t_{MEASURED}$ is the interval from when a reference signal reaches a high or low voltage level to when the output voltages have changed by 0.5 V from the measured output high or low voltage.

The decay time, t_{DECAY}, is dependent on the capacitative load, C_L, and the current load, i_L, on the output pin. It can be approximated by the following equation:

$$t_{DECAY} = \frac{C_L \times 0.5\,V}{i_L}$$

from which

$$t_{DIS} = t_{MEASURED} - t_{DECAY}$$

is calculated. If multiple pins (such as the data bus) are disabled, the measurement value is that of the last pin to stop driving.

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high-impedance state to when they start driving. The output enable time (t_{ENA}) is the interval from when a reference signal reaches a high or low voltage level to when the output has reached a specified high or low trip point, as shown in Figure 15. If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

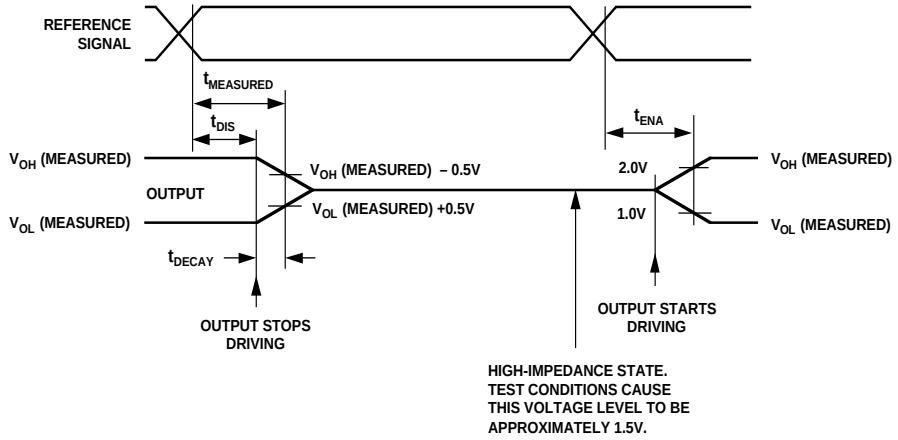


Figure 15. Output Enable/Disable

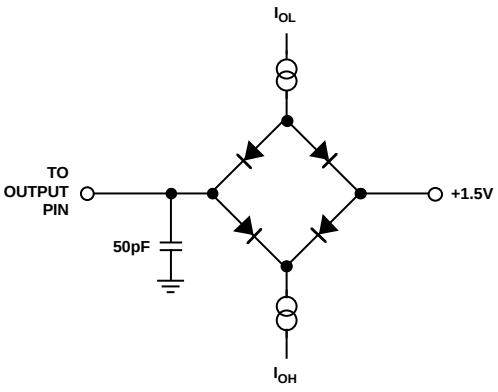


Figure 16. Equivalent Device Loading for AC Measurements (Except Output Enable/Disable)

SPECIFICATIONS (ADSP-2111)

TEST CONDITIONS

Figure 20 shows voltage reference levels for ac measurements.

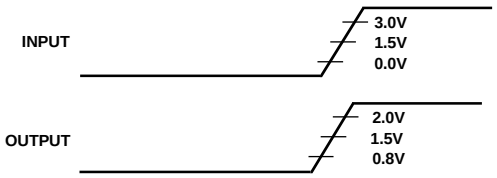


Figure 20. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Disable Time

Output pins are considered to be disabled when they have stopped driving and started a transition from the measured output high or low voltage to a high impedance state. The output disable time (t_{DIS}) is the difference of $t_{MEASURED}$ and t_{DECAY}, as shown in Figure 21. The time $t_{MEASURED}$ is the interval from when a reference signal reaches a high or low voltage level to when the output voltages have changed by 0.5 V from the measured output high or low voltage.

The decay time, t_{DECAY}, is dependent on the capacitative load, C_L, and the current load, i_L, on the output pin. It can be approximated by the following equation:

$$t_{DECAY} = \frac{C_L \times 0.5\,V}{i_L}$$

from which

$$t_{DIS} = t_{MEASURED} - t_{DECAY}$$

is calculated. If multiple pins (such as the data bus) are disabled, the measurement value is that of the last pin to stop driving.

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high-impedance state to when they start driving. The output enable time (t_{ENA}) is the interval from when a reference signal reaches a high or low voltage level to when the output has reached a specified high or low trip point, as shown in Figure 21. If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

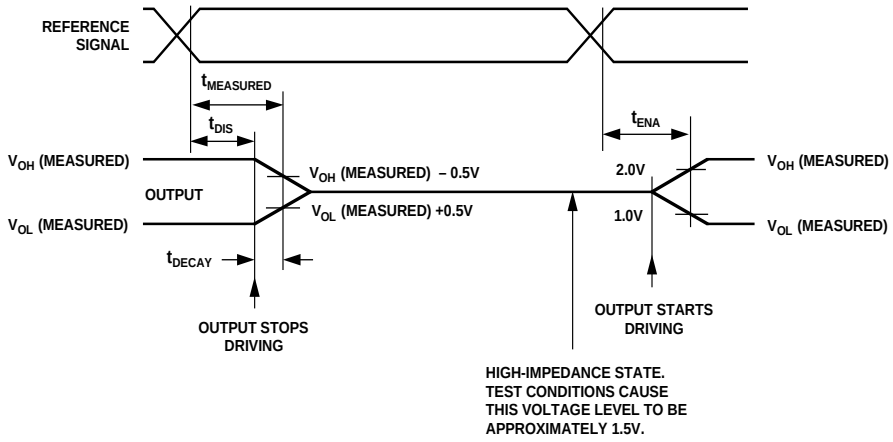


Figure 21. Output Enable/Disable

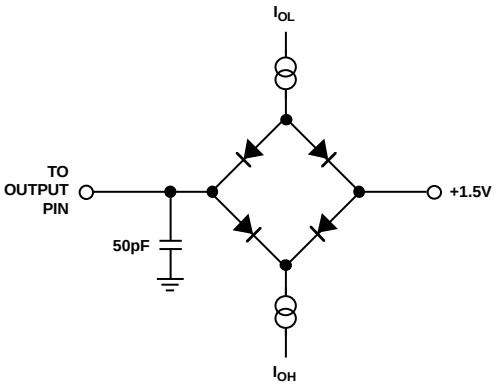


Figure 22. Equivalent Device Loading for AC Measurements (Except Output Enable/Disable)

TIMING PARAMETERS (ADSP-2101/2105/2111/2115/2161/2163)

CLOCK SIGNALS & RESET

Parameter		13 MHz Min	13 MHz Max	13.824 MHz Min	13.824 MHz Max	16.67 MHz Min	16.67 MHz Max	20 MHz Min	20 MHz Max	25 MHz Min	25 MHz Max	Frequency Dependency Min	Frequency Dependency Max	Unit
Timing Requirement:														
t_{CK}	CLKIN Period	76.9	150	72.3	150	60	150	50	150	40	150			ns
t_{CKL}	CLKIN Width Low	20		20		20		20		15		20		ns
t_{CKH}	CLKIN Width High	20		20		20		20		15		20		ns
t_{RSP}	$\overline{\text{RESET}}$ Width Low	384.5		361.5		300		250		200		$5t_{CK}$[1]		ns
Switching Characteristic:														
t_{CPL}	CLKOUT Width Low	28.5		26.2		20		15		10		$0.5t_{CK} - 10$		ns
t_{CPH}	CLKOUT Width High	28.5		26.2		20		15		10		$0.5t_{CK} - 10$		ns
t_{CKOH}	CLKIN High to CLKOUT High	0	20	0	20	0	20	0	20	0	15			ns

NOTES
[1]Applies after powerup sequence is complete. Internal phase lock loop requires no more than 2000 CLKIN cycles, assuming stable CLKIN (not including crystal oscillator startup time).

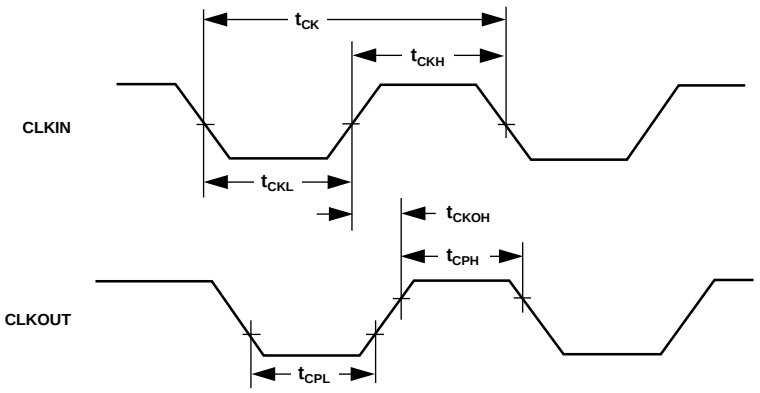


Figure 29. Clock Signals

TIMING PARAMETERS (ADSP-2101/2105/2111/2115/2161/2163)

INTERRUPTS & FLAGS

Parameter		13 MHz Min	13 MHz Max	13.824 MHz Min	13.824 MHz Max	16.67 MHz Min	16.67 MHz Max	20 MHz Min	20 MHz Max	25 MHz Min	25 MHz Max	Frequency Dependency Min	Frequency Dependency Max	Unit
Timing Requirement:														
t_{IFS}	$\overline{IRQx}$[1] or FI Setup before CLKOUT Low[2, 3]	34.2		33.1		30		27.5		25		$0.25t_{CK}$ + 15[4]		ns
t_{IFS}	$\overline{IRQx}$[1] or FI Setup before CLKOUT Low *(ADSP-2111)*[2, 3]	37.2		36.1		33		30.5		28		$0.25t_{CK}$ + 18[4]		ns
t_{IFH}	$\overline{IRQx}$[1] or FI Hold after CLKOUT High[2, 3]	19.2		18.1		15		12.5		10		$0.25t_{CK}$		ns
Switching Characteristic:														
t_{FOH}	FO Hold after CLKOUT High[5]	0		0		0		0		0		0		ns
t_{FOD}	FO Delay from CLKOUT High		15		15		15		15		12			ns

NOTES

[1]$\overline{IRQx}$=$\overline{IRQ0}$, $\overline{IRQ1}$, and $\overline{IRQ2}$.

[2]If $\overline{IRQx}$ and FI inputs meet t_{IFS} and t_{IFH} setup/hold requirements, they will be recognized during the current clock cycle; otherwise they will be recognized during the following cycle. (Refer to the "Interrupt Controller" section in Chapter 3, Program Control, of the *ADSP-2100 Family User's Manual* for further information on interrupt servicing.)

[3]Edge-sensitive interrupts require pulse widths greater than 10 ns. Level-sensitive interrupts must be held low until serviced.

[4]t_{IFS} (min) = $0.25t_{CK}$ + 20 ns for ADSP-2101TG-50, ADSP-2101TG/883B-50, ADSP-2111TG-52, and ADSP-2111TG/883B-52 (Extended Temperature Range devices).

[5]t_{FOH} (min) = –5 ns for ADSP-2111TG-52 and ADSP-2111TG/883B-52 (Extended Temperature Range devices).

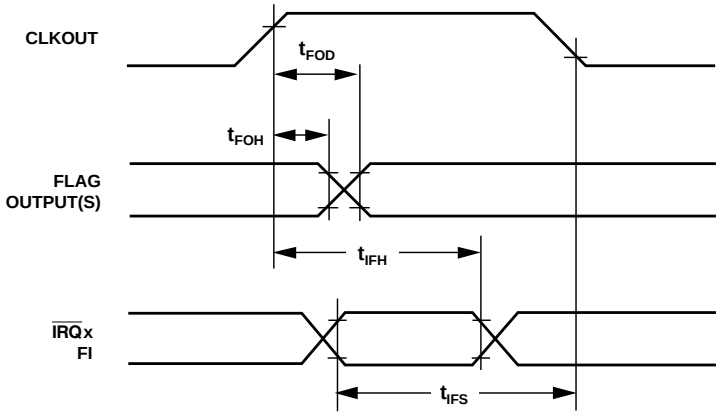


Figure 30. Interrupts & Flags

TIMING PARAMETERS (ADSP-2101/2105/2111/2115/2161/2163)

SERIAL PORTS

Parameter		12.5 MHz Min	12.5 MHz Max	13.0 MHz Min	13.0 MHz Max	13.824 MHz* Min	13.824 MHz* Max	Frequency Dependency Min	Frequency Dependency Max	Unit
Timing Requirement:										
t_{SCK}	SCLK Period	80		76.9		72.3				ns
t_{SCS}	DR/TFS/RFS Setup before SCLK Low	8		8		8				ns
t_{SCH}	DR/TFS/RFS Hold after SCLK Low	10		10		10				ns
t_{SCP}	$SCLK_{IN}$ Width	30		28		28				ns
Switching Characteristic:										
t_{CC}	CLKOUT High to $SCLK_{OUT}$	20	35	19.2	34.2	18.1	33.1	$0.25t_{CK}$	$0.25t_{CK}$ + 15ns	
t_{SCDE}	SCLK High to DT Enable	0		0		0				ns
t_{SCDV}	SCLK High to DT Valid		20		20		20			ns
t_{RH}	TFS/RFS_{OUT} Hold after SCLK High	0		0		0				ns
t_{RD}	TFS/RFS_{OUT} Delay from SCLK High		20		20		20			ns
t_{SCDH}	DT Hold after SCLK High	0		0		0				ns
t_{TDE}	TFS (Alt) to DT Enable	0		0		0				ns
t_{TDV}	TFS (Alt) to DT Valid		18		18		18			ns
t_{SCDD}	SCLK High to DT Disable		25		25		25			ns
t_{RDV}	RFS (Multichannel, Frame Delay Zero) to DT Valid		20		20		20			ns

*Maximum serial port operating frequency is 13.824 MHz for all processor speed grades except the 12.5 MHz ADSP-2101 and 13.0 MHz ADSP-2111.

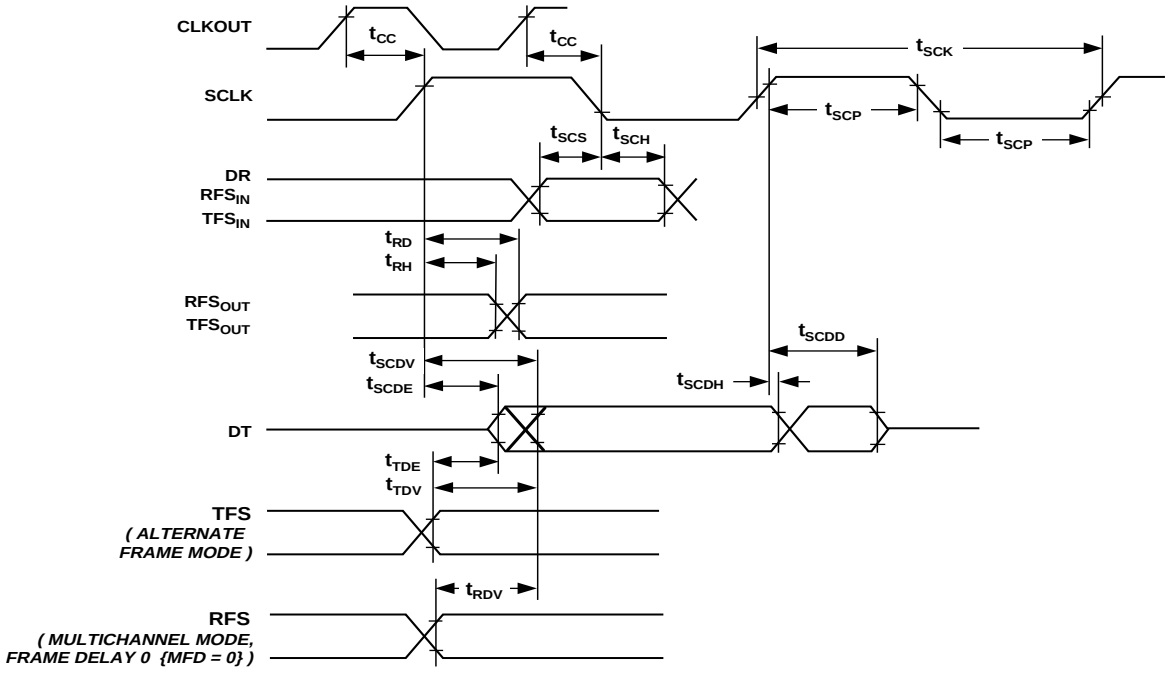
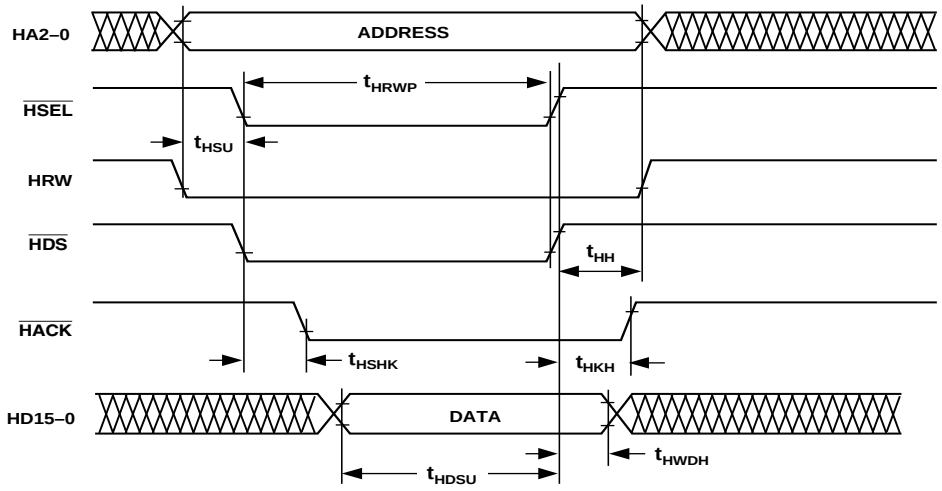


Figure 34. Serial Ports

Host Write Cycle



Host Read Cycle

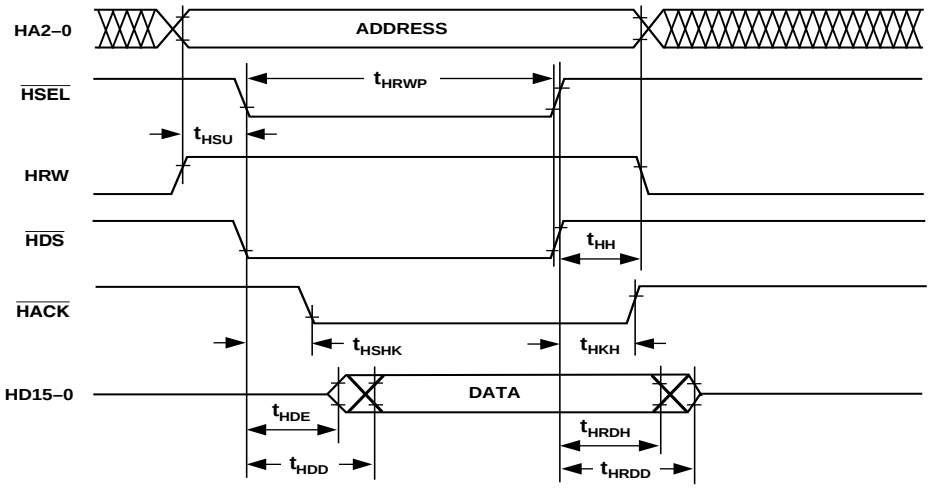


Figure 36. Host Interface Port (HMD1 = 0, HMD0 =1)

TIMING PARAMETERS (ADSP-2103/2162/2164)

SERIAL PORTS

Parameter		10.24 MHz Min	10.24 MHz Max	Frequency Dependency Min	Frequency Dependency Max	Unit
Timing Requirement:						
t_{SCK}	SCLK Period	97.6		t_{CK}		ns
t_{SCS}	DR/TFS/RFS Setup before SCLK Low	8				ns
t_{SCH}	DR/TFS/RFS Hold after SCLK Low	10				ns
t_{SCP}	$SCLK_{in}$ Width	28				ns
Switching Characteristic:						
t_{CC}	CLKOUT High to $SCLK_{out}$	24.4	39.4	$0.25t_{CK}$	$0.25t_{CK}$ + 15	ns
t_{SCDE}	SCLK High to DT Enable	0				ns
t_{SCDV}	SCLK High to DT Valid		28			ns
t_{RH}	TFS/RFS_{out} Hold after SCLK High	0				ns
t_{RD}	TFS/RFS_{out} Delay from SCLK High		28			ns
t_{SCDH}	DT Hold after SCLK High	0				ns
t_{TDE}	TFS (alt) to DT Enable	0				ns
t_{TDV}	TFS (alt) to DT Valid		18			ns
t_{SCDD}	SCLK High to DT Disable		30			ns
t_{RDV}	RFS (Multichannel, Frame Delay Zero) to DT Valid		20			ns

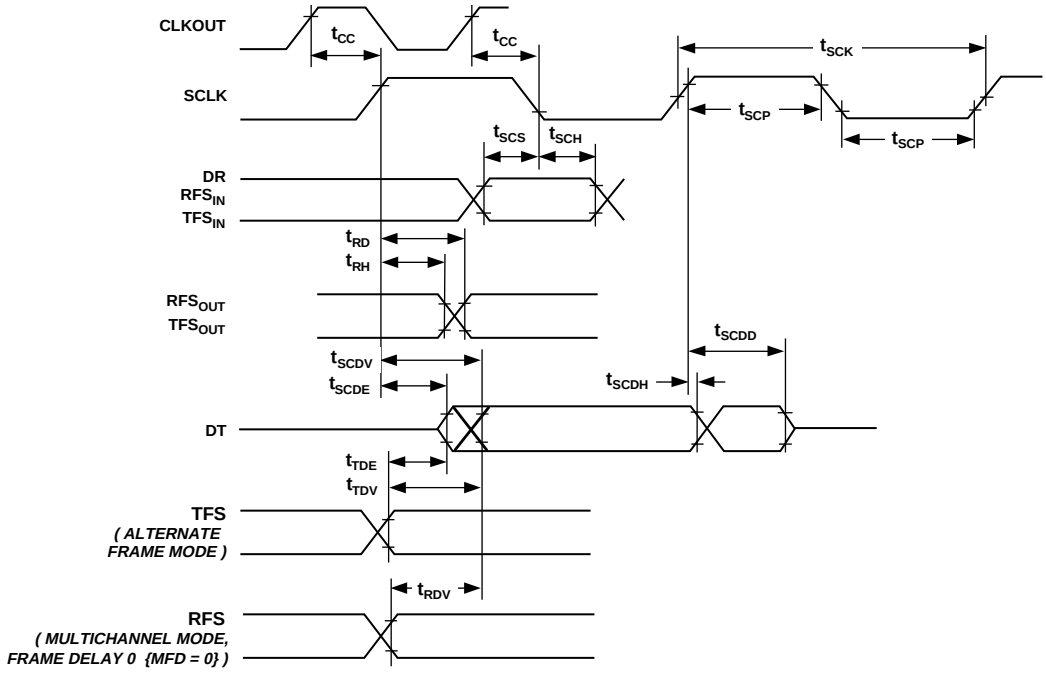
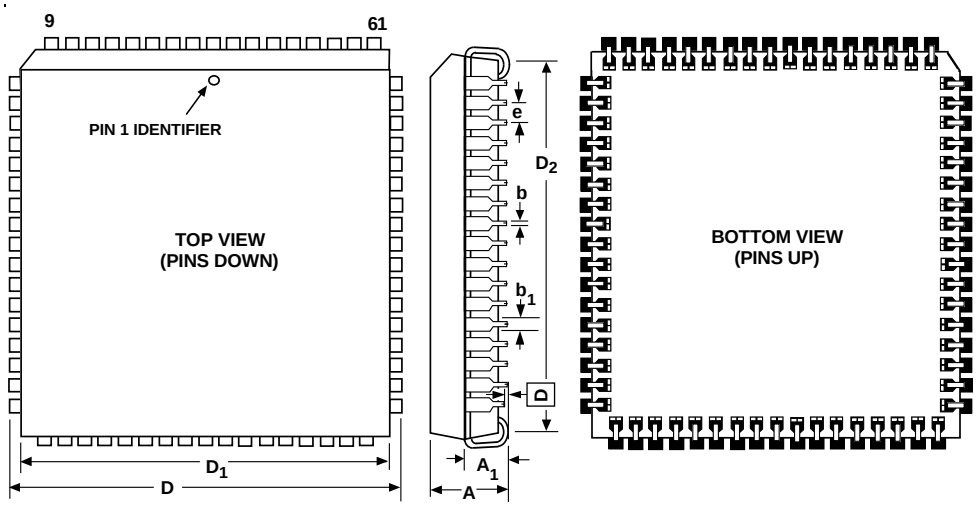


Figure 44. Serial Ports

OUTLINE DIMENSIONS

ADSP-21xx

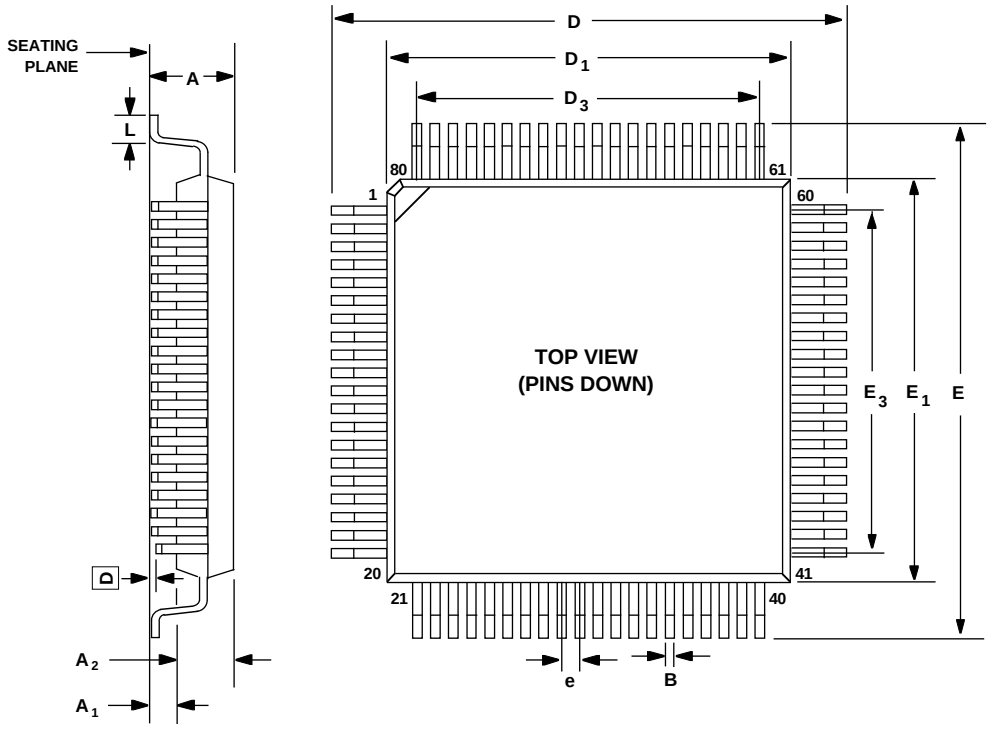
68-Lead Plastic Leaded Chip Carrier (PLCC)



SYMBOL	INCHES			MILLIMETERS		
	MIN	TYP	MAX	MIN	TYP	MAX
A	0.169	0.172	0.175	4.29	4.37	4.45
A_1		0.104			2.64	
b	0.017	0.018	0.019	0.43	0.46	0.48
b_1	0.027	0.028	0.029	0.69	0.71	0.74
D	0.985	0.990	0.995	25.02	25.15	25.27
D_1	0.950	0.952	0.954	24.13	24.18	24.23
D_2	0.895	0.910	0.925	22.73	23.11	23.50
e		0.050			1.27	
D			0.004			0.10

OUTLINE DIMENSIONS

ADSP-21xx
80-Lead Metric Plastic Quad Flatpack (PQFP)
80-Lead Metric Thin Quad Flatpack (TQFP)



PQFP

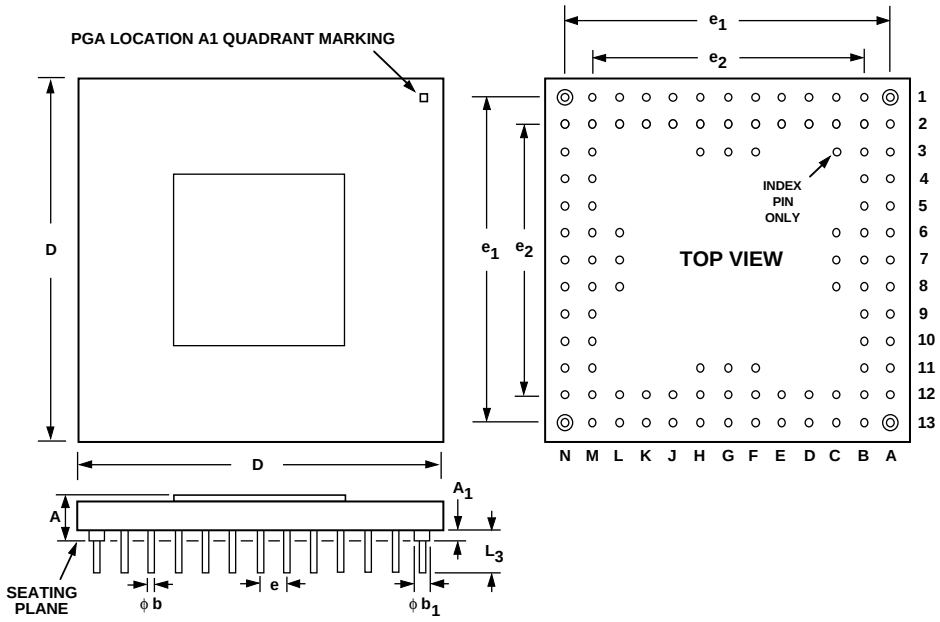
SYMBOL	MILLIMETERS			INCHES		
	MIN	TYP	MAX	MIN	TYP	MAX
A			2.45			0.096
A_1	0.25			0.010		
A_2	1.90	2.00	2.10	0.075	0.079	0.083
D, E	16.95	17.20	17.45	0.667	0.678	0.690
D_1, E_1	13.90	14.00	14.10	0.547	0.551	0.555
D_3, E_3		12.35	12.43		0.486	0.490
L	0.65	0.80	0.95	0.026	0.031	0.037
e	0.57	0.65	0.73	0.023	0.026	0.029
B	0.22	0.30	0.38	0.009	0.012	0.015
a			0.10			0.004

TQFP

MILLIMETERS			INCHES		
MIN	TYP	MAX	MIN	TYP	MAX
		1.60			0.063
0.05		0.15	0.002		0.006
1.35	1.40	1.45	0.053	0.055	0.057
15.75	16.00	16.25	0.620	0.630	0.640
13.95	14.00	14.05	0.549	0.551	0.553
	12.35	12.43		0.486	0.490
0.50	0.60	0.75	0.020	0.024	0.030
0.57	0.65	0.73	0.022	0.026	0.029
0.25	0.30	0.35	0.010	0.012	0.014
		0.10			0.004

OUTLINE DIMENSIONS

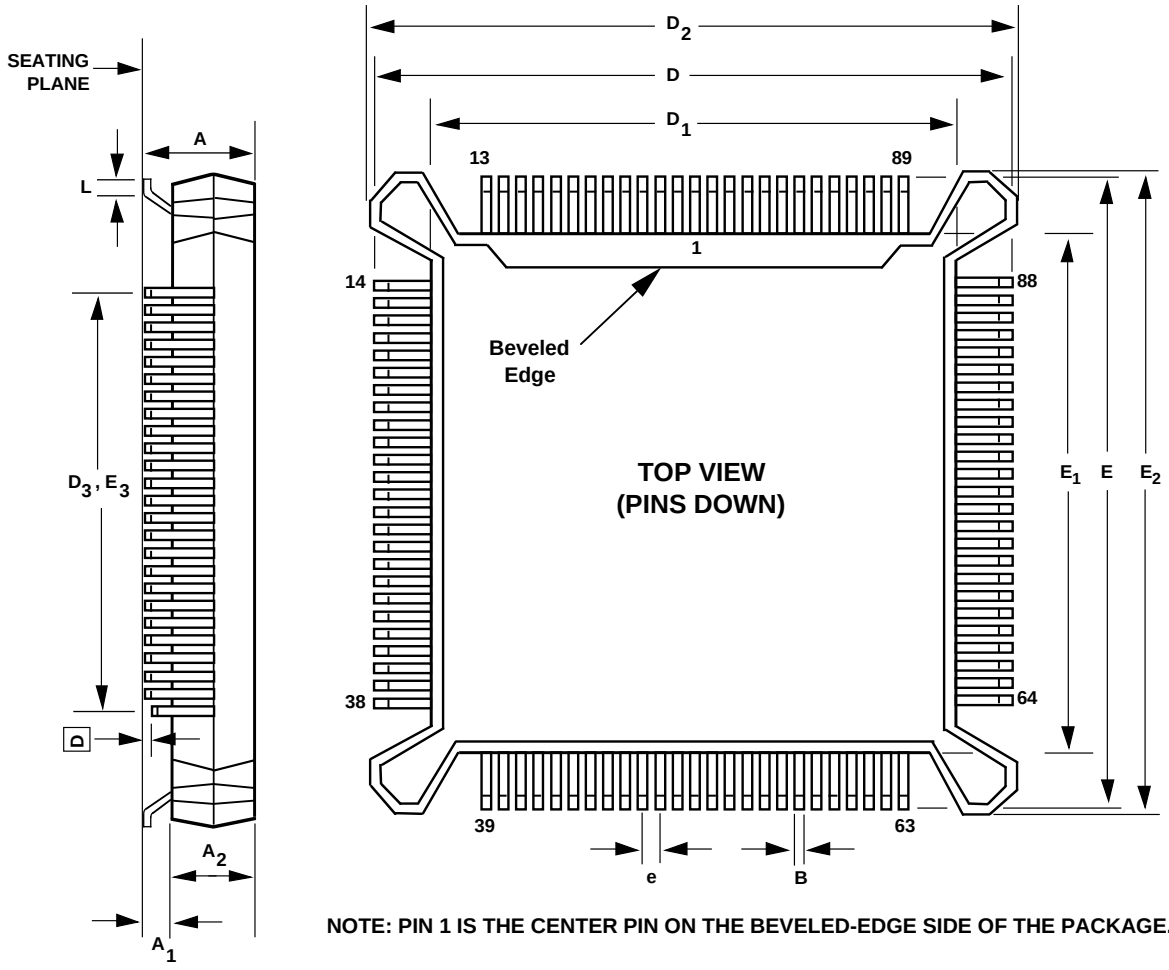
ADSP-2111
100-Pin Grid Array (PGA)



	INCHES			MILLIMETERS		
SYMBOL	MIN	TYP	MAX	MIN	TYP	MAX
A	0.123		0.169	3.12		4.29
A_1		0.050			1.27	
ϕb	0.016	0.018	0.020	0.41	0.46	0.51
ϕb_1		0.050			1.27	
D	1.308	1.32	1.342	33.22	33.53	34.09
e_1	1.188	1.20	1.212	30.18	30.48	30.78
e_2	0.988	1.00	1.012	25.10	25.4	25.70
e		0.100			2.54	
L_3		0.180			4.57	

OUTLINE DIMENSIONS

ADSP-2111
100-Lead Bumpered Plastic Quad Flatpack (PQFP)



NOTE: PIN 1 IS THE CENTER PIN ON THE BEVELED-EDGE SIDE OF THE PACKAGE.

	INCHES			MILLIMETERS		
SYMBOL	MIN	TYP	MAX	MIN	TYP	MAX
A			0.180			4.572
A_1	0.020	0.030	0.040	0.508	0.762	1.016
A_2	0.130	0.140	0.150	3.302	3.556	3.810
D, E	0.875	0.880	0.885	22.225	22.352	22.479
D_1, E_1	0.747	0.750	0.753	18.974	19.050	19.126
D_2, E_2	0.897	0.900	0.903	22.784	22.860	22.936
D_3, E_3		0.600	0.603		15.240	15.316
L	0.036		0.046	0.914		1.168
e	0.022	0.025	0.028	0.559	0.635	0.711
B	0.008		0.012	0.203		0.305
D			0.004			0.102

ORDERING GUIDE

Part Number[1]	Ambient Temperature Range	Instruction Rate (MHz)	Package Description	Package Option
ADSP-2101KG-66	0°C to +70°C	16.67 MHz	68-Pin PGA	G-68A
ADSP-2101BG-66	–40°C to +85°C	16.67 MHz	68-Pin PGA	G-68A
ADSP-2101KP-66	0°C to +70°C	16.67 MHz	68-Lead PLCC	P-68A
ADSP-2101BP-66	–40°C to +85°C	16.67 MHz	68-Lead PLCC	P-68A
ADSP-2101KS-66	0°C to +70°C	16.67 MHz	80-Lead PQFP	S-80
ADSP-2101BS-66	–40°C to +85°C	16.67 MHz	80-Lead PQFP	S-80
ADSP-2101KG-80	0°C to +70°C	20.0 MHz	68-Pin PGA	G-68A
ADSP-2101BG-80	–40°C to +85°C	20.0 MHz	68-Pin PGA	G-68A
ADSP-2101KP-80	0°C to +70°C	20.0 MHz	68-Lead PLCC	P-68A
ADSP-2101BP-80	–40°C to +85°C	20.0 MHz	68-Lead PLCC	P-68A
ADSP-2101KS-80	0°C to +70°C	20.0 MHz	80-Lead PQFP	S-80
ADSP-2101BS-80	–40°C to +85°C	20.0 MHz	80-Lead PQFP	S-80
ADSP-2101KP-100	0°C to +70°C	25.0 MHz	68-Pin PLCC	P-68A
ADSP-2101BP-100	–40°C to +85°C	25.0 MHz	68-Pin PLCC	P-68A
ADSP-2101KS-100	0°C to +70°C	25.0 MHz	80-Lead PQFP	S-80
ADSP-2101BS-100	–40°C to +85°C	25.0 MHz	80-Lead PQFP	S-80
ADSP-2101KG-100	0°C to +70°C	25.0 MHz	68-Lead PGA	G-68A
ADSP-2101BG-100	–40°C to +85°C	25.0 MHz	68-Lead PGA	G-68A
ADSP-2101TG-50	–55°C to +125°C	12.5 MHz	68-Pin PGA	G-68A
ADSP-2103KP-40 (3.3 V)	0°C to +70°C	10.24 MHz	68-Lead PLCC	P-68A
ADSP-2103BP-40 (3.3 V)	–40°C to +85°C	10.24 MHz	68-Lead PLCC	P-68A
ADSP-2103KS-40 (3.3 V)	0°C to +70°C	10.24 MHz	80-Lead PQFP	S-80
ADSP-2103BS-40 (3.3 V)	–40°C to +85°C	10.24 MHz	80-Lead PQFP	S-80
ADSP-2105KP-55	0°C to +70°C	13.824 MHz	68-Lead PLCC	P-68A
ADSP-2105BP-55	–40°C to +85°C	13.824 MHz	68-Lead PLCC	P-68A
ADSP-2105KP-80	0°C to +70°C	20.0 MHz	68-Lead PLCC	P-68A
ADSP-2105BP-80	–40°C to +85°C	20.0 MHz	68-Lead PLCC	P-68A
ADSP-2115KP-66	0°C to +70°C	16.67 MHz	68-Lead PLCC	P-68A
ADSP-2115BP-66	–40°C to +85°C	16.67 MHz	68-Lead PLCC	P-68A
ADSP-2115KS-66	0°C to +70°C	16.67 MHz	80-Lead PQFP	S-80
ADSP-2115BS-66	–40°C to +85°C	16.67 MHz	80-Lead PQFP	S-80
ADSP-2115KST-66	0°C to +70°C	16.67 MHz	80-Lead TQFP	ST-80
ADSP-2115BST-66	–40°C to +85°C	16.67 MHz	80-Lead TQFP	ST-80
ADSP-2115KP-80	0°C to +70°C	20.0 MHz	68-Lead PLCC	P-68A
ADSP-2115BP-80	–40°C to +85°C	20.0 MHz	68-Lead PLCC	P-68A
ADSP-2115KS-80	0°C to +70°C	20.0 MHz	80-Lead PQFP	S-80
ADSP-2115BS-80	–40°C to +85°C	20.0 MHz	80-Lead PQFP	S-80
ADSP-2115KST-80	0°C to +70°C	20.0 MHz	80-Lead TQFP	ST-80
ADSP-2115BST-80	–40°C to +85°C	20.0 MHz	80-Lead TQFP	ST-80
ADSP-2115KP-100	0°C to +70°C	25.0 MHz	68-Lead PLCC	P-68A
ADSP-2115BP-100	–40°C to +85°C	25.0 MHz	68-Lead PLCC	P-68A

NOTES
[1]K = Commercial Temperature Range (0°C to +70°C).
B = Industrial Temperature Range (–40°C to +85°C).
T = Extended Temperature Range (–55°C to +125°C).
G = Ceramic PGA (Pin Grid Array).
P = PLCC (Plastic Leaded Chip Carrier).
S = PQFP (Plastic Quad Flatpack).
ST = TQFP (Thin Quad Flatpack)

ORDERING GUIDE

Part Number[1]	Ambient Temperature Range	Instruction Rate (MHz)	Package Description	Package Option
ADSP-2111KG-52	0°C to +70°C	13.0 MHz	100-Pin PGA	G-100A
ADSP-2111BG-52	–40°C to +85°C	13.0 MHz	100-Pin PGA	G-100A
ADSP-2111KS-52	0°C to +70°C	13.0 MHz	100-Lead PQFP	S-100A
ADSP-2111BS-52	–40°C to +85°C	13.0 MHz	100-Lead PQFP	S-100A
ADSP-2111KG-66	0°C to +70°C	16.67 MHz	100-Pin PGA	G-100A
ADSP-2111BG-66	–40°C to +85°C	16.67 MHz	100-Pin PGA	G-100A
ADSP-2111KS-66	0°C to +70°C	16.67 MHz	100-Lead PQFP	S-100A
ADSP-2111BS-66	–40°C to +85°C	16.67 MHz	100-Lead PQFP	S-100A
ADSP-2111KG-80	0°C to +70°C	20.0 MHz	100-Pin PGA	G-100A
ADSP-2111BG-80	–40°C to +85°C	20.0 MHz	100-Pin PGA	G-100A
ADSP-2111KS-80	0°C to +70°C	20.0 MHz	100-Lead PQFP	S-100A
ADSP-2111BS-80	–40°C to +85°C	20.0 MHz	100-Lead PQFP	S-100A
ADSP-2111TG-52	–55°C to +125°C	13.0 MHz	100-Pin PGA	G-100A
ADSP-2161KP-66[2]	0°C to +70°C	16.67 MHz	68-Lead PLCC	P-68A
ADSP-2161BP-66[2]	–40°C to +85°C	16.67 MHz	68-Lead PLCC	P-68A
ADSP-2161KS-66[2]	0°C to +70°C	16.67 MHz	80-Lead PQFP	S-80
ADSP-2161BS-66[2]	–40°C to +85°C	16.67 MHz	80-Lead PQFP	S-80
ADSP-2162KP-40 (3.3 V)[2]	0°C to +70°C	10.24 MHz	68-Lead PLCC	P-68A
ADSP-2162BP-40 (3.3 V)[2]	–40°C to +85°C	10.24 MHz	68-Lead PLCC	P-68A
ADSP-2162KS-40 (3.3 V)[2]	0°C to +70°C	10.24 MHz	80-Lead PQFP	S-80
ADSP-2162BS-40 (3.3 V)[2]	–40°C to +85°C	10.24 MHz	80-Lead PQFP	S-80
ADSP-2163KP-66[2]	0°C to +70°C	16.67 MHz	68-Lead PLCC	P-68A
ADSP-2163BP-66[2]	–40°C to +85°C	16.67 MHz	68-Lead PLCC	P-68A
ADSP-2163KS-66[2]	0°C to +70°C	16.67 MHz	80-Lead PQFP	S-80
ADSP-2163BS-66[2]	–40°C to +85°C	16.67 MHz	80-Lead PQFP	S-80
ADSP-2163KP-100[2]	0°C to +70°C	25 MHz	68-Lead PLCC	P-68A
ADSP-2163BP-100[2]	–40°C to +85°C	25 MHz	68-Lead PLCC	P-68A
ADSP-2163KS-100[2]	0°C to +70°C	25 MHz	80-Lead PQFP	S-80
ADSP-2163BS-100[2]	–40°C to +85°C	25 MHz	80-Lead PQFP	S-80
ADSP-2164KP-40 (3.3 V)[2]	0°C to +70°C	10.24 MHz	68-Lead PLCC	P-68A
ADSP-2164BP-40 (3.3 V)[2]	–40°C to +85°C	10.24 MHz	68-Lead PLCC	P-68A
ADSP-2164KS-40 (3.3 V)[2]	0°C to +70°C	10.24 MHz	80-Lead PQFP	S-80
ADSP-2164BS-40 (3.3 V)[2]	–40°C to +85°C	10.24 MHz	80-Lead PQFP	S-80

NOTES
[1]K = Commercial Temperature Range (0°C to +70°C).
B = Industrial Temperature Range (–40°C to +85°C).
T = Extended Temperature Range (–55°C to +125°C).
G = Ceramic PGA (Pin Grid Array).
P = PLCC (Plastic Leaded Chip Carrier).
S = PQFP (Plastic Quad Flatpack).
[2]Minimum order quantities required. Contact factory for further information.

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