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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	Synchronous Serial Port (SSP)
Clock Rate	20MHz
Non-Volatile Memory	External
On-Chip RAM	3kB
Voltage - I/O	5.00V
Voltage - Core	5.00V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	68-LCC (J-Lead)
Supplier Device Package	68-PLCC (24.23x24.23)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-2105bp-80

Table I. ADSP-21xx Processor Features

Feature	2101	2103	2105	2115	2111
Data Memory (RAM)	1K	1K	½K	½K	1K
Program Memory (RAM)	2K	2K	1K	1K	2K
Timer	●	●	●	●	●
Serial Port 0 (Multichannel)	●	●	–	●	●
Serial Port 1	●	●	●	●	●
Host Interface Port	–	–	–	–	●
Speed Grades *(Instruction Cycle Time)*					
10.24 MHz *(76.9 ns)*	–	●	–	–	–
13.0 MHz *(76.9 ns)*	–	–	–	–	●
13.824 MHz *(72.3 ns)*	–	–	●	–	–
16.67 MHz *(60 ns)*	●	–	–	●	●
20.0 MHz *(50 ns)*	●	–	●	●	●
25 MHz *(40 ns)*	●	–	–	●	–
Supply Voltage	5 V	3.3 V	5 V	5 V	5 V
Packages					
68-Pin PGA	●	–	–	–	–
68-Lead PLCC	●	●	●	●	–
80-Lead PQFP	●	●	–	●	–
80-Lead TQFP	–	–	–	●	–
100-Pin PGA	–	–	–	–	●
100-Lead PQFP	–	–	–	–	●
Temperature Grades					
K *Commercial* 0°C to +70°C	●	●	●	●	●
B *Industrial* –40°C to +85°C	●	●	●	●	●
T *Extended* –55°C to +125°C	●	–	–	–	●

Table II. ADSP-216x ROM-Programmed Processor Features

Feature	2161	2162	2163	2164
Data Memory (RAM)	½K	½K	½K	½K
Program Memory (ROM)	8K	8K	4K	4K
Program Memory (RAM)	–	–	–	–
Timer	●	●	●	●
Serial Port 0 (Multichannel)	●	●	●	●
Serial Port 1	●	●	●	●
Supply Voltage	5 V	3.3 V	5 V	3.3 V
Speed Grades *(Instruction Cycle Time)*				
10.24 MHz *(97.6 ns)*	–	●	–	●
16.67 MHz *(60 ns)*	●	–	●	–
25 MHz *(40 ns)*	–	–	●	–
Packages				
68-Lead PLCC	●	●	●	●
80-Lead PQFP	●	●	●	●
Temperature Grades				
K *Commercial* 0°C to +70°C	●	●	●	●
B *Industrial* –40°C to +85°C	●	●	●	●

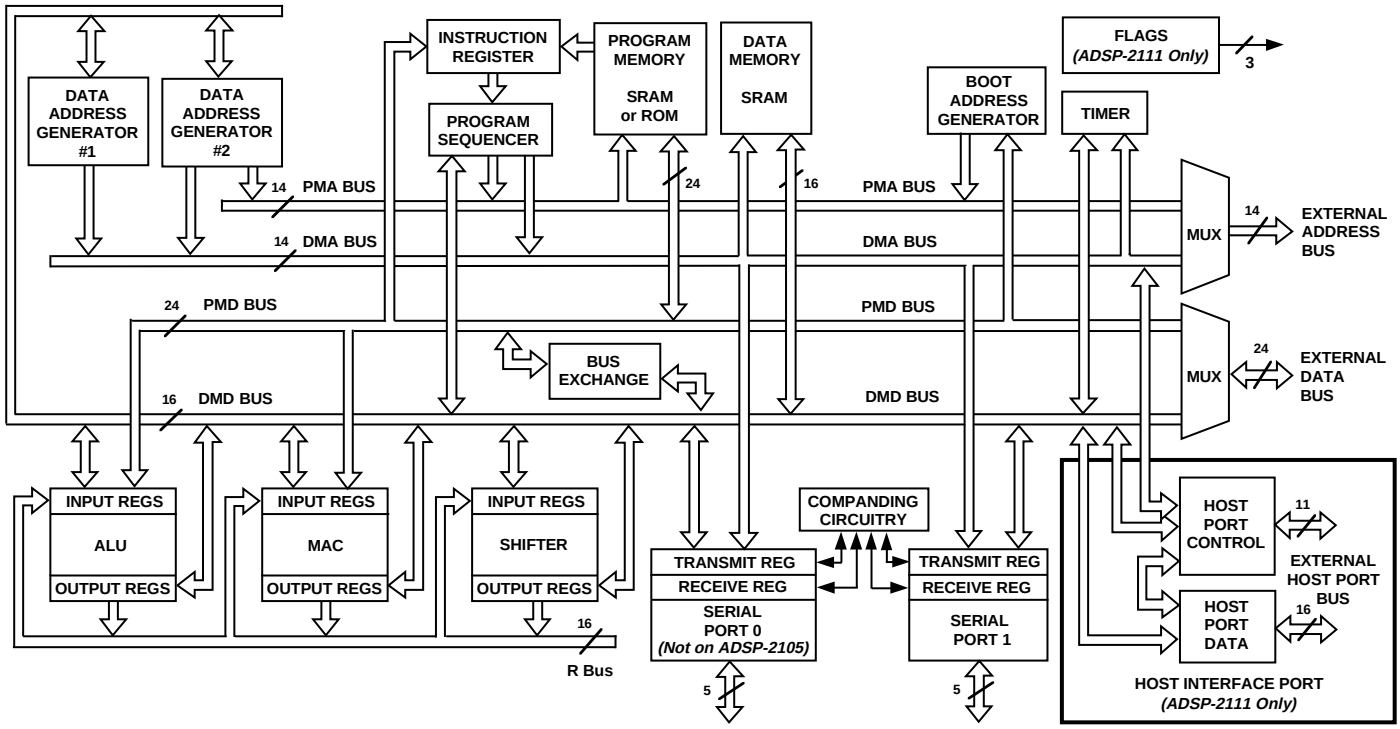


Figure 1. ADSP-21xx Block Diagram

One bus grant execution mode (GO Mode) allows the ADSP-21xx to continue running from internal memory. A second execution mode requires the processor to halt while buses are granted.

Each ADSP-21xx processor can respond to several different interrupts. There can be up to three external interrupts, configured as edge- or level-sensitive. Internal interrupts can be generated by the timer, serial ports, and, on the ADSP-2111, the host interface port. There is also a master $\overline{\text{RESET}}$ signal.

Booting circuitry provides for loading on-chip program memory automatically from byte-wide external memory. After reset, three wait states are automatically generated. This allows, for example, a 60 ns ADSP-2101 to use a 200 ns EPROM as external boot memory. Multiple programs can be selected and loaded from the EPROM with no additional hardware.

The data receive and transmit pins on SPORT1 (Serial Port 1) can be alternatively configured as a general-purpose input flag and output flag. You can use these pins for event signalling to and from an external device. The ADSP-2111 has three additional flag outputs whose states are controlled through software.

A programmable interval timer can generate periodic interrupts. A 16-bit count register (TCOUNT) is decremented every *n* cycles, where *n–1* is a scaling value stored in an 8-bit register (TSCALE). When the value of the count register reaches zero, an interrupt is generated and the count register is reloaded from a 16-bit period register (TPERIOD).

Serial Ports

The ADSP-21xx processors include two synchronous serial ports (“SPORTs”) for serial communications and multiprocessor communication. All of the ADSP-21xx processors have two serial ports (SPORT0, SPORT1) except for the ADSP-2105, which has only SPORT1.

The serial ports provide a complete synchronous serial interface with optional companding in hardware. A wide variety of framed or frameless data transmit and receive modes of operation are available. Each SPORT can generate an internal programmable serial clock or accept an external serial clock.

Each serial port has a 5-pin interface consisting of the following signals:

Signal Name	Function
SCLK	Serial Clock (I/O)
RFS	Receive Frame Synchronization (I/O)
TFS	Transmit Frame Synchronization (I/O)
DR	Serial Data Receive
DT	Serial Data Transmit

The ADSP-21xx serial ports offer the following capabilities:

Bidirectional—Each SPORT has a separate, double-buffered transmit and receive function.

Flexible Clocking—Each SPORT can use an external serial clock or generate its own clock internally.

Flexible Framing—The SPORTs have independent framing for the transmit and receive functions; each function can run in a frameless mode or with frame synchronization signals internally generated or externally generated; frame sync signals may be active high or inverted, with either of two pulse widths and timings.

Different Word Lengths—Each SPORT supports serial data word lengths from 3 to 16 bits.

Companding in Hardware—Each SPORT provides optional A-law and μ-law companding according to CCITT recommendation G.711.

Flexible Interrupt Scheme—Receive and transmit functions can generate a unique interrupt upon completion of a data word transfer.

Autobuffering with Single-Cycle Overhead—Each SPORT can automatically receive or transmit the contents of an entire circular data buffer with only one overhead cycle per data word; an interrupt is generated after the transfer of the entire buffer is completed.

Multichannel Capability (SPORT0 Only)—SPORT0 provides a multichannel interface to selectively receive or transmit a 24-word or 32-word, time-division multiplexed serial bit stream; this feature is especially useful for T1 or CEPT interfaces, or as a network communication scheme for multiple processors. (Note that the ADSP-2105 includes only SPORT1, not SPORT0, and thus does not offer multichannel operation.)

Alternate Configuration—SPORT1 can be alternatively configured as two external interrupt inputs ($\overline{IRQ0}$, $\overline{IRQ1}$) and the Flag In and Flag Out signals (FI, FO).

Host Interface Port (ADSP-2111)

The ADSP-2111 includes a Host Interface Port (HIP), a parallel I/O port that allows easy connection to a host processor. Through the HIP, the ADSP-2111 can be accessed by the host processor as a memory-mapped peripheral. The host interface port can be thought of as an area of dual-ported memory, or mailbox registers, that allows communication between the computational core of the ADSP-2111 and the host computer. The host interface port is completely asynchronous. The host processor can write data into the HIP while the ADSP-2111 is operating at full speed.

Three pins configure the HIP for operation with different types of host processors. The HSIZE pin configures HIP for 8- or 16-bit communication with the host processor. HMD0 configures the bus strobes, selecting either separate read and write strobes or a single read/write select and a host data strobe. HMD1 selects either separate address (3-bit) and data (16-bit) buses or a multiplexed 16-bit address/data bus with address latch enable. Tying these pins to appropriate values configures the ADSP-2111 for straight-wire interface to a variety of industry-standard microprocessors and microcomputers.

The HIP contains six data registers (HDR5-0) and two status registers (HSR7-6) with an associated HMASK register for masking interrupts from individual HIP data registers. The HIP data registers are memory-mapped in the internal data memory of the ADSP-2111. The two status registers provide status information to both the ADSP-2111 and the host processor. HSR7 contains a software reset bit which can be set by both the ADSP-2111 and the host.

HIP transfers can be managed using either interrupts or polling. The HIP generates an interrupt whenever an HDR register receives data from a host processor write. It also generates an interrupt when the host processor has performed a successful read of any HDR. The read/write status of the HDRs is also stored in the HSR registers.

The HMASK register bits can be used to mask the generation of read or write interrupts from individual HDR registers. Bits in the IMASK register enable and disable all HIP read interrupts or all HIP write interrupts. So, for example, a write to HDR4 will cause an interrupt only if both the *HDR4 Write* bit in HMASK and the *HIP Write* interrupt enable bit in IMASK are set.

The HIP provides a second method of booting the ADSP-2111 in which the host processor loads instructions into the HIP. The ADSP-2111 automatically transfers the data, in this case opcodes, to internal program memory. The BMODE pin determines whether the ADSP-2111 boots from the host processor through the HIP or from external EPROM over the data bus.

Interrupts

The ADSP-21xx's interrupt controller lets the processor respond to interrupts with a minimum of overhead. Up to three external interrupt input pins, $\overline{IRQ0}$, $\overline{IRQ1}$, and $\overline{IRQ2}$, are provided. $\overline{IRQ2}$ is always available as a dedicated pin; $\overline{IRQ1}$ and $\overline{IRQ0}$ may be alternately configured as part of Serial Port 1. The ADSP-21xx also supports internal interrupts from the timer, the serial ports, and the host interface port (on the ADSP-2111). The interrupts are internally prioritized and individually maskable (except for $\overline{RESET}$ which is non-maskable). The $\overline{IRQx}$ input pins can be programmed for either level- or edge-sensitivity. The interrupt priorities for each ADSP-21xx processor are shown in Table III.

The ADSP-21xx uses a vectored interrupt scheme: when an interrupt is acknowledged, the processor shifts program control to the interrupt vector address corresponding to the interrupt received. Interrupts can be optionally nested so that a higher priority interrupt can preempt the currently executing interrupt service routine. Each interrupt vector location is four instructions in length so that simple service routines can be coded entirely in this space. Longer service routines require an additional JUMP or CALL instruction.

Individual interrupt requests are logically ANDed with the bits in the IMASK register; the highest-priority unmasked interrupt is then selected.

The interrupt control register, ICNTL, allows the external interrupts to be set as either edge- or level-sensitive. Depending on bit 4 in ICNTL, interrupt service routines can either be nested (with higher priority interrupts taking precedence) or be processed sequentially (with only one interrupt service active at a time).

The interrupt force and clear register, IFC, is a write-only register that contains a force bit and a clear bit for each interrupt (except for level-sensitive interrupts and the ADSP-2111 HIP interrupts—these cannot be forced or cleared in software).

When responding to an interrupt, the ASTAT, MSTAT, and IMASK status registers are pushed onto the status stack and the PC counter is loaded with the appropriate vector address. The status stack is seven levels deep (nine levels deep on the ADSP-2111) to allow interrupt nesting. The stack is automatically popped when a return from the interrupt instruction is executed.

Pin Definitions

Table IV (on next page) shows pin definitions for the ADSP-21xx processors. Any inputs not used must be tied to V_{DD}.

Table III. Interrupt Vector Addresses & Priority

ADSP-2105 Interrupt Source	**Interrupt Vector Address**
$\overline{\text{RESET}}$ Startup	0x0000
$\overline{\text{IRQ2}}$	0x0004 *(High Priority)*
SPORT1 Transmit *or* $\overline{\text{IRQ1}}$	0x0010
SPORT1 Receive *or* $\overline{\text{IRQ0}}$	0x0014
Timer	0x0018 *(Low Priority)*

ADSP-2101/2103/2115/216x Interrupt Source	**Interrupt Vector Address**
$\overline{\text{RESET}}$ Startup	0x0000
$\overline{\text{IRQ2}}$	0x0004 *(High Priority)*
SPORT0 Transmit	0x0008
SPORT0 Receive	0x000C
SPORT1 Transmit *or* $\overline{\text{IRQ1}}$	0x0010
SPORT1 Receive *or* $\overline{\text{IRQ0}}$	0x0014
Timer	0x0018 *(Low Priority)*

ADSP-2111 Interrupt Source	**Interrupt Vector Address**
$\overline{\text{RESET}}$ Startup	0x0000
$\overline{\text{IRQ2}}$	0x0004 *(High Priority)*
HIP Write from Host	0x0008
HIP Read to Host	0x000C
SPORT0 Transmit	0x0010
SPORT0 Receive	0x0014
SPORT1 Transmit *or* $\overline{\text{IRQ1}}$	0x0018
SPORT1 Receive *or* $\overline{\text{IRQ0}}$	0x001C
Timer	0x0020 *(Low Priority)*

SYSTEM INTERFACE

Figure 3 shows a typical system for the ADSP-2101, ADSP-2115, or ADSP-2103, with two serial I/O devices, a boot EPROM, and optional external program and data memory. A total of 15K words of data memory and 16K words of program memory is addressable for the ADSP-2101 and ADSP-2103. A total of 14.5K words of data memory and 15K words of program memory is addressable for the ADSP-2115.

Figure 4 shows a system diagram for the ADSP-2105, with one serial I/O device, a boot EPROM, and optional external program and data memory. A total of 14.5K words of data memory and 15K words of program memory is addressable for the ADSP-2105.

Figure 5 shows a system diagram for the ADSP-2111, with two serial I/O devices, a host processor, a boot EPROM, and optional external program and data memory. A total of 15K words of data memory and 16K words of program memory is addressable.

Programmable wait-state generation allows the processors to easily interface to slow external memories.

The ADSP-2101, ADSP-2103, ADSP-2115, and ADSP-2111 processors also provide either: one external interrupt ($\overline{\text{IRQ2}}$) and two serial ports (SPORT0, SPORT1), *or* three external interrupts ($\overline{\text{IRQ2}}$, $\overline{\text{IRQ1}}$, $\overline{\text{IRQ0}}$) and one serial port (SPORT0).

The ADSP-2105 provides either: one external interrupt ($\overline{\text{IRQ2}}$) and one serial port (SPORT1), *or* three external interrupts ($\overline{\text{IRQ2}}$, $\overline{\text{IRQ1}}$, $\overline{\text{IRQ0}}$) with no serial port.

Clock Signals

The ADSP-21xx processors' CLKIN input may be driven by a crystal or by a TTL-compatible external clock signal. The CLKIN input may not be halted or changed in frequency during operation, nor operated below the specified low frequency limit.

If an external clock is used, it should be a TTL-compatible signal running at the instruction rate. The signal should be connected to the processor's CLKIN input; in this case, the XTAL input must be left unconnected.

Because the ADSP-21xx processors include an on-chip oscillator circuit, an external crystal may also be used. The crystal should be connected across the CLKIN and XTAL pins, with two capacitors connected as shown in Figure 2. A parallel-resonant, fundamental frequency, microprocessor-grade crystal should be used.

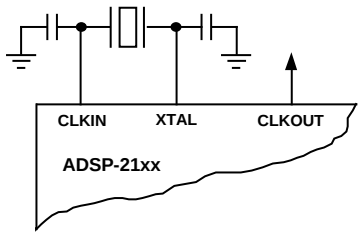


Figure 2. External Crystal Connections

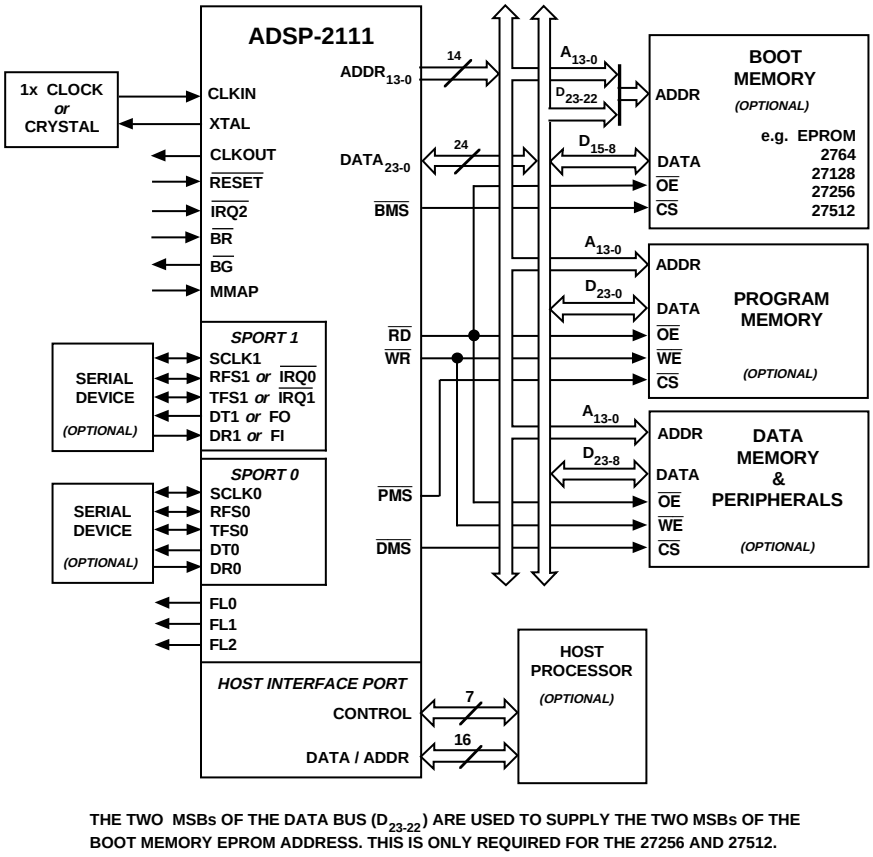


Figure 5. ADSP-2111 System

The $\overline{\text{RESET}}$ input resets all internal stack pointers to the empty stack condition, masks all interrupts, and clears the MSTAT register. When $\overline{\text{RESET}}$ is released, the boot loading sequence is performed (provided there is no pending bus request and the chip is configured for booting, with MMAP = 0). The first instruction is then fetched from internal program memory location 0x0000.

Program Memory Interface

The on-chip program memory address bus (PMA) and on-chip program memory data bus (PMD) are multiplexed with the on-chip data memory buses (DMA, DMD), creating a single external data bus and a single external address bus. The external data bus is bidirectional and is 24 bits wide to allow instruction fetches from external program memory. Program memory may contain code and data.

The external address bus is 14 bits wide. For the ADSP-2101, ADSP-2103, and ADSP-2111, these lines can directly address up to 16K words, of which 2K are on-chip. For the ADSP-2105 and ADSP-2115, the address lines can directly address up to 15K words, of which 1K is on-chip.

The data lines are bidirectional. The program memory select ($\overline{\text{PMS}}$) signal indicates accesses to program memory and can be used as a chip select signal. The write ($\overline{\text{WR}}$) signal indicates a write operation and is used as a write strobe. The read ($\overline{\text{RD}}$) signal indicates a read operation and is used as a read strobe or output enable signal.

The ADSP-21xx processors write data from their 16-bit registers to 24-bit program memory using the PX register to provide the lower eight bits. When the processor reads 16-bit data from 24-bit program memory to a 16-bit data register, the lower eight bits are placed in the PX register.

The program memory interface can generate 0 to 7 wait states for external memory devices; default is to 7 wait states after $\overline{\text{RESET}}$.

Program Memory Maps

Program memory can be mapped in two ways, depending on the state of the MMAP pin. Figure 6 shows the two program memory maps for the ADSP-2101, ADSP-2103, and ADSP-2111. Figure 8 shows the program memory maps for the ADSP-2105 and ADSP-2115. Figures 7 and 9 show the program memory maps for the ADSP-2161/62 and ADSP-2163/64, respectively.

Data Memory Interface
The data memory address bus (DMA) is 14 bits wide. The bidirectional external data bus is 24 bits wide, with the upper 16 bits used for data memory data (DMD) transfers.

The data memory select ($\overline{DMS}$) signal indicates access to data memory and can be used as a chip select signal. The write ($\overline{WR}$) signal indicates a write operation and can be used as a write strobe. The read ($\overline{RD}$) signal indicates a read operation and can be used as a read strobe or output enable signal.

The ADSP-21xx processors support memory-mapped I/O, with the peripherals memory-mapped into the data memory address space and accessed by the processor in the same manner as data memory.

Data Memory Map
ADSP-2101/ADSP-2103/ADSP-2111
For the ADSP-2101, ADSP-2103, and ADSP-2111, on-chip data memory RAM resides in the 1K words beginning at address 0x3800, as shown in Figure 10. Data memory locations from 0x3C00 to the end of data memory at 0x3FFF are reserved. Control and status registers for the system, timer, wait-state configuration, and serial port operations are located in this region of memory.

ADSP-2105/ADSP-2115
For the ADSP-2105 and ADSP-2115, on-chip data memory RAM resides in the 512 words beginning at address 0x3800, also shown in Figure 10. Data memory locations from 0x3A00 to the end of data memory at 0x3FFF are reserved. Control and status registers for the system, timer, wait-state configuration, and serial port operations are located in this region of memory.

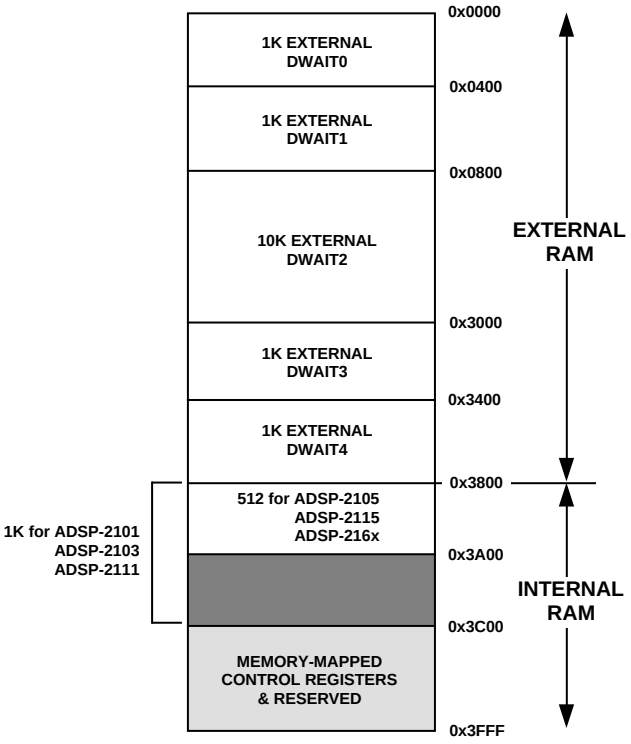


Figure 10. Data Memory Map (All Processors)

All Processors
The remaining 14K of data memory is located off-chip. This external data memory is divided into five zones, each associated with its own wait-state generator. This allows slower peripherals to be memory-mapped into data memory for which wait states are specified. By mapping peripherals into different zones, you can accommodate peripherals with different wait-state requirements. All zones default to seven wait states after $\overline{RESET}$.

Boot Memory Interface
On the ADSP-2101, ADSP-2103, and ADSP-2111, boot memory is an external 64K by 8 space, divided into eight separate 8K by 8 pages. On the ADSP-2105 and ADSP-2115, boot memory is a 32K by 8 space, divided into eight separate 4K by 8 pages. The 8-bit bytes are automatically packed into 24-bit instruction words by each processor, for loading into on-chip program memory.

Three bits in the processors' System Control Register select which page is loaded by the boot memory interface. Another bit in the System Control Register allows the forcing of a boot loading sequence under software control. Boot loading from Page 0 after $\overline{RESET}$ is initiated automatically if MMAP = 0.

The boot memory interface can generate zero to seven wait states; it defaults to three wait states after $\overline{RESET}$. This allows the ADSP-21xx to boot from a single low cost EPROM such as a 27C256. Program memory is booted one byte at a time and converted to 24-bit program memory words.

The $\overline{BMS}$ and $\overline{RD}$ signals are used to select and to strobe the boot memory interface. Only 8-bit data is read over the data bus, on pins D8-D15. To accommodate up to eight pages of boot memory, the two MSBs of the data bus are used in the boot memory interface as the two MSBs of the boot memory address: D23, D22, and A13 supply the boot page number.

The ADSP-2100 Family Assembler and Linker allow the creation of programs and data structures requiring multiple boot pages during execution.

The $\overline{BR}$ signal is recognized during the booting sequence. The bus is granted after loading the current byte is completed. $\overline{BR}$ during booting may be used to implement booting under control of a host processor.

Bus Interface
The ADSP-21xx processors can relinquish control of their data and address buses to an external device. When the external device requires control of the buses, it asserts the bus request signal ($\overline{BR}$). If the ADSP-21xx is not performing an external memory access, it responds to the active $\overline{BR}$ input in the next cycle by:

- Three-stating the data and address buses and the $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ output drivers,
- Asserting the bus grant ($\overline{BG}$) signal,
- and halting program execution.

If the Go mode is set, however, the ADSP-21xx will not halt program execution until it encounters an instruction that requires an external memory access.

If the ADSP-21xx is performing an external memory access when the external device asserts the $\overline{BR}$ signal, it will not three-state the memory interfaces or assert the $\overline{BG}$ signal until the cycle after the access completes (up to eight cycles later depending on the number of wait states). The instruction does not need to be completed when the bus is granted; the ADSP-21xx will grant the bus in between two memory accesses if an instruction requires more than one external memory access.

When the $\overline{BR}$ signal is released, the processor releases the $\overline{BG}$ signal, re-enables the output drivers and continues program execution from the point where it stopped.

The bus request feature operates at all times, including when the processor is booting and when $\overline{RESET}$ is active. If this feature is not used, the $\overline{BR}$ input should be tied high (to V_{DD}).

Low Power IDLE Instruction

The IDLE instruction places the ADSP-21xx processor in low power state in which it waits for an interrupt. When an interrupt occurs, it is serviced and execution continues with instruction following IDLE. Typically this next instruction will be a JUMP back to the IDLE instruction. This implements a low-power standby loop.

The *IDLE n* instruction is a special version of IDLE that slows the processor's internal clock signal to further reduce power consumption. The reduced clock frequency, a programmable fraction of the normal clock rate, is specified by a selectable divisor, *n*, given in the IDLE instruction. The syntax of the instruction is:

IDLE n;

where *n* = 16, 32, 64, or 128.

The instruction leaves the chip in an idle state, operating at the slower rate. While it is in this state, the processor's other internal clock signals, such as SCLK, CLKOUT, and the timer clock, are reduced by the same ratio. Upon receipt of an enabled interrupt, the processor will stay in the IDLE state for up to a maximum of *n* CLKIN cycles, where *n* is the divisor specified in the instruction, before resuming normal operation.

When the *IDLE n* instruction is used, it slows the processor's internal clock and thus its response time to incoming interrupts–the 1-cycle response time of the standard IDLE state is increased by *n*, the clock divisor. When an enabled interrupt is received, the ADSP-21xx will remain in the IDLE state for up to a maximum of *n* CLKIN cycles (where *n* = 16, 32, 64, or 128) before resuming normal operation.

When the *IDLE n* instruction is used in systems that have an externally generated serial clock (SCLK), the serial clock rate may be faster than the processor's reduced internal clock rate. Under these conditions, interrupts must not be generated at a faster rate than can be serviced, due to the additional time the processor takes to come out of the IDLE state (a maximum of *n* CLKIN cycles).

ADSP-216x Prototyping

You can prototype your ADSP-216x system with either the ADSP-2101 or ADSP-2103 RAM-based processors. When code is fully developed and debugged, it can be submitted to Analog Devices for conversion into a ADSP-216x ROM product.

The ADSP-2101 EZ-ICE emulator can be used for development of ADSP-216x systems. For the 3.3 V ADSP-2162 and ADSP-2164, a voltage converter interface board provides 3.3 V emulation.

Additional overlay memory is used for emulation of ADSP-2161/62 systems. It should be noted that due to the use of off-chip overlay memory to emulate the ADSP-2161/62, a performance loss may be experienced when both executing instructions and fetching program memory data from the off-chip overlay memory in the same cycle. This can be overcome by locating program memory data in on-chip memory.

Ordering Procedure for ADSP-216x ROM Processors

To place an order for a custom ROM-coded ADSP-2161, ADSP-2162, ADSP-2163, or ADSP-2164 processor, you must:

1. Complete the following forms contained in the *ADSP ROM Ordering Package*, available from your Analog Devices sales representative:

   ADSP-216x ROM Specification Form

   ROM Release Agreement

   ROM NRE Agreement & Minimum Quantity Order (MQO) Acceptance Agreement for Pre-Production ROM Products

2. Return the forms to Analog Devices along with two copies of the Memory Image File (.EXE file) of your ROM code. The files must be supplied on two 3.5" or 5.25" floppy disks for the IBM PC (DOS 2.01 or higher).

3. Place a purchase order with Analog Devices for non-recurring engineering changes (NRE) associated with ROM product development.

After this information is received, it is entered into Analog Devices' ROM Manager System which assigns a custom ROM model number to the product. This model number will be branded on all prototype and production units manufactured to these specifications.

To minimize the risk of code being altered during this process, Analog Devices verifies that the .EXE files on both floppy disks are identical, and recalculates the checksums for the .EXE file entered into the ROM Manager System. The checksum data, in the form of a ROM Memory Map, a hard copy of the .EXE file, and a ROM Data Verification form are returned to you for inspection.

SPECIFICATIONS (ADSP-2111)

SUPPLY CURRENT & POWER (ADSP-2111)

Parameter		Test Conditions	Min	Max	Unit
I_{DD}	Supply Current (Dynamic)[1]	@ V_{DD} = max, t_{CK} = 50 ns[2]		60	mA
		@ V_{DD} = max, t_{CK} = 60 ns[2]		52	mA
		@ V_{DD} = max, t_{CK} = 76.9 ns[2]		46	mA
I_{DD}	Supply Current (Idle)[1, 3]	@ V_{DD} = max, t_{CK} = 50 ns		18	mA
		@ V_{DD} = max, t_{CK} = 60 ns		16	mA
		@ V_{DD} = max, t_{CK} = 76.9 ns		14	mA

NOTES
[1]Current reflects device operating with no output loads.
[2]V_{IN} = 0.4 V and 2.4 V.
[3]Idle refers to ADSP-21xx state of operation during execution of IDLE instruction. Deasserted pins are driven to either V_{DD} or GND.

For typical supply current (internal power dissipation) figures, see Figure 17.

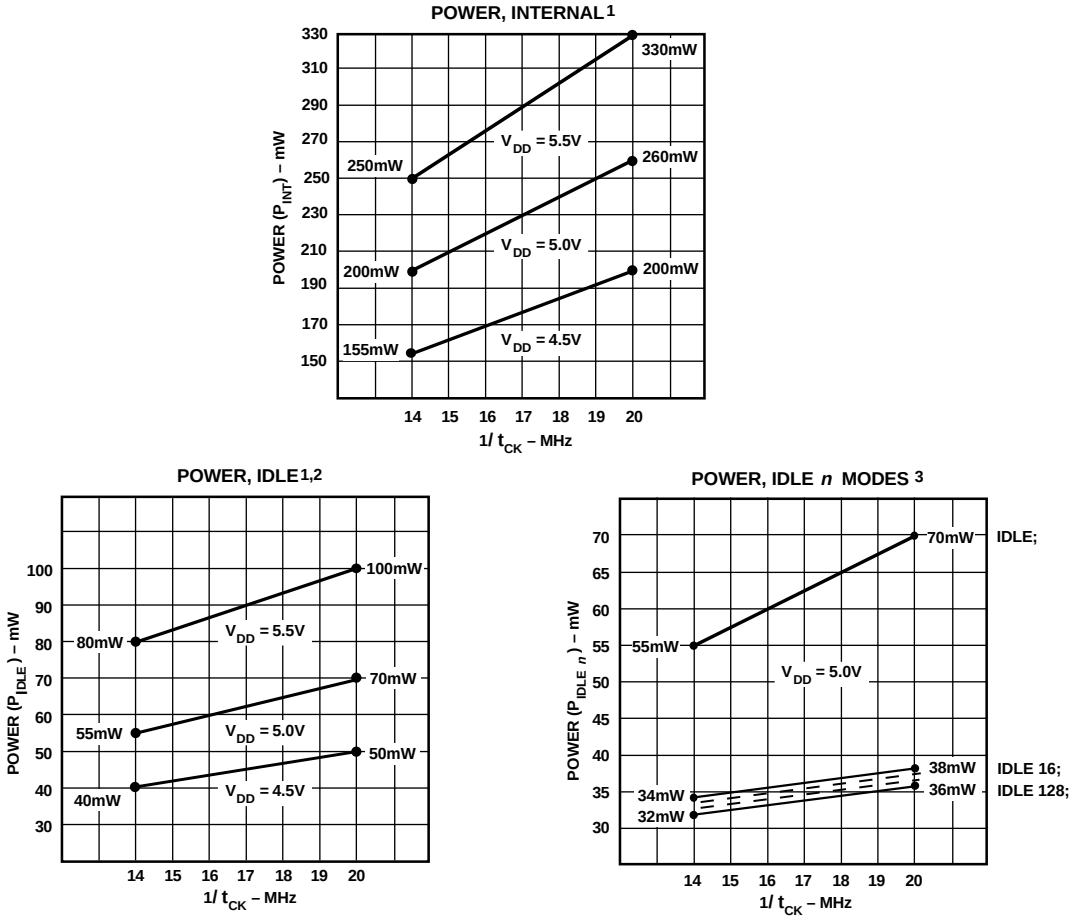


Figure 17. ADSP-2111 Power (Typical) vs. Frequency

SPECIFICATIONS (ADSP-2111)

POWER DISSIPATION EXAMPLE

To determine total power dissipation in a specific application, the following equation should be applied for each output:

$$C \times V_{DD}^2 \times f$$

C = load capacitance, f = output switching frequency.

Example:

In an ADSP-2111 application where external data memory is used and no other outputs are active, power dissipation is calculated as follows:

Assumptions:

- External data memory is accessed every cycle with 50% of the address pins switching.
- External data memory writes occur every other cycle with 50% of the data pins switching.
- Each address and data pin has a 10 pF total load at the pin.
- The application operates at V_{DD} = 5.0 V and t_{CK} = 50 ns.

$$\textit{Total Power Dissipation} = P_{INT} + (C \times V_{DD}^2 \times f)$$

P_{INT} = internal power dissipation (from Figure 17).

$(C \times V_{DD}^2 \times f)$ is calculated for each output:

Output	# of Pins	× C	× V_{DD}^2	× f
Address, $\overline{DMS}$	8	× 10 pF	× 5^2 V	× 20 MHz = 40.0 mW
Data, $\overline{WR}$	9	× 10 pF	× 5^2 V	× 10 MHz = 22.5 mW
$\overline{RD}$	1	× 10 pF	× 5^2 V	× 10 MHz = 2.5 mW
CLKOUT	1	× 10 pF	× 5^2 V	× 20 MHz = 5.0 mW
				70.0 mW

Total power dissipation for this example = P_{INT} + 70.0 mW.

ENVIRONMENTAL CONDITIONS

Ambient Temperature Rating:

$T_{AMB} = T_{CASE} - (PD \times \theta_{CA})$
T_{CASE} = Case Temperature in °C
PD = Power Dissipation in W
θ_{CA} = Thermal Resistance (Case-to-Ambient)
θ_{JA} = Thermal Resistance (Junction-to-Ambient)
θ_{JC} = Thermal Resistance (Junction-to-Case)

Package	θ_{JA}	θ_{JC}	θ_{CA}
PGA	35°C/W	18°C/W	17°C/W
PQFP	42°C/W	18°C/W	23°C/W

CAPACITIVE LOADING

Figures 18 and 19 show capacitive loading characteristics for the ADSP-2111.

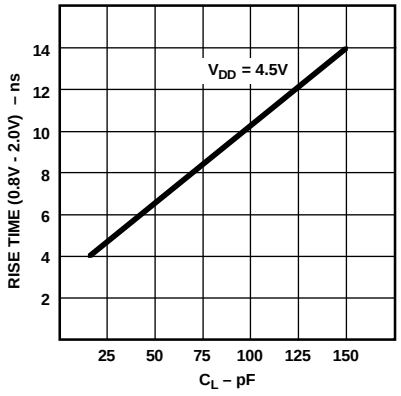


Figure 18. Typical Output Rise Time vs. Load Capacitance, C_L (at Maximum Ambient Operating Temperature)

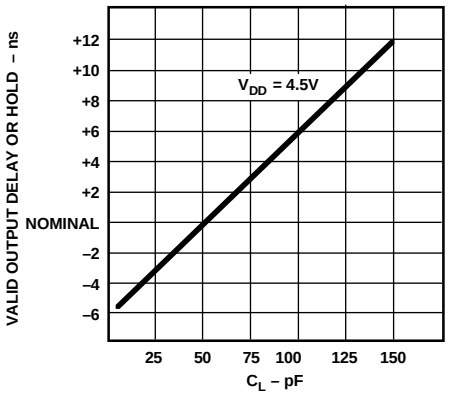


Figure 19. Typical Output Valid Delay or Hold vs. Load Capacitance, C_L (at Maximum Ambient Operating Temperature)

SPECIFICATIONS (ADSP-2103/2162/2164)

POWER DISSIPATION EXAMPLE

To determine total power dissipation in a specific application, the following equation should be applied for each output:

$$C \times V_{DD}^2 \times f$$

C = load capacitance, f = output switching frequency.

Example:

In an ADSP-2103 application where external data memory is used and no other outputs are active, power dissipation is calculated as follows:

Assumptions:

- External data memory is accessed every cycle with 50% of the address pins switching.
- External data memory writes occur every other cycle with 50% of the data pins switching.
- Each address and data pin has a 10 pF total load at the pin.
- The application operates at V_{DD} = 3.3 V and t_{CK} = 100 ns.

$$\textit{Total Power Dissipation} = P_{INT} + (C \times V_{DD}^2 \times f)$$

P_{INT} = internal power dissipation (from Figure 23).

$(C \times V_{DD}^2 \times f)$ is calculated for each output:

Output	# of Pins	× C	× V_{DD}^2	× f	
Address, $\overline{DMS}$	8	× 10 pF	× 3.3^2 V	× 10 MHz	= 8.71 mW
Data, $\overline{WR}$	9	× 10 pF	× 3.3^2 V	× 5 MHz	= 4.90 mW
$\overline{RD}$	1	× 10 pF	× 3.3^2 V	× 5 MHz	= 0.55 mW
CLKOUT	1	× 10 pF	× 3.3^2 V	× 10 MHz	= 1.09 mW
					15.25 mW

Total power dissipation for this example = P_{INT} + 15.25 mW.

ENVIRONMENTAL CONDITIONS

Ambient Temperature Rating:

$T_{AMB} = T_{CASE} - (PD \times \theta_{CA})$
T_{CASE} = Case Temperature in °C
PD = Power Dissipation in W
θ_{CA} = Thermal Resistance (Case-to-Ambient)
θ_{JA} = Thermal Resistance (Junction-to-Ambient)
θ_{JC} = Thermal Resistance (Junction-to-Case)

Package	θ_{JA}	θ_{JC}	θ_{CA}
PGA	27°C/W	16°C/W	11°C/W
PQFP	60°C/W	18°C/W	42°C/W

CAPACITIVE LOADING

Figures 24 and 25 show capacitive loading characteristics for the ADSP-2103, ADSP-2162, and ADSP-2164.

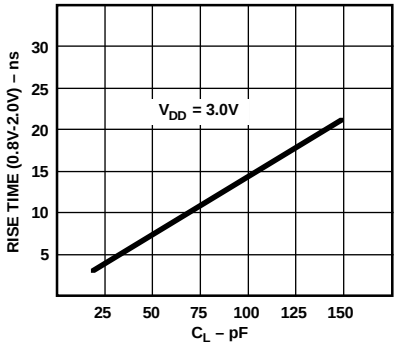


Figure 24. Typical Output Rise Time vs. Load Capacitance, C_L (at Maximum Ambient Operating Temperature)

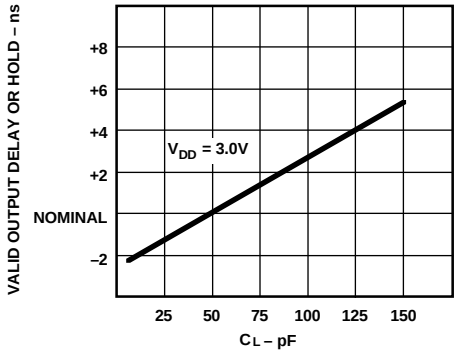


Figure 25. Typical Output Valid Delay or Hold vs. Load Capacitance, C_L (at Maximum Ambient Operating Temperature)

TIMING PARAMETERS (ADSP-2101/2105/2111/2115/2161/2163)

GENERAL NOTES

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, you cannot meaningfully add parameters to derive longer times.

TIMING NOTES

Switching characteristics specify how the processor changes its signals. You have no control over this timing—circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics tell you what the processor will do in a given circumstance. You can also use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

MEMORY REQUIREMENTS

The table below shows common memory device specifications and the corresponding ADSP-21xx timing parameters, for your convenience.

Memory Device Specification	ADSP-21xx Timing Parameter	Timing Parameter Definition
Address Setup to Write Start	t_{ASW}	A0–A13, $\overline{\text{DMS}}$, $\overline{\text{PMS}}$ Setup before $\overline{\text{WR}}$ Low
Address Setup to Write End	t_{AW}	A0–A13, $\overline{\text{DMS}}$, $\overline{\text{PMS}}$ Setup before $\overline{\text{WR}}$ Deasserted
Address Hold Time	t_{WRA}	A0–A13, $\overline{\text{DMS}}$, $\overline{\text{PMS}}$ Hold after $\overline{\text{WR}}$ Deasserted
Data Setup Time	t_{DW}	Data Setup before $\overline{\text{WR}}$ High
Data Hold Time	t_{DH}	Data Hold after $\overline{\text{WR}}$ High
$\overline{\text{OE}}$ to Data Valid	t_{RDD}	$\overline{\text{RD}}$ Low to Data Valid
Address Access Time	t_{AA}	A0–A13, $\overline{\text{DMS}}$, $\overline{\text{PMS}}$, $\overline{\text{BMS}}$ to Data Valid

TIMING PARAMETERS (ADSP-2101/2105/2111/2115/2161/2163)

CLOCK SIGNALS & RESET

Parameter		13 MHz Min	13 MHz Max	13.824 MHz Min	13.824 MHz Max	16.67 MHz Min	16.67 MHz Max	20 MHz Min	20 MHz Max	25 MHz Min	25 MHz Max	Frequency Dependency Min	Frequency Dependency Max	Unit
Timing Requirement:														
t_{CK}	CLKIN Period	76.9	150	72.3	150	60	150	50	150	40	150			ns
t_{CKL}	CLKIN Width Low	20		20		20		20		15		20		ns
t_{CKH}	CLKIN Width High	20		20		20		20		15		20		ns
t_{RSP}	$\overline{\text{RESET}}$ Width Low	384.5		361.5		300		250		200		$5t_{CK}$[1]		ns
Switching Characteristic:														
t_{CPL}	CLKOUT Width Low	28.5		26.2		20		15		10		$0.5t_{CK} - 10$		ns
t_{CPH}	CLKOUT Width High	28.5		26.2		20		15		10		$0.5t_{CK} - 10$		ns
t_{CKOH}	CLKIN High to CLKOUT High	0	20	0	20	0	20	0	20	0	15			ns

NOTES
[1]Applies after powerup sequence is complete. Internal phase lock loop requires no more than 2000 CLKIN cycles, assuming stable CLKIN (not including crystal oscillator startup time).

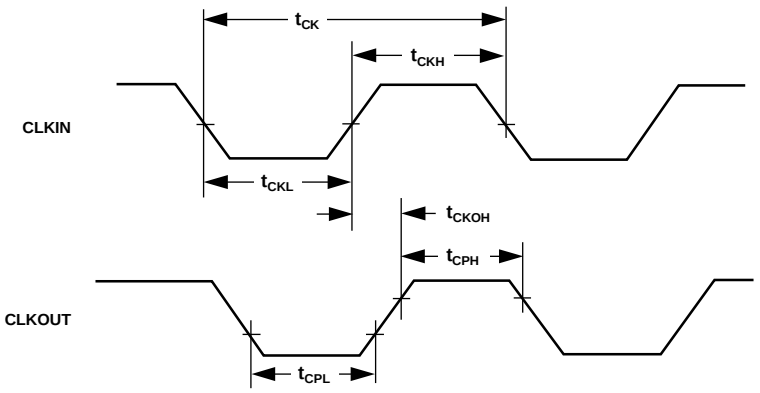
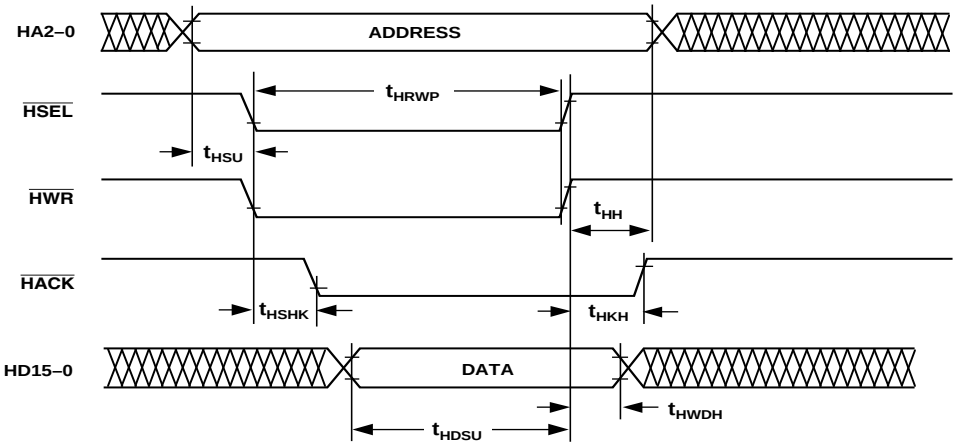


Figure 29. Clock Signals

Host Write Cycle



Host Read Cycle

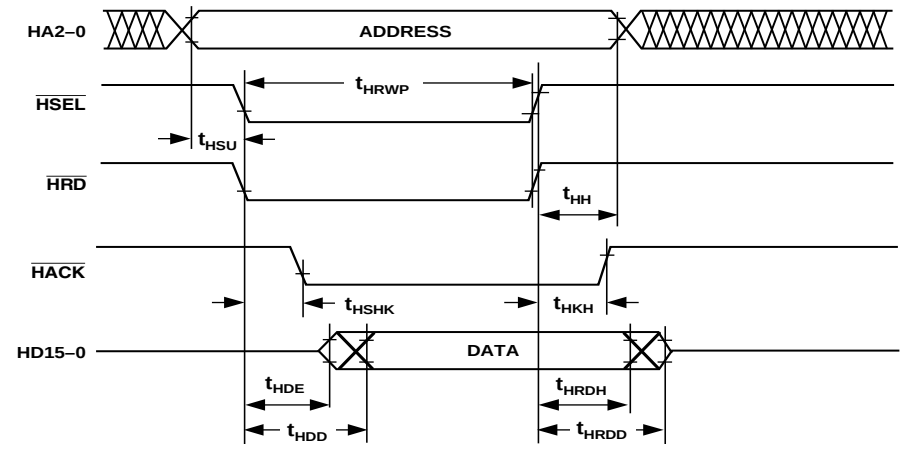


Figure 35. Host Interface Port (HMD1 = 0, HMD0 = 0)

TIMING PARAMETERS (ADSP-2111)

HOST INTERFACE PORT
Multiplexed Data & Address (HMD1 = 1)
Read Strobe & Write Strobe (HMD0 = 0)

Parameter	13.0 MHz Min	13.0 MHz Max	16.67 MHz Min	16.67 MHz Max	20 MHz Min	20 MHz Max	*No Frequency Dependency*	Unit
Timing Requirement:								
t_{HALP} ALE Pulse Width	15		15		15			ns
t_{HASU} HAD15-0 Address Setup before ALE Low	5		5		5			ns
t_{HAH} HAD15-0 Address Hold after ALE Low	2		2		2			ns
t_{HALS} Start of Write or Read after ALE Low[1, 2]	15		15		15			ns
t_{HDSU} HAD15-0 Data Setup before End of Write[3]	8		8		8			ns
t_{HWDH} HAD15-0 Data Hold after End of Write[3]	3		3		3			ns
t_{HRWP} Read or Write Pulse Width[5]	30		30		30			ns
Switching Characteristic:								
t_{HSHK} $\overline{HACK}$ Low after Start of Write or Read[1, 2]	0	20	0	20	0	20		ns
t_{HKH} $\overline{HACK}$ Hold after End of Write or Read[3, 4]	0	20	0	20	0	20		ns
t_{HDE} HAD15-0 Data Enabled after Start of Read[2]	0		0		0			ns
t_{HDD} HAD15-0 Data Valid after Start of Read[2]		23		23		23		ns
t_{HRDH} HAD15-0 Data Hold after End of Read[4]	0		0		0			ns
t_{HRDD} HAD15-0 Data Disabled after End of Read[4]		10		10		10		ns

NOTES
[1]Start of Write = $\overline{HWR}$ Low and $\overline{HSEL}$ Low.
[2]Start of Read = $\overline{HRD}$ Low and $\overline{HSEL}$ Low.
[3]End of Write = $\overline{HWR}$ High or $\overline{HSEL}$ High.
[4]End of Read = $\overline{HRD}$ High or $\overline{HSEL}$ High.
[5]Read Pulse Width = $\overline{HRD}$ Low and $\overline{HSEL}$ Low, Write Pulse Width = $\overline{HWR}$ Low and $\overline{HSEL}$ Low.

TIMING PARAMETERS (ADSP-2103/2162/2164)

GENERAL NOTES

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, you cannot meaningfully add parameters to derive longer times.

TIMING NOTES

Switching characteristics specify how the processor changes its signals. You have no control over this timing—circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics tell you what the processor will do in a given circumstance. You can also use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

MEMORY REQUIREMENTS

The table below shows common memory device specifications and the corresponding ADSP-21xx timing parameters, for your convenience.

Memory Specification	ADSP-21xx Timing Parameter	Timing Parameter Definition
Address Setup to Write Start	t_{ASW}	A0–A13, $\overline{\text{DMS}}$, $\overline{\text{PMS}}$ Setup before $\overline{\text{WR}}$ Low
Address Setup to Write End	t_{AW}	A0–A13, $\overline{\text{DMS}}$, $\overline{\text{PMS}}$ Setup before $\overline{\text{WR}}$ Deasserted
Address Hold Time	t_{WRA}	A0–A13, $\overline{\text{DMS}}$, $\overline{\text{PMS}}$ Hold after $\overline{\text{WR}}$ Deasserted
Data Setup Time	t_{DW}	Data Setup before $\overline{\text{WR}}$ High
Data Hold Time	t_{DH}	Data Hold after $\overline{\text{WR}}$ High
$\overline{\text{OE}}$ to Data Valid	t_{RDD}	$\overline{\text{RD}}$ Low to Data Valid
Address Access Time	t_{AA}	A0–A13, $\overline{\text{DMS}}$, $\overline{\text{PMS}}$, $\overline{\text{BMS}}$ to Data Valid

TIMING PARAMETERS (ADSP-2103/2162/2164)

MEMORY WRITE

Parameter		10.24 MHz Min	10.24 MHz Max	Frequency Dependency Min	Frequency Dependency Max	Unit
Switching Characteristic:						
t_{DW}	Data Setup before $\overline{WR}$ High	38.8		$0.5t_{CK} - 10 + w$		ns
t_{DH}	Data Hold after $\overline{WR}$ High	14.4		$0.25t_{CK} - 10$		ns
t_{WP}	$\overline{WR}$ Pulse Width	43.8		$0.5t_{CK} - 5 + w$		ns
t_{WDE}	$\overline{WR}$ Low to Data Enabled	0				
t_{ASW}	A0–A13, $\overline{DMS}$, $\overline{PMS}$ Setup before $\overline{WR}$ Low	12.4		$0.25t_{CK} - 12$		ns
t_{DDR}	Data Disable before $\overline{WR}$ or $\overline{RD}$ Low	14.4		$0.25t_{CK} - 10$		ns
t_{CWR}	CLKOUT High to $\overline{WR}$ Low	19.4	34.4	$0.25t_{CK} - 5$	$0.25t_{CK} + 10$	ns
t_{AW}	A0–A13, $\overline{DMS}$, $\overline{PMS}$, Setup before $\overline{WR}$ Deasserted	58.2		$0.75t_{CK} - 15 + w$		ns
t_{WRA}	A0–A13, $\overline{DMS}$, $\overline{PMS}$ Hold After $\overline{WR}$ Deasserted	14.4		$0.25t_{CK} - 10$		ns
t_{WWR}	$\overline{WR}$ High to $\overline{RD}$ or $\overline{WR}$ Low	38.8		$0.5t_{CK} - 10$		ns

w = wait states × t_{CK}.

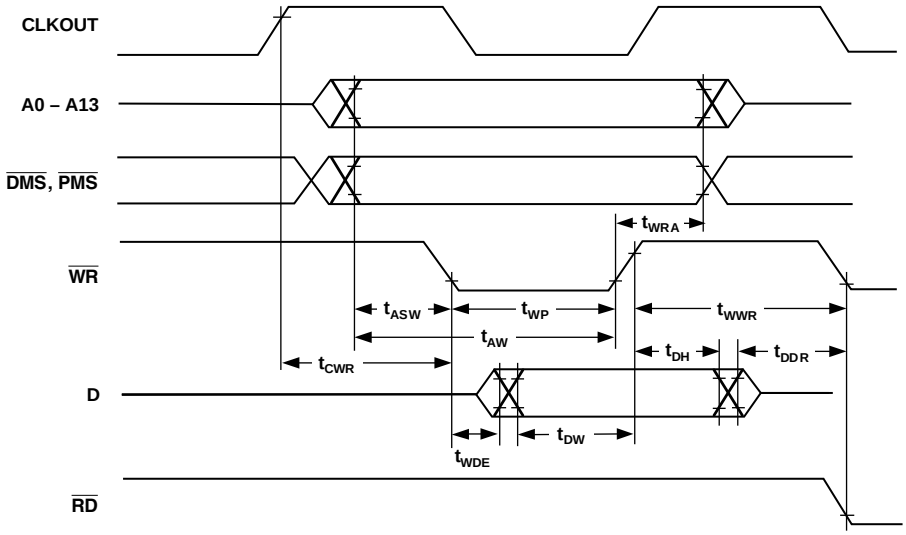


Figure 43. Memory Write

ORDERING GUIDE

Part Number[1]	Ambient Temperature Range	Instruction Rate (MHz)	Package Description	Package Option
ADSP-2101KG-66	0°C to +70°C	16.67 MHz	68-Pin PGA	G-68A
ADSP-2101BG-66	–40°C to +85°C	16.67 MHz	68-Pin PGA	G-68A
ADSP-2101KP-66	0°C to +70°C	16.67 MHz	68-Lead PLCC	P-68A
ADSP-2101BP-66	–40°C to +85°C	16.67 MHz	68-Lead PLCC	P-68A
ADSP-2101KS-66	0°C to +70°C	16.67 MHz	80-Lead PQFP	S-80
ADSP-2101BS-66	–40°C to +85°C	16.67 MHz	80-Lead PQFP	S-80
ADSP-2101KG-80	0°C to +70°C	20.0 MHz	68-Pin PGA	G-68A
ADSP-2101BG-80	–40°C to +85°C	20.0 MHz	68-Pin PGA	G-68A
ADSP-2101KP-80	0°C to +70°C	20.0 MHz	68-Lead PLCC	P-68A
ADSP-2101BP-80	–40°C to +85°C	20.0 MHz	68-Lead PLCC	P-68A
ADSP-2101KS-80	0°C to +70°C	20.0 MHz	80-Lead PQFP	S-80
ADSP-2101BS-80	–40°C to +85°C	20.0 MHz	80-Lead PQFP	S-80
ADSP-2101KP-100	0°C to +70°C	25.0 MHz	68-Pin PLCC	P-68A
ADSP-2101BP-100	–40°C to +85°C	25.0 MHz	68-Pin PLCC	P-68A
ADSP-2101KS-100	0°C to +70°C	25.0 MHz	80-Lead PQFP	S-80
ADSP-2101BS-100	–40°C to +85°C	25.0 MHz	80-Lead PQFP	S-80
ADSP-2101KG-100	0°C to +70°C	25.0 MHz	68-Lead PGA	G-68A
ADSP-2101BG-100	–40°C to +85°C	25.0 MHz	68-Lead PGA	G-68A
ADSP-2101TG-50	–55°C to +125°C	12.5 MHz	68-Pin PGA	G-68A
ADSP-2103KP-40 (3.3 V)	0°C to +70°C	10.24 MHz	68-Lead PLCC	P-68A
ADSP-2103BP-40 (3.3 V)	–40°C to +85°C	10.24 MHz	68-Lead PLCC	P-68A
ADSP-2103KS-40 (3.3 V)	0°C to +70°C	10.24 MHz	80-Lead PQFP	S-80
ADSP-2103BS-40 (3.3 V)	–40°C to +85°C	10.24 MHz	80-Lead PQFP	S-80
ADSP-2105KP-55	0°C to +70°C	13.824 MHz	68-Lead PLCC	P-68A
ADSP-2105BP-55	–40°C to +85°C	13.824 MHz	68-Lead PLCC	P-68A
ADSP-2105KP-80	0°C to +70°C	20.0 MHz	68-Lead PLCC	P-68A
ADSP-2105BP-80	–40°C to +85°C	20.0 MHz	68-Lead PLCC	P-68A
ADSP-2115KP-66	0°C to +70°C	16.67 MHz	68-Lead PLCC	P-68A
ADSP-2115BP-66	–40°C to +85°C	16.67 MHz	68-Lead PLCC	P-68A
ADSP-2115KS-66	0°C to +70°C	16.67 MHz	80-Lead PQFP	S-80
ADSP-2115BS-66	–40°C to +85°C	16.67 MHz	80-Lead PQFP	S-80
ADSP-2115KST-66	0°C to +70°C	16.67 MHz	80-Lead TQFP	ST-80
ADSP-2115BST-66	–40°C to +85°C	16.67 MHz	80-Lead TQFP	ST-80
ADSP-2115KP-80	0°C to +70°C	20.0 MHz	68-Lead PLCC	P-68A
ADSP-2115BP-80	–40°C to +85°C	20.0 MHz	68-Lead PLCC	P-68A
ADSP-2115KS-80	0°C to +70°C	20.0 MHz	80-Lead PQFP	S-80
ADSP-2115BS-80	–40°C to +85°C	20.0 MHz	80-Lead PQFP	S-80
ADSP-2115KST-80	0°C to +70°C	20.0 MHz	80-Lead TQFP	ST-80
ADSP-2115BST-80	–40°C to +85°C	20.0 MHz	80-Lead TQFP	ST-80
ADSP-2115KP-100	0°C to +70°C	25.0 MHz	68-Lead PLCC	P-68A
ADSP-2115BP-100	–40°C to +85°C	25.0 MHz	68-Lead PLCC	P-68A

NOTES
[1]K = Commercial Temperature Range (0°C to +70°C).
B = Industrial Temperature Range (–40°C to +85°C).
T = Extended Temperature Range (–55°C to +125°C).
G = Ceramic PGA (Pin Grid Array).
P = PLCC (Plastic Leaded Chip Carrier).
S = PQFP (Plastic Quad Flatpack).
ST = TQFP (Thin Quad Flatpack)

ORDERING GUIDE

Part Number[1]	Ambient Temperature Range	Instruction Rate (MHz)	Package Description	Package Option
ADSP-2111KG-52	0°C to +70°C	13.0 MHz	100-Pin PGA	G-100A
ADSP-2111BG-52	–40°C to +85°C	13.0 MHz	100-Pin PGA	G-100A
ADSP-2111KS-52	0°C to +70°C	13.0 MHz	100-Lead PQFP	S-100A
ADSP-2111BS-52	–40°C to +85°C	13.0 MHz	100-Lead PQFP	S-100A
ADSP-2111KG-66	0°C to +70°C	16.67 MHz	100-Pin PGA	G-100A
ADSP-2111BG-66	–40°C to +85°C	16.67 MHz	100-Pin PGA	G-100A
ADSP-2111KS-66	0°C to +70°C	16.67 MHz	100-Lead PQFP	S-100A
ADSP-2111BS-66	–40°C to +85°C	16.67 MHz	100-Lead PQFP	S-100A
ADSP-2111KG-80	0°C to +70°C	20.0 MHz	100-Pin PGA	G-100A
ADSP-2111BG-80	–40°C to +85°C	20.0 MHz	100-Pin PGA	G-100A
ADSP-2111KS-80	0°C to +70°C	20.0 MHz	100-Lead PQFP	S-100A
ADSP-2111BS-80	–40°C to +85°C	20.0 MHz	100-Lead PQFP	S-100A
ADSP-2111TG-52	–55°C to +125°C	13.0 MHz	100-Pin PGA	G-100A
ADSP-2161KP-66[2]	0°C to +70°C	16.67 MHz	68-Lead PLCC	P-68A
ADSP-2161BP-66[2]	–40°C to +85°C	16.67 MHz	68-Lead PLCC	P-68A
ADSP-2161KS-66[2]	0°C to +70°C	16.67 MHz	80-Lead PQFP	S-80
ADSP-2161BS-66[2]	–40°C to +85°C	16.67 MHz	80-Lead PQFP	S-80
ADSP-2162KP-40 (3.3 V)[2]	0°C to +70°C	10.24 MHz	68-Lead PLCC	P-68A
ADSP-2162BP-40 (3.3 V)[2]	–40°C to +85°C	10.24 MHz	68-Lead PLCC	P-68A
ADSP-2162KS-40 (3.3 V)[2]	0°C to +70°C	10.24 MHz	80-Lead PQFP	S-80
ADSP-2162BS-40 (3.3 V)[2]	–40°C to +85°C	10.24 MHz	80-Lead PQFP	S-80
ADSP-2163KP-66[2]	0°C to +70°C	16.67 MHz	68-Lead PLCC	P-68A
ADSP-2163BP-66[2]	–40°C to +85°C	16.67 MHz	68-Lead PLCC	P-68A
ADSP-2163KS-66[2]	0°C to +70°C	16.67 MHz	80-Lead PQFP	S-80
ADSP-2163BS-66[2]	–40°C to +85°C	16.67 MHz	80-Lead PQFP	S-80
ADSP-2163KP-100[2]	0°C to +70°C	25 MHz	68-Lead PLCC	P-68A
ADSP-2163BP-100[2]	–40°C to +85°C	25 MHz	68-Lead PLCC	P-68A
ADSP-2163KS-100[2]	0°C to +70°C	25 MHz	80-Lead PQFP	S-80
ADSP-2163BS-100[2]	–40°C to +85°C	25 MHz	80-Lead PQFP	S-80
ADSP-2164KP-40 (3.3 V)[2]	0°C to +70°C	10.24 MHz	68-Lead PLCC	P-68A
ADSP-2164BP-40 (3.3 V)[2]	–40°C to +85°C	10.24 MHz	68-Lead PLCC	P-68A
ADSP-2164KS-40 (3.3 V)[2]	0°C to +70°C	10.24 MHz	80-Lead PQFP	S-80
ADSP-2164BS-40 (3.3 V)[2]	–40°C to +85°C	10.24 MHz	80-Lead PQFP	S-80

NOTES
[1]K = Commercial Temperature Range (0°C to +70°C).
B = Industrial Temperature Range (–40°C to +85°C).
T = Extended Temperature Range (–55°C to +125°C).
G = Ceramic PGA (Pin Grid Array).
P = PLCC (Plastic Leaded Chip Carrier).
S = PQFP (Plastic Quad Flatpack).
[2]Minimum order quantities required. Contact factory for further information.

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