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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	Serial Port
Clock Rate	20MHz
Non-Volatile Memory	External
On-Chip RAM	1.5kB
Voltage - I/O	5.00V
Voltage - Core	5V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	68-LCC (J-Lead)
Supplier Device Package	68-PLCC (24.23x24.23)
Purchase URL	https://www.e-xfl.com/product-detail/rochester-electronics/adsp-2105bpz-80

Fabricated in a high speed, submicron, double-layer metal CMOS process, the highest-performance ADSP-21xx processors operate at 25 MHz with a 40 ns instruction cycle time. Every instruction can execute in a single cycle. Fabrication in CMOS results in low power dissipation.

The ADSP-2100 Family's flexible architecture and comprehensive instruction set support a high degree of parallelism. In one cycle the ADSP-21xx can perform all of the following operations:

- Generate the next program address
- Fetch the next instruction
- Perform one or two data moves
- Update one or two data address pointers
- Perform a computation
- Receive and transmit data via one or two serial ports
- Receive and/or transmit data via the host interface port (ADSP-2111 only)

The ADSP-2101, ADSP-2105, and ADSP-2115 comprise the basic set of processors of the family. Each of these three devices contains program and data memory RAM, an interval timer, and one or two serial ports. The ADSP-2103 is a 3.3 volt power supply version of the ADSP-2101; it is identical to the ADSP-2101 in all other characteristics. Table I shows the features of each ADSP-21xx processor.

The ADSP-2111 adds a 16-bit host interface port (HIP) to the basic set of ADSP-21xx integrated features. The host port provides a simple interface to host microprocessors or microcontrollers such as the 8031, 68000, or ISA bus.

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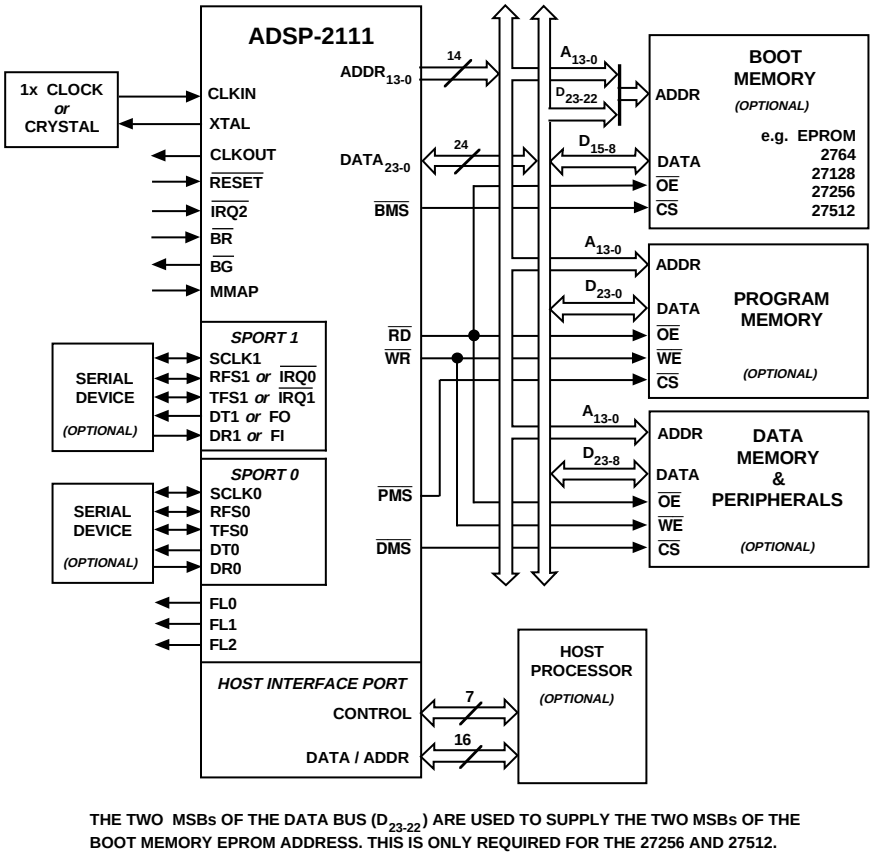


Figure 5. ADSP-2111 System

The $\overline{\text{RESET}}$ input resets all internal stack pointers to the empty stack condition, masks all interrupts, and clears the MSTAT register. When $\overline{\text{RESET}}$ is released, the boot loading sequence is performed (provided there is no pending bus request and the chip is configured for booting, with MMAP = 0). The first instruction is then fetched from internal program memory location 0x0000.

Program Memory Interface

The on-chip program memory address bus (PMA) and on-chip program memory data bus (PMD) are multiplexed with the on-chip data memory buses (DMA, DMD), creating a single external data bus and a single external address bus. The external data bus is bidirectional and is 24 bits wide to allow instruction fetches from external program memory. Program memory may contain code and data.

The external address bus is 14 bits wide. For the ADSP-2101, ADSP-2103, and ADSP-2111, these lines can directly address up to 16K words, of which 2K are on-chip. For the ADSP-2105 and ADSP-2115, the address lines can directly address up to 15K words, of which 1K is on-chip.

The data lines are bidirectional. The program memory select ($\overline{\text{PMS}}$) signal indicates accesses to program memory and can be used as a chip select signal. The write ($\overline{\text{WR}}$) signal indicates a write operation and is used as a write strobe. The read ($\overline{\text{RD}}$) signal indicates a read operation and is used as a read strobe or output enable signal.

The ADSP-21xx processors write data from their 16-bit registers to 24-bit program memory using the PX register to provide the lower eight bits. When the processor reads 16-bit data from 24-bit program memory to a 16-bit data register, the lower eight bits are placed in the PX register.

The program memory interface can generate 0 to 7 wait states for external memory devices; default is to 7 wait states after $\overline{\text{RESET}}$.

Program Memory Maps

Program memory can be mapped in two ways, depending on the state of the MMAP pin. Figure 6 shows the two program memory maps for the ADSP-2101, ADSP-2103, and ADSP-2111. Figure 8 shows the program memory maps for the ADSP-2105 and ADSP-2115. Figures 7 and 9 show the program memory maps for the ADSP-2161/62 and ADSP-2163/64, respectively.

ADSP-2101/ADSP-2103/ADSP-2111

When MMAP = 0, on-chip program memory RAM occupies 2K words beginning at address 0x0000. Off-chip program memory uses the remaining 14K words beginning at address 0x0800. In this configuration–when MMAP = 0–the boot loading sequence (described below in "Boot Memory Interface") is automatically initiated when $\overline{\text{RESET}}$ is released.

When MMAP = 1, 14K words of off-chip program memory begin at address 0x0000 and on-chip program memory RAM is located in the upper 2K words, beginning at address 0x3800. In this configuration, program memory is not booted although it can be written to and read under program control.

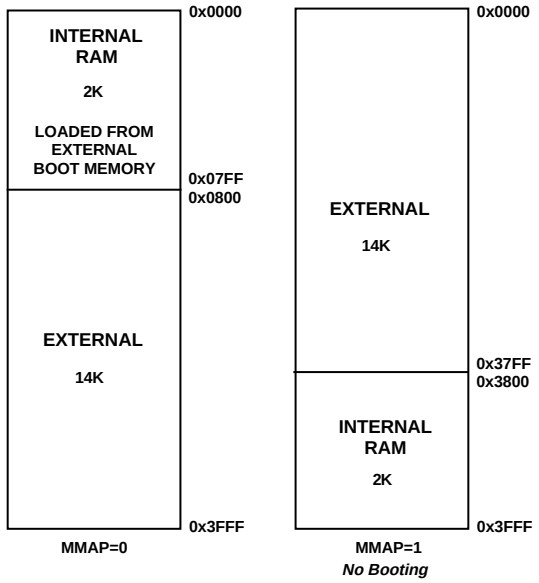


Figure 6. ADSP-2101/ADSP-2103/ADSP-2111 Program Memory Maps

ADSP-2105/ADSP-2115

When MMAP = 0, on-chip program memory RAM occupies 1K words beginning at address 0x0000. Off-chip program memory uses the remaining 14K words beginning at address 0x0800. In this configuration–when MMAP = 0–the boot loading sequence (described below in "Boot Memory Interface") is automatically initiated when $\overline{\text{RESET}}$ is released.

When MMAP = 1, 14K words of off-chip program memory begin at address 0x0000 and on-chip program memory RAM is located in the 1K words between addresses 0x3800–0x3BFF. In this configuration, program memory is not booted although it can be written to and read under program control.

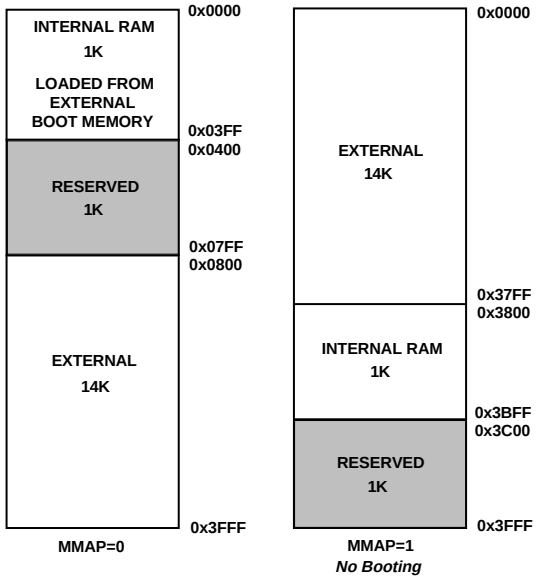


Figure 8. ADSP-2105/ADSP-2115 Program Memory Maps

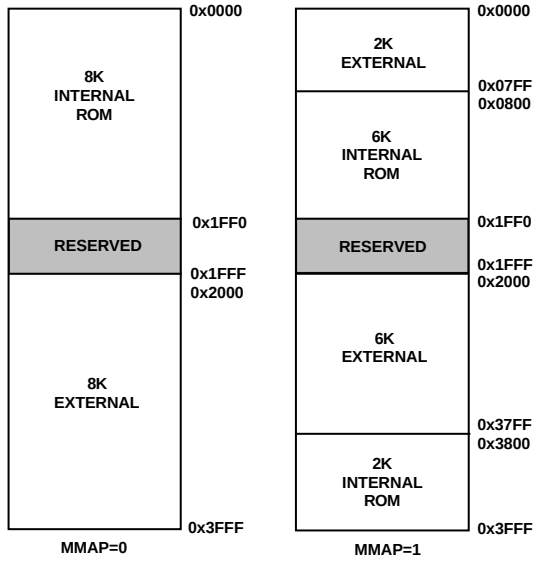


Figure 7. ADSP-2161/62 Program Memory Maps

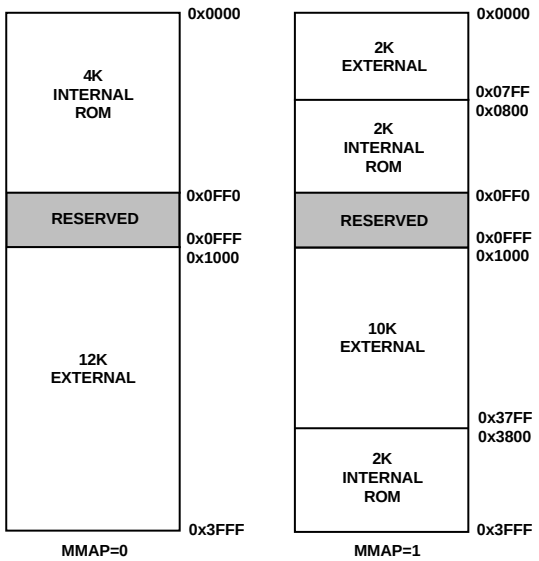


Figure 9. ADSP-2163/64 Program Memory Maps

Data Memory Interface
The data memory address bus (DMA) is 14 bits wide. The bidirectional external data bus is 24 bits wide, with the upper 16 bits used for data memory data (DMD) transfers.

The data memory select ($\overline{DMS}$) signal indicates access to data memory and can be used as a chip select signal. The write ($\overline{WR}$) signal indicates a write operation and can be used as a write strobe. The read ($\overline{RD}$) signal indicates a read operation and can be used as a read strobe or output enable signal.

The ADSP-21xx processors support memory-mapped I/O, with the peripherals memory-mapped into the data memory address space and accessed by the processor in the same manner as data memory.

Data Memory Map
ADSP-2101/ADSP-2103/ADSP-2111
For the ADSP-2101, ADSP-2103, and ADSP-2111, on-chip data memory RAM resides in the 1K words beginning at address 0x3800, as shown in Figure 10. Data memory locations from 0x3C00 to the end of data memory at 0x3FFF are reserved. Control and status registers for the system, timer, wait-state configuration, and serial port operations are located in this region of memory.

ADSP-2105/ADSP-2115
For the ADSP-2105 and ADSP-2115, on-chip data memory RAM resides in the 512 words beginning at address 0x3800, also shown in Figure 10. Data memory locations from 0x3A00 to the end of data memory at 0x3FFF are reserved. Control and status registers for the system, timer, wait-state configuration, and serial port operations are located in this region of memory.

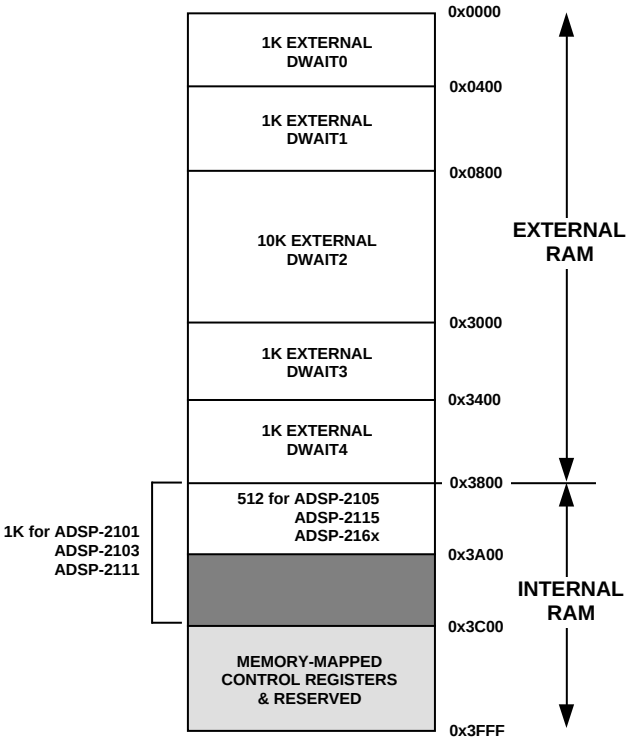


Figure 10. Data Memory Map (All Processors)

All Processors
The remaining 14K of data memory is located off-chip. This external data memory is divided into five zones, each associated with its own wait-state generator. This allows slower peripherals to be memory-mapped into data memory for which wait states are specified. By mapping peripherals into different zones, you can accommodate peripherals with different wait-state requirements. All zones default to seven wait states after $\overline{RESET}$.

Boot Memory Interface
On the ADSP-2101, ADSP-2103, and ADSP-2111, boot memory is an external 64K by 8 space, divided into eight separate 8K by 8 pages. On the ADSP-2105 and ADSP-2115, boot memory is a 32K by 8 space, divided into eight separate 4K by 8 pages. The 8-bit bytes are automatically packed into 24-bit instruction words by each processor, for loading into on-chip program memory.

Three bits in the processors' System Control Register select which page is loaded by the boot memory interface. Another bit in the System Control Register allows the forcing of a boot loading sequence under software control. Boot loading from Page 0 after $\overline{RESET}$ is initiated automatically if MMAP = 0.

The boot memory interface can generate zero to seven wait states; it defaults to three wait states after $\overline{RESET}$. This allows the ADSP-21xx to boot from a single low cost EPROM such as a 27C256. Program memory is booted one byte at a time and converted to 24-bit program memory words.

The $\overline{BMS}$ and $\overline{RD}$ signals are used to select and to strobe the boot memory interface. Only 8-bit data is read over the data bus, on pins D8-D15. To accommodate up to eight pages of boot memory, the two MSBs of the data bus are used in the boot memory interface as the two MSBs of the boot memory address: D23, D22, and A13 supply the boot page number.

The ADSP-2100 Family Assembler and Linker allow the creation of programs and data structures requiring multiple boot pages during execution.

The $\overline{BR}$ signal is recognized during the booting sequence. The bus is granted after loading the current byte is completed. $\overline{BR}$ during booting may be used to implement booting under control of a host processor.

Bus Interface
The ADSP-21xx processors can relinquish control of their data and address buses to an external device. When the external device requires control of the buses, it asserts the bus request signal ($\overline{BR}$). If the ADSP-21xx is not performing an external memory access, it responds to the active $\overline{BR}$ input in the next cycle by:

- Three-stating the data and address buses and the $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ output drivers,
- Asserting the bus grant ($\overline{BG}$) signal,
- and halting program execution.

If the Go mode is set, however, the ADSP-21xx will not halt program execution until it encounters an instruction that requires an external memory access.

RECOMMENDED OPERATING CONDITIONS

Parameter		K Grade Min	K Grade Max	B Grade Min	B Grade Max	T Grade Min	T Grade Max	Unit
V_{DD}	Supply Voltage	4.50	5.50	4.50	5.50	4.50	5.50	V
T_{AMB}	Ambient Operating Temperature	0	+70	–40	+85	–55	+125	°C

See "Environmental Conditions" for information on thermal specifications.

ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	Min	Max	Unit
V_{IH}	Hi-Level Input Voltage[3, 5]	@ V_{DD} = max	2.0		V
V_{IH}	Hi-Level CLKIN Voltage	@ V_{DD} = max	2.2		V
V_{IL}	Lo-Level Input Voltage[1, 3]	@ V_{DD} = min		0.8	V
V_{OH}	Hi-Level Output Voltage[2, 3, 7]	@ V_{DD} = min, I_{OH} = –0.5 mA	2.4		V
		@ V_{DD} = min, I_{OH} = –100 µA[8]	V_{DD} – 0.3		V
V_{OL}	Lo-Level Output Voltage[2, 3, 7]	@ V_{DD} = min, I_{OL} = 2 mA		0.4	V
I_{IH}	Hi-Level Input Current[1]	@ V_{DD} = max, V_{IN} = V_{DD} max		10	µA
I_{IL}	Lo-Level Input Current[1]	@ V_{DD} = max, V_{IN} = 0 V		10	µA
I_{OZH}	Tristate Leakage Current[4]	@ V_{DD} = max, V_{IN} = V_{DD} max[6]		10	µA
I_{OZL}	Tristate Leakage Current[4]	@ V_{DD} = max, V_{IN} = 0 V[6]		10	µA
C_I	Input Pin Capacitance[1, 8, 9]	@ V_{IN} = 2.5 V, f_{IN} = 1.0 MHz, T_{AMB} = 25°C		8	pF
C_O	Output Pin Capacitance[4, 8, 9, 10]	@ V_{IN} = 2.5 V, f_{IN} = 1.0 MHz, T_{AMB} = 25°C		8	pF

NOTES
[1]Input-only pins: CLKIN, $\overline{\text{RESET}}$, $\overline{\text{IRQ2}}$, $\overline{\text{BR}}$, MMAP, DR1, DR0 (not on ADSP-2105).
[2]Output pins: $\overline{\text{BG}}$, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, A0–A13, CLKOUT, DT1, DT0 (not on ADSP-2105).
[3]Bidirectional pins: D0–D23, SCLK1, RFS1, TFS1, SCLK0 (not on ADSP-2105), RFS0 (not on ADSP-2105), TFS0 (not on ADSP-2105).
[4]Tristatable pins: A0–A13, D0–D23, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, DT1, SCLK1, RSF1, TFS1, DT0 (not on ADSP-2105), SCLK0 (not on ADSP-2105), RFS0 (not on ADSP-2105), TFS0 (not on ADSP-2105).
[5]Input-only pins: $\overline{\text{RESET}}$, $\overline{\text{IRQ2}}$, $\overline{\text{BR}}$, MMAP, DR1, DR0 (not on ADSP-2105).
[6]0 V on $\overline{\text{BR}}$, CLKIN Active (to force tristate condition).
[7]Although specified for TTL outputs, all ADSP-21xx outputs are CMOS-compatible and will drive to V_{DD} and GND, assuming no dc loads.
[8]Guaranteed but not tested.
[9]Applies to PGA, PLCC, PQFP package types.
[10]Output pin capacitance is the capacitive load for any three-stated output pin.
Specifications subject to change without notice.

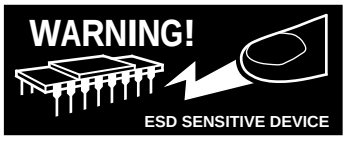
ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . –0.3 V to +7 V
Input Voltage . . . . . –0.3 V to V_{DD} + 0.3 V
Output Voltage Swing . . . . . –0.3 V to V_{DD} + 0.3 V
Operating Temperature Range (Ambient) . . . –55°C to +125°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (10 sec) PGA . . . . . +300°C
Lead Temperature (5 sec) PLCC, PQFP, TQFP . . . . +280°C

*Stresses greater than those listed above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADSP-21xx processors feature proprietary ESD protection circuitry to dissipate high energy electrostatic discharges (Human Body Model), permanent damage may occur to devices subjected to such discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Unused devices must be stored in conductive foam or shunts, and the foam should be discharged to the destination socket before the devices are removed. Per method 3015 of MIL-STD-883, the ADSP-21xx processors have been classified as Class 1 devices.



SPECIFICATIONS (ADSP-2111)

POWER DISSIPATION EXAMPLE

To determine total power dissipation in a specific application, the following equation should be applied for each output:

$$C \times V_{DD}^2 \times f$$

C = load capacitance, f = output switching frequency.

Example:

In an ADSP-2111 application where external data memory is used and no other outputs are active, power dissipation is calculated as follows:

Assumptions:

- External data memory is accessed every cycle with 50% of the address pins switching.
- External data memory writes occur every other cycle with 50% of the data pins switching.
- Each address and data pin has a 10 pF total load at the pin.
- The application operates at V_{DD} = 5.0 V and t_{CK} = 50 ns.

$$\textit{Total Power Dissipation} = P_{INT} + (C \times V_{DD}^2 \times f)$$

P_{INT} = internal power dissipation (from Figure 17).

$(C \times V_{DD}^2 \times f)$ is calculated for each output:

Output	# of Pins	× C	× V_{DD}^2	× f
Address, $\overline{DMS}$	8	× 10 pF	× 5^2 V	× 20 MHz = 40.0 mW
Data, $\overline{WR}$	9	× 10 pF	× 5^2 V	× 10 MHz = 22.5 mW
$\overline{RD}$	1	× 10 pF	× 5^2 V	× 10 MHz = 2.5 mW
CLKOUT	1	× 10 pF	× 5^2 V	× 20 MHz = 5.0 mW
				70.0 mW

Total power dissipation for this example = P_{INT} + 70.0 mW.

ENVIRONMENTAL CONDITIONS

Ambient Temperature Rating:

$T_{AMB} = T_{CASE} - (PD \times \theta_{CA})$
T_{CASE} = Case Temperature in °C
PD = Power Dissipation in W
θ_{CA} = Thermal Resistance (Case-to-Ambient)
θ_{JA} = Thermal Resistance (Junction-to-Ambient)
θ_{JC} = Thermal Resistance (Junction-to-Case)

Package	θ_{JA}	θ_{JC}	θ_{CA}
PGA	35°C/W	18°C/W	17°C/W
PQFP	42°C/W	18°C/W	23°C/W

CAPACITIVE LOADING

Figures 18 and 19 show capacitive loading characteristics for the ADSP-2111.

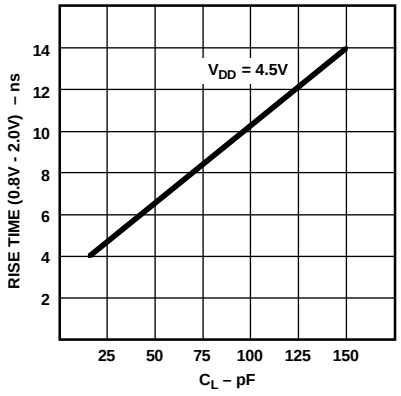


Figure 18. Typical Output Rise Time vs. Load Capacitance, C_L (at Maximum Ambient Operating Temperature)

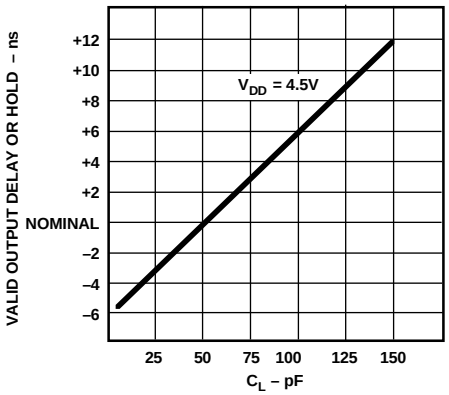


Figure 19. Typical Output Valid Delay or Hold vs. Load Capacitance, C_L (at Maximum Ambient Operating Temperature)

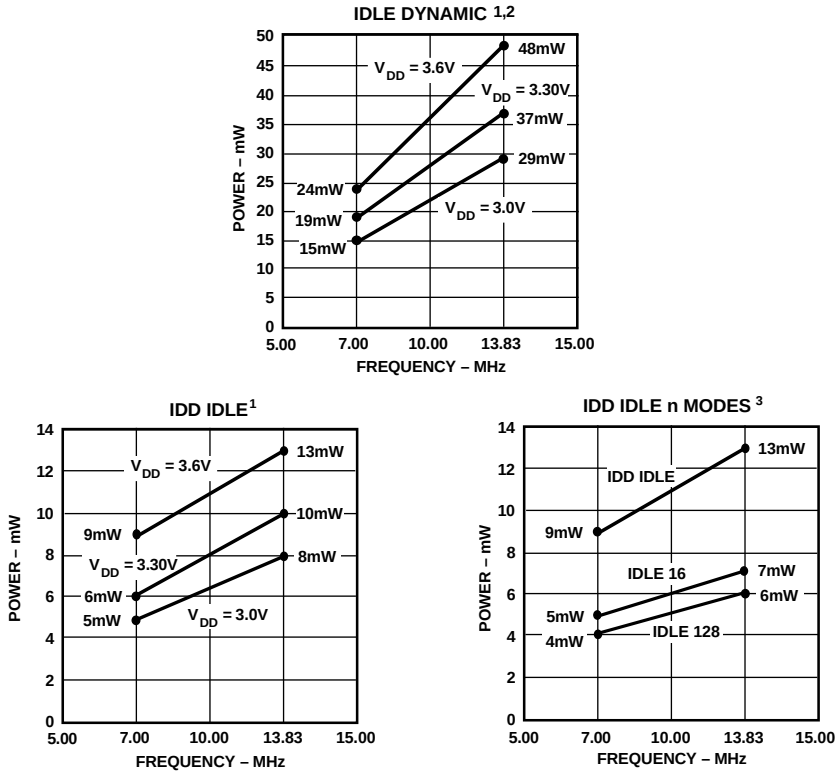
SPECIFICATIONS (ADSP-2103/2162/2164)

SUPPLY CURRENT & POWER (ADSP-2103/2162/2164)

Parameter		Test Conditions	Min	Max	Unit
I_{DD}	Supply Current (Dynamic)[1]	@ V_{DD} = max, t_{CK} = 72.3 ns[2]		14	mA
I_{DD}	Supply Current (Idle)[1, 3]	@ V_{DD} = max, t_{CK} = 72.3 ns		4	mA

NOTES
[1]Current reflects device operating with no output loads.
[2]V_{IN} = 0.4 V and 2.4 V.
[3]Idle refers to ADSP-21xx state of operation during execution of IDLE instruction. Deasserted pins are driven to either V_{DD} or GND.

For typical supply current (internal power dissipation) figures, see Figure 23.



VALID FOR ALL TEMPERATURE GRADES.
1 POWER REFLECTS DEVICE OPERATING WITH NO OUTPUT LOADS.
2 IDLE REFERS TO ADSP-21xx OPERATION DURING EXECUTION OF IDLE INSTRUCTION. DEASSERTED PINS ARE DRIVEN TO EITHER V_{DD} OR GND.
3 MAXIMUM POWER DISSIPATION AT V_{DD} = 3.6V DURING EXECUTION OF *IDLE n* INSTRUCTION.

Figure 23. ADSP-2103 Power (Typical) vs. Frequency

TIMING PARAMETERS (ADSP-2101/2105/2111/2115/2161/2163)

INTERRUPTS & FLAGS

Parameter		13 MHz Min	13 MHz Max	13.824 MHz Min	13.824 MHz Max	16.67 MHz Min	16.67 MHz Max	20 MHz Min	20 MHz Max	25 MHz Min	25 MHz Max	Frequency Dependency Min	Frequency Dependency Max	Unit
Timing Requirement:														
t_{IFS}	$\overline{IRQx}$[1] or FI Setup before CLKOUT Low[2, 3]	34.2		33.1		30		27.5		25		$0.25t_{CK}$ + 15[4]		ns
t_{IFS}	$\overline{IRQx}$[1] or FI Setup before CLKOUT Low *(ADSP-2111)*[2, 3]	37.2		36.1		33		30.5		28		$0.25t_{CK}$ + 18[4]		ns
t_{IFH}	$\overline{IRQx}$[1] or FI Hold after CLKOUT High[2, 3]	19.2		18.1		15		12.5		10		$0.25t_{CK}$		ns
Switching Characteristic:														
t_{FOH}	FO Hold after CLKOUT High[5]	0		0		0		0		0		0		ns
t_{FOD}	FO Delay from CLKOUT High		15		15		15		15		12			ns

NOTES

[1]$\overline{IRQx}$=$\overline{IRQ0}$, $\overline{IRQ1}$, and $\overline{IRQ2}$.

[2]If $\overline{IRQx}$ and FI inputs meet t_{IFS} and t_{IFH} setup/hold requirements, they will be recognized during the current clock cycle; otherwise they will be recognized during the following cycle. (Refer to the "Interrupt Controller" section in Chapter 3, Program Control, of the *ADSP-2100 Family User's Manual* for further information on interrupt servicing.)

[3]Edge-sensitive interrupts require pulse widths greater than 10 ns. Level-sensitive interrupts must be held low until serviced.

[4]t_{IFS} (min) = $0.25t_{CK}$ + 20 ns for ADSP-2101TG-50, ADSP-2101TG/883B-50, ADSP-2111TG-52, and ADSP-2111TG/883B-52 (Extended Temperature Range devices).

[5]t_{FOH} (min) = –5 ns for ADSP-2111TG-52 and ADSP-2111TG/883B-52 (Extended Temperature Range devices).

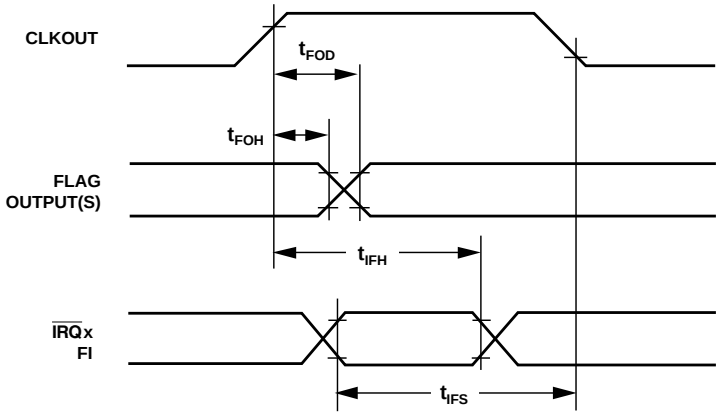


Figure 30. Interrupts & Flags

TIMING PARAMETERS (ADSP-2101/2105/2111/2115/2161/2163)

BUS REQUEST/GRANT

Parameter	13 MHz Min	13 MHz Max	13.824 MHz Min	13.824 MHz Max	16.67 MHz Min	16.67 MHz Max	20 MHz Min	20 MHz Max	25 MHz Min	25 MHz Max	Frequency Dependency Min	Frequency Dependency Max	Unit
Timing Requirement:													
t_{BH} $\overline{BR}$ Hold after CLKOUT High[1]	24.2		23.1		20		17.5		15		$0.25t_{CK}$ + 5		ns
t_{BS} $\overline{BR}$ Setup before CLKOUT Low[1]	39.2		38.1		35		32.5		30		$0.25t_{CK}$ + 20		ns
Switching Characteristic:													
t_{SD} CLKOUT High to $\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ Disable		39.2		38.1		35		32.5		30		$0.25t_{CK}$ + 20	ns
t_{SDB} $\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ Disable to $\overline{BG}$ Low	0		0		0		0		0		0		ns
t_{SE} $\overline{BG}$ High to $\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ Enable	0		0		0		0		0		0		ns
t_{SEC} $\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ Enable to CLKOUT High	9.2		8.1		5		2.5		1.5[2]		$0.25t_{CK} - 10$[2]		ns

NOTES

[1]If $\overline{BR}$ meets the t_{BS} and t_{BH} setup/hold requirements, it will be recognized in the current processor cycle; otherwise it is recognized in the following cycle. $\overline{BR}$ requires a pulse width greater than 10 ns.

[2]For 25 MHz only the minimum frequency dependency formula for $t_{SEC} = (0.25t_{CK} - 8.5)$.

Section 10.2.4, "Bus Request/Grant," on page 212 of the *ADSP-2100 Family User's Manual (1st Edition, 1993)* states that "When $\overline{BR}$ is recognized, the processor responds immediately by asserting $\overline{BG}$ during the same cycle." This is incorrect for the current versions of all ADSP-21xx processors: $\overline{BG}$ is asserted in the cycle after $\overline{BR}$ is recognized. No external synchronization circuit is needed when $\overline{BR}$ is generated as an asynchronous signal.

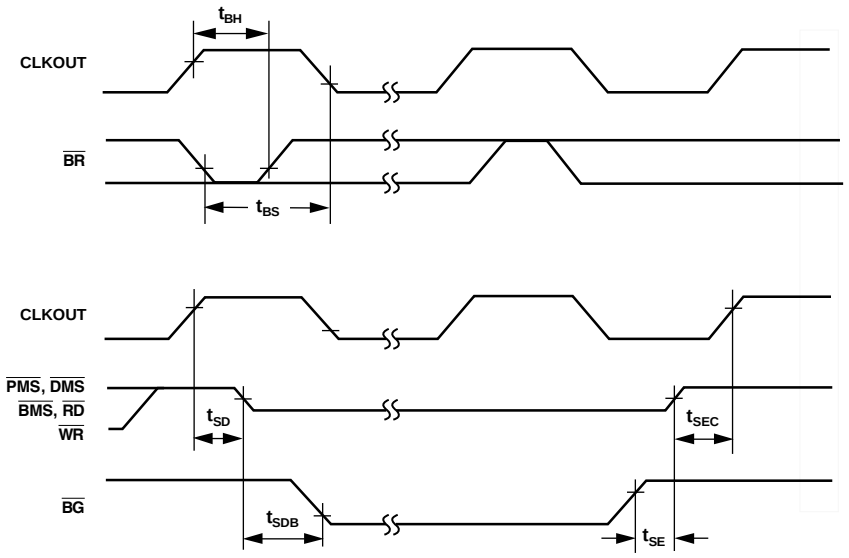


Figure 31. Bus Request/Grant

TIMING PARAMETERS (ADSP-2101/2105/2111/2115/2161/2163)

MEMORY READ

Parameter		13 MHz Min	13 MHz Max	13.824 MHz Min	13.824 MHz Max	16.67 MHz Min	16.67 MHz Max	20 MHz Min	20 MHz Max	25 MHz Min	25 MHz Max	Unit
Timing Requirement:												
t_{RDD}	$\overline{RD}$ Low to Data Valid		23.5		23.2		17		12		7	ns
t_{AA}	A0–A13, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$ to Data Valid		37.7		36.2		27		19.5		12	ns
t_{RDH}	Data Hold from $\overline{RD}$ High	0		0		0		0		0		ns
Switching Characteristic:												
t_{RP}	$\overline{RD}$ Pulse Width	33.5		28.2		22		17		12		ns
t_{CRD}	CLKOUT High to $\overline{RD}$ Low	14.2	29.2	13.1	28.1	10	25	7.5	22.5	5	20	ns
t_{ASR}	A0–A13, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$ Setup before $\overline{RD}$ Low	9.2		8.1		5		2.5		1.5[1]		ns
t_{RDA}	A0–A13, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$ Hold after $\overline{RD}$ Deasserted	10.2		9.1		6		3.5		1		ns
t_{RWR}	$\overline{RD}$ High to $\overline{RD}$ or $\overline{WR}$ Low	33.5		31.2		25		20		15		ns

Parameter		Frequency Dependency (CLKIN ≤ 25 MHz) Min	Max	Unit
Timing Requirement:				
t_{RDD}	$\overline{RD}$ Low to Data Valid		$0.5t_{CK} - 13 + w$	ns
t_{AA}	A0–A13, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$ to Data Valid		$0.75t_{CK} - 18 + w$	ns
t_{RDH}	Data Hold from $\overline{RD}$ High	0		
Switching Characteristic:				
t_{RP}	$\overline{RD}$ Pulse Width	$0.5t_{CK} - 8 + w$		ns
t_{CRD}	CLKOUT High to $\overline{RD}$ Low	$0.25t_{CK} - 5$	$0.25t_{CK} + 10$	ns
t_{ASR}	A0–A13, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$ Setup before $\overline{RD}$ Low	$0.25t_{CK} - 10$[1]		ns
t_{RDA}	A0–A13, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$ Hold after $\overline{RD}$ Deasserted	$0.25t_{CK} - 9$		ns
t_{RWR}	$\overline{RD}$ High to $\overline{RD}$ or $\overline{WR}$ Low	$0.5t_{CK} - 5$		ns

NOTES
[1]For 25 MHz only minimum frequency dependency formula for $t_{ASR} = (0.25t_{CK} - 8.5)$.
w = wait states × t_{CK}.

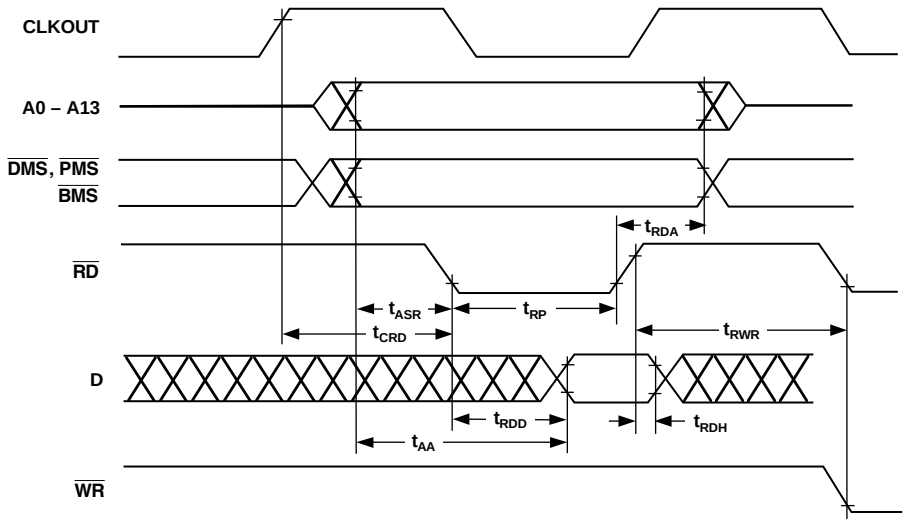


Figure 32. Memory Read

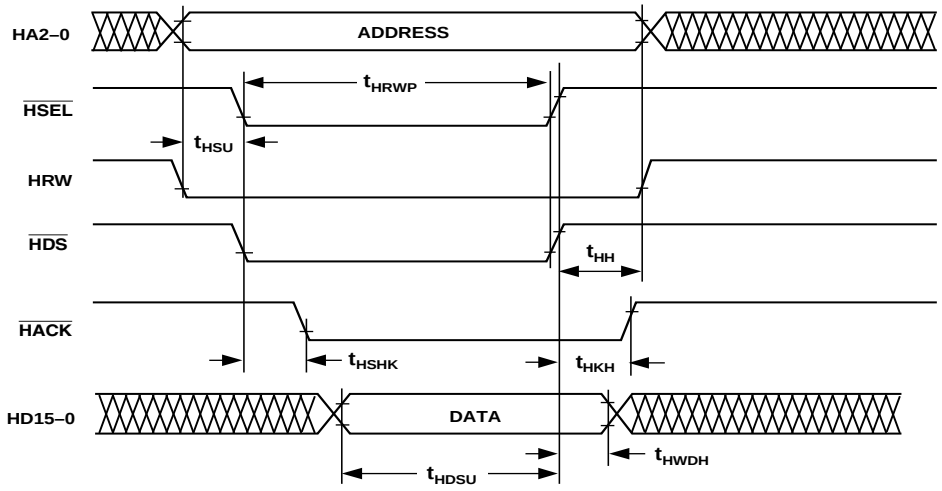
TIMING PARAMETERS (ADSP-2111)

HOST INTERFACE PORT
Separate Data & Address (HMD1 = 0)
Read/Write Strobe & Data Strobe (HMD0 = 1)

Parameter	13.0 MHz Min	13.0 MHz Max	16.67 MHz Min	16.67 MHz Max	20 MHz Min	20 MHz Max	*No Frequency Dependency*	Unit
Timing Requirement:								
t_{HSU} HA2-0, HRW Setup before Start of Write or Read[1]	8		8		8			ns
t_{HDSU} Data Setup before End of Write[2]	8		8		8			ns
t_{HWDH} Data Hold after End of Write[2]	3		3		3			ns
t_{HH} HA2-0, HRW Hold after End of Write or Read[2]	3		3		3			ns
t_{HRWP} Read or Write Pulse Width[3]	30		30		30			ns
Switching Characteristic:								
t_{HSHK} $\overline{\text{HACK}}$ Low after Start of Write or Read[1]	0	20	0	20	0	20		ns
t_{HKH} $\overline{\text{HACK}}$ Hold after End of Write or Read[2]	0	20	0	20	0	20		ns
t_{HDE} Data Enabled after Start of Read[1]	0		0		0			ns
t_{HDD} Data Valid after Start of Read[1]		23		23		23		ns
t_{HRDH} Data Hold after End of Read[2]	0		0		0			ns
t_{HRDD} Data Disabled after End of Read[2]		10		10		10		ns

NOTES
[1]Start of Write or Read = $\overline{\text{HDS}}$ Low and $\overline{\text{HSEL}}$ Low.
[2]End of Write or Read = $\overline{\text{HDS}}$ High or $\overline{\text{HSEL}}$ High.
[3]Read or Write Pulse Width = $\overline{\text{HDS}}$ Low and $\overline{\text{HSEL}}$ Low.

Host Write Cycle



Host Read Cycle

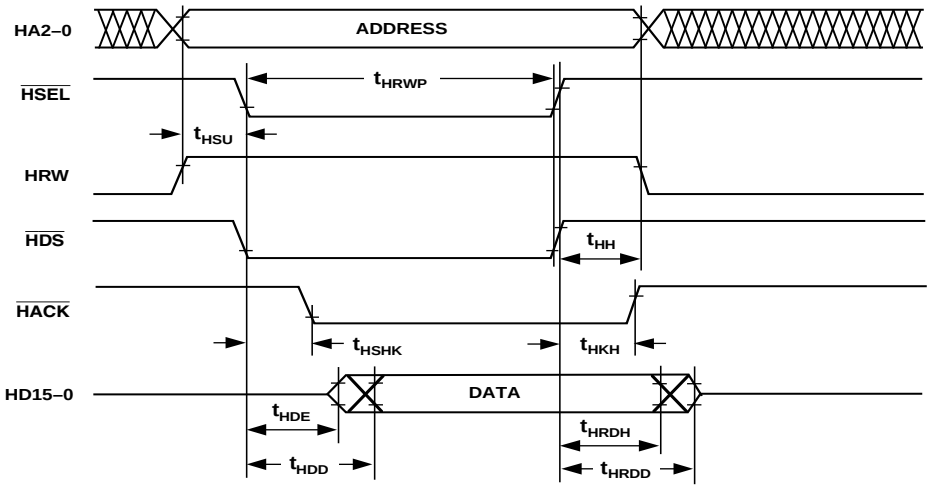


Figure 36. Host Interface Port (HMD1 = 0, HMD0 =1)

TIMING PARAMETERS (ADSP-2111)

HOST INTERFACE PORT
Multiplexed Data & Address (HMD1 = 1)
Read Strobe & Write Strobe (HMD0 = 0)

Parameter	13.0 MHz Min	13.0 MHz Max	16.67 MHz Min	16.67 MHz Max	20 MHz Min	20 MHz Max	*No Frequency Dependency*	Unit
Timing Requirement:								
t_{HALP} ALE Pulse Width	15		15		15			ns
t_{HASU} HAD15-0 Address Setup before ALE Low	5		5		5			ns
t_{HAH} HAD15-0 Address Hold after ALE Low	2		2		2			ns
t_{HALS} Start of Write or Read after ALE Low[1, 2]	15		15		15			ns
t_{HDSU} HAD15-0 Data Setup before End of Write[3]	8		8		8			ns
t_{HWDH} HAD15-0 Data Hold after End of Write[3]	3		3		3			ns
t_{HRWP} Read or Write Pulse Width[5]	30		30		30			ns
Switching Characteristic:								
t_{HSHK} $\overline{HACK}$ Low after Start of Write or Read[1, 2]	0	20	0	20	0	20		ns
t_{HKH} $\overline{HACK}$ Hold after End of Write or Read[3, 4]	0	20	0	20	0	20		ns
t_{HDE} HAD15-0 Data Enabled after Start of Read[2]	0		0		0			ns
t_{HDD} HAD15-0 Data Valid after Start of Read[2]		23		23		23		ns
t_{HRDH} HAD15-0 Data Hold after End of Read[4]	0		0		0			ns
t_{HRDD} HAD15-0 Data Disabled after End of Read[4]		10		10		10		ns

NOTES
[1]Start of Write = $\overline{HWR}$ Low and $\overline{HSEL}$ Low.
[2]Start of Read = $\overline{HRD}$ Low and $\overline{HSEL}$ Low.
[3]End of Write = $\overline{HWR}$ High or $\overline{HSEL}$ High.
[4]End of Read = $\overline{HRD}$ High or $\overline{HSEL}$ High.
[5]Read Pulse Width = $\overline{HRD}$ Low and $\overline{HSEL}$ Low, Write Pulse Width = $\overline{HWR}$ Low and $\overline{HSEL}$ Low.

TIMING PARAMETERS (ADSP-2111)

HOST INTERFACE PORT
Multiplexed Data & Address (HMD1 = 1)
Read/Write Strobe & Data Strobe (HMD0 = 1)

Parameter	13.0 MHz Min	13.0 MHz Max	16.67 MHz Min	16.67 MHz Max	20 MHz Min	20 MHz Max	*No Frequency Dependency*	Unit
Timing Requirement:								
t_{HALP} ALE Pulse Width	15		15		15			ns
t_{HASU} HAD15-0 Address Setup before ALE Low	5		5		5			ns
t_{HAH} HAD15-0 Address Hold after ALE Low	2		2		2			ns
t_{HALS} Start of Write or Read after ALE Low[1]	15		15		15			ns
t_{HSU} HRW Setup before Start of Write or Read[1]	8		8		8			ns
t_{HDSU} HAD15-0 Data Setup before End of Write[2]	5		5		5			ns
t_{HWDH} HAD15-0 Data Hold after End of Write[2]	3		3		3			ns
t_{HH} HRW Hold after End of Write or Read[2]	3		3		3			ns
t_{HRWP} Read or Write Pulse Width[3]	30		30		30			ns
Switching Characteristic:								
t_{HSHK} $\overline{\text{HACK}}$ Low after Start of Write or Read[1]	0	20	0	20	0	20		ns
t_{HKH} $\overline{\text{HACK}}$ Hold after End of Write or Read[2]	0	20	0	20	0	20		ns
t_{HDE} HAD15-0 Data Enabled after Start of Read[1]	0		0		0			ns
t_{HDD} HAD15-0 Data Valid after Start of Read[1]		23		23		23		ns
t_{HRDH} HAD15-0 Data Hold after End of Read[2]	0		0		0			ns
t_{HRDD} HAD15-0 Data Disabled after End of Read[2]		10		10		10		ns

NOTES
[1]Start of Write or Read = $\overline{\text{HDS}}$ Low and $\overline{\text{HSEL}}$ Low.
[2]End of Write or Read = $\overline{\text{HDS}}$ High or $\overline{\text{HSEL}}$ High.
[3]Read or Write Pulse Width = $\overline{\text{HDS}}$ Low and $\overline{\text{HSEL}}$ Low.

Host Write Cycle

Host Read Cycle

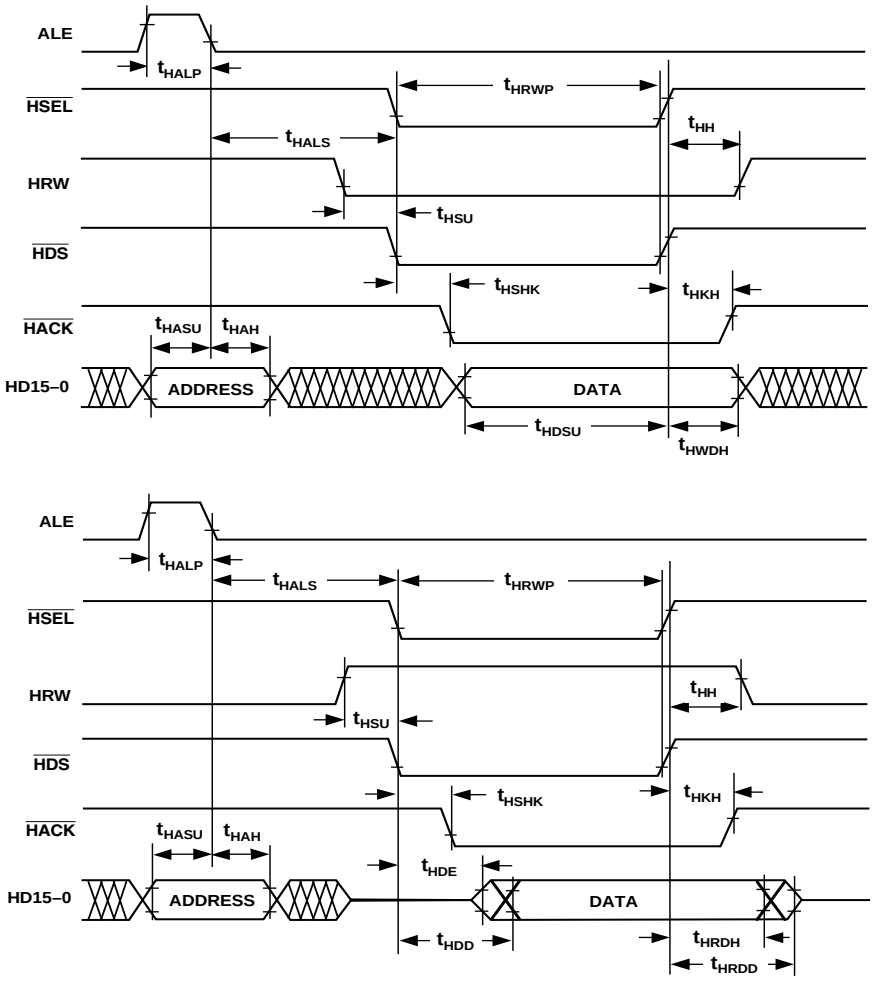


Figure 38. Host Interface Port (HMD1 = 1, HMD0 = 1)

TIMING PARAMETERS (ADSP-2103/2162/2164)

BUS REQUEST/GRANT

Parameter		10.24 MHz Min	10.24 MHz Max	Frequency Dependency Min	Frequency Dependency Max	Unit
Timing Requirement:						
t_{BH}	$\overline{BR}$ Hold after CLKOUT High[1]	29.4		$0.25t_{CK}$ + 5		ns
t_{BS}	$\overline{BR}$ Setup before CLKOUT Low[1]	44.4		$0.25t_{CK}$ + 20		ns
Switching Characteristic:						
t_{SD}	CLKOUT High to $\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ Disable		44.4		$0.25t_{CK}$ + 20	ns
t_{SDB}	$\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ Disable to $\overline{BG}$ Low	0				ns
t_{SE}	$\overline{BG}$ High to $\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ Enable	0				ns
t_{SEC}	$\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ Enable to CLKOUT High	14.4		$0.25t_{CK}$ – 10		ns

NOTES

[1]If $\overline{BR}$ meets the t_{BS} and t_{BH} setup/hold requirements, it will be recognized in the current processor cycle; otherwise it is recognized in the following cycle. $\overline{BR}$ requires a pulse width greater than 10 ns.

Section 10.2.4, "Bus Request/Grant," of the *ADSP-2100 Family User's Manual (1st Edition, ©1993)* states that "When $\overline{BR}$ is recognized, the processor responds immediately by asserting $\overline{BG}$ during the same cycle." This is incorrect for the current versions of all ADSP-21xx processors: $\overline{BG}$ is asserted in the cycle after $\overline{BR}$ is recognized. No external synchronization circuit is needed when $\overline{BR}$ is generated as an asynchronous signal.

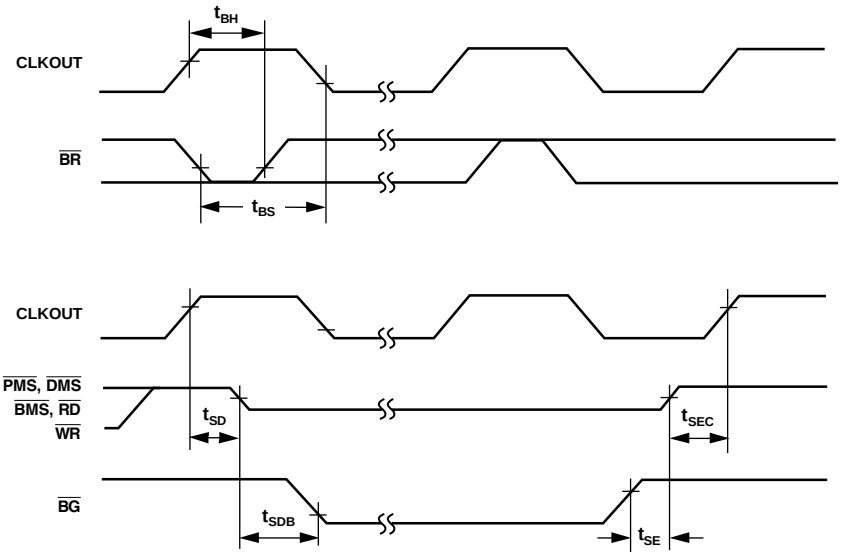


Figure 41. Bus Request/Grant

TIMING PARAMETERS (ADSP-2103/2162/2164)

MEMORY READ

Parameter		10.24 MHz Min	10.24 MHz Max	Frequency Dependency Min	Frequency Dependency Max	Unit
Timing Requirement:						
t_{RDD}	$\overline{RD}$ Low to Data Valid		33.8		$0.5t_{CK} - 15 + w$	ns
t_{AA}	A0–A13, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$ to Data Valid		49.2		$0.75t_{CK} - 24 + w$	ns
t_{RDH}	Data Hold from $\overline{RD}$ High	0				ns
Switching Characteristic:						
t_{RP}	$\overline{RD}$ Pulse Width	43.8		$0.5t_{CK} - 5 + w$		ns
t_{CRD}	CLKOUT High to $\overline{RD}$ Low	19.4	34.4	$0.25t_{CK} - 5$	$0.25t_{CK} + 10$	ns
t_{ASR}	A0–A13, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$ Setup before $\overline{RD}$ Low	12.4		$0.25t_{CK} - 12$		ns
t_{RDA}	A0–A13, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$ Hold after $\overline{RD}$ Deasserted	14.4		$0.25t_{CK} - 10$		ns
t_{RWR}	$\overline{RD}$ High to $\overline{RD}$ or $\overline{WR}$ Low	38.8		$0.5t_{CK} - 10$		ns

w = wait states × t_{CK}.

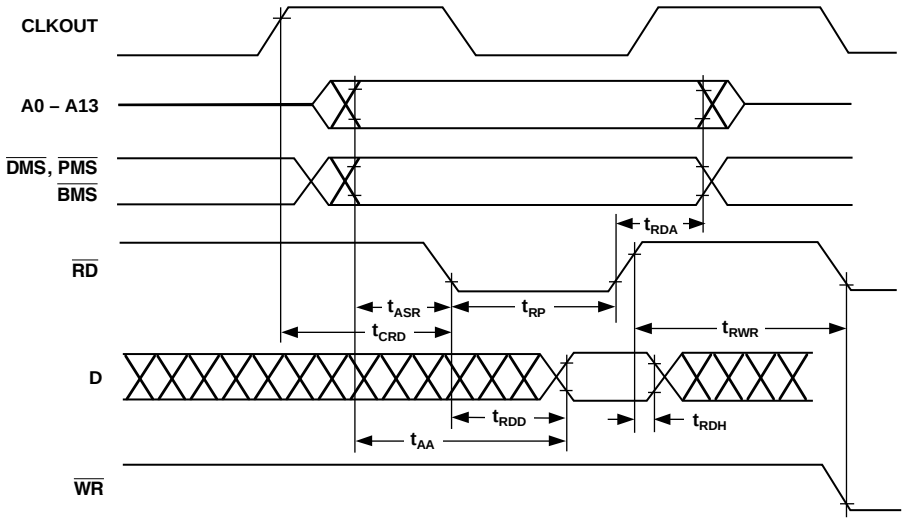
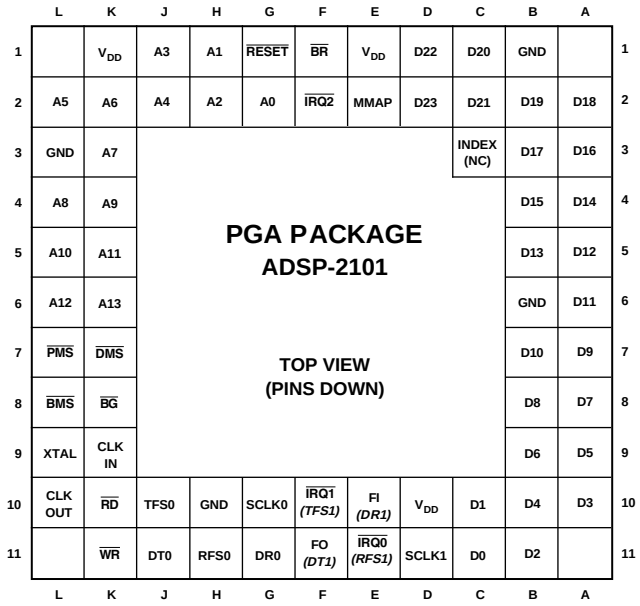
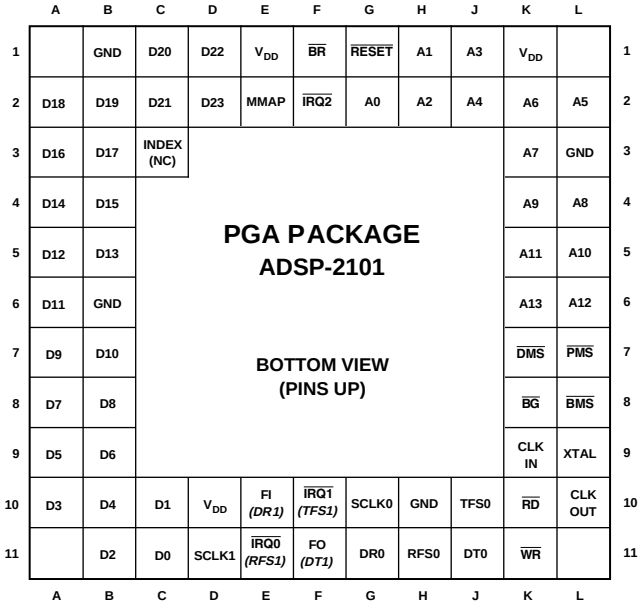


Figure 42. Memory Read

PIN CONFIGURATIONS

68-Pin PGA





NC = NO CONNECT

PGA Number	Pin Name
K11	$\overline{WR}$
K10	$\overline{RD}$
J11	DT0
J10	TFS0
H11	RFS0
H10	GND
G11	DR0
G10	SCLK0
F11	FO *(DT1)*
F10	$\overline{IRQ1}$ *(TFS1)*
E11	$\overline{IRQ0}$ *(RFS1)*
E10	FI *(DR1)*
D11	SCLK1
D10	V_{DD}
C11	D0
C10	D1
B11	D2

PGA Number	Pin Name
A10	D3
B10	D4
A9	D5
B9	D6
A8	D7
B8	D8
A7	D9
B7	D10
A6	D11
B6	GND
A5	D12
B5	D13
A4	D14
B4	D15
A3	D16
B3	D17
A2	D18

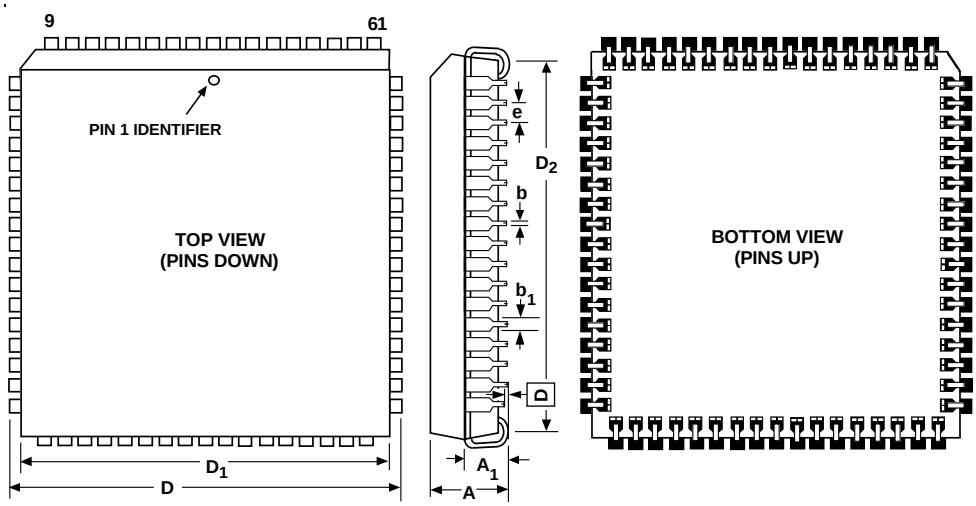
PGA Number	Pin Name
B1	GND
B2	D19
C1	D20
C2	D21
D1	D22
D2	D23
E1	V_{DD}
E2	MMAP
F1	$\overline{BR}$
F2	$\overline{IRQ2}$
G1	$\overline{RESET}$
G2	A0
H1	A1
H2	A2
J1	A3
J2	A4
K1	V_{DD}

PGA Number	Pin Name
L2	A5
K2	A6
L3	GND
K3	A7
L4	A8
K4	A9
L5	A10
K5	A11
L6	A12
K6	A13
L7	$\overline{PMS}$
K7	$\overline{DMS}$
L8	$\overline{BMS}$
K8	$\overline{BG}$
L9	XTAL
K9	CLKIN
L10	CLKOUT
C3	Index (NC)

OUTLINE DIMENSIONS

ADSP-21xx

68-Lead Plastic Leaded Chip Carrier (PLCC)



SYMBOL	INCHES			MILLIMETERS		
	MIN	TYP	MAX	MIN	TYP	MAX
A	0.169	0.172	0.175	4.29	4.37	4.45
A_1		0.104			2.64	
b	0.017	0.018	0.019	0.43	0.46	0.48
b_1	0.027	0.028	0.029	0.69	0.71	0.74
D	0.985	0.990	0.995	25.02	25.15	25.27
D_1	0.950	0.952	0.954	24.13	24.18	24.23
D_2	0.895	0.910	0.925	22.73	23.11	23.50
e		0.050			1.27	
D			0.004			0.10

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C1891b–10–2/96