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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	-
Interface	-
Clock Rate	-
Non-Volatile Memory	-
On-Chip RAM	-
Voltage - I/O	-
Voltage - Core	-
Operating Temperature	-
Mounting Type	-
Package / Case	-
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-2111bg-80

Fabricated in a high speed, submicron, double-layer metal CMOS process, the highest-performance ADSP-21xx processors operate at 25 MHz with a 40 ns instruction cycle time. Every instruction can execute in a single cycle. Fabrication in CMOS results in low power dissipation.

The ADSP-2100 Family's flexible architecture and comprehensive instruction set support a high degree of parallelism. In one cycle the ADSP-21xx can perform all of the following operations:

- Generate the next program address
- Fetch the next instruction
- Perform one or two data moves
- Update one or two data address pointers
- Perform a computation
- Receive and transmit data via one or two serial ports
- Receive and/or transmit data via the host interface port (ADSP-2111 only)

The ADSP-2101, ADSP-2105, and ADSP-2115 comprise the basic set of processors of the family. Each of these three devices contains program and data memory RAM, an interval timer, and one or two serial ports. The ADSP-2103 is a 3.3 volt power supply version of the ADSP-2101; it is identical to the ADSP-2101 in all other characteristics. Table I shows the features of each ADSP-21xx processor.

The ADSP-2111 adds a 16-bit host interface port (HIP) to the basic set of ADSP-21xx integrated features. The host port provides a simple interface to host microprocessors or microcontrollers such as the 8031, 68000, or ISA bus.

TABLE OF CONTENTS

The interrupt force and clear register, IFC, is a write-only register that contains a force bit and a clear bit for each interrupt (except for level-sensitive interrupts and the ADSP-2111 HIP interrupts—these cannot be forced or cleared in software).

When responding to an interrupt, the ASTAT, MSTAT, and IMASK status registers are pushed onto the status stack and the PC counter is loaded with the appropriate vector address. The status stack is seven levels deep (nine levels deep on the ADSP-2111) to allow interrupt nesting. The stack is automatically popped when a return from the interrupt instruction is executed.

Pin Definitions

Table IV (on next page) shows pin definitions for the ADSP-21xx processors. Any inputs not used must be tied to V_{DD}.

Table III. Interrupt Vector Addresses & Priority

ADSP-2105 Interrupt Source	**Interrupt Vector Address**
$\overline{\text{RESET}}$ Startup	0x0000
$\overline{\text{IRQ2}}$	0x0004 *(High Priority)*
SPORT1 Transmit *or* $\overline{\text{IRQ1}}$	0x0010
SPORT1 Receive *or* $\overline{\text{IRQ0}}$	0x0014
Timer	0x0018 *(Low Priority)*

ADSP-2101/2103/2115/216x Interrupt Source	**Interrupt Vector Address**
$\overline{\text{RESET}}$ Startup	0x0000
$\overline{\text{IRQ2}}$	0x0004 *(High Priority)*
SPORT0 Transmit	0x0008
SPORT0 Receive	0x000C
SPORT1 Transmit *or* $\overline{\text{IRQ1}}$	0x0010
SPORT1 Receive *or* $\overline{\text{IRQ0}}$	0x0014
Timer	0x0018 *(Low Priority)*

ADSP-2111 Interrupt Source	**Interrupt Vector Address**
$\overline{\text{RESET}}$ Startup	0x0000
$\overline{\text{IRQ2}}$	0x0004 *(High Priority)*
HIP Write from Host	0x0008
HIP Read to Host	0x000C
SPORT0 Transmit	0x0010
SPORT0 Receive	0x0014
SPORT1 Transmit *or* $\overline{\text{IRQ1}}$	0x0018
SPORT1 Receive *or* $\overline{\text{IRQ0}}$	0x001C
Timer	0x0020 *(Low Priority)*

SYSTEM INTERFACE

Figure 3 shows a typical system for the ADSP-2101, ADSP-2115, or ADSP-2103, with two serial I/O devices, a boot EPROM, and optional external program and data memory. A total of 15K words of data memory and 16K words of program memory is addressable for the ADSP-2101 and ADSP-2103. A total of 14.5K words of data memory and 15K words of program memory is addressable for the ADSP-2115.

Figure 4 shows a system diagram for the ADSP-2105, with one serial I/O device, a boot EPROM, and optional external program and data memory. A total of 14.5K words of data memory and 15K words of program memory is addressable for the ADSP-2105.

Figure 5 shows a system diagram for the ADSP-2111, with two serial I/O devices, a host processor, a boot EPROM, and optional external program and data memory. A total of 15K words of data memory and 16K words of program memory is addressable.

Programmable wait-state generation allows the processors to easily interface to slow external memories.

The ADSP-2101, ADSP-2103, ADSP-2115, and ADSP-2111 processors also provide either: one external interrupt ($\overline{\text{IRQ2}}$) and two serial ports (SPORT0, SPORT1), *or* three external interrupts ($\overline{\text{IRQ2}}$, $\overline{\text{IRQ1}}$, $\overline{\text{IRQ0}}$) and one serial port (SPORT0).

The ADSP-2105 provides either: one external interrupt ($\overline{\text{IRQ2}}$) and one serial port (SPORT1), *or* three external interrupts ($\overline{\text{IRQ2}}$, $\overline{\text{IRQ1}}$, $\overline{\text{IRQ0}}$) with no serial port.

Clock Signals

The ADSP-21xx processors' CLKIN input may be driven by a crystal or by a TTL-compatible external clock signal. The CLKIN input may not be halted or changed in frequency during operation, nor operated below the specified low frequency limit.

If an external clock is used, it should be a TTL-compatible signal running at the instruction rate. The signal should be connected to the processor's CLKIN input; in this case, the XTAL input must be left unconnected.

Because the ADSP-21xx processors include an on-chip oscillator circuit, an external crystal may also be used. The crystal should be connected across the CLKIN and XTAL pins, with two capacitors connected as shown in Figure 2. A parallel-resonant, fundamental frequency, microprocessor-grade crystal should be used.

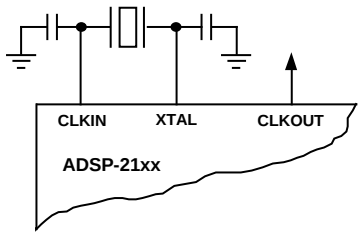
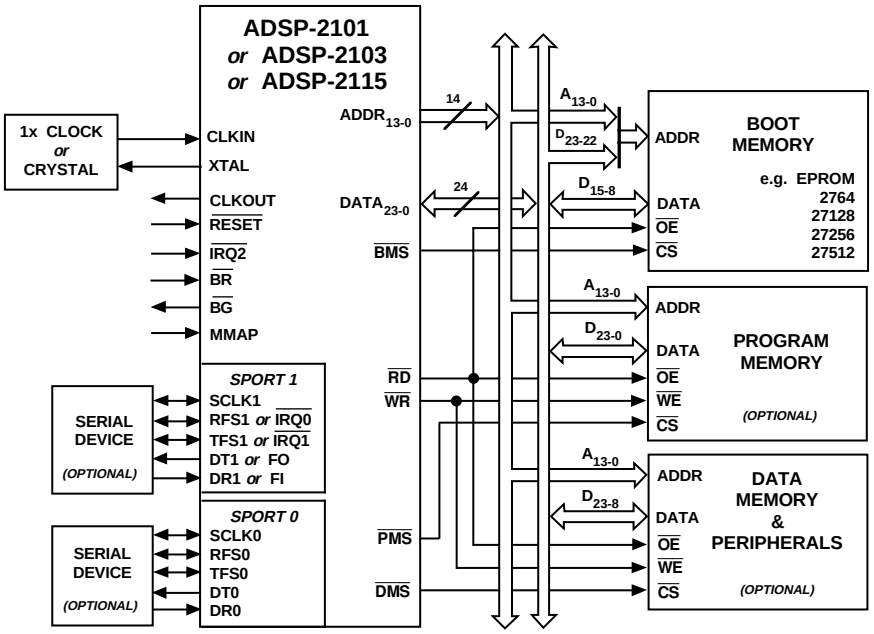
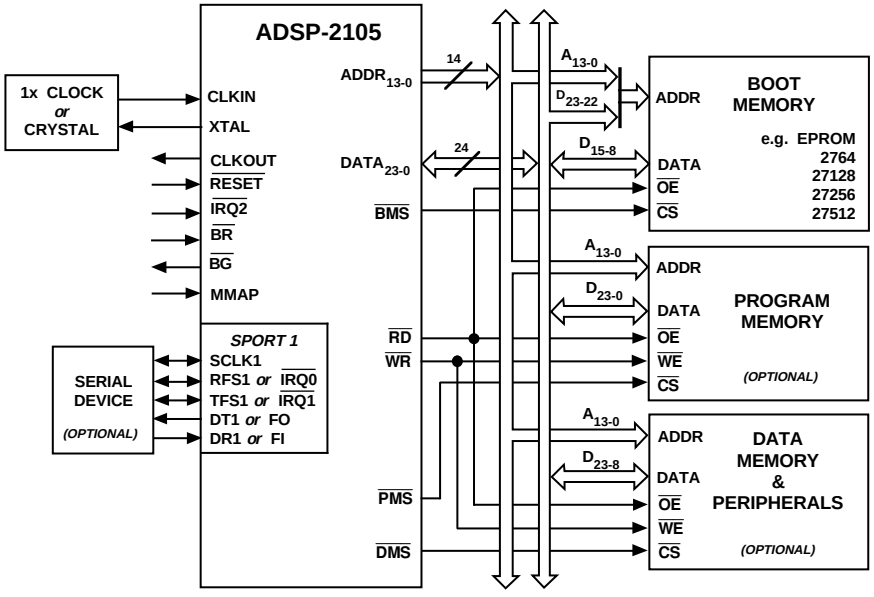


Figure 2. External Crystal Connections



THE TWO MSBs OF THE DATA BUS (D_{23-22}) ARE USED TO SUPPLY THE TWO MSBs OF THE BOOT MEMORY EPROM ADDRESS. THIS IS ONLY REQUIRED FOR THE 27256 AND 27512.

Figure 3. ADSP-2101/ADSP-2103/ADSP-2115 System



THE TWO MSBs OF THE DATA BUS (D_{23-22}) ARE USED TO SUPPLY THE TWO MSBs OF THE BOOT MEMORY EPROM ADDRESS. THIS IS ONLY REQUIRED FOR THE 27256 AND 27512.

Figure 4. ADSP-2105 System

Data Memory Interface
The data memory address bus (DMA) is 14 bits wide. The bidirectional external data bus is 24 bits wide, with the upper 16 bits used for data memory data (DMD) transfers.

The data memory select ($\overline{DMS}$) signal indicates access to data memory and can be used as a chip select signal. The write ($\overline{WR}$) signal indicates a write operation and can be used as a write strobe. The read ($\overline{RD}$) signal indicates a read operation and can be used as a read strobe or output enable signal.

The ADSP-21xx processors support memory-mapped I/O, with the peripherals memory-mapped into the data memory address space and accessed by the processor in the same manner as data memory.

Data Memory Map
ADSP-2101/ADSP-2103/ADSP-2111
For the ADSP-2101, ADSP-2103, and ADSP-2111, on-chip data memory RAM resides in the 1K words beginning at address 0x3800, as shown in Figure 10. Data memory locations from 0x3C00 to the end of data memory at 0x3FFF are reserved. Control and status registers for the system, timer, wait-state configuration, and serial port operations are located in this region of memory.

ADSP-2105/ADSP-2115
For the ADSP-2105 and ADSP-2115, on-chip data memory RAM resides in the 512 words beginning at address 0x3800, also shown in Figure 10. Data memory locations from 0x3A00 to the end of data memory at 0x3FFF are reserved. Control and status registers for the system, timer, wait-state configuration, and serial port operations are located in this region of memory.

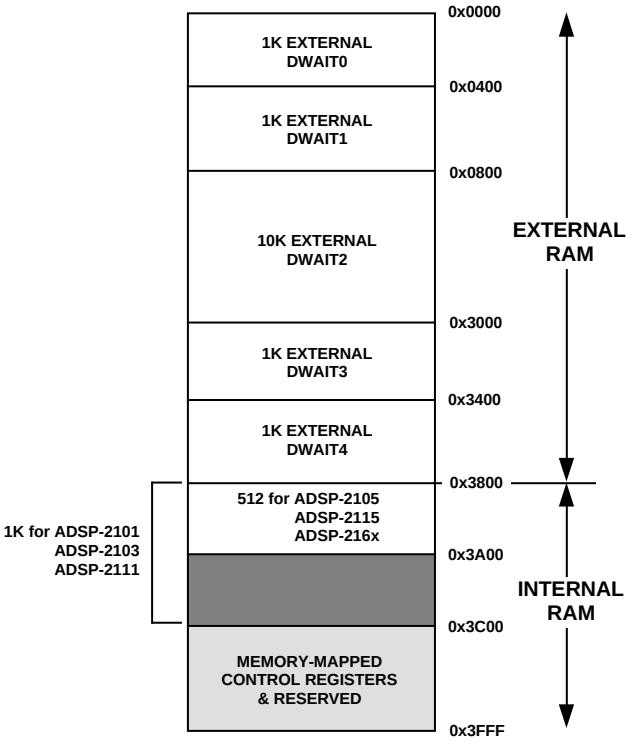


Figure 10. Data Memory Map (All Processors)

All Processors
The remaining 14K of data memory is located off-chip. This external data memory is divided into five zones, each associated with its own wait-state generator. This allows slower peripherals to be memory-mapped into data memory for which wait states are specified. By mapping peripherals into different zones, you can accommodate peripherals with different wait-state requirements. All zones default to seven wait states after $\overline{RESET}$.

Boot Memory Interface
On the ADSP-2101, ADSP-2103, and ADSP-2111, boot memory is an external 64K by 8 space, divided into eight separate 8K by 8 pages. On the ADSP-2105 and ADSP-2115, boot memory is a 32K by 8 space, divided into eight separate 4K by 8 pages. The 8-bit bytes are automatically packed into 24-bit instruction words by each processor, for loading into on-chip program memory.

Three bits in the processors' System Control Register select which page is loaded by the boot memory interface. Another bit in the System Control Register allows the forcing of a boot loading sequence under software control. Boot loading from Page 0 after $\overline{RESET}$ is initiated automatically if MMAP = 0.

The boot memory interface can generate zero to seven wait states; it defaults to three wait states after $\overline{RESET}$. This allows the ADSP-21xx to boot from a single low cost EPROM such as a 27C256. Program memory is booted one byte at a time and converted to 24-bit program memory words.

The $\overline{BMS}$ and $\overline{RD}$ signals are used to select and to strobe the boot memory interface. Only 8-bit data is read over the data bus, on pins D8-D15. To accommodate up to eight pages of boot memory, the two MSBs of the data bus are used in the boot memory interface as the two MSBs of the boot memory address: D23, D22, and A13 supply the boot page number.

The ADSP-2100 Family Assembler and Linker allow the creation of programs and data structures requiring multiple boot pages during execution.

The $\overline{BR}$ signal is recognized during the booting sequence. The bus is granted after loading the current byte is completed. $\overline{BR}$ during booting may be used to implement booting under control of a host processor.

Bus Interface
The ADSP-21xx processors can relinquish control of their data and address buses to an external device. When the external device requires control of the buses, it asserts the bus request signal ($\overline{BR}$). If the ADSP-21xx is not performing an external memory access, it responds to the active $\overline{BR}$ input in the next cycle by:

- Three-stating the data and address buses and the $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ output drivers,
- Asserting the bus grant ($\overline{BG}$) signal,
- and halting program execution.

If the Go mode is set, however, the ADSP-21xx will not halt program execution until it encounters an instruction that requires an external memory access.

If the ADSP-21xx is performing an external memory access when the external device asserts the $\overline{BR}$ signal, it will not three-state the memory interfaces or assert the $\overline{BG}$ signal until the cycle after the access completes (up to eight cycles later depending on the number of wait states). The instruction does not need to be completed when the bus is granted; the ADSP-21xx will grant the bus in between two memory accesses if an instruction requires more than one external memory access.

When the $\overline{BR}$ signal is released, the processor releases the $\overline{BG}$ signal, re-enables the output drivers and continues program execution from the point where it stopped.

The bus request feature operates at all times, including when the processor is booting and when $\overline{RESET}$ is active. If this feature is not used, the $\overline{BR}$ input should be tied high (to V_{DD}).

Low Power IDLE Instruction

The IDLE instruction places the ADSP-21xx processor in low power state in which it waits for an interrupt. When an interrupt occurs, it is serviced and execution continues with instruction following IDLE. Typically this next instruction will be a JUMP back to the IDLE instruction. This implements a low-power standby loop.

The *IDLE n* instruction is a special version of IDLE that slows the processor's internal clock signal to further reduce power consumption. The reduced clock frequency, a programmable fraction of the normal clock rate, is specified by a selectable divisor, *n*, given in the IDLE instruction. The syntax of the instruction is:

IDLE n;

where *n* = 16, 32, 64, or 128.

The instruction leaves the chip in an idle state, operating at the slower rate. While it is in this state, the processor's other internal clock signals, such as SCLK, CLKOUT, and the timer clock, are reduced by the same ratio. Upon receipt of an enabled interrupt, the processor will stay in the IDLE state for up to a maximum of *n* CLKIN cycles, where *n* is the divisor specified in the instruction, before resuming normal operation.

When the *IDLE n* instruction is used, it slows the processor's internal clock and thus its response time to incoming interrupts–the 1-cycle response time of the standard IDLE state is increased by *n*, the clock divisor. When an enabled interrupt is received, the ADSP-21xx will remain in the IDLE state for up to a maximum of *n* CLKIN cycles (where *n* = 16, 32, 64, or 128) before resuming normal operation.

When the *IDLE n* instruction is used in systems that have an externally generated serial clock (SCLK), the serial clock rate may be faster than the processor's reduced internal clock rate. Under these conditions, interrupts must not be generated at a faster rate than can be serviced, due to the additional time the processor takes to come out of the IDLE state (a maximum of *n* CLKIN cycles).

ADSP-216x Prototyping

You can prototype your ADSP-216x system with either the ADSP-2101 or ADSP-2103 RAM-based processors. When code is fully developed and debugged, it can be submitted to Analog Devices for conversion into a ADSP-216x ROM product.

The ADSP-2101 EZ-ICE emulator can be used for development of ADSP-216x systems. For the 3.3 V ADSP-2162 and ADSP-2164, a voltage converter interface board provides 3.3 V emulation.

Additional overlay memory is used for emulation of ADSP-2161/62 systems. It should be noted that due to the use of off-chip overlay memory to emulate the ADSP-2161/62, a performance loss may be experienced when both executing instructions and fetching program memory data from the off-chip overlay memory in the same cycle. This can be overcome by locating program memory data in on-chip memory.

Ordering Procedure for ADSP-216x ROM Processors

To place an order for a custom ROM-coded ADSP-2161, ADSP-2162, ADSP-2163, or ADSP-2164 processor, you must:

1. Complete the following forms contained in the *ADSP ROM Ordering Package*, available from your Analog Devices sales representative:

   ADSP-216x ROM Specification Form

   ROM Release Agreement

   ROM NRE Agreement & Minimum Quantity Order (MQO) Acceptance Agreement for Pre-Production ROM Products

2. Return the forms to Analog Devices along with two copies of the Memory Image File (.EXE file) of your ROM code. The files must be supplied on two 3.5" or 5.25" floppy disks for the IBM PC (DOS 2.01 or higher).

3. Place a purchase order with Analog Devices for non-recurring engineering changes (NRE) associated with ROM product development.

After this information is received, it is entered into Analog Devices' ROM Manager System which assigns a custom ROM model number to the product. This model number will be branded on all prototype and production units manufactured to these specifications.

To minimize the risk of code being altered during this process, Analog Devices verifies that the .EXE files on both floppy disks are identical, and recalculates the checksums for the .EXE file entered into the ROM Manager System. The checksum data, in the form of a ROM Memory Map, a hard copy of the .EXE file, and a ROM Data Verification form are returned to you for inspection.

SPECIFICATIONS (ADSP-2101/2105/2115/2161/2163)

POWER DISSIPATION EXAMPLE

To determine total power dissipation in a specific application, the following equation should be applied for each output:

$$C \times V_{DD}^2 \times f$$

C = load capacitance, f = output switching frequency.

Example:
In an ADSP-2101 application where external data memory is used and no other outputs are active, power dissipation is calculated as follows:

Assumptions:

- External data memory is accessed every cycle with 50% of the address pins switching.
- External data memory writes occur every other cycle with 50% of the data pins switching.
- Each address and data pin has a 10 pF total load at the pin.
- The application operates at V_{DD} = 5.0 V and t_{CK} = 50 ns.

$$\textit{Total Power Dissipation} = P_{INT} + (C \times V_{DD}^2 \times f)$$

P_{INT} = internal power dissipation (from Figure 11).

$(C \times V_{DD}^2 \times f)$ is calculated for each output:

Output	# of Pins	× C	× V_{DD}^2	× f
Address, $\overline{DMS}$	8	× 10 pF	× 5^2 V	× 20 MHz = 40.0 mW
Data, $\overline{WR}$	9	× 10 pF	× 5^2 V	× 10 MHz = 22.5 mW
$\overline{RD}$	1	× 10 pF	× 5^2 V	× 10 MHz = 2.5 mW
CLKOUT	1	× 10 pF	× 5^2 V	× 20 MHz = 5.0 mW
				70.0 mW

Total power dissipation for this example = P_{INT} + 70.0 mW.

ENVIRONMENTAL CONDITIONS

Ambient Temperature Rating:

$T_{AMB} = T_{CASE} - (PD \times \theta_{CA})$
T_{CASE} = Case Temperature in °C
PD = Power Dissipation in W
θ_{CA} = Thermal Resistance (Case-to-Ambient)
θ_{JA} = Thermal Resistance (Junction-to-Ambient)
θ_{JC} = Thermal Resistance (Junction-to-Case)

Package	θ_{JA}	θ_{JC}	θ_{CA}
PGA	18°C/W	9°C/W	9°C/W
PLCC	27°C/W	16°C/W	11°C/W
PQFP	60°C/W	18°C/W	42°C/W
TQFP	60°C/W	18°C/W	42°C/W

CAPACITIVE LOADING

Figures 12 and 13 show capacitive loading characteristics for the ADSP-2101, ADSP-2105, ADSP-2115, and ADSP-2161/2163.

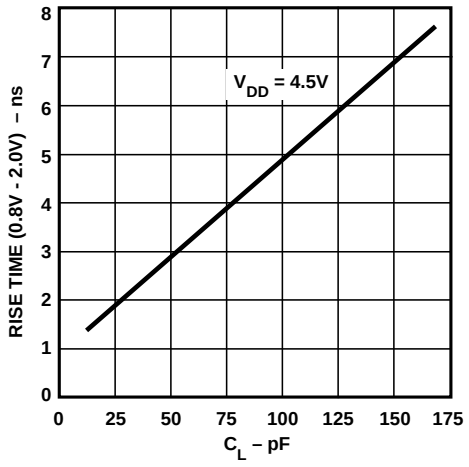


Figure 12. Typical Output Rise Time vs. Load Capacitance, C_L (at Maximum Ambient Operating Temperature)

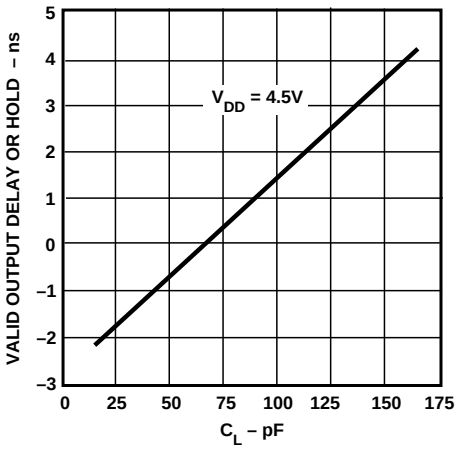


Figure 13. Typical Output Valid Delay or Hold vs. Load Capacitance, C_L (at Maximum Ambient Operating Temperature)

SPECIFICATIONS (ADSP-2101/2105/2115/2161/2163)

TEST CONDITIONS

Figure 14 shows voltage reference levels for ac measurements.

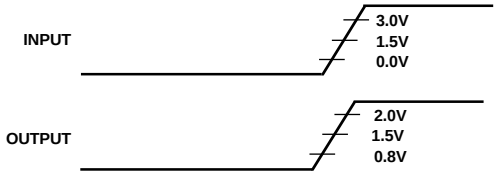


Figure 14. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Disable Time

Output pins are considered to be disabled when they have stopped driving and started a transition from the measured output high or low voltage to a high impedance state. The output disable time (t_{DIS}) is the difference of $t_{MEASURED}$ and t_{DECAY}, as shown in Figure 15. The time $t_{MEASURED}$ is the interval from when a reference signal reaches a high or low voltage level to when the output voltages have changed by 0.5 V from the measured output high or low voltage.

The decay time, t_{DECAY}, is dependent on the capacitative load, C_L, and the current load, i_L, on the output pin. It can be approximated by the following equation:

$$t_{DECAY} = \frac{C_L \times 0.5\,V}{i_L}$$

from which

$$t_{DIS} = t_{MEASURED} - t_{DECAY}$$

is calculated. If multiple pins (such as the data bus) are disabled, the measurement value is that of the last pin to stop driving.

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high-impedance state to when they start driving. The output enable time (t_{ENA}) is the interval from when a reference signal reaches a high or low voltage level to when the output has reached a specified high or low trip point, as shown in Figure 15. If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

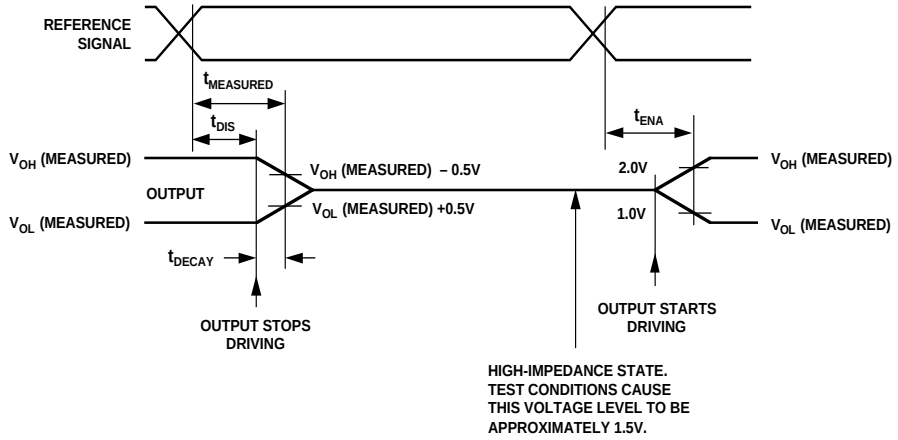


Figure 15. Output Enable/Disable

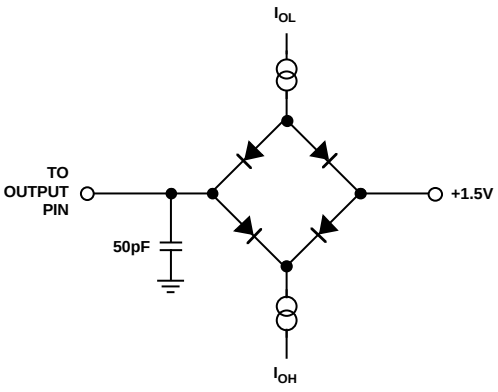


Figure 16. Equivalent Device Loading for AC Measurements (Except Output Enable/Disable)

SPECIFICATIONS (ADSP-2111)

SUPPLY CURRENT & POWER (ADSP-2111)

Parameter		Test Conditions	Min	Max	Unit
I_{DD}	Supply Current (Dynamic)[1]	@ V_{DD} = max, t_{CK} = 50 ns[2]		60	mA
		@ V_{DD} = max, t_{CK} = 60 ns[2]		52	mA
		@ V_{DD} = max, t_{CK} = 76.9 ns[2]		46	mA
I_{DD}	Supply Current (Idle)[1, 3]	@ V_{DD} = max, t_{CK} = 50 ns		18	mA
		@ V_{DD} = max, t_{CK} = 60 ns		16	mA
		@ V_{DD} = max, t_{CK} = 76.9 ns		14	mA

NOTES
[1]Current reflects device operating with no output loads.
[2]V_{IN} = 0.4 V and 2.4 V.
[3]Idle refers to ADSP-21xx state of operation during execution of IDLE instruction. Deasserted pins are driven to either V_{DD} or GND.

For typical supply current (internal power dissipation) figures, see Figure 17.

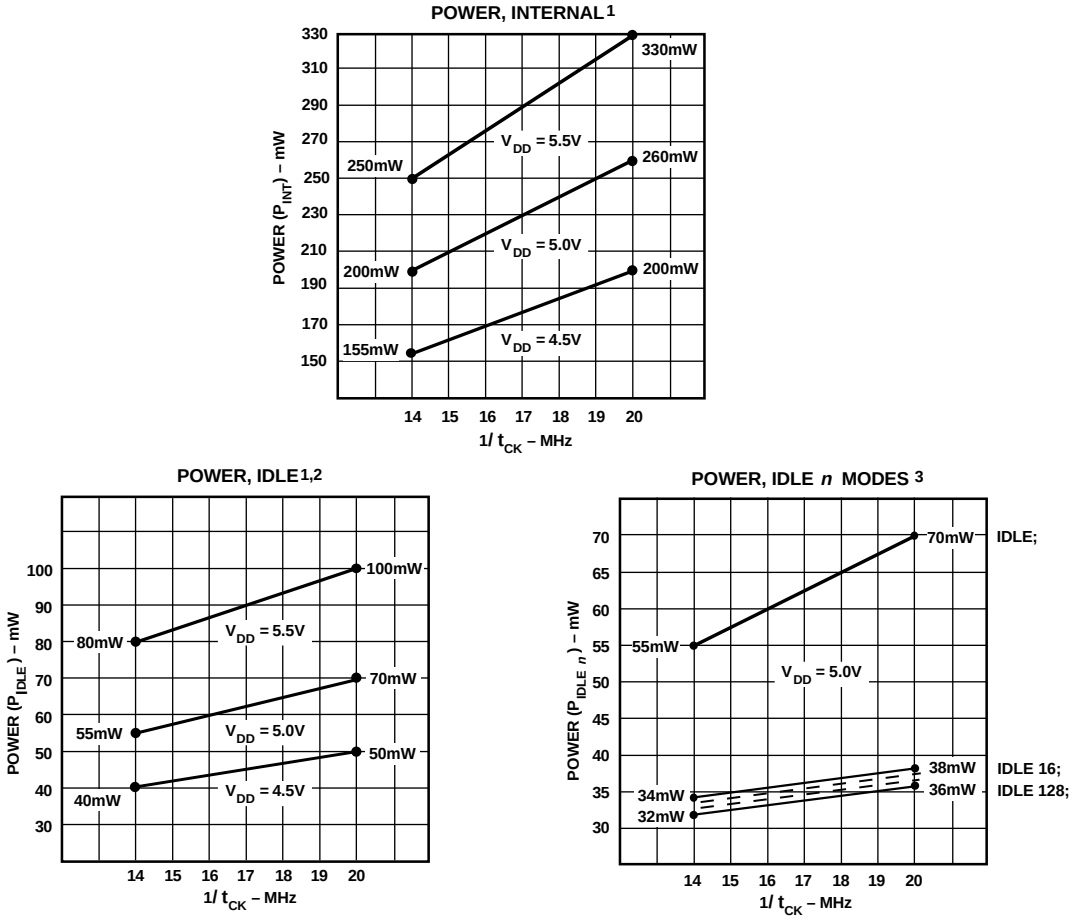


Figure 17. ADSP-2111 Power (Typical) vs. Frequency

SPECIFICATIONS (ADSP-2111)

POWER DISSIPATION EXAMPLE

To determine total power dissipation in a specific application, the following equation should be applied for each output:

$$C \times V_{DD}^2 \times f$$

C = load capacitance, f = output switching frequency.

Example:

In an ADSP-2111 application where external data memory is used and no other outputs are active, power dissipation is calculated as follows:

Assumptions:

- External data memory is accessed every cycle with 50% of the address pins switching.
- External data memory writes occur every other cycle with 50% of the data pins switching.
- Each address and data pin has a 10 pF total load at the pin.
- The application operates at V_{DD} = 5.0 V and t_{CK} = 50 ns.

$$\textit{Total Power Dissipation} = P_{INT} + (C \times V_{DD}^2 \times f)$$

P_{INT} = internal power dissipation (from Figure 17).

$(C \times V_{DD}^2 \times f)$ is calculated for each output:

Output	# of Pins	× C	× V_{DD}^2	× f
Address, $\overline{DMS}$	8	× 10 pF	× 5^2 V	× 20 MHz = 40.0 mW
Data, $\overline{WR}$	9	× 10 pF	× 5^2 V	× 10 MHz = 22.5 mW
$\overline{RD}$	1	× 10 pF	× 5^2 V	× 10 MHz = 2.5 mW
CLKOUT	1	× 10 pF	× 5^2 V	× 20 MHz = 5.0 mW
				70.0 mW

Total power dissipation for this example = P_{INT} + 70.0 mW.

ENVIRONMENTAL CONDITIONS

Ambient Temperature Rating:

$T_{AMB} = T_{CASE} - (PD \times \theta_{CA})$
T_{CASE} = Case Temperature in °C
PD = Power Dissipation in W
θ_{CA} = Thermal Resistance (Case-to-Ambient)
θ_{JA} = Thermal Resistance (Junction-to-Ambient)
θ_{JC} = Thermal Resistance (Junction-to-Case)

Package	θ_{JA}	θ_{JC}	θ_{CA}
PGA	35°C/W	18°C/W	17°C/W
PQFP	42°C/W	18°C/W	23°C/W

CAPACITIVE LOADING

Figures 18 and 19 show capacitive loading characteristics for the ADSP-2111.

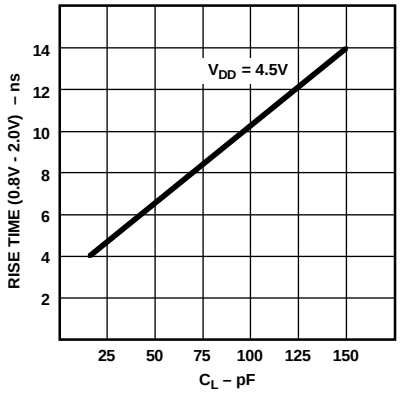


Figure 18. Typical Output Rise Time vs. Load Capacitance, C_L (at Maximum Ambient Operating Temperature)

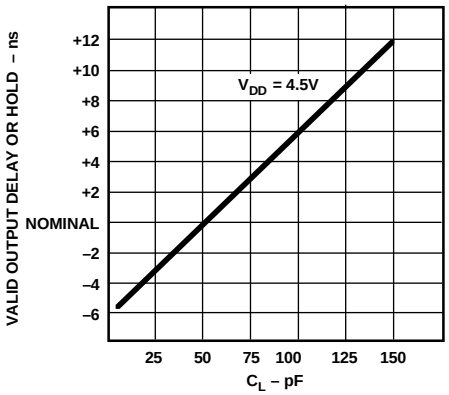


Figure 19. Typical Output Valid Delay or Hold vs. Load Capacitance, C_L (at Maximum Ambient Operating Temperature)

SPECIFICATIONS (ADSP-2111)

TEST CONDITIONS

Figure 20 shows voltage reference levels for ac measurements.

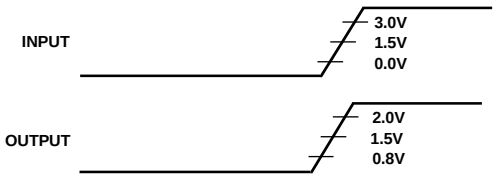


Figure 20. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Disable Time

Output pins are considered to be disabled when they have stopped driving and started a transition from the measured output high or low voltage to a high impedance state. The output disable time (t_{DIS}) is the difference of $t_{MEASURED}$ and t_{DECAY}, as shown in Figure 21. The time $t_{MEASURED}$ is the interval from when a reference signal reaches a high or low voltage level to when the output voltages have changed by 0.5 V from the measured output high or low voltage.

The decay time, t_{DECAY}, is dependent on the capacitative load, C_L, and the current load, i_L, on the output pin. It can be approximated by the following equation:

$$t_{DECAY} = \frac{C_L \times 0.5\,V}{i_L}$$

from which

$$t_{DIS} = t_{MEASURED} - t_{DECAY}$$

is calculated. If multiple pins (such as the data bus) are disabled, the measurement value is that of the last pin to stop driving.

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high-impedance state to when they start driving. The output enable time (t_{ENA}) is the interval from when a reference signal reaches a high or low voltage level to when the output has reached a specified high or low trip point, as shown in Figure 21. If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

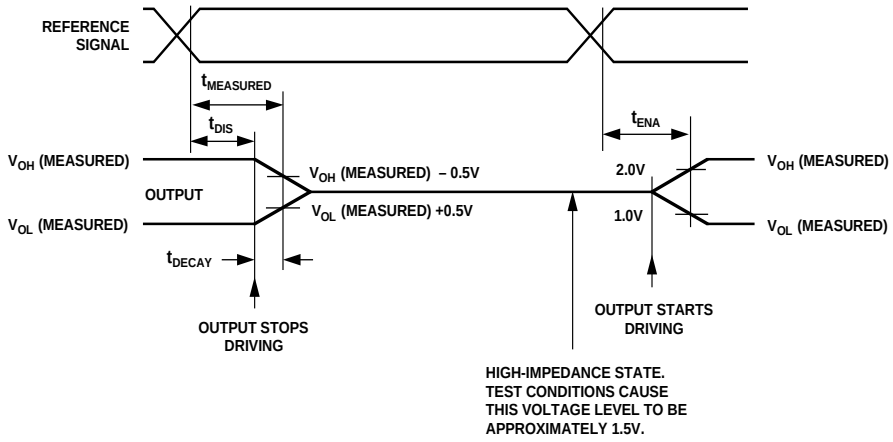


Figure 21. Output Enable/Disable

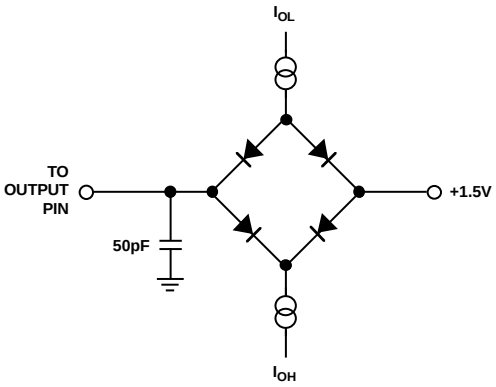


Figure 22. Equivalent Device Loading for AC Measurements (Except Output Enable/Disable)

TIMING PARAMETERS (ADSP-2101/2105/2111/2115/2161/2163)

GENERAL NOTES

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, you cannot meaningfully add parameters to derive longer times.

TIMING NOTES

Switching characteristics specify how the processor changes its signals. You have no control over this timing—circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics tell you what the processor will do in a given circumstance. You can also use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

MEMORY REQUIREMENTS

The table below shows common memory device specifications and the corresponding ADSP-21xx timing parameters, for your convenience.

Memory Device Specification	ADSP-21xx Timing Parameter	Timing Parameter Definition
Address Setup to Write Start	t_{ASW}	A0–A13, $\overline{\text{DMS}}$, $\overline{\text{PMS}}$ Setup before $\overline{\text{WR}}$ Low
Address Setup to Write End	t_{AW}	A0–A13, $\overline{\text{DMS}}$, $\overline{\text{PMS}}$ Setup before $\overline{\text{WR}}$ Deasserted
Address Hold Time	t_{WRA}	A0–A13, $\overline{\text{DMS}}$, $\overline{\text{PMS}}$ Hold after $\overline{\text{WR}}$ Deasserted
Data Setup Time	t_{DW}	Data Setup before $\overline{\text{WR}}$ High
Data Hold Time	t_{DH}	Data Hold after $\overline{\text{WR}}$ High
$\overline{\text{OE}}$ to Data Valid	t_{RDD}	$\overline{\text{RD}}$ Low to Data Valid
Address Access Time	t_{AA}	A0–A13, $\overline{\text{DMS}}$, $\overline{\text{PMS}}$, $\overline{\text{BMS}}$ to Data Valid

TIMING PARAMETERS (ADSP-2101/2105/2111/2115/2161/2163)

CLOCK SIGNALS & RESET

Parameter		13 MHz Min	13 MHz Max	13.824 MHz Min	13.824 MHz Max	16.67 MHz Min	16.67 MHz Max	20 MHz Min	20 MHz Max	25 MHz Min	25 MHz Max	Frequency Dependency Min	Frequency Dependency Max	Unit
Timing Requirement:														
t_{CK}	CLKIN Period	76.9	150	72.3	150	60	150	50	150	40	150			ns
t_{CKL}	CLKIN Width Low	20		20		20		20		15		20		ns
t_{CKH}	CLKIN Width High	20		20		20		20		15		20		ns
t_{RSP}	$\overline{\text{RESET}}$ Width Low	384.5		361.5		300		250		200		$5t_{CK}$[1]		ns
Switching Characteristic:														
t_{CPL}	CLKOUT Width Low	28.5		26.2		20		15		10		$0.5t_{CK} - 10$		ns
t_{CPH}	CLKOUT Width High	28.5		26.2		20		15		10		$0.5t_{CK} - 10$		ns
t_{CKOH}	CLKIN High to CLKOUT High	0	20	0	20	0	20	0	20	0	15			ns

NOTES
[1]Applies after powerup sequence is complete. Internal phase lock loop requires no more than 2000 CLKIN cycles, assuming stable CLKIN (not including crystal oscillator startup time).

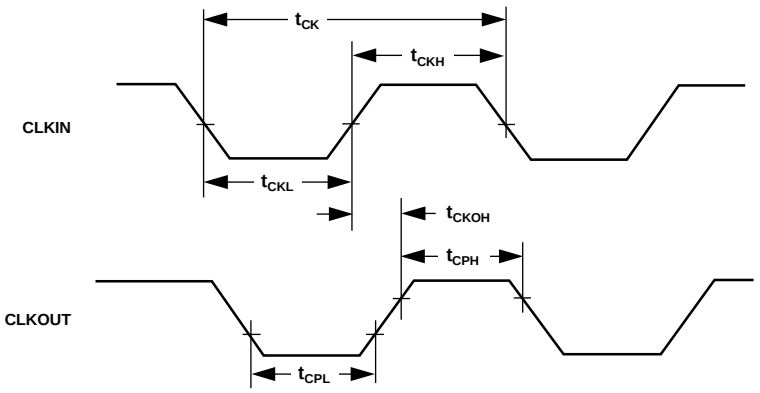


Figure 29. Clock Signals

TIMING PARAMETERS (ADSP-2101/2105/2111/2115/2161/2163)

MEMORY READ

Parameter		13 MHz Min	13 MHz Max	13.824 MHz Min	13.824 MHz Max	16.67 MHz Min	16.67 MHz Max	20 MHz Min	20 MHz Max	25 MHz Min	25 MHz Max	Unit
Timing Requirement:												
t_{RDD}	$\overline{RD}$ Low to Data Valid		23.5		23.2		17		12		7	ns
t_{AA}	A0–A13, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$ to Data Valid		37.7		36.2		27		19.5		12	ns
t_{RDH}	Data Hold from $\overline{RD}$ High	0		0		0		0		0		ns
Switching Characteristic:												
t_{RP}	$\overline{RD}$ Pulse Width	33.5		28.2		22		17		12		ns
t_{CRD}	CLKOUT High to $\overline{RD}$ Low	14.2	29.2	13.1	28.1	10	25	7.5	22.5	5	20	ns
t_{ASR}	A0–A13, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$ Setup before $\overline{RD}$ Low	9.2		8.1		5		2.5		1.5[1]		ns
t_{RDA}	A0–A13, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$ Hold after $\overline{RD}$ Deasserted	10.2		9.1		6		3.5		1		ns
t_{RWR}	$\overline{RD}$ High to $\overline{RD}$ or $\overline{WR}$ Low	33.5		31.2		25		20		15		ns

Parameter		Frequency Dependency (CLKIN ≤ 25 MHz) Min	Max	Unit
Timing Requirement:				
t_{RDD}	$\overline{RD}$ Low to Data Valid		$0.5t_{CK} - 13 + w$	ns
t_{AA}	A0–A13, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$ to Data Valid		$0.75t_{CK} - 18 + w$	ns
t_{RDH}	Data Hold from $\overline{RD}$ High	0		
Switching Characteristic:				
t_{RP}	$\overline{RD}$ Pulse Width	$0.5t_{CK} - 8 + w$		ns
t_{CRD}	CLKOUT High to $\overline{RD}$ Low	$0.25t_{CK} - 5$	$0.25t_{CK} + 10$	ns
t_{ASR}	A0–A13, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$ Setup before $\overline{RD}$ Low	$0.25t_{CK} - 10$[1]		ns
t_{RDA}	A0–A13, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$ Hold after $\overline{RD}$ Deasserted	$0.25t_{CK} - 9$		ns
t_{RWR}	$\overline{RD}$ High to $\overline{RD}$ or $\overline{WR}$ Low	$0.5t_{CK} - 5$		ns

NOTES
[1]For 25 MHz only minimum frequency dependency formula for $t_{ASR} = (0.25t_{CK} - 8.5)$.
w = wait states × t_{CK}.

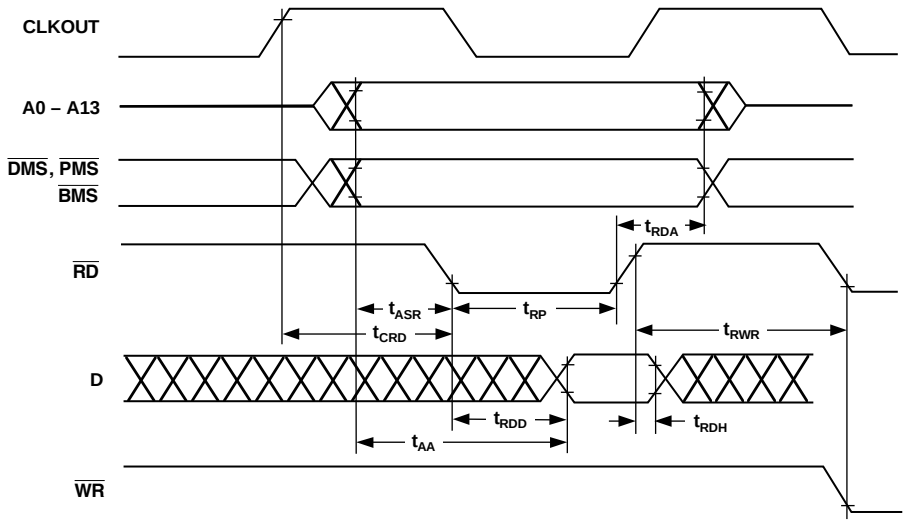


Figure 32. Memory Read

TIMING PARAMETERS (ADSP-2101/2105/2111/2115/2161/2163)

SERIAL PORTS

Parameter		12.5 MHz Min	12.5 MHz Max	13.0 MHz Min	13.0 MHz Max	13.824 MHz* Min	13.824 MHz* Max	Frequency Dependency Min	Frequency Dependency Max	Unit
Timing Requirement:										
t_{SCK}	SCLK Period	80		76.9		72.3				ns
t_{SCS}	DR/TFS/RFS Setup before SCLK Low	8		8		8				ns
t_{SCH}	DR/TFS/RFS Hold after SCLK Low	10		10		10				ns
t_{SCP}	$SCLK_{IN}$ Width	30		28		28				ns
Switching Characteristic:										
t_{CC}	CLKOUT High to $SCLK_{OUT}$	20	35	19.2	34.2	18.1	33.1	$0.25t_{CK}$	$0.25t_{CK}$ + 15ns	
t_{SCDE}	SCLK High to DT Enable	0		0		0				ns
t_{SCDV}	SCLK High to DT Valid		20		20		20			ns
t_{RH}	TFS/RFS_{OUT} Hold after SCLK High	0		0		0				ns
t_{RD}	TFS/RFS_{OUT} Delay from SCLK High		20		20		20			ns
t_{SCDH}	DT Hold after SCLK High	0		0		0				ns
t_{TDE}	TFS (Alt) to DT Enable	0		0		0				ns
t_{TDV}	TFS (Alt) to DT Valid		18		18		18			ns
t_{SCDD}	SCLK High to DT Disable		25		25		25			ns
t_{RDV}	RFS (Multichannel, Frame Delay Zero) to DT Valid		20		20		20			ns

*Maximum serial port operating frequency is 13.824 MHz for all processor speed grades except the 12.5 MHz ADSP-2101 and 13.0 MHz ADSP-2111.

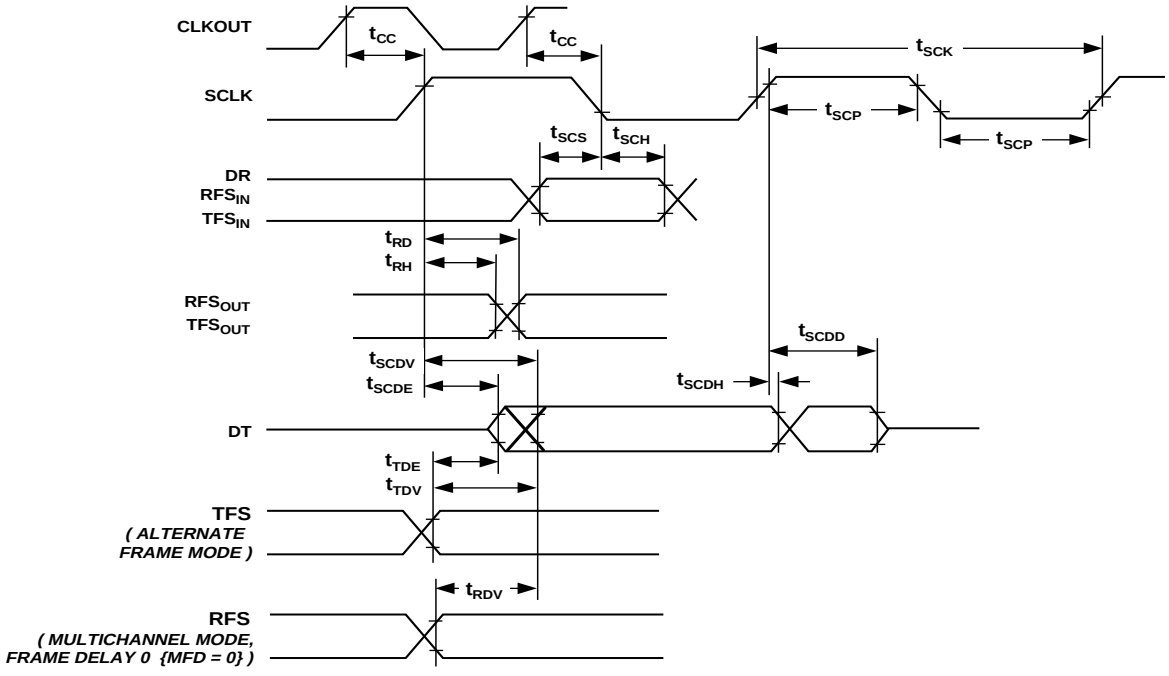
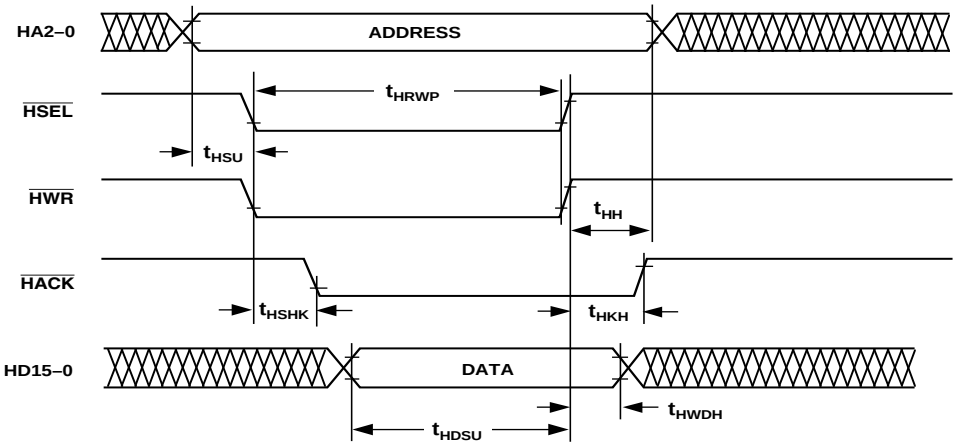


Figure 34. Serial Ports

Host Write Cycle



Host Read Cycle

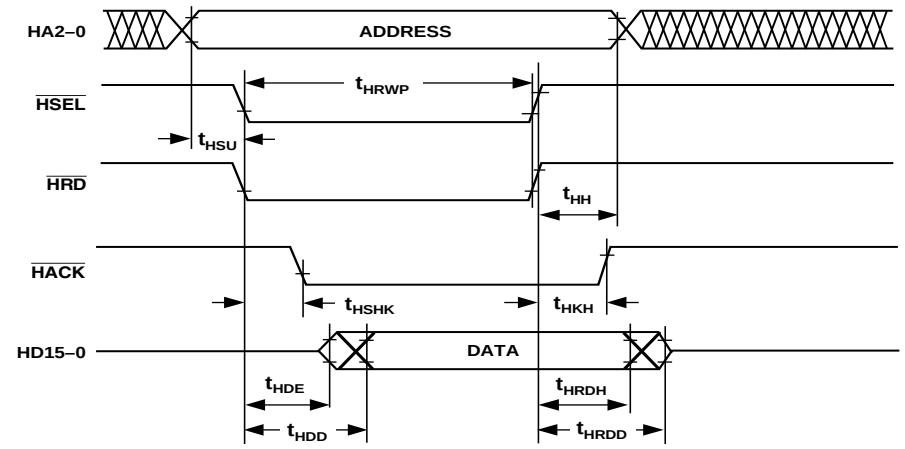


Figure 35. Host Interface Port (HMD1 = 0, HMD0 = 0)

Host Write Cycle

Host Read Cycle

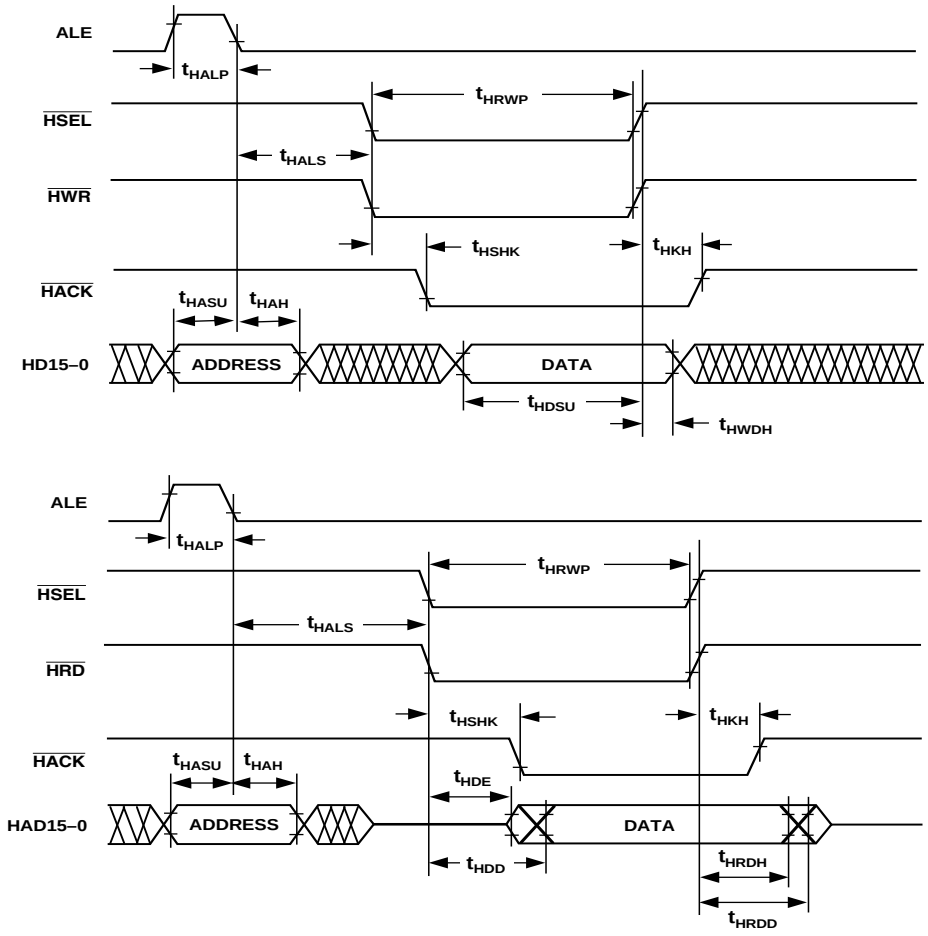


Figure 37. Host Interface Port (HMD1 = 1, HMD0 = 0)

TIMING PARAMETERS (ADSP-2103/2162/2164)

MEMORY WRITE

Parameter		10.24 MHz Min	10.24 MHz Max	Frequency Dependency Min	Frequency Dependency Max	Unit
Switching Characteristic:						
t_{DW}	Data Setup before $\overline{WR}$ High	38.8		$0.5t_{CK} - 10 + w$		ns
t_{DH}	Data Hold after $\overline{WR}$ High	14.4		$0.25t_{CK} - 10$		ns
t_{WP}	$\overline{WR}$ Pulse Width	43.8		$0.5t_{CK} - 5 + w$		ns
t_{WDE}	$\overline{WR}$ Low to Data Enabled	0				
t_{ASW}	A0–A13, $\overline{DMS}$, $\overline{PMS}$ Setup before $\overline{WR}$ Low	12.4		$0.25t_{CK} - 12$		ns
t_{DDR}	Data Disable before $\overline{WR}$ or $\overline{RD}$ Low	14.4		$0.25t_{CK} - 10$		ns
t_{CWR}	CLKOUT High to $\overline{WR}$ Low	19.4	34.4	$0.25t_{CK} - 5$	$0.25t_{CK} + 10$	ns
t_{AW}	A0–A13, $\overline{DMS}$, $\overline{PMS}$, Setup before $\overline{WR}$ Deasserted	58.2		$0.75t_{CK} - 15 + w$		ns
t_{WRA}	A0–A13, $\overline{DMS}$, $\overline{PMS}$ Hold After $\overline{WR}$ Deasserted	14.4		$0.25t_{CK} - 10$		ns
t_{WWR}	$\overline{WR}$ High to $\overline{RD}$ or $\overline{WR}$ Low	38.8		$0.5t_{CK} - 10$		ns

w = wait states × t_{CK}.

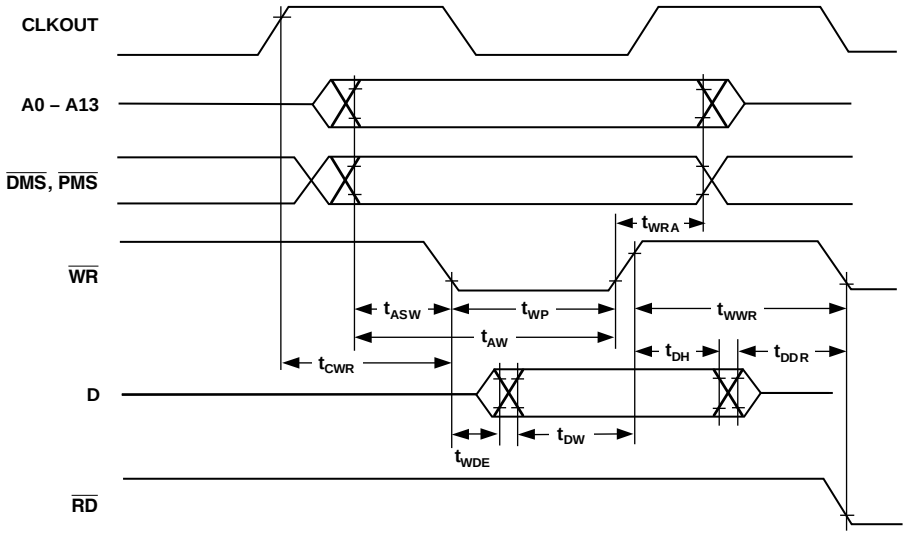
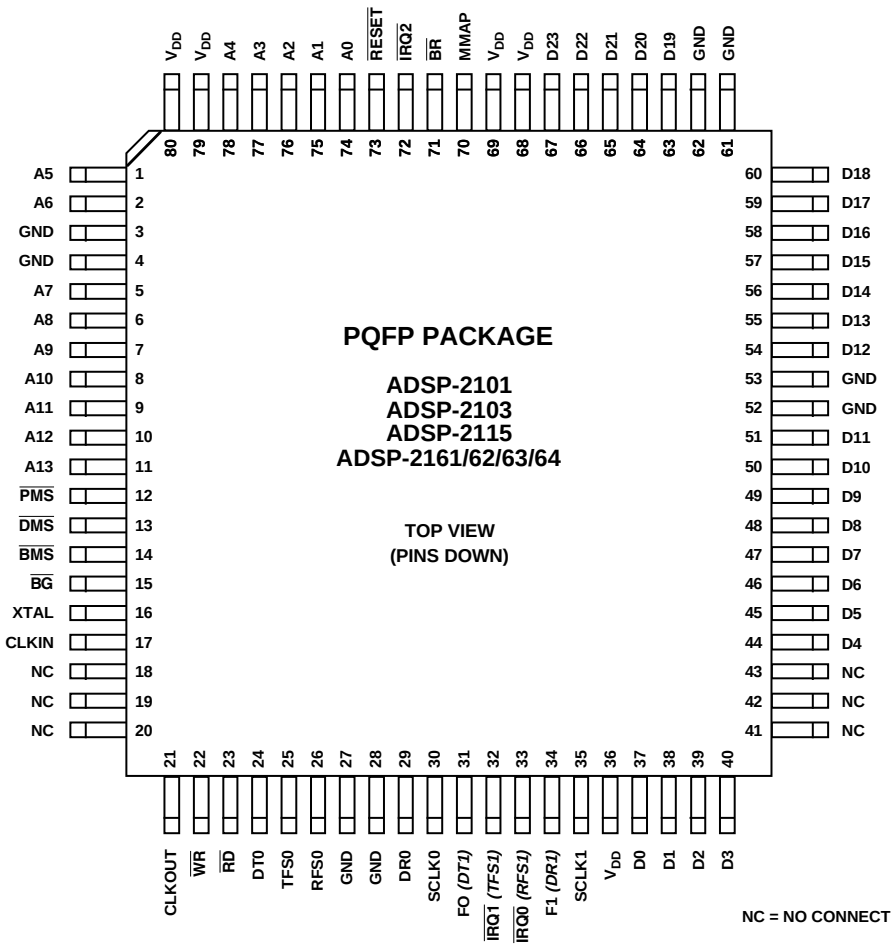


Figure 43. Memory Write

PIN CONFIGURATIONS

80-Lead PQFP
80-Lead TQFP



PQFP/ TQFP Number	Pin Name
1	A5
2	A6
3	GND
4	GND
5	A7
6	A8
7	A9
8	A10
9	A11
10	A12
11	A13
12	$\overline{PMS}$
13	$\overline{DMS}$
14	$\overline{BMS}$
15	$\overline{BG}$
16	XTAL
17	CLKIN
18	NC
19	NC
20	NC

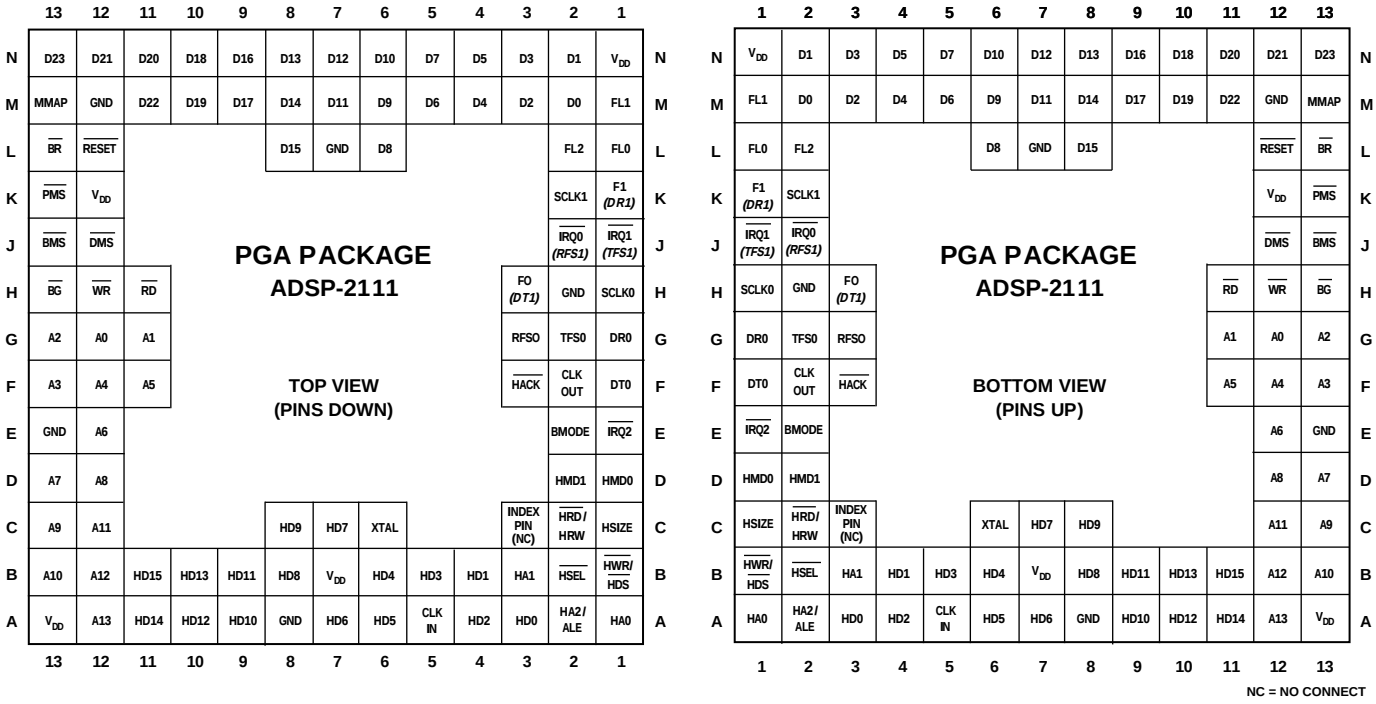
PQFP/ TQFP Number	Pin Name
21	CLKOUT
22	$\overline{WR}$
23	$\overline{RD}$
24	DT0
25	TFS0
26	RFS0
27	GND
28	GND
29	DR0
30	SCLK0
31	FO *(DT1)*
32	$\overline{IRQ1}$ *(TFS1)*
33	$\overline{IRQ0}$ *(RFS1)*
34	FI *(DR1)*
35	SCLK1
36	V_{DD}
37	D0
38	D1
39	D2
40	D3

PQFP/ TQFP Number	Pin Name
41	NC
42	NC
43	NC
44	D4
45	D5
46	D6
47	D7
48	D8
49	D9
50	D10
51	D11
52	GND
53	GND
54	D12
55	D13
56	D14
57	D15
58	D16
59	D17
60	D18

PQFP/ TQFP Number	Pin Name
61	GND
62	GND
63	D19
64	D20
65	D21
66	D22
67	D23
68	V_{DD}
69	V_{DD}
70	MMAP
71	$\overline{BR}$
72	$\overline{IRQ2}$
73	$\overline{RESET}$
74	A0
75	A1
76	A2
77	A3
78	A4
79	V_{DD}
80	V_{DD}

PIN CONFIGURATIONS

100-Pin PGA



PGA Number	Pin Name
N13	D23
N12	D21
M13	MMAP
M12	GND
L13	$\overline{BR}$
L12	$\overline{RESET}$
K13	$\overline{PMS}$
K12	V_{DD}
J13	$\overline{BMS}$
J12	$\overline{DMS}$
H13	$\overline{BG}$
H12	$\overline{WR}$
H11	$\overline{RD}$
G13	A2
G12	A0
G11	A1
F13	A3
F12	A4
F11	A5
E13	GND
E12	A6
D13	A7
D12	A8
C13	A9
C12	A11

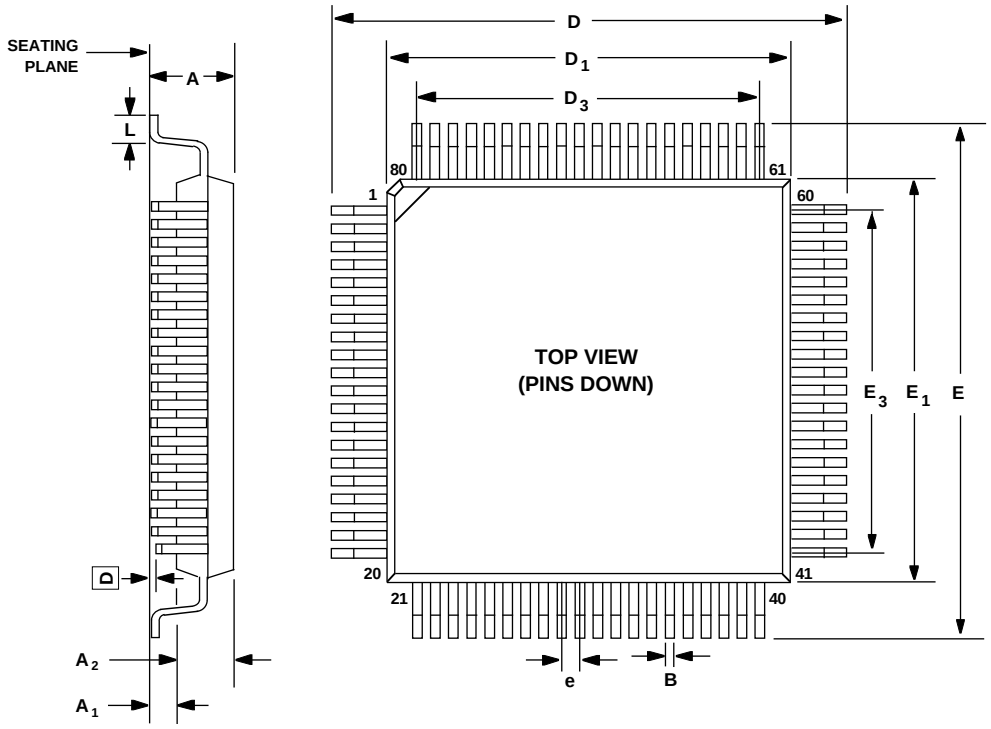
PGA Number	Pin Name
B13	A10
A13	V_{DD}
A12	A13
B12	A12
A11	HD14
B11	HD15
A10	HD12
B10	HD13
A9	HD10
B9	HD11
A8	GND
B8	HD8
C8	HD9
A7	HD6
B7	V_{DD}
C7	HD7
A6	HD5
B6	HD4
C6	XTAL
A5	CLKIN
B5	HD3
A4	HD2
B4	HD1
A3	HD0
B3	HA1

PGA Number	Pin Name
C3	Index (NC)
A2	HA2/ALE
A1	HA0
B1	$\overline{HWR}$/$\overline{HDS}$
B2	$\overline{HSEL}$
C1	HSIZE
C2	$\overline{HRD}$/HRW
D1	HMD0
D2	HMD1
E1	$\overline{IRQ2}$
E2	BMODE
F1	DT0
F2	CLKOUT
F3	$\overline{HACK}$
G1	DR0
G2	TFS0
G3	RFS0
H1	SCLK0
H2	GND
H3	FO *(DT1)*
J1	$\overline{IRQ1}$ *(TFS1)*
J2	$\overline{IRQ0}$ *(RFS1)*
K1	FI *(DR1)*
K2	SCLK1
L1	FL0

PGA Number	Pin Name
L2	FL2
M1	FL1
N1	V_{DD}
N2	D1
M2	D0
N3	D3
M3	D2
N4	D5
M4	D4
N5	D7
M5	D6
N6	D10
M6	D9
L6	D8
N7	D12
M7	D11
L7	GND
N8	D13
M8	D14
L8	D15
N9	D16
M9	D17
N10	D18
M10	D19
N11	D20
M11	D22

OUTLINE DIMENSIONS

ADSP-21xx
80-Lead Metric Plastic Quad Flatpack (PQFP)
80-Lead Metric Thin Quad Flatpack (TQFP)



PQFP

SYMBOL	MILLIMETERS			INCHES		
	MIN	TYP	MAX	MIN	TYP	MAX
A			2.45			0.096
A_1	0.25			0.010		
A_2	1.90	2.00	2.10	0.075	0.079	0.083
D, E	16.95	17.20	17.45	0.667	0.678	0.690
D_1, E_1	13.90	14.00	14.10	0.547	0.551	0.555
D_3, E_3		12.35	12.43		0.486	0.490
L	0.65	0.80	0.95	0.026	0.031	0.037
e	0.57	0.65	0.73	0.023	0.026	0.029
B	0.22	0.30	0.38	0.009	0.012	0.015
a			0.10			0.004

TQFP

MILLIMETERS			INCHES		
MIN	TYP	MAX	MIN	TYP	MAX
		1.60			0.063
0.05		0.15	0.002		0.006
1.35	1.40	1.45	0.053	0.055	0.057
15.75	16.00	16.25	0.620	0.630	0.640
13.95	14.00	14.05	0.549	0.551	0.553
	12.35	12.43		0.486	0.490
0.50	0.60	0.75	0.020	0.024	0.030
0.57	0.65	0.73	0.022	0.026	0.029
0.25	0.30	0.35	0.010	0.012	0.014
		0.10			0.004