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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	Synchronous Serial Port (SSP)
Clock Rate	25MHz
Non-Volatile Memory	External
On-Chip RAM	3kB
Voltage - I/O	5.00V
Voltage - Core	5.00V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	68-LCC (J-Lead)
Supplier Device Package	68-PLCC (24.23x24.23)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-2115bpz-100

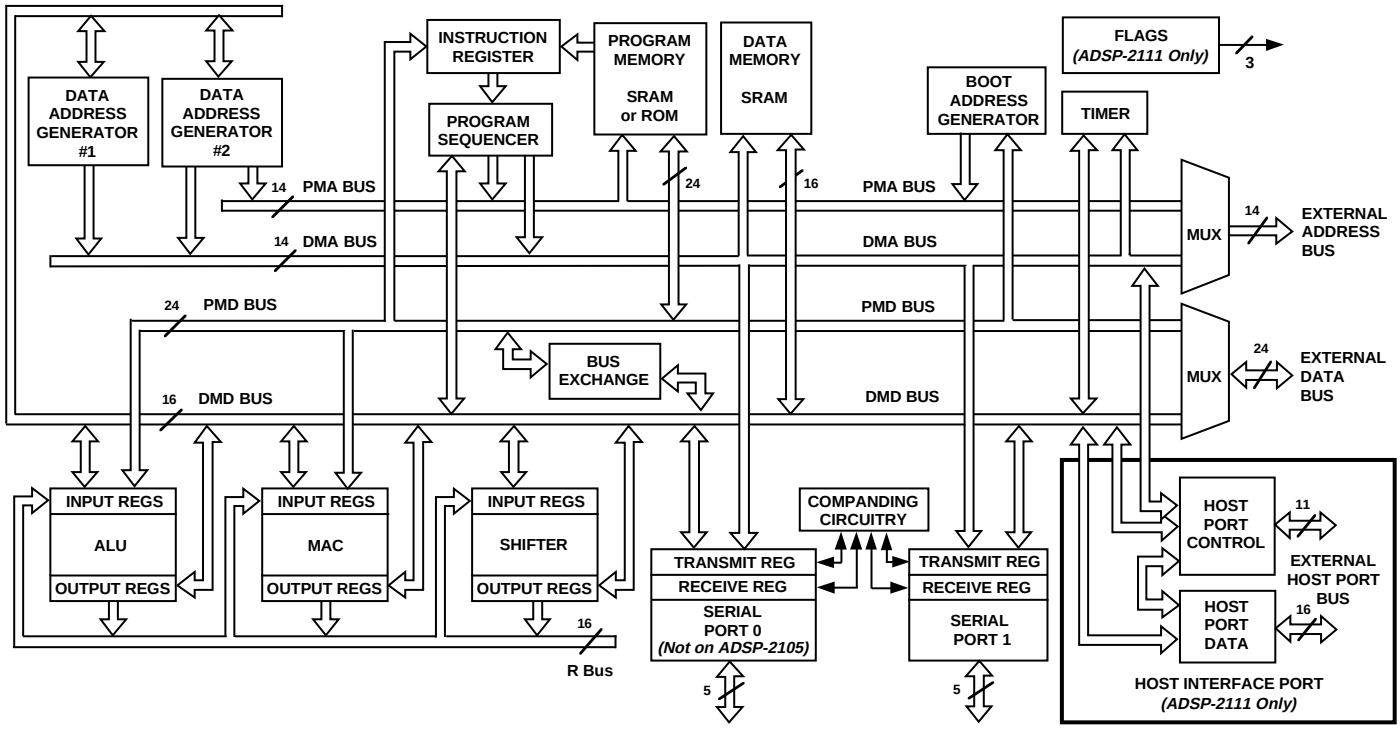


Figure 1. ADSP-21xx Block Diagram

One bus grant execution mode (GO Mode) allows the ADSP-21xx to continue running from internal memory. A second execution mode requires the processor to halt while buses are granted.

Each ADSP-21xx processor can respond to several different interrupts. There can be up to three external interrupts, configured as edge- or level-sensitive. Internal interrupts can be generated by the timer, serial ports, and, on the ADSP-2111, the host interface port. There is also a master $\overline{\text{RESET}}$ signal.

Booting circuitry provides for loading on-chip program memory automatically from byte-wide external memory. After reset, three wait states are automatically generated. This allows, for example, a 60 ns ADSP-2101 to use a 200 ns EPROM as external boot memory. Multiple programs can be selected and loaded from the EPROM with no additional hardware.

The data receive and transmit pins on SPORT1 (Serial Port 1) can be alternatively configured as a general-purpose input flag and output flag. You can use these pins for event signalling to and from an external device. The ADSP-2111 has three additional flag outputs whose states are controlled through software.

A programmable interval timer can generate periodic interrupts. A 16-bit count register (TCOUNT) is decremented every *n* cycles, where *n–1* is a scaling value stored in an 8-bit register (TSCALE). When the value of the count register reaches zero, an interrupt is generated and the count register is reloaded from a 16-bit period register (TPERIOD).

Serial Ports

The ADSP-21xx processors include two synchronous serial ports (“SPORTs”) for serial communications and multiprocessor communication. All of the ADSP-21xx processors have two serial ports (SPORT0, SPORT1) except for the ADSP-2105, which has only SPORT1.

The serial ports provide a complete synchronous serial interface with optional companding in hardware. A wide variety of framed or frameless data transmit and receive modes of operation are available. Each SPORT can generate an internal programmable serial clock or accept an external serial clock.

Each serial port has a 5-pin interface consisting of the following signals:

Signal Name	Function
SCLK	Serial Clock (I/O)
RFS	Receive Frame Synchronization (I/O)
TFS	Transmit Frame Synchronization (I/O)
DR	Serial Data Receive
DT	Serial Data Transmit

The ADSP-21xx serial ports offer the following capabilities:

Bidirectional—Each SPORT has a separate, double-buffered transmit and receive function.

Flexible Clocking—Each SPORT can use an external serial clock or generate its own clock internally.

A clock output signal (CLKOUT) is generated by the processor, synchronized to the processor's internal cycles.

Reset

The $\overline{\text{RESET}}$ signal initiates a complete reset of the ADSP-21xx. The $\overline{\text{RESET}}$ signal must be asserted when the chip is powered up to assure proper initialization. If the $\overline{\text{RESET}}$ signal is applied during initial power-up, it must be held long enough to allow the processor's internal clock to stabilize. If $\overline{\text{RESET}}$ is activated at any time after power-up and the input clock frequency does not change, the processor's internal clock continues and does not require this stabilization time.

The power-up sequence is defined as the total time required for the crystal oscillator circuit to stabilize after a valid V_{DD} is applied to the processor and for the internal phase-locked loop (PLL) to lock onto the specific crystal frequency. A minimum of 2000 t_{CK} cycles will ensure that the PLL has locked (this does not, however, include the crystal oscillator start-up time). During this power-up sequence the $\overline{\text{RESET}}$ signal should be held low. On any subsequent resets, the $\overline{\text{RESET}}$ signal must meet the minimum pulse width specification, t_{RSP}.

To generate the $\overline{\text{RESET}}$ signal, use either an RC circuit with an external Schmidt trigger or a commercially available reset IC. (Do not use only an RC circuit.)

Table IV. ADSP-21xx Pin Definitions

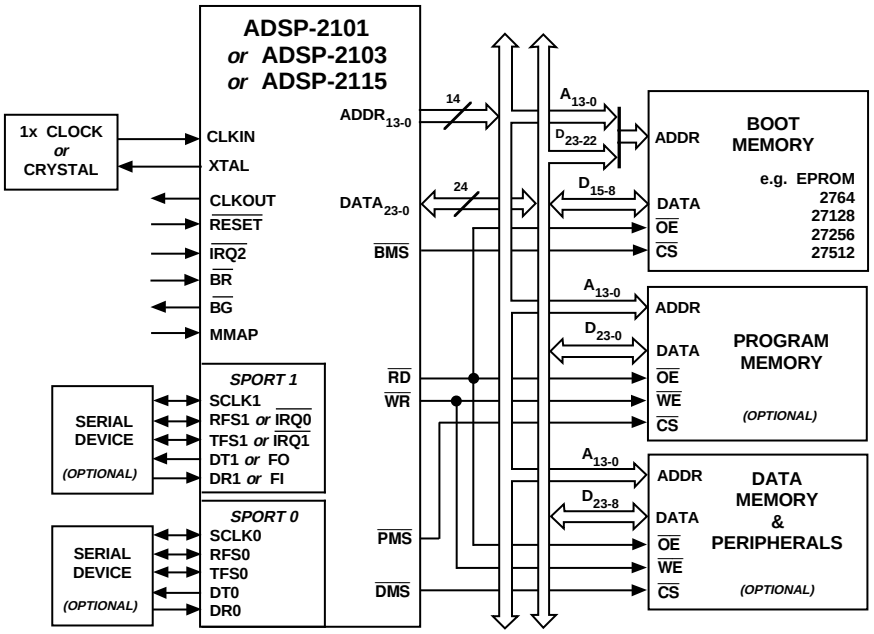
Pin Name(s)	# of Pins	Input / Output	Function
Address	14	O	Address outputs for program, data and boot memory.
Data[1]	24	I/O	Data I/O pins for program and data memories. Input only for boot memory, with two MSBs used for boot memory addresses. Unused data lines may be left floating.
$\overline{\text{RESET}}$	1	I	Processor Reset Input
$\overline{\text{IRQ2}}$	1	I	External Interrupt Request #2
$\overline{\text{BR}}$[2]	1	I	External Bus Request Input
$\overline{\text{BG}}$	1	O	External Bus Grant Output
$\overline{\text{PMS}}$	1	O	External Program Memory Select
$\overline{\text{DMS}}$	1	O	External Data Memory Select
$\overline{\text{BMS}}$	1	O	Boot Memory Select
$\overline{\text{RD}}$	1	O	External Memory Read Enable
$\overline{\text{WR}}$	1	O	External Memory Write Enable
MMAP	1	I	Memory Map Select Input
CLKIN, XTAL	2	I	External Clock or Quartz Crystal Input
CLKOUT	1	O	Processor Clock Output
V_{DD}			Power Supply Pins
GND			Ground Pins
SPORT0[3]	5	I/O	Serial Port 0 Pins *(TFS0, RFS0, DT0, DR0, SCLK0)*
SPORT1	5	I/O	Serial Port 1 Pins *(TFS1, RFS1, DT1, DR1, SCLK1)*
or Interrupts & Flags:			
$\overline{\text{IRQ0}}$ *(RFS1)*	1	I	External Interrupt Request #0
$\overline{\text{IRQ1}}$ *(TFS1)*	1	I	External Interrupt Request #1
FI *(DR1)*	1	I	Flag Input Pin
FO *(DT1)*	1	O	Flag Output Pin
FL2–0 *(ADSP-2111 Only)*	3	O	General Purpose Flag Output Pins
Host Interface Port (ADSP-2111 Only)			
$\overline{\text{HSEL}}$	1	I	HIP Select Input
$\overline{\text{HACK}}$	1	O	HIP Acknowledge Output
HSIZE	1	I	8/16-Bit Host Select *(0 = 16-Bit, 1 = 8-Bit)*
BMODE	1	I	Boot Mode Select *(0 = Standard EPROM Booting, 1 = HIP Booting)*
HMD0	1	I	Bus Strobe Select *(0 =* $\overline{\text{RD}}$/$\overline{\text{WR}}$*, 1 =* RW/$\overline{\text{DS}}$*)*
HMD1	1	I	HIP Address/Data Mode Select *(0 = Separate, 1 = Multiplexed)*
$\overline{\text{HRD}}$/HRW	1	I	HIP Read Strobe *or* Read/Write Select
$\overline{\text{HWR}}$/$\overline{\text{HDS}}$	1	I	HIP Write Strobe *or* Host Data Strobe Select
HD15–0/HAD15-0	16	I/O	HIP Data *or* HIP Data and Address
HA2/ALE	1	I	Host Address 2 Input *or* Address Latch Enable Input
HA1–0/Unused	2	I	Host Address 1 and 0 Inputs

NOTES

[1]Unused data bus lines may be left floating.

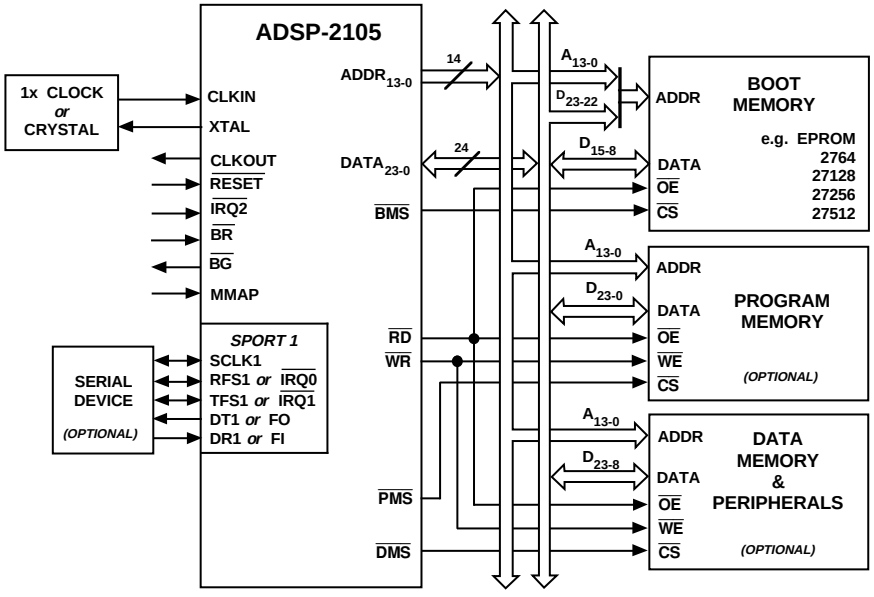
[2]$\overline{\text{BR}}$ must be tied high (to V_{DD}) if not used.

[3]ADSP-2105 does not have SPORT0. (SPORT0 pins are No Connects on the ADSP-2105.)



THE TWO MSBs OF THE DATA BUS (D_{23-22}) ARE USED TO SUPPLY THE TWO MSBs OF THE BOOT MEMORY EPROM ADDRESS. THIS IS ONLY REQUIRED FOR THE 27256 AND 27512.

Figure 3. ADSP-2101/ADSP-2103/ADSP-2115 System



THE TWO MSBs OF THE DATA BUS (D_{23-22}) ARE USED TO SUPPLY THE TWO MSBs OF THE BOOT MEMORY EPROM ADDRESS. THIS IS ONLY REQUIRED FOR THE 27256 AND 27512.

Figure 4. ADSP-2105 System

Data Memory Interface
The data memory address bus (DMA) is 14 bits wide. The bidirectional external data bus is 24 bits wide, with the upper 16 bits used for data memory data (DMD) transfers.

The data memory select ($\overline{DMS}$) signal indicates access to data memory and can be used as a chip select signal. The write ($\overline{WR}$) signal indicates a write operation and can be used as a write strobe. The read ($\overline{RD}$) signal indicates a read operation and can be used as a read strobe or output enable signal.

The ADSP-21xx processors support memory-mapped I/O, with the peripherals memory-mapped into the data memory address space and accessed by the processor in the same manner as data memory.

Data Memory Map
ADSP-2101/ADSP-2103/ADSP-2111
For the ADSP-2101, ADSP-2103, and ADSP-2111, on-chip data memory RAM resides in the 1K words beginning at address 0x3800, as shown in Figure 10. Data memory locations from 0x3C00 to the end of data memory at 0x3FFF are reserved. Control and status registers for the system, timer, wait-state configuration, and serial port operations are located in this region of memory.

ADSP-2105/ADSP-2115
For the ADSP-2105 and ADSP-2115, on-chip data memory RAM resides in the 512 words beginning at address 0x3800, also shown in Figure 10. Data memory locations from 0x3A00 to the end of data memory at 0x3FFF are reserved. Control and status registers for the system, timer, wait-state configuration, and serial port operations are located in this region of memory.

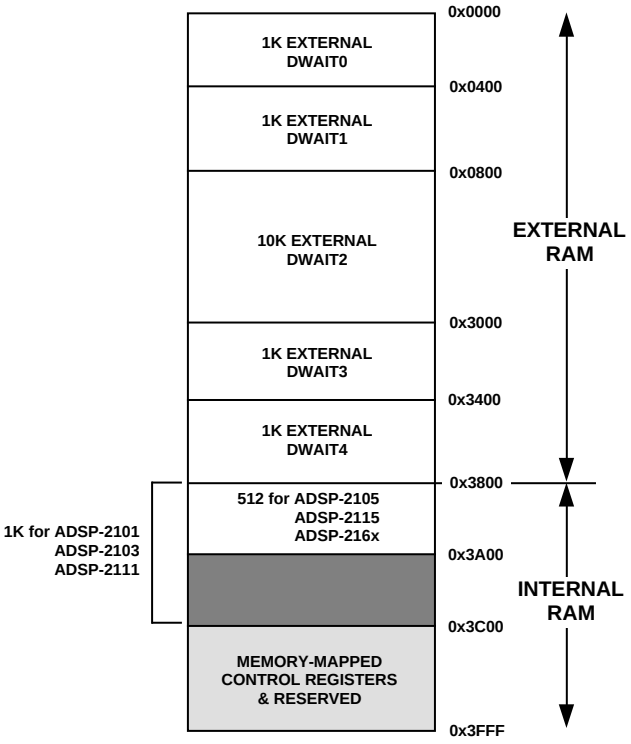


Figure 10. Data Memory Map (All Processors)

All Processors
The remaining 14K of data memory is located off-chip. This external data memory is divided into five zones, each associated with its own wait-state generator. This allows slower peripherals to be memory-mapped into data memory for which wait states are specified. By mapping peripherals into different zones, you can accommodate peripherals with different wait-state requirements. All zones default to seven wait states after $\overline{RESET}$.

Boot Memory Interface
On the ADSP-2101, ADSP-2103, and ADSP-2111, boot memory is an external 64K by 8 space, divided into eight separate 8K by 8 pages. On the ADSP-2105 and ADSP-2115, boot memory is a 32K by 8 space, divided into eight separate 4K by 8 pages. The 8-bit bytes are automatically packed into 24-bit instruction words by each processor, for loading into on-chip program memory.

Three bits in the processors' System Control Register select which page is loaded by the boot memory interface. Another bit in the System Control Register allows the forcing of a boot loading sequence under software control. Boot loading from Page 0 after $\overline{RESET}$ is initiated automatically if MMAP = 0.

The boot memory interface can generate zero to seven wait states; it defaults to three wait states after $\overline{RESET}$. This allows the ADSP-21xx to boot from a single low cost EPROM such as a 27C256. Program memory is booted one byte at a time and converted to 24-bit program memory words.

The $\overline{BMS}$ and $\overline{RD}$ signals are used to select and to strobe the boot memory interface. Only 8-bit data is read over the data bus, on pins D8-D15. To accommodate up to eight pages of boot memory, the two MSBs of the data bus are used in the boot memory interface as the two MSBs of the boot memory address: D23, D22, and A13 supply the boot page number.

The ADSP-2100 Family Assembler and Linker allow the creation of programs and data structures requiring multiple boot pages during execution.

The $\overline{BR}$ signal is recognized during the booting sequence. The bus is granted after loading the current byte is completed. $\overline{BR}$ during booting may be used to implement booting under control of a host processor.

Bus Interface
The ADSP-21xx processors can relinquish control of their data and address buses to an external device. When the external device requires control of the buses, it asserts the bus request signal ($\overline{BR}$). If the ADSP-21xx is not performing an external memory access, it responds to the active $\overline{BR}$ input in the next cycle by:

- Three-stating the data and address buses and the $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ output drivers,
- Asserting the bus grant ($\overline{BG}$) signal,
- and halting program execution.

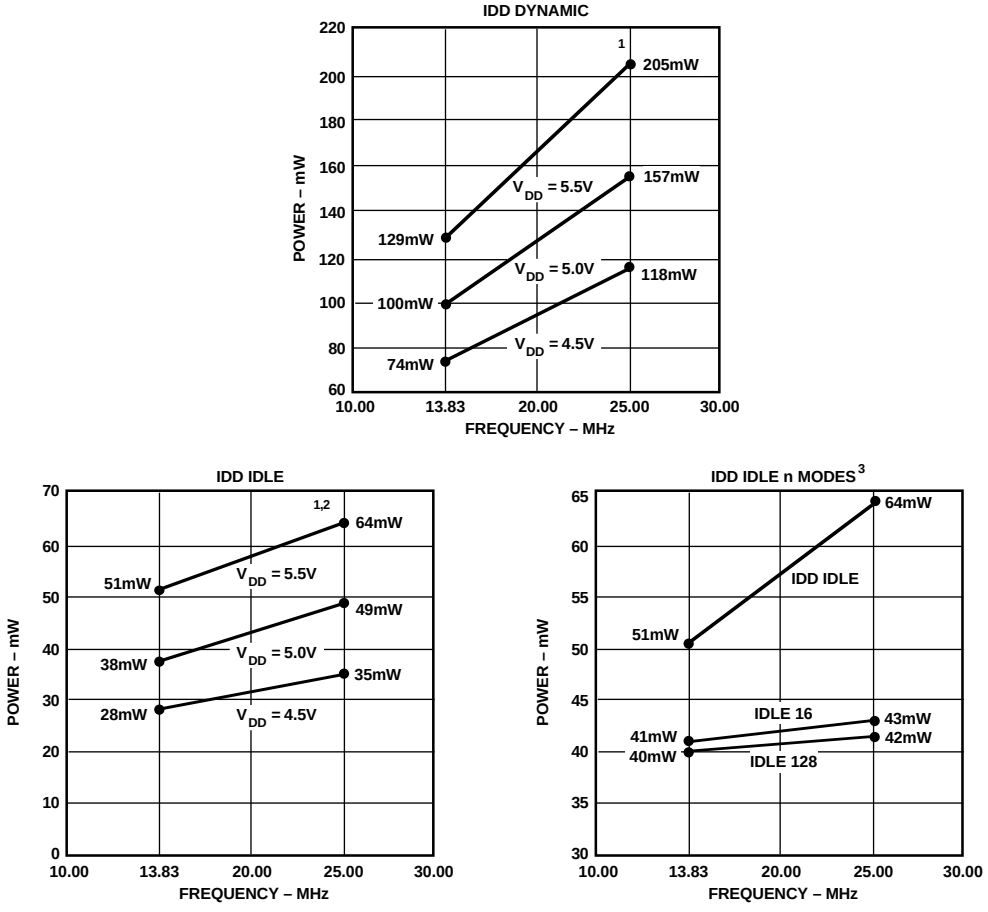
If the Go mode is set, however, the ADSP-21xx will not halt program execution until it encounters an instruction that requires an external memory access.

SPECIFICATIONS (ADSP-2101/2105/2115/2161/2163)

SUPPLY CURRENT & POWER (ADSP-2101/2105/2115/2161/2163)

Parameter		Test Conditions	Min	Max	Unit
I_{DD}	Supply Current (Dynamic)[1]	@ V_{DD} = max, t_{CK} = 40 ns[2]		38	mA
		@ V_{DD} = max, t_{CK} = 50 ns[2]		31	mA
		@ V_{DD} = max, t_{CK} = 72.3 ns[2]		24	mA
I_{DD}	Supply Current (Idle)[1, 3]	@ V_{DD} = max, t_{CK} = 40 ns[4]		12	mA
		@ V_{DD} = max, t_{CK} = 50 ns		11	mA
		@ V_{DD} = max, t_{CK} = 72.3 ns		10	mA

NOTES
[1]Current reflects device operating with no output loads.
[2]V_{IN} = 0.4 V and 2.4 V.
[3]Idle refers to ADSP-21xx state of operation during execution of IDLE instruction. Deasserted pins are driven to either V_{DD} or GND.
[4]ADSP-2105 is not available in a 25 MHz speed grade.
For typical supply current (internal power dissipation) figures, see Figure 11.



VALID FOR ALL TEMPERATURE GRADES.
1 POWER REFLECTS DEVICE OPERATING WITH NO OUTPUT LOADS.
2 IDLE REFERS TO ADSP-21xx OPERATION DURING EXECUTION OF IDLE INSTRUCTION. DEASSERTED PINS ARE DRIVEN TO EITHER V_{DD} OR GND.
3 MAXIMUM POWER DISSIPATION AT V_{DD} = 5.5V DURING EXECUTION OF *IDLE n* INSTRUCTION.

Figure 11. ADSP-2101 Power (Typical) vs. Frequency

SPECIFICATIONS (ADSP-2101/2105/2115/2161/2163)

TEST CONDITIONS

Figure 14 shows voltage reference levels for ac measurements.

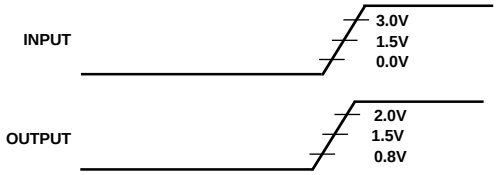


Figure 14. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Disable Time

Output pins are considered to be disabled when they have stopped driving and started a transition from the measured output high or low voltage to a high impedance state. The output disable time (t_{DIS}) is the difference of $t_{MEASURED}$ and t_{DECAY}, as shown in Figure 15. The time $t_{MEASURED}$ is the interval from when a reference signal reaches a high or low voltage level to when the output voltages have changed by 0.5 V from the measured output high or low voltage.

The decay time, t_{DECAY}, is dependent on the capacitative load, C_L, and the current load, i_L, on the output pin. It can be approximated by the following equation:

$$t_{DECAY} = \frac{C_L \times 0.5\,V}{i_L}$$

from which

$$t_{DIS} = t_{MEASURED} - t_{DECAY}$$

is calculated. If multiple pins (such as the data bus) are disabled, the measurement value is that of the last pin to stop driving.

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high-impedance state to when they start driving. The output enable time (t_{ENA}) is the interval from when a reference signal reaches a high or low voltage level to when the output has reached a specified high or low trip point, as shown in Figure 15. If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

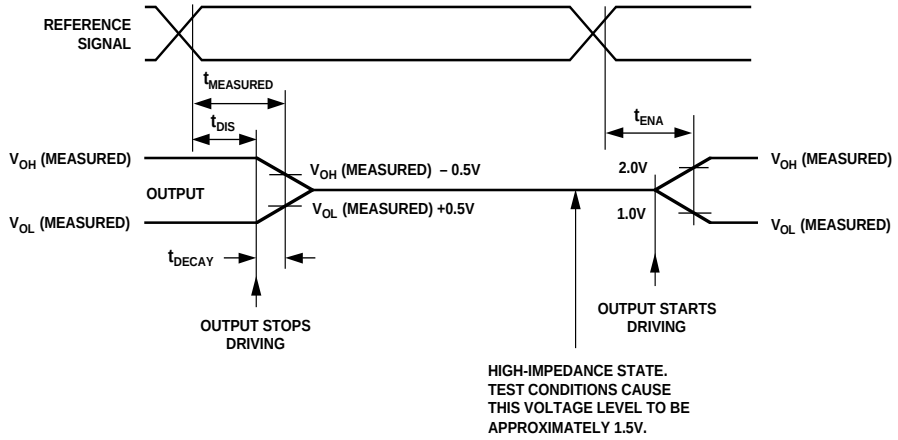


Figure 15. Output Enable/Disable

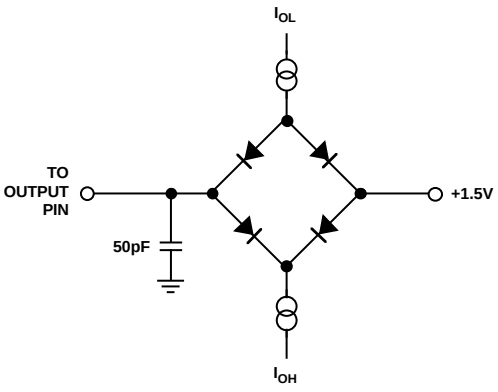


Figure 16. Equivalent Device Loading for AC Measurements (Except Output Enable/Disable)

SPECIFICATIONS (ADSP-2111)

POWER DISSIPATION EXAMPLE

To determine total power dissipation in a specific application, the following equation should be applied for each output:

$$C \times V_{DD}^2 \times f$$

C = load capacitance, f = output switching frequency.

Example:

In an ADSP-2111 application where external data memory is used and no other outputs are active, power dissipation is calculated as follows:

Assumptions:

- External data memory is accessed every cycle with 50% of the address pins switching.
- External data memory writes occur every other cycle with 50% of the data pins switching.
- Each address and data pin has a 10 pF total load at the pin.
- The application operates at V_{DD} = 5.0 V and t_{CK} = 50 ns.

$$\textit{Total Power Dissipation} = P_{INT} + (C \times V_{DD}^2 \times f)$$

P_{INT} = internal power dissipation (from Figure 17).

$(C \times V_{DD}^2 \times f)$ is calculated for each output:

Output	# of Pins	× C	× V_{DD}^2	× f
Address, $\overline{DMS}$	8	× 10 pF	× 5^2 V	× 20 MHz = 40.0 mW
Data, $\overline{WR}$	9	× 10 pF	× 5^2 V	× 10 MHz = 22.5 mW
$\overline{RD}$	1	× 10 pF	× 5^2 V	× 10 MHz = 2.5 mW
CLKOUT	1	× 10 pF	× 5^2 V	× 20 MHz = 5.0 mW
				70.0 mW

Total power dissipation for this example = P_{INT} + 70.0 mW.

ENVIRONMENTAL CONDITIONS

Ambient Temperature Rating:

$T_{AMB} = T_{CASE} - (PD \times \theta_{CA})$
T_{CASE} = Case Temperature in °C
PD = Power Dissipation in W
θ_{CA} = Thermal Resistance (Case-to-Ambient)
θ_{JA} = Thermal Resistance (Junction-to-Ambient)
θ_{JC} = Thermal Resistance (Junction-to-Case)

Package	θ_{JA}	θ_{JC}	θ_{CA}
PGA	35°C/W	18°C/W	17°C/W
PQFP	42°C/W	18°C/W	23°C/W

CAPACITIVE LOADING

Figures 18 and 19 show capacitive loading characteristics for the ADSP-2111.

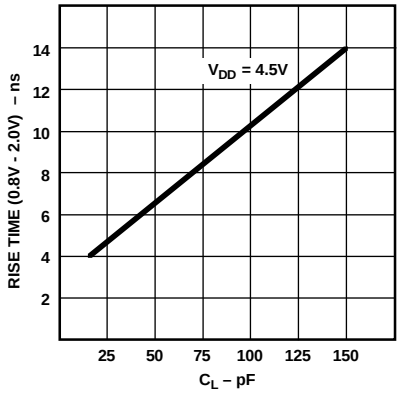


Figure 18. Typical Output Rise Time vs. Load Capacitance, C_L (at Maximum Ambient Operating Temperature)

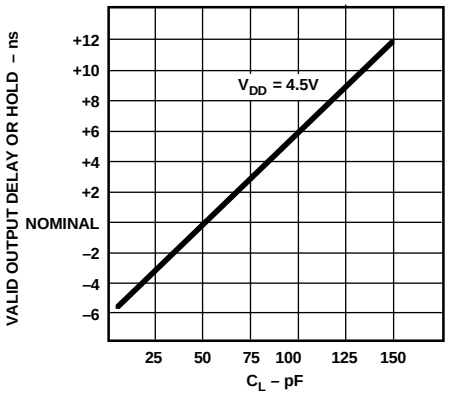


Figure 19. Typical Output Valid Delay or Hold vs. Load Capacitance, C_L (at Maximum Ambient Operating Temperature)

SPECIFICATIONS (ADSP-2103/2162/2164)

POWER DISSIPATION EXAMPLE

To determine total power dissipation in a specific application, the following equation should be applied for each output:

$$C \times V_{DD}^2 \times f$$

C = load capacitance, f = output switching frequency.

Example:

In an ADSP-2103 application where external data memory is used and no other outputs are active, power dissipation is calculated as follows:

Assumptions:

- External data memory is accessed every cycle with 50% of the address pins switching.
- External data memory writes occur every other cycle with 50% of the data pins switching.
- Each address and data pin has a 10 pF total load at the pin.
- The application operates at V_{DD} = 3.3 V and t_{CK} = 100 ns.

$$\textit{Total Power Dissipation} = P_{INT} + (C \times V_{DD}^2 \times f)$$

P_{INT} = internal power dissipation (from Figure 23).

$(C \times V_{DD}^2 \times f)$ is calculated for each output:

Output	# of Pins	× C	× V_{DD}^2	× f	
Address, $\overline{DMS}$	8	× 10 pF	× 3.3^2 V	× 10 MHz	= 8.71 mW
Data, $\overline{WR}$	9	× 10 pF	× 3.3^2 V	× 5 MHz	= 4.90 mW
$\overline{RD}$	1	× 10 pF	× 3.3^2 V	× 5 MHz	= 0.55 mW
CLKOUT	1	× 10 pF	× 3.3^2 V	× 10 MHz	= 1.09 mW
					15.25 mW

Total power dissipation for this example = P_{INT} + 15.25 mW.

ENVIRONMENTAL CONDITIONS

Ambient Temperature Rating:

$T_{AMB} = T_{CASE} - (PD \times \theta_{CA})$
T_{CASE} = Case Temperature in °C
PD = Power Dissipation in W
θ_{CA} = Thermal Resistance (Case-to-Ambient)
θ_{JA} = Thermal Resistance (Junction-to-Ambient)
θ_{JC} = Thermal Resistance (Junction-to-Case)

Package	θ_{JA}	θ_{JC}	θ_{CA}
PGA	27°C/W	16°C/W	11°C/W
PQFP	60°C/W	18°C/W	42°C/W

CAPACITIVE LOADING

Figures 24 and 25 show capacitive loading characteristics for the ADSP-2103, ADSP-2162, and ADSP-2164.

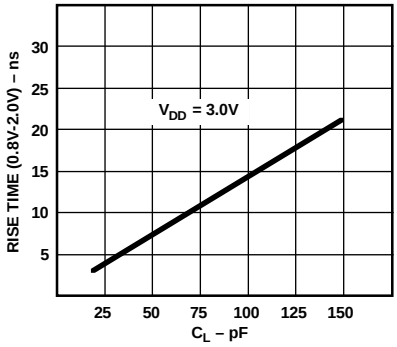


Figure 24. Typical Output Rise Time vs. Load Capacitance, C_L (at Maximum Ambient Operating Temperature)

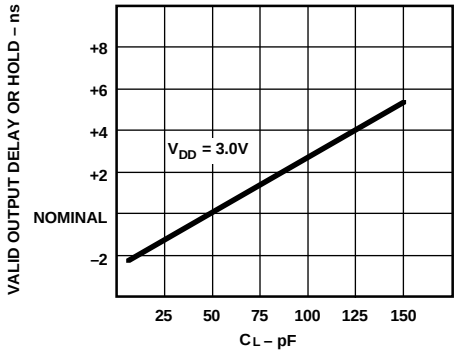


Figure 25. Typical Output Valid Delay or Hold vs. Load Capacitance, C_L (at Maximum Ambient Operating Temperature)

TIMING PARAMETERS (ADSP-2101/2105/2111/2115/2161/2163)

GENERAL NOTES

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, you cannot meaningfully add parameters to derive longer times.

TIMING NOTES

Switching characteristics specify how the processor changes its signals. You have no control over this timing—circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics tell you what the processor will do in a given circumstance. You can also use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

MEMORY REQUIREMENTS

The table below shows common memory device specifications and the corresponding ADSP-21xx timing parameters, for your convenience.

Memory Device Specification	ADSP-21xx Timing Parameter	Timing Parameter Definition
Address Setup to Write Start	t_{ASW}	A0–A13, $\overline{\text{DMS}}$, $\overline{\text{PMS}}$ Setup before $\overline{\text{WR}}$ Low
Address Setup to Write End	t_{AW}	A0–A13, $\overline{\text{DMS}}$, $\overline{\text{PMS}}$ Setup before $\overline{\text{WR}}$ Deasserted
Address Hold Time	t_{WRA}	A0–A13, $\overline{\text{DMS}}$, $\overline{\text{PMS}}$ Hold after $\overline{\text{WR}}$ Deasserted
Data Setup Time	t_{DW}	Data Setup before $\overline{\text{WR}}$ High
Data Hold Time	t_{DH}	Data Hold after $\overline{\text{WR}}$ High
$\overline{\text{OE}}$ to Data Valid	t_{RDD}	$\overline{\text{RD}}$ Low to Data Valid
Address Access Time	t_{AA}	A0–A13, $\overline{\text{DMS}}$, $\overline{\text{PMS}}$, $\overline{\text{BMS}}$ to Data Valid

TIMING PARAMETERS (ADSP-2101/2105/2111/2115/2161/2163)

INTERRUPTS & FLAGS

Parameter		13 MHz Min	13 MHz Max	13.824 MHz Min	13.824 MHz Max	16.67 MHz Min	16.67 MHz Max	20 MHz Min	20 MHz Max	25 MHz Min	25 MHz Max	Frequency Dependency Min	Frequency Dependency Max	Unit
Timing Requirement:														
t_{IFS}	$\overline{IRQx}$[1] or FI Setup before CLKOUT Low[2, 3]	34.2		33.1		30		27.5		25		$0.25t_{CK}$ + 15[4]		ns
t_{IFS}	$\overline{IRQx}$[1] or FI Setup before CLKOUT Low *(ADSP-2111)*[2, 3]	37.2		36.1		33		30.5		28		$0.25t_{CK}$ + 18[4]		ns
t_{IFH}	$\overline{IRQx}$[1] or FI Hold after CLKOUT High[2, 3]	19.2		18.1		15		12.5		10		$0.25t_{CK}$		ns
Switching Characteristic:														
t_{FOH}	FO Hold after CLKOUT High[5]	0		0		0		0		0		0		ns
t_{FOD}	FO Delay from CLKOUT High		15		15		15		15		12			ns

NOTES

[1]$\overline{IRQx}$=$\overline{IRQ0}$, $\overline{IRQ1}$, and $\overline{IRQ2}$.

[2]If $\overline{IRQx}$ and FI inputs meet t_{IFS} and t_{IFH} setup/hold requirements, they will be recognized during the current clock cycle; otherwise they will be recognized during the following cycle. (Refer to the "Interrupt Controller" section in Chapter 3, Program Control, of the *ADSP-2100 Family User's Manual* for further information on interrupt servicing.)

[3]Edge-sensitive interrupts require pulse widths greater than 10 ns. Level-sensitive interrupts must be held low until serviced.

[4]t_{IFS} (min) = $0.25t_{CK}$ + 20 ns for ADSP-2101TG-50, ADSP-2101TG/883B-50, ADSP-2111TG-52, and ADSP-2111TG/883B-52 (Extended Temperature Range devices).

[5]t_{FOH} (min) = –5 ns for ADSP-2111TG-52 and ADSP-2111TG/883B-52 (Extended Temperature Range devices).

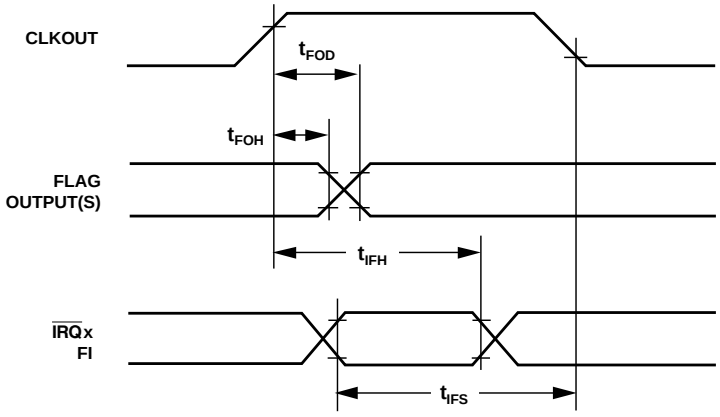


Figure 30. Interrupts & Flags

TIMING PARAMETERS (ADSP-2101/2105/2111/2115/2161/2163)

SERIAL PORTS

Parameter		12.5 MHz Min	12.5 MHz Max	13.0 MHz Min	13.0 MHz Max	13.824 MHz* Min	13.824 MHz* Max	Frequency Dependency Min	Frequency Dependency Max	Unit
Timing Requirement:										
t_{SCK}	SCLK Period	80		76.9		72.3				ns
t_{SCS}	DR/TFS/RFS Setup before SCLK Low	8		8		8				ns
t_{SCH}	DR/TFS/RFS Hold after SCLK Low	10		10		10				ns
t_{SCP}	$SCLK_{IN}$ Width	30		28		28				ns
Switching Characteristic:										
t_{CC}	CLKOUT High to $SCLK_{OUT}$	20	35	19.2	34.2	18.1	33.1	$0.25t_{CK}$	$0.25t_{CK}$ + 15ns	
t_{SCDE}	SCLK High to DT Enable	0		0		0				ns
t_{SCDV}	SCLK High to DT Valid		20		20		20			ns
t_{RH}	TFS/RFS_{OUT} Hold after SCLK High	0		0		0				ns
t_{RD}	TFS/RFS_{OUT} Delay from SCLK High		20		20		20			ns
t_{SCDH}	DT Hold after SCLK High	0		0		0				ns
t_{TDE}	TFS (Alt) to DT Enable	0		0		0				ns
t_{TDV}	TFS (Alt) to DT Valid		18		18		18			ns
t_{SCDD}	SCLK High to DT Disable		25		25		25			ns
t_{RDV}	RFS (Multichannel, Frame Delay Zero) to DT Valid		20		20		20			ns

*Maximum serial port operating frequency is 13.824 MHz for all processor speed grades except the 12.5 MHz ADSP-2101 and 13.0 MHz ADSP-2111.

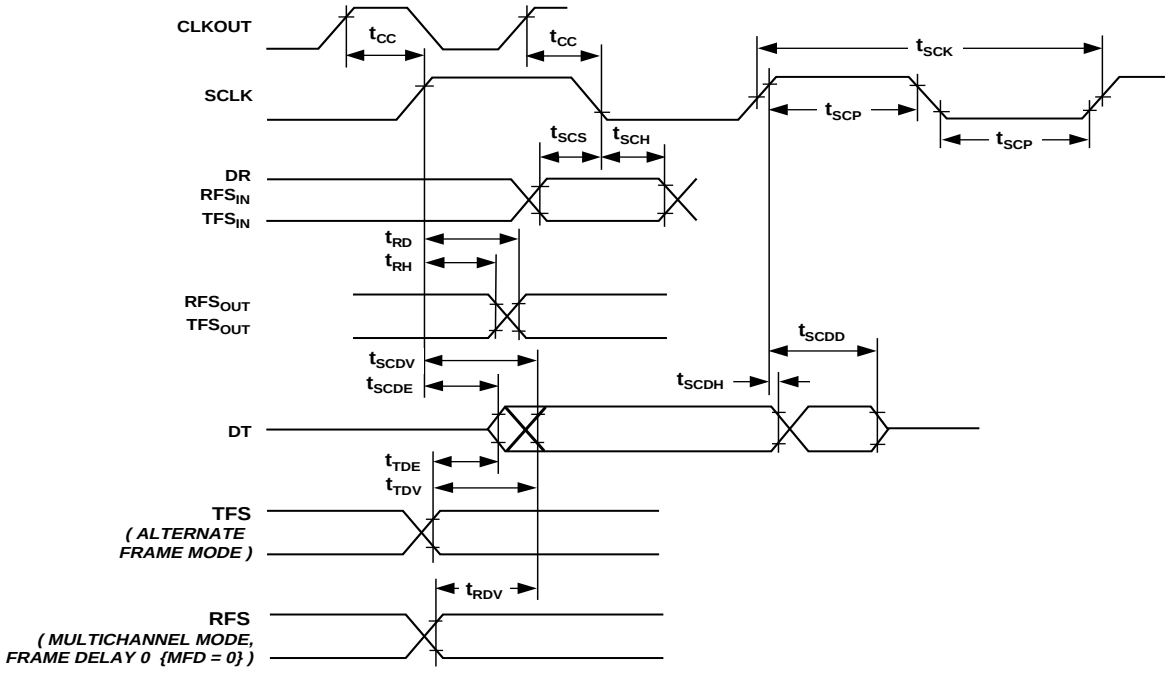


Figure 34. Serial Ports

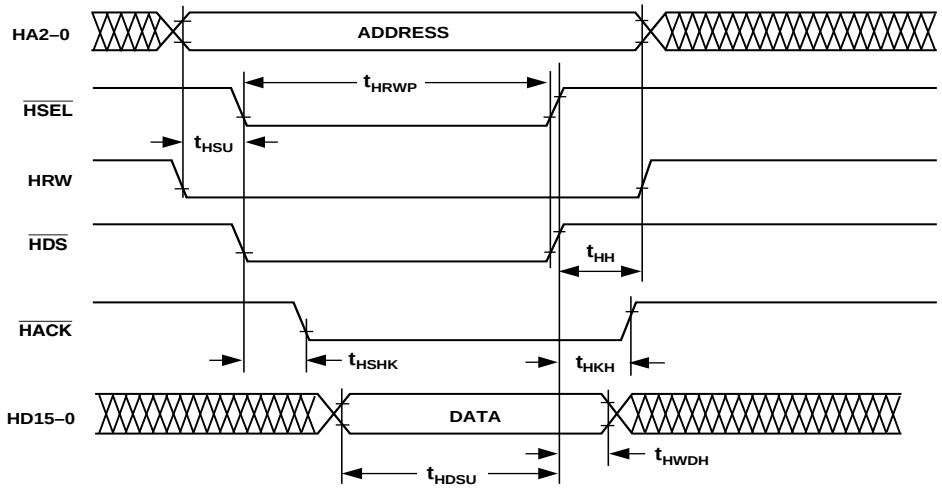
TIMING PARAMETERS (ADSP-2111)

HOST INTERFACE PORT
Separate Data & Address (HMD1 = 0)
Read Strobe & Write Strobe (HMD0 = 0)

Parameter	13.0 MHz Min	13.0 MHz Max	16.67 MHz Min	16.67 MHz Max	20 MHz Min	20 MHz Max	*No Frequency Dependency*	Unit
Timing Requirement:								
t_{HSU} HA2-0 Setup before Start of Write or Read[1, 2]	8		8		8			ns
t_{HDSU} Data Setup before End of Write[3]	8		8		8			ns
t_{HWDH} Data Hold after End of Write[3]	3		3		3			ns
t_{HH} HA2-0 Hold after End of Write or Read[3, 4]	3		3		3			ns
t_{HRWP} Read or Write Pulse Width[5]	30		30		30			ns
Switching Characteristic:								
t_{HSHK} $\overline{\text{HACK}}$ Low after Start of Write or Read[1, 2]	0	20	0	20	0	20		ns
t_{HKH} $\overline{\text{HACK}}$ Hold after End of Write or Read[3, 4]	0	20	0	20	0	20		ns
t_{HDE} Data Enabled after Start of Read[2]	0		0		0			ns
t_{HDD} Data Valid after Start of Read[2]		23		23		23		ns
t_{HRDH} Data Hold after End of Read[4]	0		0		0			ns
t_{HRDD} Data Disabled after End of Read[4]		10		10		10		ns

NOTES
[1]Start of Write = $\overline{\text{HWR}}$ Low and $\overline{\text{HSEL}}$ Low.
[2]Start of Read = $\overline{\text{HRD}}$ Low and $\overline{\text{HSEL}}$ Low.
[3]End of Write = $\overline{\text{HWR}}$ High or $\overline{\text{HSEL}}$ High.
[4]End of Read = $\overline{\text{HRD}}$ High or $\overline{\text{HSEL}}$ High.
[5]Read Pulse Width = $\overline{\text{HRD}}$ Low and $\overline{\text{HSEL}}$ Low, Write Pulse Width = $\overline{\text{HWR}}$ Low and $\overline{\text{HSEL}}$ Low.

Host Write Cycle



Host Read Cycle

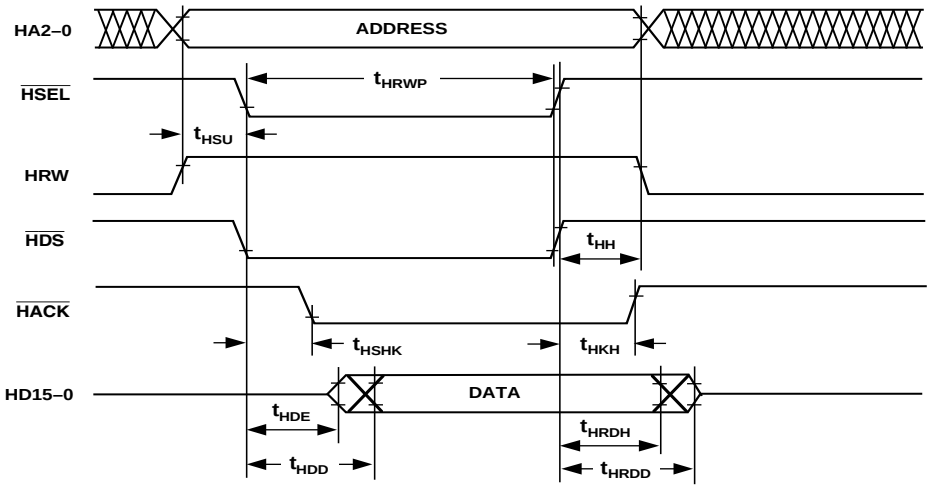


Figure 36. Host Interface Port (HMD1 = 0, HMD0 =1)

TIMING PARAMETERS (ADSP-2111)

HOST INTERFACE PORT
Multiplexed Data & Address (HMD1 = 1)
Read Strobe & Write Strobe (HMD0 = 0)

Parameter	13.0 MHz Min	13.0 MHz Max	16.67 MHz Min	16.67 MHz Max	20 MHz Min	20 MHz Max	*No Frequency Dependency*	Unit
Timing Requirement:								
t_{HALP} ALE Pulse Width	15		15		15			ns
t_{HASU} HAD15-0 Address Setup before ALE Low	5		5		5			ns
t_{HAH} HAD15-0 Address Hold after ALE Low	2		2		2			ns
t_{HALS} Start of Write or Read after ALE Low[1, 2]	15		15		15			ns
t_{HDSU} HAD15-0 Data Setup before End of Write[3]	8		8		8			ns
t_{HWDH} HAD15-0 Data Hold after End of Write[3]	3		3		3			ns
t_{HRWP} Read or Write Pulse Width[5]	30		30		30			ns
Switching Characteristic:								
t_{HSHK} $\overline{HACK}$ Low after Start of Write or Read[1, 2]	0	20	0	20	0	20		ns
t_{HKH} $\overline{HACK}$ Hold after End of Write or Read[3, 4]	0	20	0	20	0	20		ns
t_{HDE} HAD15-0 Data Enabled after Start of Read[2]	0		0		0			ns
t_{HDD} HAD15-0 Data Valid after Start of Read[2]		23		23		23		ns
t_{HRDH} HAD15-0 Data Hold after End of Read[4]	0		0		0			ns
t_{HRDD} HAD15-0 Data Disabled after End of Read[4]		10		10		10		ns

NOTES
[1]Start of Write = $\overline{HWR}$ Low and $\overline{HSEL}$ Low.
[2]Start of Read = $\overline{HRD}$ Low and $\overline{HSEL}$ Low.
[3]End of Write = $\overline{HWR}$ High or $\overline{HSEL}$ High.
[4]End of Read = $\overline{HRD}$ High or $\overline{HSEL}$ High.
[5]Read Pulse Width = $\overline{HRD}$ Low and $\overline{HSEL}$ Low, Write Pulse Width = $\overline{HWR}$ Low and $\overline{HSEL}$ Low.

Host Write Cycle

Host Read Cycle

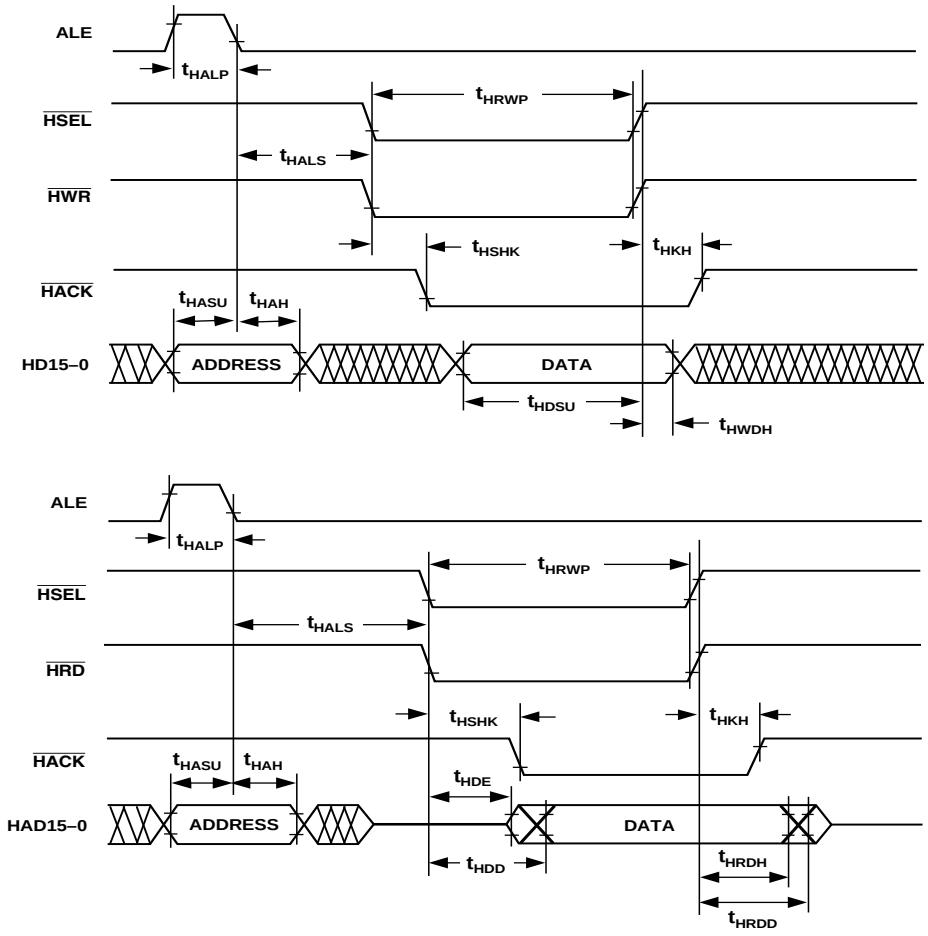


Figure 37. Host Interface Port (HMD1 = 1, HMD0 = 0)

TIMING PARAMETERS (ADSP-2103/2162/2164)

CLOCK SIGNALS & RESET

Parameter		10.24 MHz Min	10.24 MHz Max	Frequency Dependency Min	Frequency Dependency Max	Unit
Timing Requirement:						
t_{CK}	CLKIN Period	97.6	150			ns
t_{CKL}	CLKIN Width Low	20				ns
t_{CKH}	CLKIN Width High	20				ns
t_{RSP}	$\overline{\text{RESET}}$ Width Low	488		$5t_{CK}$[1]		ns
Switching Characteristic:						
t_{CPL}	CLKOUT Width Low	38.8		$0.5t_{CK} - 10$		ns
t_{CPH}	CLKOUT Width High	38.8		$0.5t_{CK} - 10$		ns
t_{CKOH}	CLKIN High to CLKOUT High	0	20			ns

NOTES
[1]Applies after powerup sequence is complete. Internal phase lock loop requires no more than 2000 CLKIN cycles assuming stable CLKIN (not including crystal oscillator startup time).

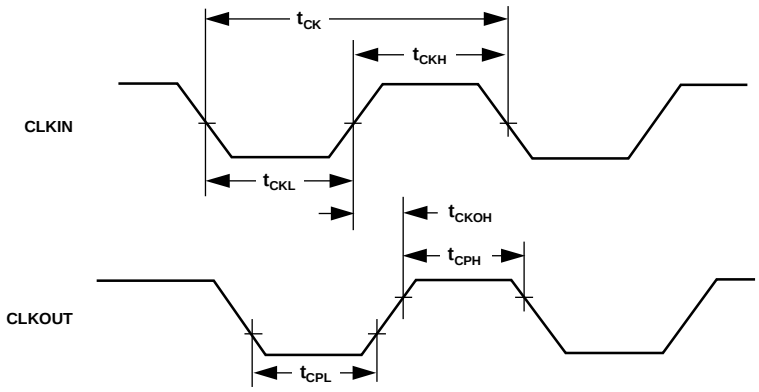
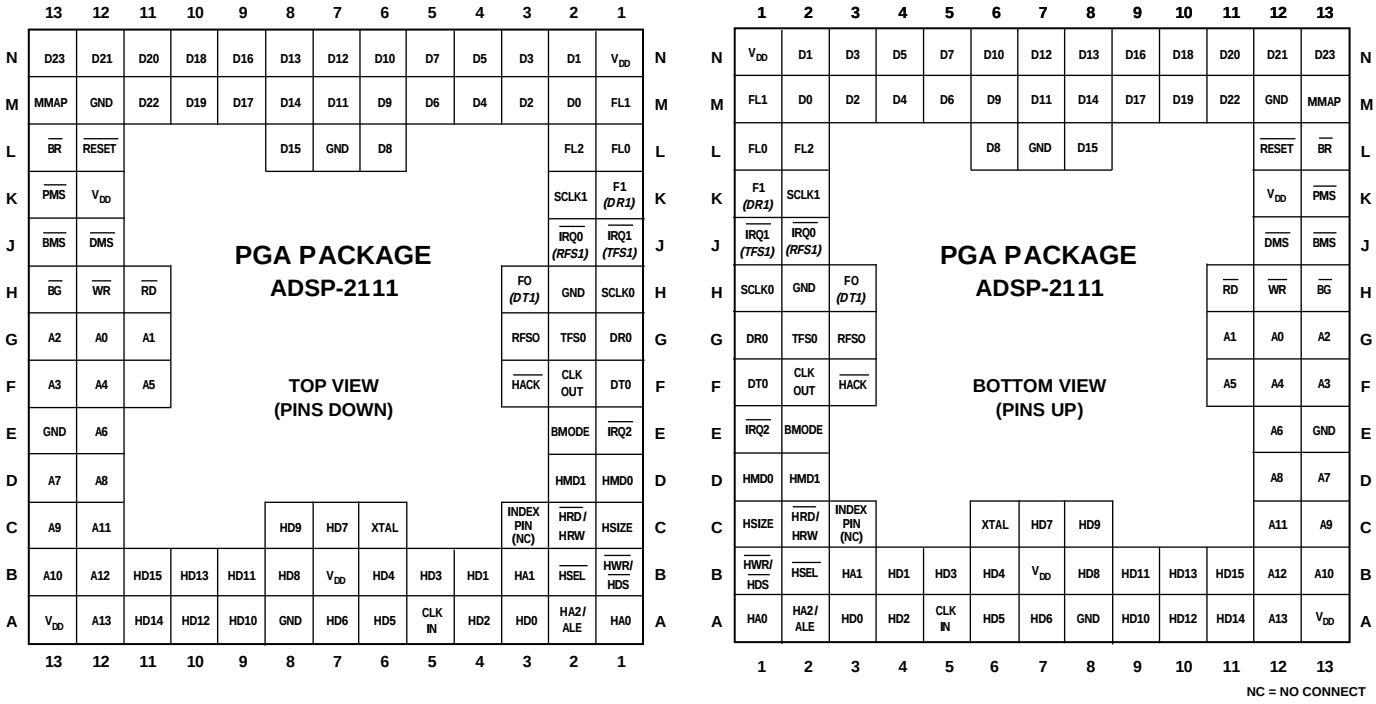


Figure 39. Clock Signals

PIN CONFIGURATIONS

100-Pin PGA



PGA Number	Pin Name
N13	D23
N12	D21
M13	MMAP
M12	GND
L13	$\overline{BR}$
L12	$\overline{RESET}$
K13	$\overline{PMS}$
K12	V_{DD}
J13	$\overline{BMS}$
J12	$\overline{DMS}$
H13	$\overline{BG}$
H12	$\overline{WR}$
H11	$\overline{RD}$
G13	A2
G12	A0
G11	A1
F13	A3
F12	A4
F11	A5
E13	GND
E12	A6
D13	A7
D12	A8
C13	A9
C12	A11

PGA Number	Pin Name
B13	A10
A13	V_{DD}
A12	A13
B12	A12
A11	HD14
B11	HD15
A10	HD12
B10	HD13
A9	HD10
B9	HD11
A8	GND
B8	HD8
C8	HD9
A7	HD6
B7	V_{DD}
C7	HD7
A6	HD5
B6	HD4
C6	XTAL
A5	CLKIN
B5	HD3
A4	HD2
B4	HD1
A3	HD0
B3	HA1

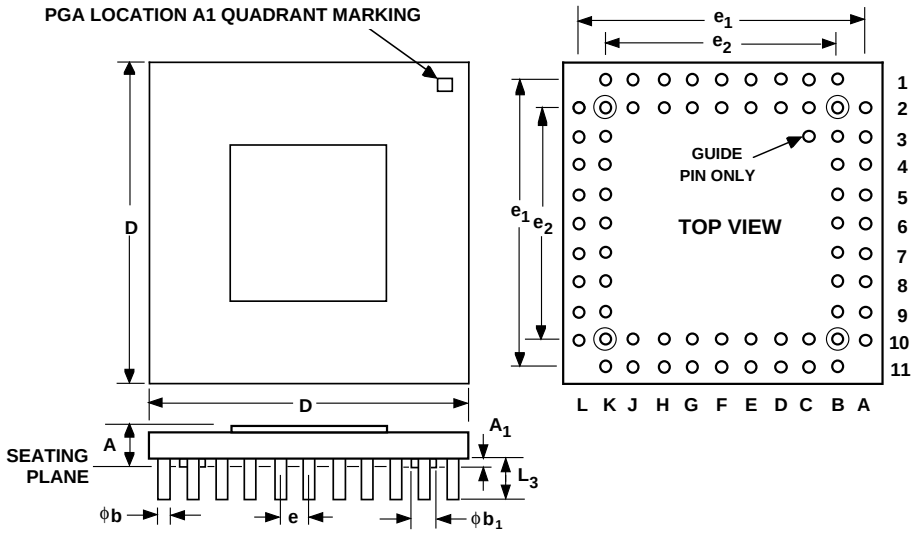
PGA Number	Pin Name
C3	Index (NC)
A2	HA2/ALE
A1	HA0
B1	$\overline{HWR}$/$\overline{HDS}$
B2	$\overline{HSEL}$
C1	HSIZE
C2	$\overline{HRD}$/HRW
D1	HMD0
D2	HMD1
E1	$\overline{IRQ2}$
E2	BMODE
F1	DT0
F2	CLKOUT
F3	$\overline{HACK}$
G1	DR0
G2	TFS0
G3	RFS0
H1	SCLK0
H2	GND
H3	FO *(DT1)*
J1	$\overline{IRQ1}$ *(TFS1)*
J2	$\overline{IRQ0}$ *(RFS1)*
K1	FI *(DR1)*
K2	SCLK1
L1	FL0

PGA Number	Pin Name
L2	FL2
M1	FL1
N1	V_{DD}
N2	D1
M2	D0
N3	D3
M3	D2
N4	D5
M4	D4
N5	D7
M5	D6
N6	D10
M6	D9
L6	D8
N7	D12
M7	D11
L7	GND
N8	D13
M8	D14
L8	D15
N9	D16
M9	D17
N10	D18
M10	D19
N11	D20
M11	D22

OUTLINE DIMENSIONS

ADSP-2101

68-Pin Grid Array (PGA)

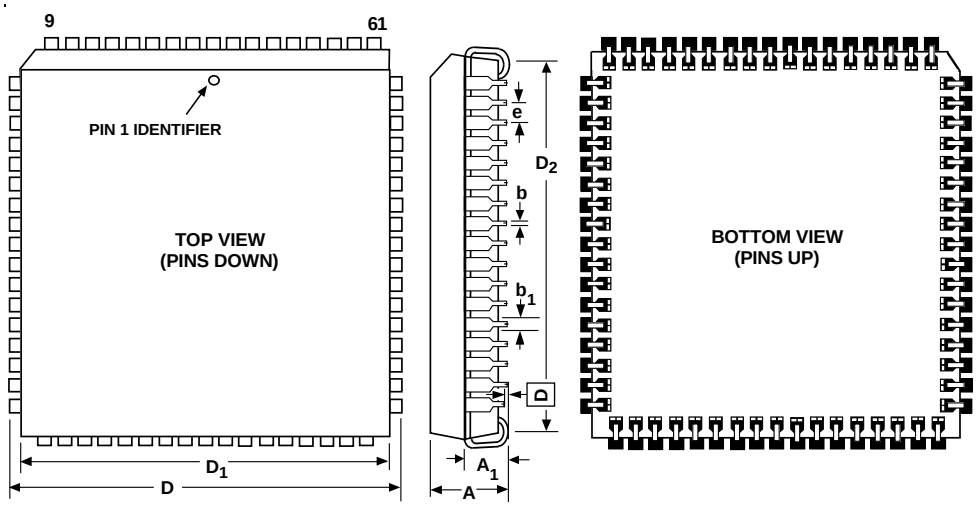


SYMBOL	INCHES			MILLIMETERS		
	MIN	TYP	MAX	MIN	TYP	MAX
A	0.123		0.164	3.12		4.17
A_1		0.50			1.27	
ϕb	0.016	0.018	0.020		0.46	
ϕb_1		0.050			1.27	
D	1.086		1.110	27.58		28.19
e_1	0.988		1.012	25.10		25.70
e_2	0.788		0.812	20.02		20.62
e		0.100			2.54	
L_3		0.180			4.57	

OUTLINE DIMENSIONS

ADSP-21xx

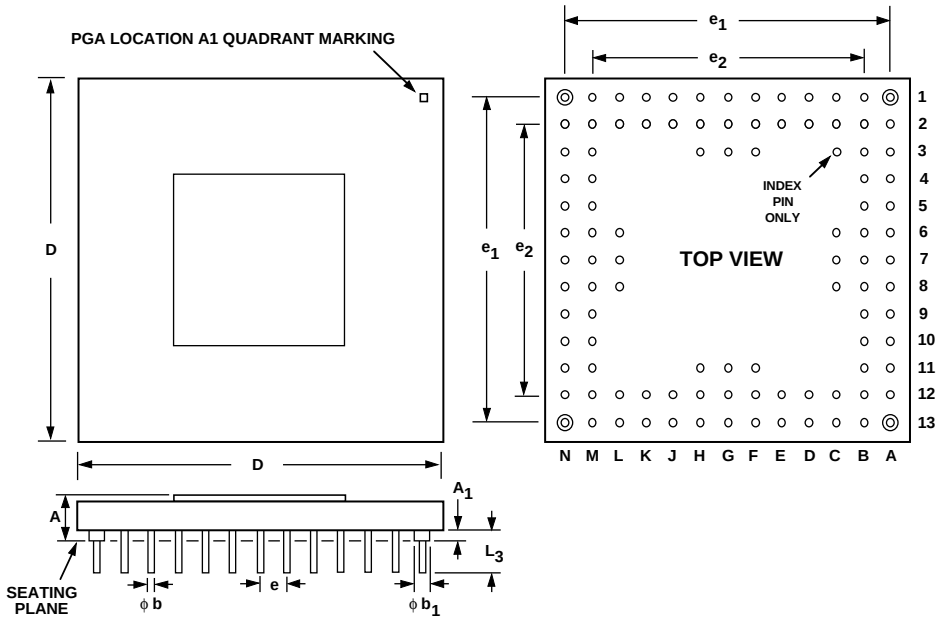
68-Lead Plastic Leaded Chip Carrier (PLCC)



SYMBOL	INCHES			MILLIMETERS		
	MIN	TYP	MAX	MIN	TYP	MAX
A	0.169	0.172	0.175	4.29	4.37	4.45
A_1		0.104			2.64	
b	0.017	0.018	0.019	0.43	0.46	0.48
b_1	0.027	0.028	0.029	0.69	0.71	0.74
D	0.985	0.990	0.995	25.02	25.15	25.27
D_1	0.950	0.952	0.954	24.13	24.18	24.23
D_2	0.895	0.910	0.925	22.73	23.11	23.50
e		0.050			1.27	
D			0.004			0.10

OUTLINE DIMENSIONS

ADSP-2111
100-Pin Grid Array (PGA)



	INCHES			MILLIMETERS		
SYMBOL	MIN	TYP	MAX	MIN	TYP	MAX
A	0.123		0.169	3.12		4.29
A_1		0.050			1.27	
ϕb	0.016	0.018	0.020	0.41	0.46	0.51
ϕb_1		0.050			1.27	
D	1.308	1.32	1.342	33.22	33.53	34.09
e_1	1.188	1.20	1.212	30.18	30.48	30.78
e_2	0.988	1.00	1.012	25.10	25.4	25.70
e		0.100			2.54	
L_3		0.180			4.57	