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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	740
Core Size	8-Bit
Speed	10MHz
Connectivity	SIO, UART/USART
Peripherals	LCD, WDT
Number of I/O	49
Program Memory Size	32KB (32K x 8)
Program Memory Type	QzROM
EEPROM Size	-
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External, Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-BQFP
Supplier Device Package	80-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m38238g8fp-u0

3823 Group

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

REJ03B0146-0202
Rev.2.02
Jun.19.2007

DESCRIPTION

The 3823 group is the 8-bit microcomputer based on the 740 family core technology.

The 3823 group has the LCD drive control circuit, an 8-channel A/D converter, a serial interface, a watchdog timer, a ROM correction function, and as additional functions.

The various microcomputers in the 3823 group include variations of internal memory size and packaging. For details, refer to the section on part numbering.

FEATURES

- Basic machine-language instructions 71
- The minimum instruction execution time ..... 0.4 µs
  (at f(XIN) = 10 MHz, High-speed mode)
- Memory size
  ROM ..... 16 K to 60 K bytes
  RAM ..... 640 to 2560 bytes
- ROM correction function ..... 32 bytes × 2 blocks
- Watchdog timer ..... 8-bit × 1
- Programmable input/output ports 49
- Input ports 5
- Software pull-up/pull-down resistors (Ports P0-P7 except port $P4_0$)
- Interrupts ..... 17 sources, 16 vectors
  (includes key input interrupt)
- Key Input Interrupt (Key-on Wake-Up) 8
- Timers ..... 8-bit × 3, 16-bit × 2
- Serial interface ..... 8-bit × 1 (UART or Clock-synchronized)
- A/D converter ..... 10-bit × 8 channels or 8-bit × 8 channels
- LCD drive control circuit
  Bias 1/2, 1/3
  Duty 1/2, 1/3, 1/4
  Common output 4
  Segment output 32
- Main clock generating circuits ..... Built-in feedback resistor
  (connect to external ceramic resonator or quartz-crystal oscillator)
- Sub-clock generating circuits
  (connect to external quartz-crystal oscillator or on-chip oscillator)
- Power source voltage
  In frequency/2 mode (f(XIN) ≤ 10 MHz) ..... 4.5 to 5.5 V
  In frequency/2 mode (f(XIN) ≤ 8 MHz) ..... 4.0 to 5.5 V
  In frequency/4 mode (f(XIN) ≤ 10 MHz) ..... 2.5 to 5.5 V
  In frequency/4 mode (f(XIN) ≤ 8 MHz) ..... 2.0 to 5.5 V
  In frequency/4 mode (f(XIN) ≤ 5 MHz) ..... 1.8 to 5.5 V
  In frequency/8 mode (f(XIN) ≤ 10 MHz) ..... 2.5 to 5.5 V
  In frequency/8 mode (f(XIN) ≤ 8 MHz) ..... 2.0 to 5.5 V
  In frequency/8 mode (f(XIN) ≤ 5 MHz) ..... 1.8 to 5.5 V
  In low-speed mode ..... 1.8 to 5.5 V
- Power dissipation
  In frequency/2 mode ..... 18 mW (std.)
  (at f(XIN) = 8 MHz, Vcc = 5 V, Ta = 25 °C)
  In low-speed mode at XCIN ..... 18 µW (std.)
  (at f(XIN) stopped, f(XCIN) = 32 kHz, Vcc = 2.5 V, Ta = 25 °C)
  In low-speed mode at on-chip oscillator ..... 35 µW (std.)
  (at f(XIN) stopped, f(XCIN) = stopped, Vcc = 2.5 V, Ta = 25 °C)
- Operating temperature range ..... – 20 to 85 °C

APPLICATIONS

Camera, audio equipment, household appliances, consumer electronics, etc.

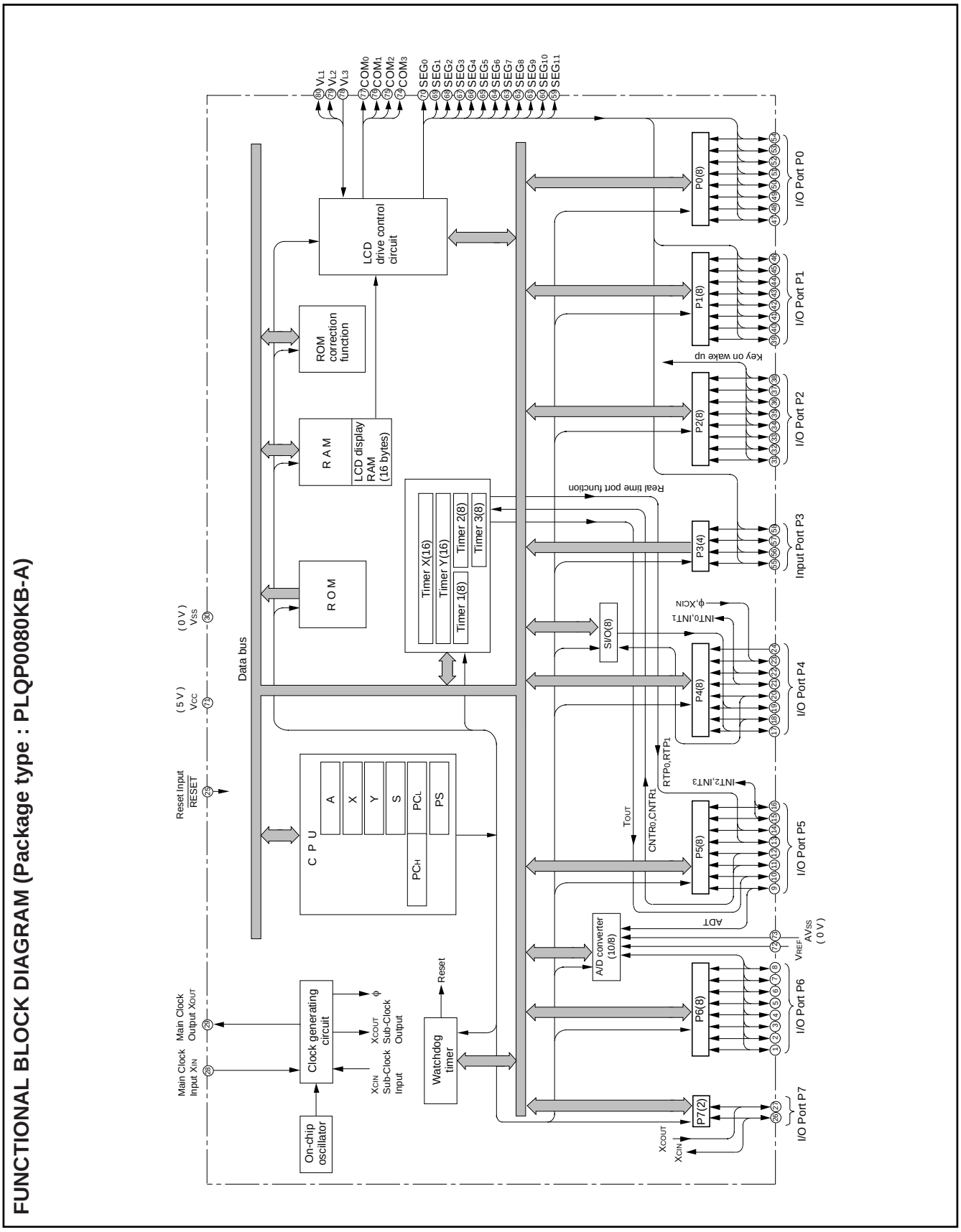


Fig. 3 Functional block diagram

Table 3 Pin description (2)

Pin	Name	Function	Function except a port function
$P4_0$	Input port P4	•1-bit Input port. •CMOS compatible input level.	•QzROM program power pin
$P4_1/\phi$	I/O port P4	•7-bit I/O port. •CMOS compatible input level. •CMOS 3-state output structure. •I/O direction register allows each pin to be individually programmed as either input or output. •Pull-up control is enabled.	•ϕ clock output pin
$P4_2/INT_0$, $P4_3/INT_1$			•Interrupt input pins
$P4_4/RxD$, $P4_5/TxD$, $P4_6/SCLK$, $P4_7/SRDY/SOUT$			•Serial interface function pins
$P5_0/INT_2$, $P5_1/INT_3$	I/O port P5	•8-bit I/O port. •CMOS compatible input level. •CMOS 3-state output structure. •I/O direction register allows each pin to be individually programmed as either input or output. •Pull-up control is enabled.	•Interrupt input pins
$P5_2/RTP_0$, $P5_3/RTP_1$			•Real time port function pins
$P5_4/CNTR_0$, $P5_5/CNTR_1$			•Timer X, Y function pins
$P5_6/TOUT$			•Timer 2 output pins
$P5_7/ADT$			•A/D trigger input pins
$P6_0/AN_0$–$P6_7/AN_7$	I/O port P6	•8-bit I/O port. •CMOS compatible input level. •CMOS 3-state output structure. •I/O direction register allows each pin to be individually programmed as either input or output. •Pull-up control is enabled.	•A/D conversion input pins
$P7_0/XCOUT$, $P7_1/XCIN$	I/O port P7	•2-bit I/O port. •CMOS compatible input level. •CMOS 3-state output structure. •I/O direction register allows each pin to be individually programmed as either input or output. •Pull-up control is enabled.	•Sub-clock generating circuit I/O pins. (Connect a resonator. External clock cannot be used.)

PART NUMBERING

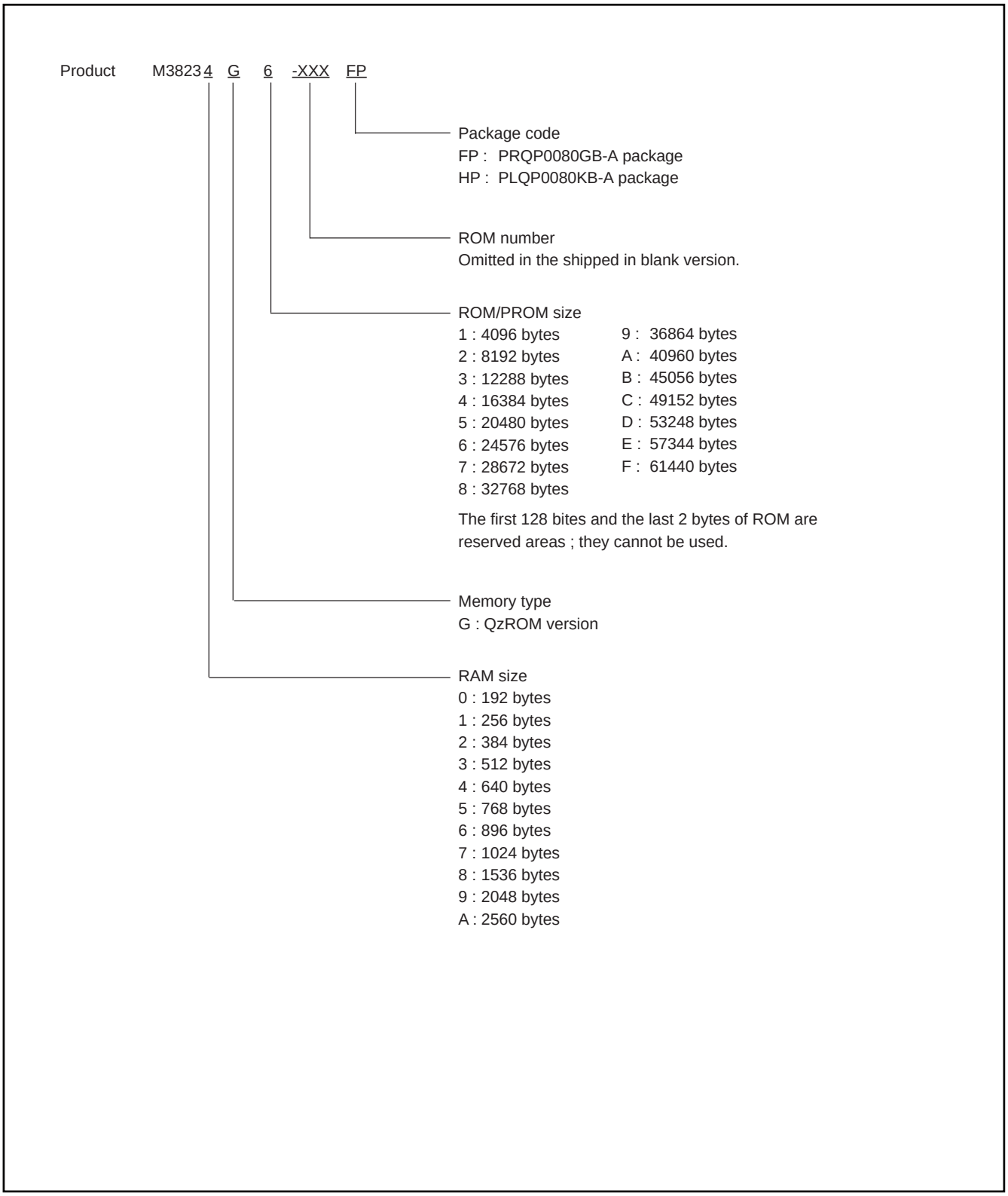


Fig. 4 Part numbering

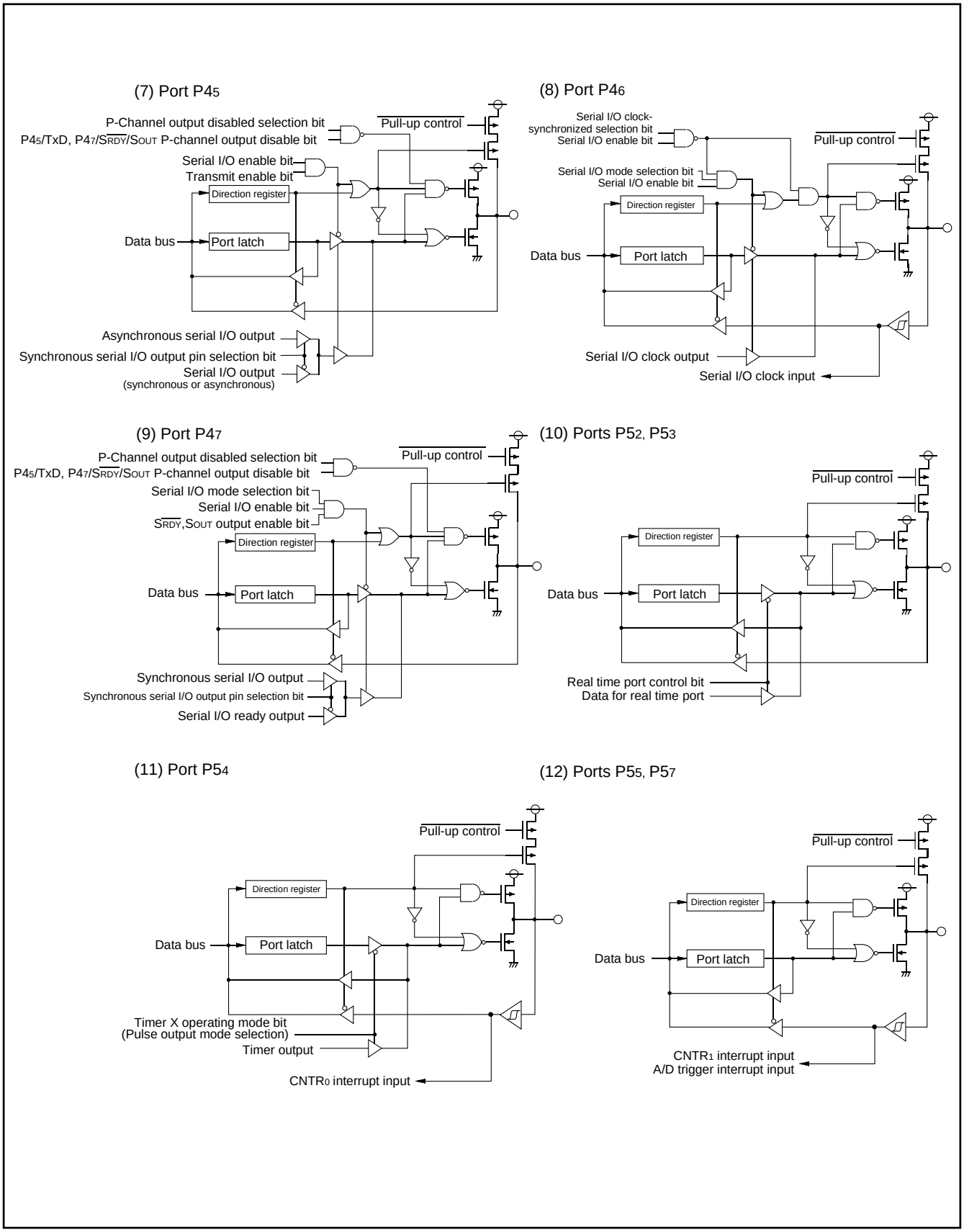


Fig. 14 Port block diagram (2)

Termination of unused pins

• Termination of common pins

I/O ports: Select an input port or an output port and follow each processing method.

Output ports: Open.

Input ports: If the input level become unstable, through current flow to an input circuit, and the power supply current may increase.

Especially, when expecting low consumption current (at STP or WIT instruction execution etc.), pull-up or pull-down input ports to prevent through current (built-in resistor can be used). Pull-down the $P4_0$/(V_{PP}) pin.

We recommend processing unused pins through a resistor which can secure $I_{OH(avg)}$ or $I_{OL(avg)}$.

Because, when an I/O port or a pin which have an output function is selected as an input port, it may operate as an output port by incorrect operation etc.

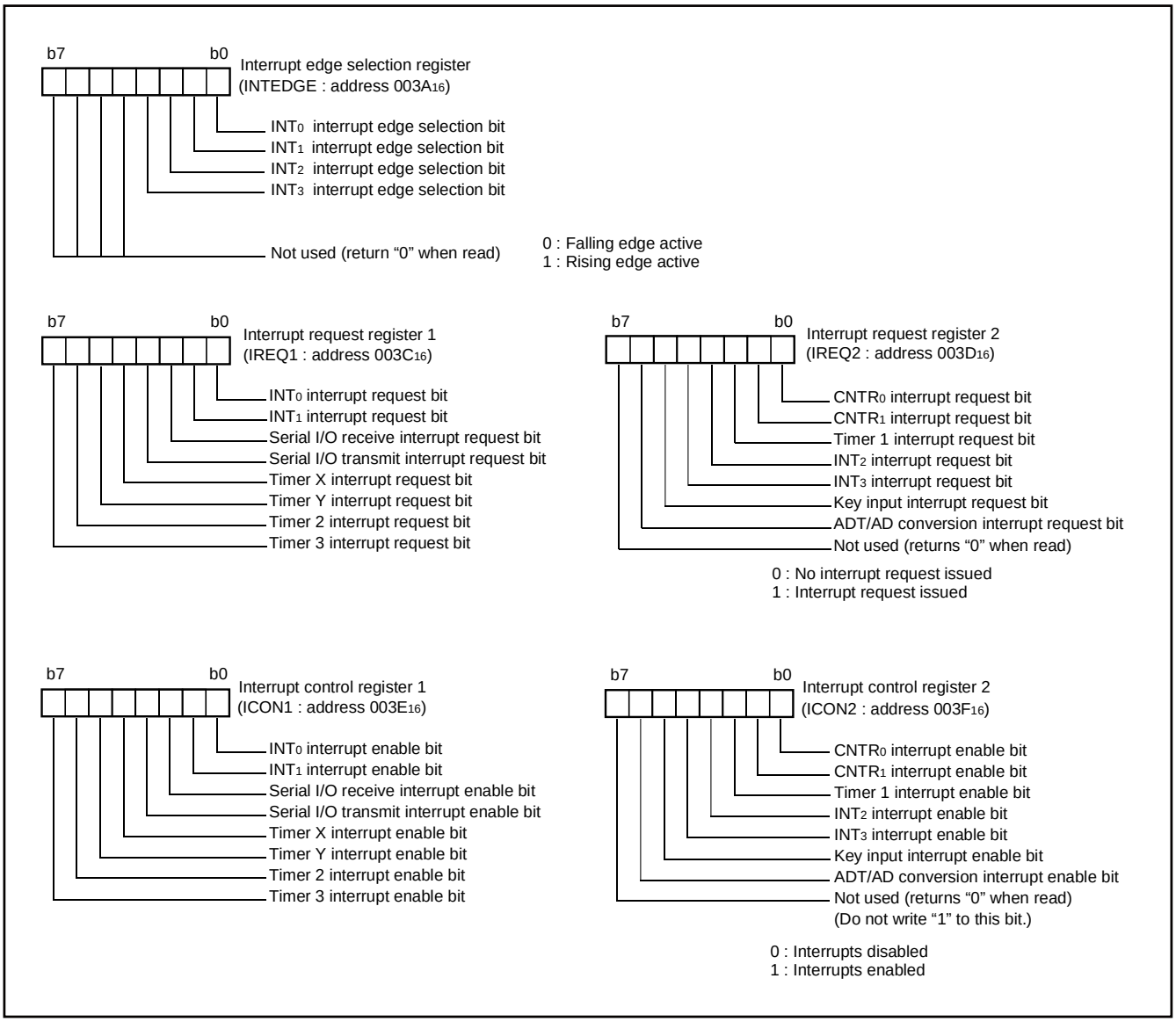


Fig. 17 Structure of interrupt-related registers

SERIAL INTERFACE
Serial I/O

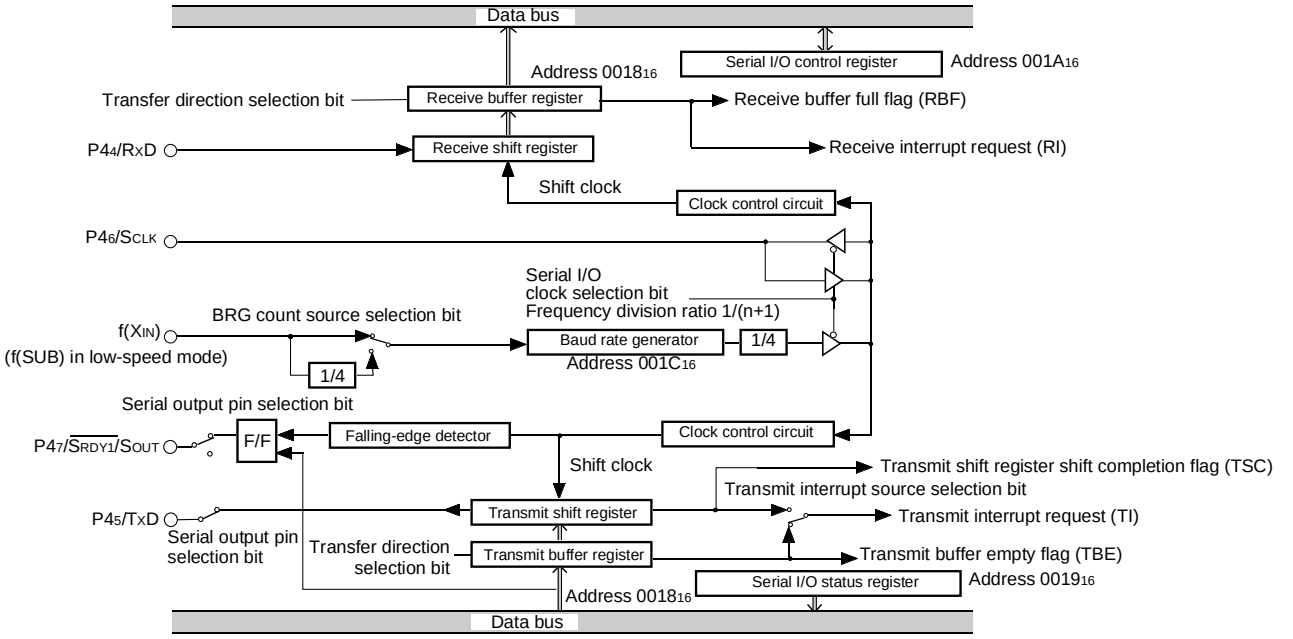
Serial I/O can be used as either clock synchronous or asynchronous (UART) serial I/O. A dedicated timer (baud rate generator) is also provided for baud rate generation.

(1) Clock Synchronous Serial I/O Mode

Clock synchronous serial I/O can be selected by setting the mode selection bit of the serial I/O control register to “1”.

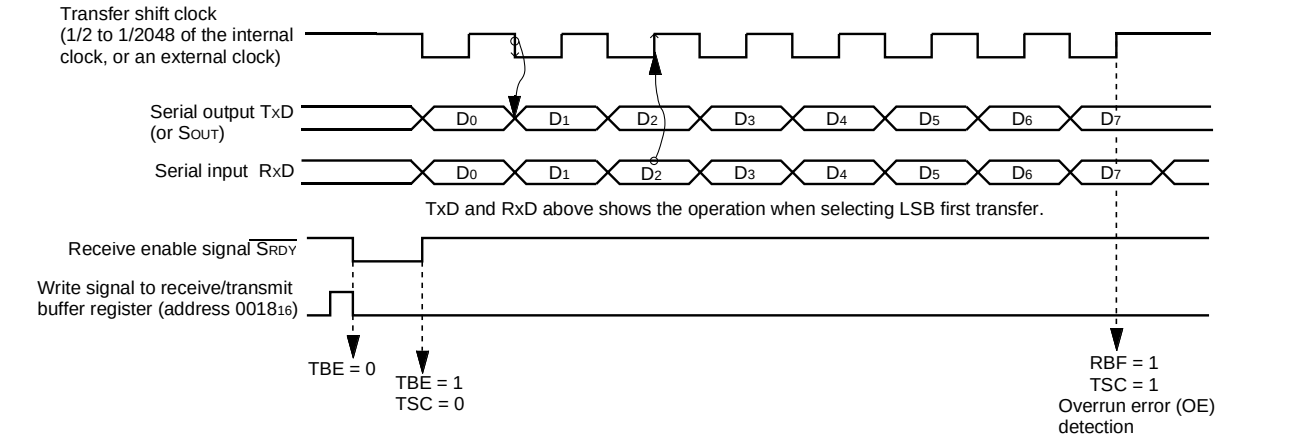
For clock synchronous serial I/O, the transmitter and the receiver must use the same clock. If an internal clock is used, transfer is started by a write signal to the transmit/receive buffer register.

The MSB first transfer is selected as the transfer direction by setting the bit 0 in the peripheral function expansion register to “1”. Also, the synchronous serial I/O output switches to the P47/SRDY/SOUT pin by setting the bit 1 in the peripheral function expansion register to “1”.



Note: f(SUB) is the source oscillation frequency in low-speed mode. f(SUB) shows the oscillation frequency of XCIN or the on-chip oscillator.

Fig. 26 Block diagram of clock synchronous serial I/O



Notes
1 : The transmit interrupt (TI) can be generated either when the transmit buffer register has emptied (TBE=1) or after the transmit shift operation has ended (TSC=1), by setting the transmit interrupt source selection bit (TIC) of the serial I/O control register.
2 : If data is written to the transmit buffer register when TSC=0, the transmit clock is generated continuously and serial data is output continuously from the TxD pin.
3 : The receive interrupt (RI) is set when the receive buffer full flag (RBF) becomes “1” .

Fig. 27 Operation of clock synchronous serial I/O function

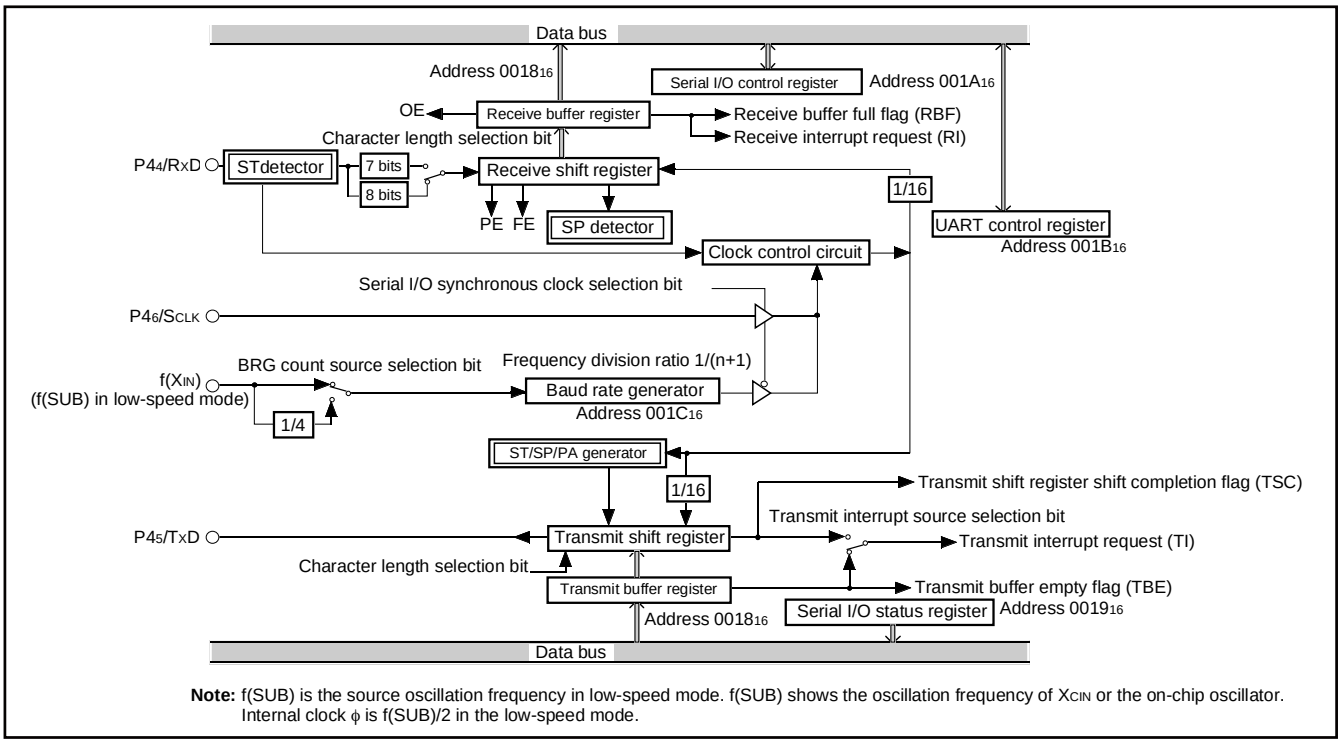
(2) Asynchronous Serial I/O (UART) Mode

Clock asynchronous serial I/O mode (UART) can be selected by clearing the serial I/O mode selection bit of the serial I/O control register to “0”.

Eight serial data transfer formats can be selected, and the transfer formats used by a transmitter and receiver must be identical.

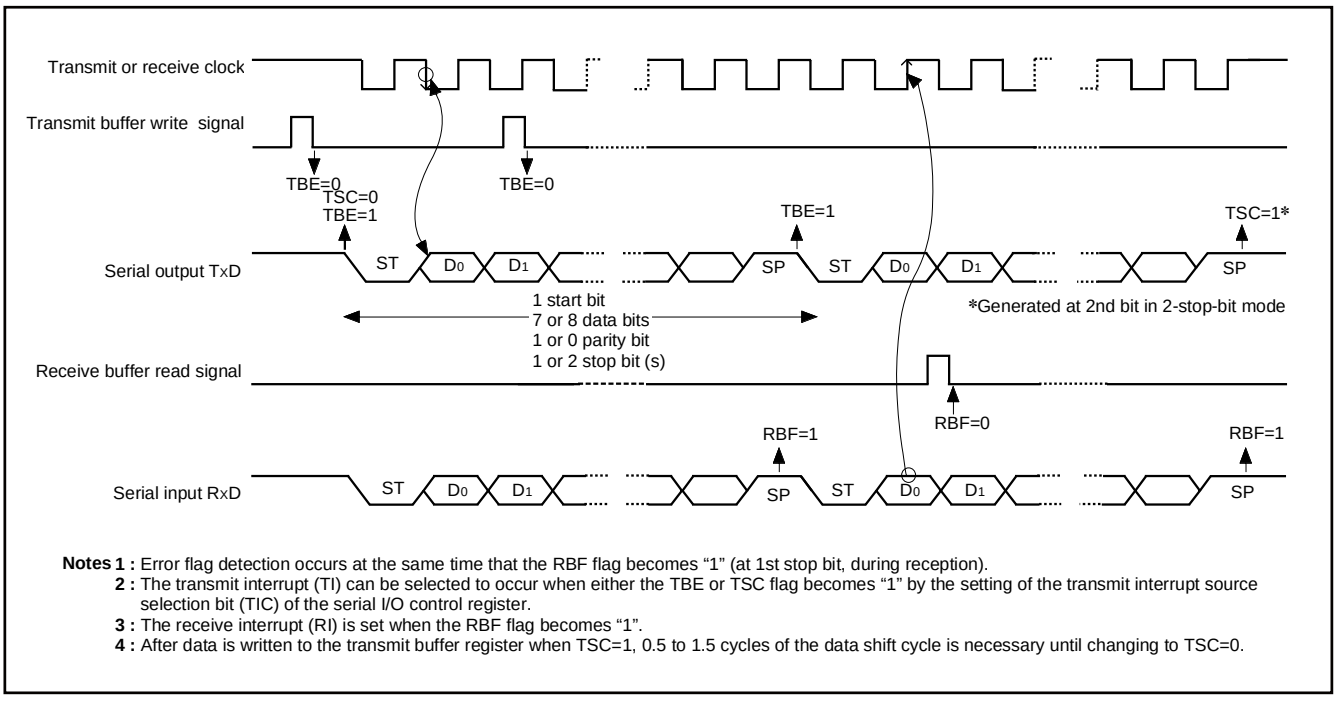
The transmit and receive shift registers each have a buffer register, but the two buffers have the same address in memory. Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer, and receive data is read from the receive buffer.

The transmit buffer can also hold the next data to be transmitted, and the receive buffer register can hold a character while the next character is being received.



Note: f(SUB) is the source oscillation frequency in low-speed mode. f(SUB) shows the oscillation frequency of XCIN or the on-chip oscillator. Internal clock ϕ is f(SUB)/2 in the low-speed mode.

Fig. 28 Block diagram of UART serial I/O



Notes 1 : Error flag detection occurs at the same time that the RBF flag becomes “1” (at 1st stop bit, during reception).
2 : The transmit interrupt (TI) can be selected to occur when either the TBE or TSC flag becomes “1” by the setting of the transmit interrupt source selection bit (TIC) of the serial I/O control register.
3 : The receive interrupt (RI) is set when the RBF flag becomes “1”.
4 : After data is written to the transmit buffer register when TSC=1, 0.5 to 1.5 cycles of the data shift cycle is necessary until changing to TSC=0.

Fig. 29 Operation of UART serial I/O function

[Transmit Buffer/Receive Buffer Register (TB/RB)] 0018$_{16}$

The transmit buffer register and the receive buffer register are located at the same address. The transmit buffer register is write-only and the receive buffer register is read-only. If a character bit length is 7 bits, the MSB of data stored in the receive buffer register is “0”.

[Serial I/O Status Register (SIOSTS)] 0019$_{16}$

The read-only serial I/O status register consists of seven flags (bits 0 to 6) which indicate the operating status of the serial I/O function and various errors.

Three of the flags (bits 4 to 6) are valid only in UART mode.

The receive buffer full flag (bit 1) is cleared to “0” when the receive buffer is read.

If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer register, and the receive buffer full flag is set. A write to the serial I/O status register clears all the error flags OE, PE, FE, and SE. Writing “0” to the serial I/O enable bit (SIOE) also clears all the status flags, including the error flags.

All bits of the serial I/O status register are initialized to “0” at reset, but if the transmit enable bit (bit 4) of the serial I/O control register has been set to “1”, the transmit shift register shift completion flag (bit 2) and the transmit buffer empty flag (bit 0) become “1”.

[Serial I/O Control Register (SIOCON)] 001A$_{16}$

The serial I/O control register contains eight control bits for the serial I/O function.

[UART Control Register (UARTCON)]001B$_{16}$

The UART control register consists of four control bits (bits 0 to 3) which are valid when asynchronous serial I/O is selected and set the data format of an data transfer. One bit in this register (bit 4) is always valid and sets the output structure of the P4$_5$/TxD pin.

[Baud Rate Generator (BRG)] 001C$_{16}$

The baud rate generator determines the baud rate for serial transfer.

The baud rate generator divides the frequency of the count source by 1/(n + 1), where n is the value written to the baud rate generator.

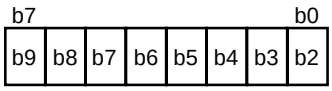
■Notes on serial I/O

When setting the transmit enable bit to “1”, the serial I/O transmit interrupt request bit is automatically set to “1”. When not requiring the interrupt occurrence synchronized with the transmission enalbed, take the following sequence.

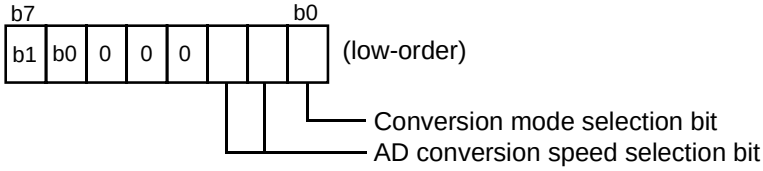
①Set the serial I/O transmit interrupt enable bit to “0” (disabled).
②Set the transmit enable bit to “1”.
③Set the serial I/O transmit interrupt request bit to “0” after 1 or more instructions have been executed.
④Set the serial I/O transmit interrupt enable bit to “1” (enabled).

• 10 bit reading (Read address 0035$_{16}$ before 0036$_{16}$)

AD conversion high-order register (Address 0035$_{16}$) ADH



AD conversion low-order register (Address 0036$_{16}$) ADL



Note: The bit 5 to bit 3 of address 0036$_{16}$ become "0" at reading.

• 8 bit reading (Read only address 0035$_{16}$)

(Address 0035$_{16}$)

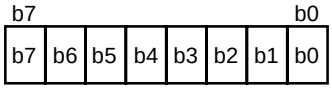


Fig. 34 A/D conversion register reading

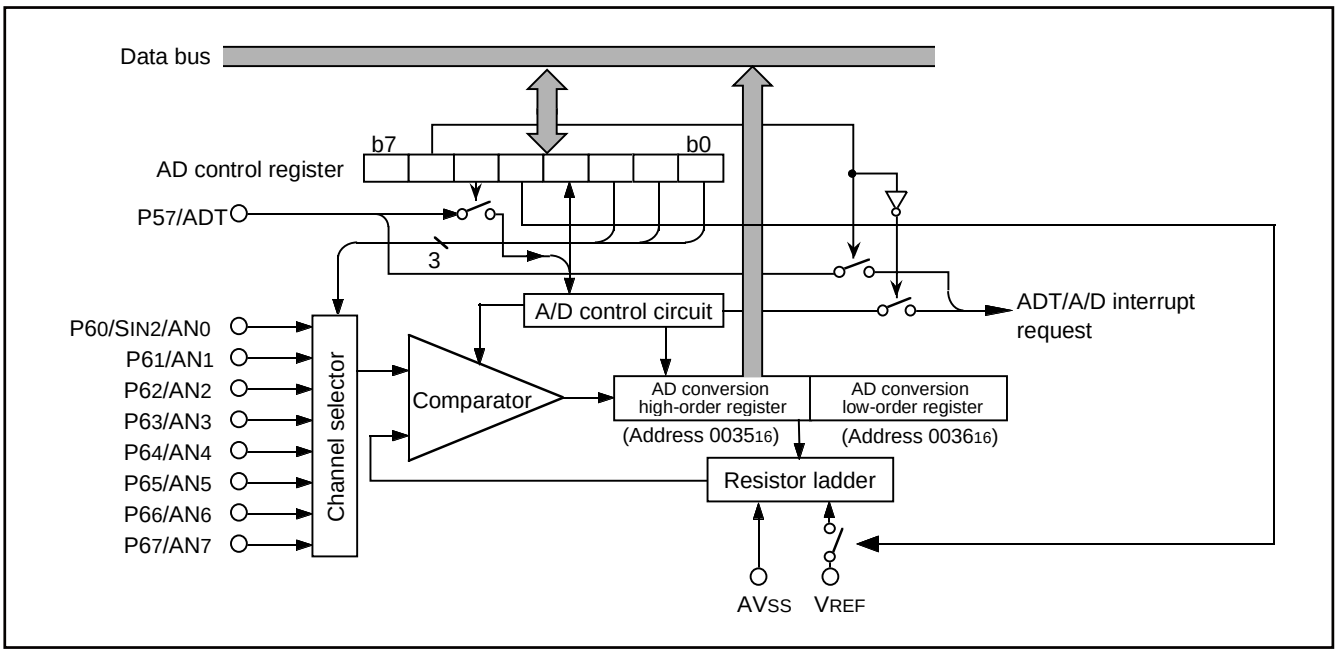


Fig. 35 A/D converter block diagram

		Address	Register Contents
(1)	Port P0 direction register	000116	0016
(2)	Port P1 direction register	000316	0016
(3)	Port P2 direction register	000516	0016
(4)	Port P4 direction register	000916	0016
(5)	Port P5 direction register	000B16	0016
(6)	Port P6 direction register	000D16	0016
(7)	Port P7 direction register	000F16	0016
(8)	ROM correctoin enable register (RCR)	001416	0016
(9)	PULL register A	001616	0 0 0 0 1 0 1 1
(10)	PULL register B	001716	0016
(11)	Sirial I/O status register	001916	1 0 0 0 0 0 0 0
(12)	Sirial I/O control register	001A16	0016
(13)	UART control register	001B16	1 1 1 0 0 0 0 0
(14)	Timer X high-order register	002016	FF16
(15)	Timer X low-order register	002116	FF16
(16)	Timer Y high-order register	002216	FF16
(17)	Timer Y low-order register	002316	FF16
(18)	Timer 1 register	002416	FF16
(19)	Timer 2 register	002516	0116
(20)	Timer 3 register	002616	FF16
(21)	Timer X mode register	002716	0016
(22)	Timer Y mode register	002816	0016
(23)	Timer 123 mode register	002916	0016
(24)	ϕ output control register	002A16	0016
(25)	CPU mode extension register	002B16	0016
(26)	Temporary data register 0	002C16	0016
(27)	Temporary data register 1	002D16	0016
(28)	Temporary data register 2	002E16	0016
(29)	RRF register	002F16	0016
(30)	Peripheral function extension register	003016	0016
(31)	AD control register	003416	0 0 0 0 1 0 0 0
(32)	AD conversion low-order register	003616	X X 0 0 0 0 0 0
(33)	Watchdog timer control register	003716	0 0 1 1 1 1 1 1
(34)	Segment output enable register	003816	0016
(35)	LCD mode register	003916	0016
(36)	Interrupt edge selection register	003A16	0016
(37)	CPU mode register	003B16	0 1 0 0 1 0 0 0
(38)	Interrupt request register 1	003C16	0016
(39)	Interrupt request register 2	003D16	0016
(40)	Interrupt control register 1	003E16	0016
(41)	Interrupt control register 2	003F16	0016
(42)	Processor status register	(PS)	X X X X X 1 X X
(43)	Program counter	(PC_H)	Contents of address FFFD16
		(PC_L)	Contents of address FFFC16

Note: The contents of all other registers and RAM are undefined after reset, so they must be initialized by software.
X: undefined

Fig. 53 Initial status of microcomputer after reset

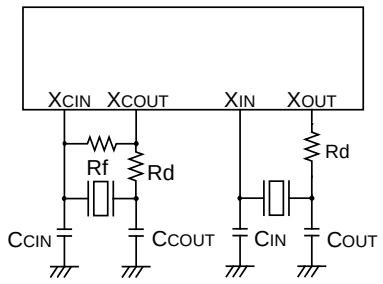
CLOCK GENERATING CIRCUIT

The 3823 group has two built-in oscillation circuits. An oscillation circuit can be formed by connecting a resonator between XIN and XOUT (XCIN and XCOUT). Use the circuit constants in accordance with the resonator manufacturer's recommended values. The oscillation start voltage and the oscillation start time differ in accordance with an oscillator, a circuit constant, or temperature, etc.

When power supply voltage is low and the high frequency oscillator is used, an oscillation start will require sufficient conditions. No external resistor is needed between XIN and XOUT since a feedback resistor exists on-chip. (an external feed-back resistor may be needed depending on conditions.) However, an external feedback resistor is needed between XCIN and XCOUT since a resistor does not exist between them.

To supply a clock signal externally, input it to the XIN pin and make the XOUT pin open. The sub-clock XCIN-XCOUT oscillation circuit cannot directly input clocks that are externally generated. Accordingly, be sure to cause an external resonator to oscillate.

Immediately after poweron, only the XIN oscillation circuit starts oscillating, and XCIN and XCOUT pins function as I/O ports.



Note : Insert a damping resistor if required. The resistance will vary depending on the oscillator and the oscillation drive capacity setting. Use the value recommended by the maker of the oscillator. Also, if the oscillator manufacturer's data sheet specifies that a feedback resistor be added external to the chip though a feedback resistor exists on-chip, insert a feedback resistor between XIN and XOUT following the instruction.

Fig. 54 Ceramic resonator circuit example

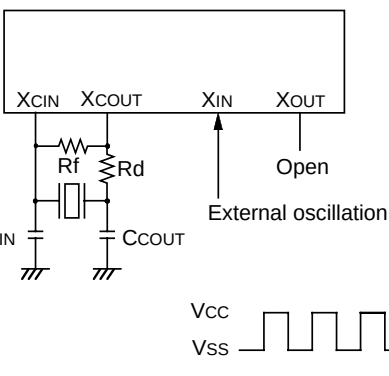


Fig. 55 External clock input circuit

Frequency Control

(1) frequency/8 Mode

The internal clock ϕ is the frequency of XIN divided by 8.
After reset, this mode is selected.

(2) frequency/4 Mode

The internal clock ϕ is the frequency of XIN divided by 4.

(3) frequency/2 Mode

The internal clock ϕ is half the frequency of XIN.

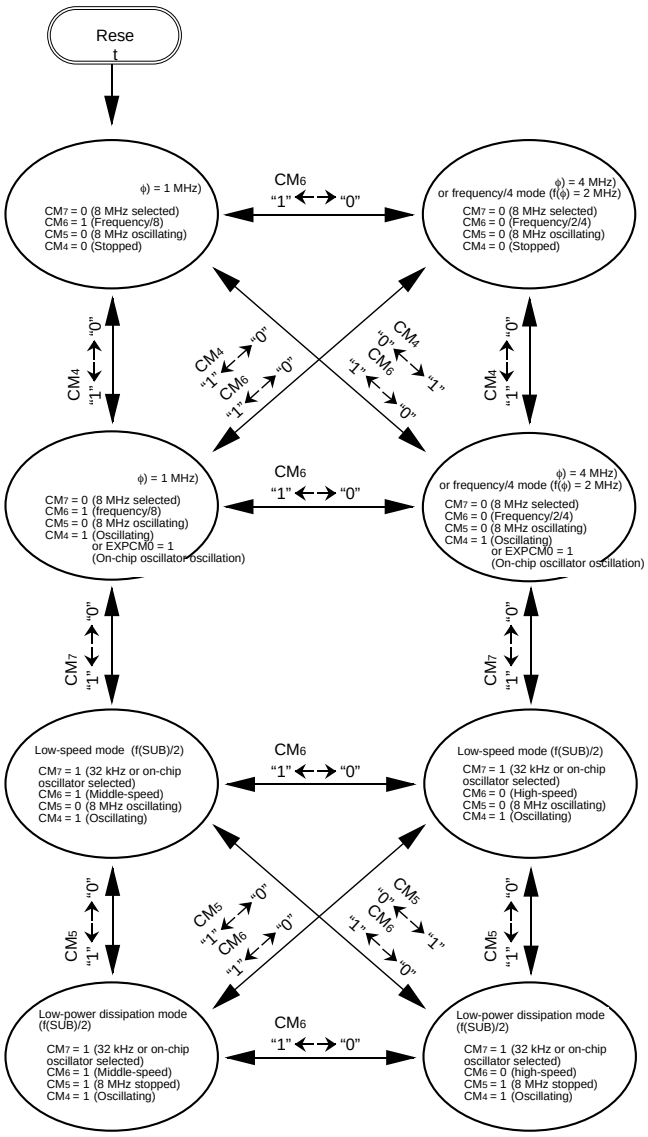
(4) Low-speed Mode

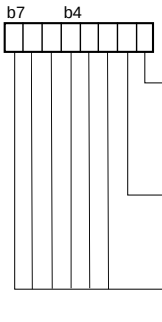
- The internal clock ϕ is the frequency of XIN or on-chip oscillation frequency divided by 2.
- A low-power consumption operation can be realized by stopping the main clock XIN in this mode. To stop the main clock, set bit 5 of the CPU mode register to “1”.
  When the main clock XIN is restarted, set enough time for oscillation to stabilize by programming.
  In low speed mode, the system clock ϕ can be switched to the on-chip oscillator or XCIN. Use the on-chip oscillator control bit (bit 0 in the CPU mode expansion register) for settings. To set this bit to “0” from “1”, wait until XCIN oscillation stabilizes.

Note 1: If you switch the mode between frequency/2/4/8 mode and low-speed, stabilize both XIN and XCIN oscillations. The sufficient time is required for the sub-clock to stabilize, especially immediately after poweron and at returning from stop mode. When switching the mode between middle/high-speed and low-speed, set the frequency on condition that f(XIN) > 3f(XCIN).

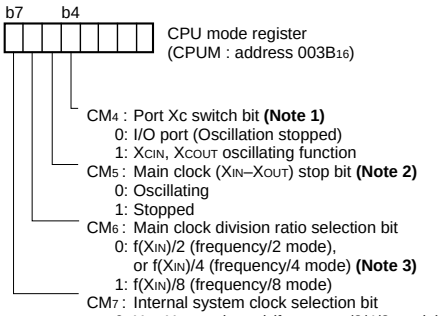
2: In frequency/2/4/8 mode, XIN-XOUT oscillation does not stop even if the main clock (XIN-XOUT) stop bit is set to "1".

3: In low speed mode, XCIN-XCOUT oscillation does not stop even if the port XC switch bit is set to "0".





Note 1 : The on-chip oscillator is selected for the operation clock in low-speed mode regardless of XCIN-XCOUT.
2 : Valid only when the main clock division ratio selection bit (bit 6 in the CPU mode register) is set to "0". When "1" (frequency/8 mode) is selected for the main clock division ratio selection bit or when the internal system clock selection bit is set to 1, set "0" to the frequency/4 mode control bit.



Note 1 : In low speed mode (XCIN is selected as the system clock ϕ), XCIN-XCOUT oscillation does not stop even if the port XC switch bit is set to "0".
2 : In frequency/2/4/8 mode, XIN-XOUT oscillation does not stop even if the main clock (XIN-XOUT) stop bit is set to "1".
3 : When the system clock ϕ is divided by 4 of f(XIN), set the bit 6 in the CPU mode register to "0" after setting the bit 1 in the CPU mode extension register to "1".
4 : When using the on-chip oscillator in low-speed mode, set the bit 7 in the CPU mode register to "1" after setting the bit 0 in the CPU mode extension register to "1".

Notes
1 : Switch the mode by the allows shown between the mode blocks. (Do not switch between the mode directly without an allow.)
2 : The all modes can be switched to the stop mode or the wait mode and returned to the source mode when the stop mode or the wait mode is ended.
3 : Timer and LCD operate in the wait mode.
4 : When the stop mode is ended, a delay of approximately 1 ms occurs automatically by timer 1 and timer 2 in frequency/2/4/8 mode.
5 : When the stop mode is ended, a delay of approximately 0.25 s occurs automatically by timer 1 and timer 2 in low-speed mode.
6 : Wait until oscillation stabilizes after oscillating the main clock XIN before the switching from the low-speed mode to frequency/2/4/8 mode.
7 : The example assumes that 8 MHz is being applied to the XIN pin and 32 kHz to the XCIN pin. ϕ indicates the internal clock.
8 : f(SUB) is the source oscillation frequency in low-speed mode. f(SUB) shows the oscillation frequency of XCIN or the on-chip oscillator. Internal clock ϕ is f(SUB)/2 in the low-speed mode.
9 : Set the CPU mode expansion register in advance when switching to low-speed mode which uses mode divided by 4 and on-chip oscillator.
10: In low speed mode, the system clock ϕ can be switched to the on-chip oscillator or XCIN. Use the on-chip oscillator control bit (bit 0 in the CPU mode expansion register) for settings. To set this bit to "0" from "1", wait until XCIN oscillation stabilizes.

Fig. 57 State transitions of system clock

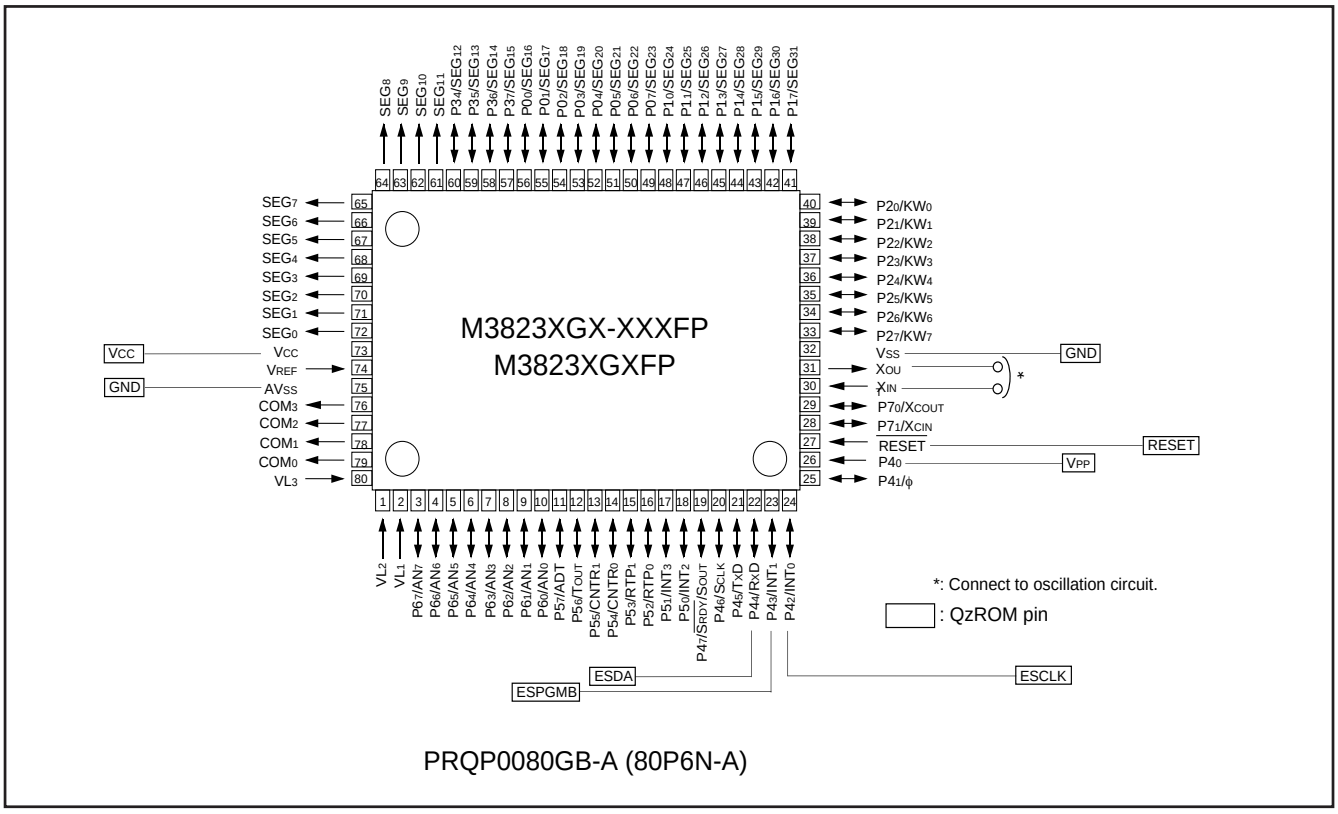


Fig. 58 Pin connection diagram (M3823XGX-XXXFP)

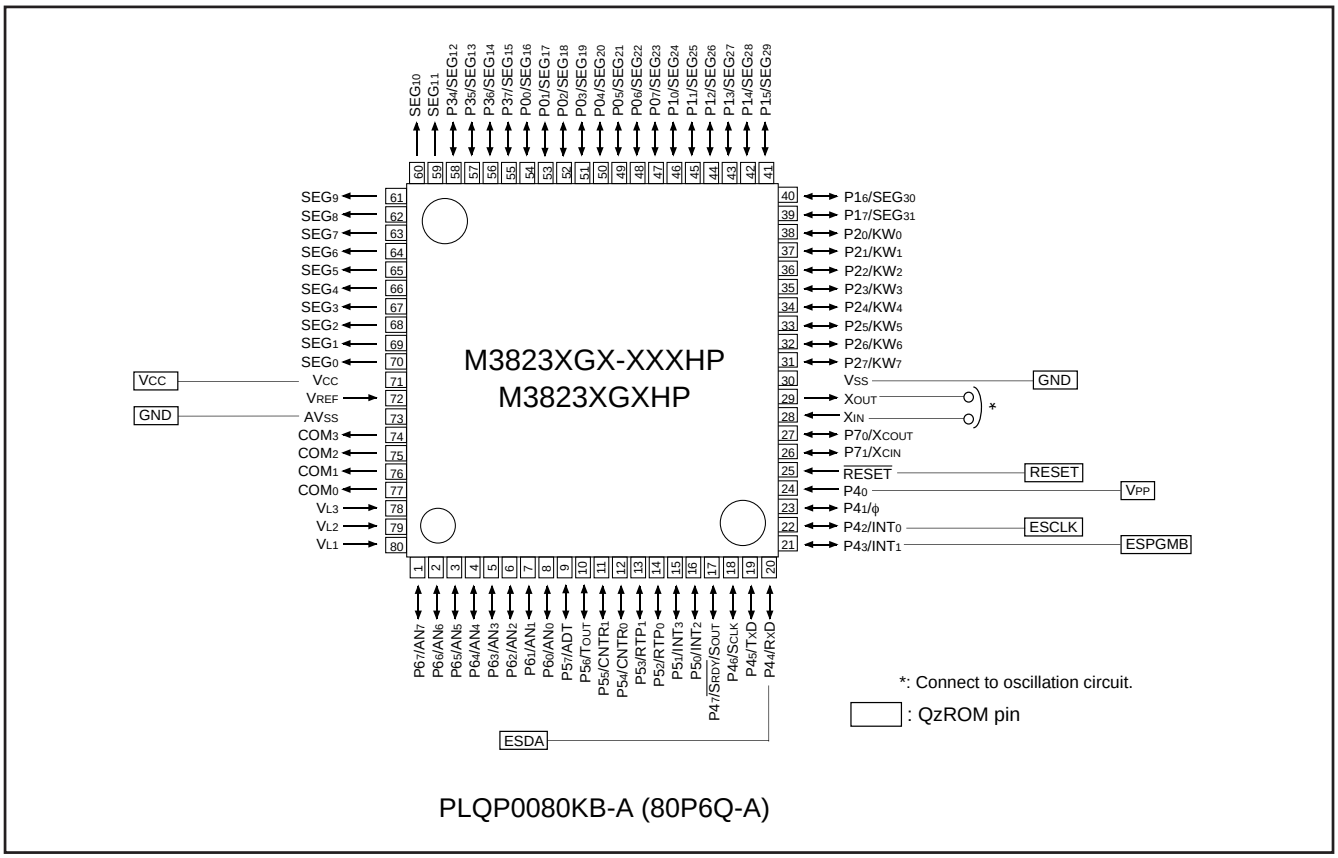


Fig. 59 Pin connection diagram (M3823XGX-XXXHP)

NOTES ON PROGRAMMING

Processor Status Register

The contents of the processor status register (PS) after a reset are undefined, except for the interrupt disable flag (I) which is “1”. After a reset, initialize flags which affect program execution.
In particular, it is essential to initialize the index X mode (T) and the decimal mode (D) flags because of their effect on calculations. Initialize these flags at the beginning of the program.

Interrupt

The contents of the interrupt request bits do not change immediately after they have been written. After writing to an interrupt request register, execute at least one instruction before performing a BBC or BBS instruction.

Decimal Calculations

- To calculate in decimal notation, set the decimal mode flag (D) to “1”, then execute an ADC or SBC instruction. After executing an ADC or SBC instruction, execute at least one instruction before executing a SEC, CLC, or CLD instruction.

- In decimal mode, the values of the negative (N), overflow (V), and zero (Z) flags are invalid.

Timers

If a value n (between 0 and 255) is written to a timer latch, the frequency division ratio is 1/(n + 1).

Multiplication and Division Instructions

The index mode (T) and the decimal mode (D) flags do not affect the MUL and DIV instruction.
The execution of these instructions does not change the contents of the processor status register.

Ports

The contents of the port direction registers cannot be read.
The following cannot be used:

- The data transfer instruction (LDA, etc.)
- The operation instruction when the index X mode flag (T) is “1”
- The addressing mode which uses the value of a direction register as an index
- The bit-test instruction (BBC or BBS, etc.) to a direction register
- The read-modify-write instruction (ROR, CLB, or SEB, etc.) to a direction register

Use instructions such as LDM and STA, etc., to set the port direction registers.

Serial Interface

In clock synchronous serial I/O, if the receive side is using an external clock and it is to output the $\overline{\text{SRDY}}$ signal, set the transmit enable bit, the receive enable bit, and the $\overline{\text{SRDY}}$ output enable bit to “1”.
Serial I/O continues to output the final bit from the TxD pin after transmission is completed.

A/D Converter

The comparator is constructed linked to a capacitor. The conversion accuracy may be low because the charge is lost if the conversion speed is not enough. Accordingly, set f(XIN) to at least 500kHz during A/D conversion in the middle-or high-speed mode.
Also, do not execute the STP or WIT instruction during an A/D conversion.
In the low-speed mode, since the A/D conversion is executed by the on-chip oscillator, the minimum value of f(XIN) frequency is not limited.

LCD Drive Control Circuit

Execution of the STP instruction sets the LCD enable bit (bit 3 of the LCD mode register) to “0” and the LCD panel turns off.To make the LCD panel turn on after returning from the stop mode, set the LCD enable bit to “1”.

Instruction Execution Time

The instruction execution time is obtained by multiplying the frequency of the internal clock ϕ by the number of cycles needed to execute an instruction.
The number of cycles required to execute an instruction is shown in the list of machine instructions.
The frequency of the internal clock ϕ is half of the XIN frequency.

Table 17 Recommended operating conditions (3)

(V_{CC} = 1.8 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
$\Sigma I_{OH(peak)}$	"H" total peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$ **(Note 1)**			–40	mA
$\Sigma I_{OH(peak)}$	"H" total peak output current	$P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note 1)**			–40	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$ **(Note 1)**			40	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current	$P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note 1)**			40	mA
$\Sigma I_{OH(avg)}$	"H" total average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$ **(Note 1)**			–20	mA
$\Sigma I_{OH(avg)}$	"H" total average output current	$P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note 1)**			–20	mA
$\Sigma I_{OL(avg)}$	"L" total average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$ **(Note 1)**			20	mA
$\Sigma I_{OL(avg)}$	"L" total average output current	$P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note 1)**			20	mA
$I_{OH(peak)}$	"H" peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$ **(Note 2)**			–2	mA
$I_{OH(peak)}$	"H" peak output current	$P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note 2)**			–5	mA
$I_{OL(peak)}$	"L" peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$ **(Note 2)**			5	mA
$I_{OL(peak)}$	"L" peak output current	$P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note 2)**			10	mA
$I_{OH(avg)}$	"H" average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$ **(Note 3)**			–1.0	mA
$I_{OH(avg)}$	"H" average output current	$P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note 3)**			–2.5	mA
$I_{OL(avg)}$	"L" average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$ **(Note 3)**			2.5	mA
$I_{OL(avg)}$	"L" average output current	$P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note 3)**			5.0	mA
f(CNTR0) f(CNTR1)	Input frequency for timers X and Y (duty cycle 50%)	(4.5 V ≤ V_{CC} ≤ 5.5 V)			5.0	MHz
		(4.0 V ≤ V_{CC} ≤ 4.5 V)			2 × V_{CC} – 4	MHz
		(2.0 V ≤ V_{CC} ≤ 4.0 V)			0.75 × V_{CC} + 1	MHz
		(V_{CC} ≤ 2.0 V)			6.25 × V_{CC} - 10	MHz
f(X_{IN})	Main clock input oscillation frequency (duty cycle 50%) **(Note 4)**	Frequency/2 mode (4.5 V ≤ V_{CC} ≤ 5.5 V)			10.0	MHz
		Frequency/2 mode (4.0 V ≤ V_{CC} ≤ 4.5 V)			4 × V_{CC} – 8	MHz
		Frequency/2 mode (2.0 V ≤ V_{CC} ≤ 4.0 V)			1.5 × V_{CC} + 2	MHz
		Frequency/2 mode (1.8 V ≤ V_{CC} ≤ 2.0 V)			12.5 × V_{CC} - 20	MHz
		Frequency/4 mode (2.5 V ≤ V_{CC} ≤ 5.5 V)			10.0	MHz
		Frequency/4 mode (2.0 V ≤ V_{CC} ≤ 2.5 V)			4 × V_{CC}	MHz
		Frequency/4 mode (1.8 V ≤ V_{CC} ≤ 2.0 V)			15 × V_{CC} – 22	MHz
		Frequency/8 mode (2.5 V ≤ V_{CC} ≤ 5.5 V)			10.0	MHz
		Frequency/8 mode (2.0 V ≤ V_{CC} ≤ 2.5 V)			4 × V_{CC}	MHz
		Frequency/8 mode (1.8 V ≤ V_{CC} ≤ 2.0 V)			15 × V_{CC} – 22	MHz
f(X_{CIN})	Sub-clock input oscillation frequency (duty cycle 50%) **(Note 5)**			32.768	80	kHz

Notes 1: The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.

2: The peak output current is the peak current flowing in each port.

3: The average output current is an average value measured over 100 ms.

4: When the A/D converter is used, refer to the recommended operating condition for A/D converter.

5: When using the microcomputer in low-speed mode, make sure that the sub-clock input oscillation frequency on condition that $f(X_{CIN}) < f(X_{IN})/3$.

Table 18 Electrical characteristics (1)
(V_{CC} = 4.0 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$	I_{OH} = –2.5 mA	V_{CC}–2.0			V
		I_{OH} = –0.6 mA V_{CC} = 2.5 V	V_{CC}–1.0			V
V_{OH}	"H" output voltage $P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note)**	I_{OH} = –5 mA	V_{CC}–2.0			V
		I_{OH} = –1.25 mA	V_{CC}–0.5			V
		I_{OH} = –1.25 mA V_{CC} = 2.5 V	V_{CC}–1.0			V
V_{OL}	"L" output voltage $P0_0$–$P0_7$, $P1_0$–$P7$	I_{OL} = 5 mA			2.0	V
		I_{OL} = 1.25 mA			0.5	V
		I_{OL} = 1.25 mA V_{CC} = 2.5 V			1.0	V
V_{OL}	"L" output voltage $P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note)**	I_{OL} = 10 mA			2.0	V
		I_{OL} = 2.5 mA			0.5	V
		I_{OL} = 2.5 mA V_{CC} = 2.5 V			1.0	V
V_{T+} – V_{T-}	Hysteresis INT_0–INT_3, ADT, $CNTR_0$, $CNTR_1$, $P2_0$–$P2_7$			0.5		V
V_{T+} – V_{T-}	Hysteresis S_{CLK}, R_XD			0.5		V
V_{T+} – V_{T-}	Hysteresis $\overline{RESET}$	$\overline{RESET}$: V_{CC} = 2.0 V to 5.5 V		0.5		V
I_{IH}	"H" input current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P3_4$–$P3_7$	V_I = V_{CC} Pull-downs "off"			5.0	µA
		V_{CC} = 5 V, V_I = V_{CC} Pull-downs "on"	30	70	140	µA
		V_{CC} = 3 V, V_I = V_{CC} Pull-downs "on"	6.0	25	45	µA
I_{IH}	"H" input current $P2_0$–$P2_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note)**	V_I = V_{CC}			5.0	µA
I_{IH}	"H" input current $\overline{RESET}$	V_I = V_{CC}			5.0	µA
I_{IH}	"H" input current X_{IN}	V_I = V_{CC}		4.0		µA
I_{IL}	"L" input current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P3_4$–$P3_7$,$P4_0$	V_I = V_{SS}			–5.0	µA
I_{IL}	"L" input current $P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note)**	V_I = V_{SS} Pull-ups "off"			–5.0	µA
		V_{CC} = 5 V, V_I = V_{SS} Pull-ups "on"	–30	–70	–140	µA
		V_{CC} = 3 V, V_I = V_{SS} Pull-ups "on"	–6.0	–25	–45	µA
I_{IL}	"L" input current $\overline{RESET}$	V_I = V_{SS}			–5.0	µA
I_{IL}	"L" input current X_{IN}	V_I = V_{SS}		–4.0		µA
V_{RAM}	RAM hold voltage	When clock is stopped	1.8		5.5	V

Note: When "1" is set to the port X_C switch bit (bit 4 at address $003B_{16}$) of CPU mode register, the drive ability of port $P7_0$ is different from the value above mentioned.

Table 19 Electrical characteristics (2)

(V_{CC} = 1.8 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions			Limits			Unit
					Min.	Typ.	Max.	
I_{CC}	Power source current	Frequency/2 mode	V_{CC} = 5.0 V	f(X_{IN}) = 10 MHz		4.3	8.6	mA
				f(X_{IN}) = 8 MHz		3.7	7.4	mA
				f(X_{IN}) = 4 MHz		2.5	5.0	mA
			V_{CC} = 2.5 V	f(X_{IN}) = 4 MHz		0.8	1.6	mA
				f(X_{IN}) = 2 MHz		0.4	0.8	mA
		Frequency/4 mode	V_{CC} = 5.0 V	f(X_{IN}) = 10 MHz		2.9	5.8	mA
				f(X_{IN}) = 8 MHz		2.5	5.0	mA
				f(X_{IN}) = 4 MHz		1.7	3.4	mA
			V_{CC} = 2.5 V	f(X_{IN}) = 10 MHz		1.0	2.0	mA
				f(X_{IN}) = 8 MHz		0.8	1.6	mA
				f(X_{IN}) = 4 MHz		0.5	1.0	mA
				f(X_{IN}) = 2 MHz		0.3	0.6	mA
		Frequency/8 mode	V_{CC} = 5.0 V	f(X_{IN}) = 10 MHz		2.2	4.4	mA
				f(X_{IN}) = 8 MHz		1.9	3.8	mA
				f(X_{IN}) = 4 MHz		1.4	2.8	mA
				f(X_{IN}) = 2 MHz		1.0	2.0	mA
			V_{CC} = 2.5 V	f(X_{IN}) = 10 MHz		0.7	1.4	mA
				f(X_{IN}) = 8 MHz		0.6	1.2	mA
				f(X_{IN}) = 4 MHz		0.4	0.8	mA
				f(X_{IN}) = 2 MHz		0.2	0.4	mA
		Frequency/2/4/8 mode In WIT state	V_{CC} = 5.0 V	f(X_{IN}) = 10 MHz		1.35	2.7	mA
				f(X_{IN}) = 8 MHz		1.2	2.4	mA
				f(X_{IN}) = 4 MHz		0.9	1.8	mA
				f(X_{IN}) = 2 MHz		0.8	1.6	mA
			V_{CC} = 2.5 V	f(X_{IN}) = 10 MHz		0.35	0.7	mA
				f(X_{IN}) = 8 MHz		0.3	0.6	mA
				f(X_{IN}) = 4 MHz		0.2	0.4	mA
				f(X_{IN}) = 2 MHz		0.15	0.3	mA
		Low-speed mode f(X_{IN}) = stopped	V_{CC} = 5.0 V	f(X_{CIN}) = 32 kHz		13	26	µA
				On-chip oscillator		80	240	µA
			V_{CC} = 2.5 V	f(X_{CIN}) = 32 kHz		7	14	µA
				On-chip oscillator		14	42	µA
		Low-speed mode f(X_{IN}) = stopped In WIT state	V_{CC} = 5.0 V	f(X_{CIN}) = 32 kHz		5.5	11	µA
				On-chip oscillator		20	60	µA
			V_{CC} = 2.5 V	f(X_{CIN}) = 32 kHz		3.5	7	µA
				On-chip oscillator		3.5	10	µA
		Current increased at A/D converter operating		V_{CC} = 5 V, all modes		500		µA
				V_{CC} = 2.5 V, all modes		50		µA
		All oscillation stopped Ta = 25 °C, Output transistors “off” (in STP state)				0.1	1.0	µA
		All oscillation stopped Ta = 85 °C, Output transistors “off” (in STP state)					10	µA
R_{OCO}	On-chip oscillator oscillatoin	V_{CC} = 2.5 V, Ta = 25 °C				80		kHz

Table 20 A/D converter characteristics (1) (in 8 bit A/D mode)
(V_{CC} = 1.8 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
–	Resolution				8	Bits
ABS	Absolute accuracy (excluding quantization error)	ADL2 = “0”, ADL1 = “0”, CPUM7 = “0” 2.2 V ≤ V_{CC} = V_{REF} ≤ 5.5 V f(X_{IN}) = 2 × V_{CC} MHz ≤ 10 MHz			±2	LSB
		ADL2 = “0”, ADL1 = “0”, CPUM7 = “0” 2.0 V ≤ V_{CC} = V_{REF} < 2.2 V f(X_{IN}) = 4.4 MHz			±3	LSB
		ADL2 = “0”, ADL1 = “1”, CPUM7 = “0” V_{CC} = V_{REF} = 4.0 to 5.5 V f(X_{IN}) = 2 × V_{CC} MHz ≤ 10 MHz			±3	LSB
		ADL2 = “1”, ADL1 = “0”, CPUM7 = “1” and EXPCM0 = “1” V_{CC} = V_{REF} = 1.8 to 2.2 V			±4	LSB
t_{CONV}	Conversion time	f(X_{IN}) = 8 MHz (ADL2 = “0”, ADL1 = “0”, CPUM7 = “0”)			TC(X_{IN})×100	µs
R_{LADDER}	Ladder resistor		12	35	100	kΩ
I_{VREF}	Reference power source input current	V_{REF} = 5 V	50	150	200	µA
I_{IA}	Analog port input current				5.0	µA

Table 21 A/D converter characteristics (2) (in 10 bit A/D mode)
(V_{CC} = 1.8 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
–	Resolution				10	Bits
ABS	Absolute accuracy (excluding quantization error)	ADL2 = “0”, ADL1 = “0”, CPUM7 = “0” 2.2 V ≤ V_{CC} = V_{REF} ≤ 5.5 V f(X_{IN}) = 2 × V_{CC} MHz ≤ 10 MHz			±4	LSB
		ADL2 = “0”, ADL1 = “1”, CPUM7 = “0” V_{CC} = V_{REF} = 4.0 to 5.5 V f(X_{IN}) = 2 × V_{CC} MHz ≤ 10 MHz			±4	LSB
		ADL2 = “1”, ADL1 = “0”, CPUM7 = “1” and EXPCM0 = “1” V_{CC} = V_{REF} = 1.8 to 2.2 V			±4	LSB
t_{CONV}	Conversion time	f(X_{IN}) = 8 MHz (ADL2 = “0”, ADL1 = “0”, CPUM7 = “0”)			TC(X_{IN})×100	µs
R_{LADDER}	Ladder resistor		12	35	100	kΩ
I_{VREF}	Reference power source input current	V_{REF} = 5 V	50	150	200	µA
I_{IA}	Analog port input current				5.0	µA