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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	740
Core Size	8-Bit
Speed	10MHz
Connectivity	SIO, UART/USART
Peripherals	LCD, WDT
Number of I/O	49
Program Memory Size	60KB (60K x 8)
Program Memory Type	QzROM
EEPROM Size	-
RAM Size	2.5K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External, Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-BQFP
Supplier Device Package	80-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m3823agffp-u0

3823 Group

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

REJ03B0146-0202
Rev.2.02
Jun.19.2007

DESCRIPTION

The 3823 group is the 8-bit microcomputer based on the 740 family core technology.

The 3823 group has the LCD drive control circuit, an 8-channel A/D converter, a serial interface, a watchdog timer, a ROM correction function, and as additional functions.

The various microcomputers in the 3823 group include variations of internal memory size and packaging. For details, refer to the section on part numbering.

FEATURES

- Basic machine-language instructions 71
- The minimum instruction execution time ..... 0.4 µs
  (at f(XIN) = 10 MHz, High-speed mode)
- Memory size
  ROM ..... 16 K to 60 K bytes
  RAM ..... 640 to 2560 bytes
- ROM correction function ..... 32 bytes × 2 blocks
- Watchdog timer ..... 8-bit × 1
- Programmable input/output ports 49
- Input ports 5
- Software pull-up/pull-down resistors (Ports P0-P7 except port $P4_0$)
- Interrupts ..... 17 sources, 16 vectors
  (includes key input interrupt)
- Key Input Interrupt (Key-on Wake-Up) 8
- Timers ..... 8-bit × 3, 16-bit × 2
- Serial interface ..... 8-bit × 1 (UART or Clock-synchronized)
- A/D converter ..... 10-bit × 8 channels or 8-bit × 8 channels
- LCD drive control circuit
  Bias 1/2, 1/3
  Duty 1/2, 1/3, 1/4
  Common output 4
  Segment output 32
- Main clock generating circuits ..... Built-in feedback resistor
  (connect to external ceramic resonator or quartz-crystal oscillator)
- Sub-clock generating circuits
  (connect to external quartz-crystal oscillator or on-chip oscillator)
- Power source voltage
  In frequency/2 mode (f(XIN) ≤ 10 MHz) ..... 4.5 to 5.5 V
  In frequency/2 mode (f(XIN) ≤ 8 MHz) ..... 4.0 to 5.5 V
  In frequency/4 mode (f(XIN) ≤ 10 MHz) ..... 2.5 to 5.5 V
  In frequency/4 mode (f(XIN) ≤ 8 MHz) ..... 2.0 to 5.5 V
  In frequency/4 mode (f(XIN) ≤ 5 MHz) ..... 1.8 to 5.5 V
  In frequency/8 mode (f(XIN) ≤ 10 MHz) ..... 2.5 to 5.5 V
  In frequency/8 mode (f(XIN) ≤ 8 MHz) ..... 2.0 to 5.5 V
  In frequency/8 mode (f(XIN) ≤ 5 MHz) ..... 1.8 to 5.5 V
  In low-speed mode ..... 1.8 to 5.5 V
- Power dissipation
  In frequency/2 mode ..... 18 mW (std.)
  (at f(XIN) = 8 MHz, Vcc = 5 V, Ta = 25 °C)
  In low-speed mode at XCIN ..... 18 µW (std.)
  (at f(XIN) stopped, f(XCIN) = 32 kHz, Vcc = 2.5 V, Ta = 25 °C)
  In low-speed mode at on-chip oscillator ..... 35 µW (std.)
  (at f(XIN) stopped, f(XCIN) = stopped, Vcc = 2.5 V, Ta = 25 °C)
- Operating temperature range ..... – 20 to 85 °C

APPLICATIONS

Camera, audio equipment, household appliances, consumer electronics, etc.

I/O PORTS

Direction Registers (ports P2, P41-P47, and P5-P7)

The 3823 group has 49 programmable I/O pins arranged in seven I/O ports (ports P0–P2, P41–P47 and P5-P7). The I/O ports P2, P41–P47 and P5-P7 have direction registers which determine the input/output direction of each individual pin. Each bit in a direction register corresponds to one pin, and each pin can be set to be input port or output port.

When “0” is written to the bit corresponding to a pin, that pin becomes an input pin. When “1” is written to that bit, that pin becomes an output pin.

If data is read from a pin set to output, the value of the port output latch is read, not the value of the pin itself. Pins set to input are floating. If a pin set to input is written to, only the port output latch is written to and the pin remains floating.

Direction Registers (ports P0 and P1)

Ports P0 and P1 have direction registers which determine the input/output direction of each individual port.

Each port in a direction register corresponds to one port, each port can be set to be input or output. When “0” is written to the bit 0 of a direction register, that port becomes an input port. When “1” is written to that port, that port becomes an output port. Bits 1 to 7 of ports P0 and P1 direction registers are not used.

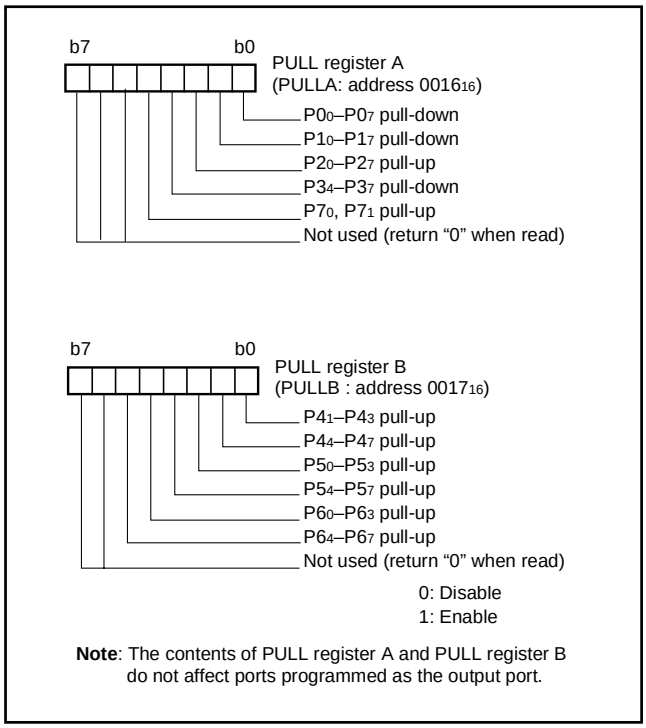
Ports P3 and P40

These ports are only for input.

Pull-up/Pull-down Control

By setting the PULL register A (address 0016$_{16}$) or the PULL register B (address 0017$_{16}$), ports except for port P40 can control either pull-down or pull-up (pins that are shared with the segment output pins for LCD are pull-down; all other pins are pull-up) with a program.

However, the contents of PULL register A and PULL register B do not affect ports programmed as the output ports.



Note: The contents of PULL register A and PULL register B do not affect ports programmed as the output port.

Fig. 12 Structure of PULL register A and PULL register B

Table 8 Termination of unused pins

Pin	Termination 1 (recommend)	Termination 2	Termination 3
P00/SEG16–P17/SEG23	I/O port	When selecting SEG output, open.	–
P10/SEG24–P17/SEG31			
P20/KW0–P27/KW7		When selecting KW function, perform termination of input port.	–
P34/SEG12–P37/SEG15	Input port	When selecting SEG output, open.	–
P40/(VPP)	Input port (pull-down)	–	–
P41/ϕ	I/O port	When selecting ϕ output, open.	–
P42/INT0		When selecting INT0 function, perform termination of input port.	–
P43/INT1		When selecting INT1 function, perform termination of input port.	–
P44/RxD		When selecting RxD function, perform termination of input port.	–
P45/TxD		When selecting TxD function, perform termination of output port.	–
P46/SCLK		When selecting external clock input, perform termination of input port.	When selecting internal clock output, perform termination of output port.
P47/$\overline{\text{SRDY}}$/SOUT		When selecting $\overline{\text{SRDY}}$ function, perform termination of output port.	When selecting SOUT function, perform termination of output port.
P50/INT2		When selecting INT2 function, perform termination of input port.	–
P51/INT3		When selecting INT3 function, perform termination of input port.	–
P52/RTP0		When selecting RTP0 function, perform termination of output port.	–
P53/RTP1		When selecting RTP1 function, perform termination of output port.	–
P54/CNTR0		When selecting CNTR0 input function, perform termination of input port.	When selecting CNTR0 output function, perform termination of output port.
P55/CNTR1		When selecting CNTR1 function, perform termination of input port.	–
P56/TOUT		When selecting TOUT function, perform termination of output port.	–
P57/ADT		When selecting ADT function, perform termination of input port.	–
P60/AN0–P67/AN7		When selecting AN function, these pins can be opened. (A/D conversion result cannot be guaranteed.)	–
P70/XCOUT P71/XCIN		Do not select XCIN-XCOUT oscillation function by program.	–
VL3 (Note)	Connect to VSS	–	–
VL2 (Note)	Connect to VSS	–	–
VL1 (Note)	Connect to VSS	–	–
COM0–COM3	Open	–	–
SEG0–SEG11	Open	–	–
AVSS	Connect to VSS	–	–
VREF	Connect to VCC or VSS	–	–
XOUT	When an external clock is input to the XIN pin, leave the XOUT pin open.	–	–

Note : The termination of VL3, VL2 and VL1 is applied when the bit 3 of the LCD mode register is “0”

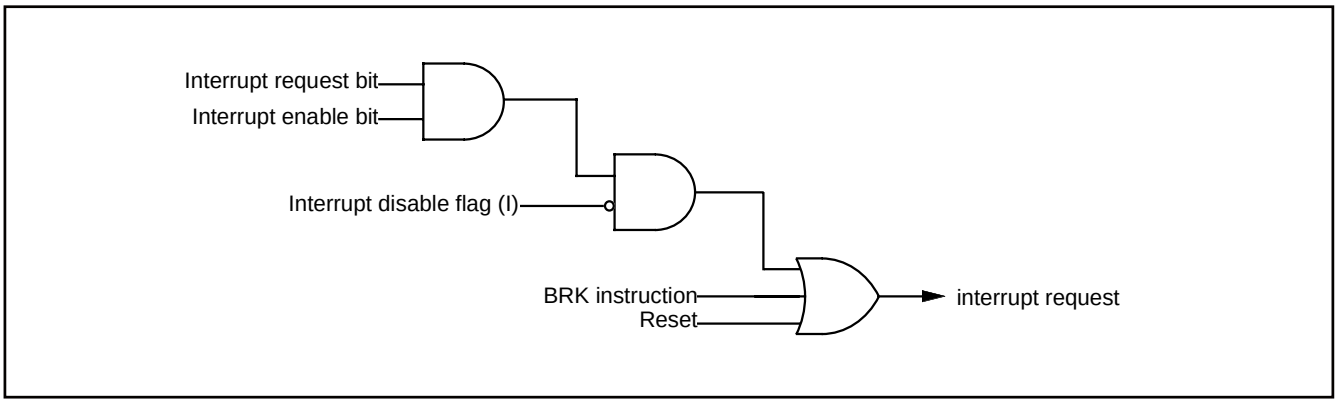


Fig. 16 Interrupt control diagram

Interrupt Disable Flag

The interrupt disable flag is assigned to bit 2 of the processor status register. This flag controls the acceptance of all interrupt requests except for the BRK instruction. When this flag is set to “1”, the acceptance of interrupt requests is disabled. When it is set to “0”, acceptance of interrupt requests is enabled. This flag is set to “1” with the SET instruction and set to “0” with the CLI instruction.

When an interrupt request is accepted, the contents of the processor status register are pushed onto the stack while the interrupt disable flag remaines set to “0”. Subsequently, this flag is automatically set to “1” and multiple interrupts are disabled.

To use multiple interrupts, set this flag to “0” with the CLI instruction within the interrupt processing routine.

The contents of the processor status register are popped off the stack with the RTI instruction.

Interrupt Request Bits

Once an interrupt request is generated, the corresponding interrupt request bit is set to “1” and remaines “1” until the request is accepted. When the request is accepted, this bit is automatically set to “0”.

Each interrupt request bit can be set to “0”, but cannot be set to “1”, by software.

Interrupt Enable Bits

The interrupt enable bits control the acceptance of the corresponding interrupt requests. When an interrupt enable bit is set to “0”, the acceptance of the corresponding interrupt request is disabled. If an interrupt request occurs in this condition, the corresponding interrupt request bit is set to “1”, but the interrupt request is not accepted. When an interrupt enable bit is set to “1”, acceptance of the corresponding interrupt request is enabled.

Each interrupt enable bit can be set to “0” or “1” by software.

The interrupt enable bit for an unused interrupt should be set to “0”.

Interrupt Source Selection

The following combinations can be selected by the interrupt source selection bit of the AD control register (bit 6 of the address 0039_{16}).

- ADT or A/D conversion (refer Table 9)

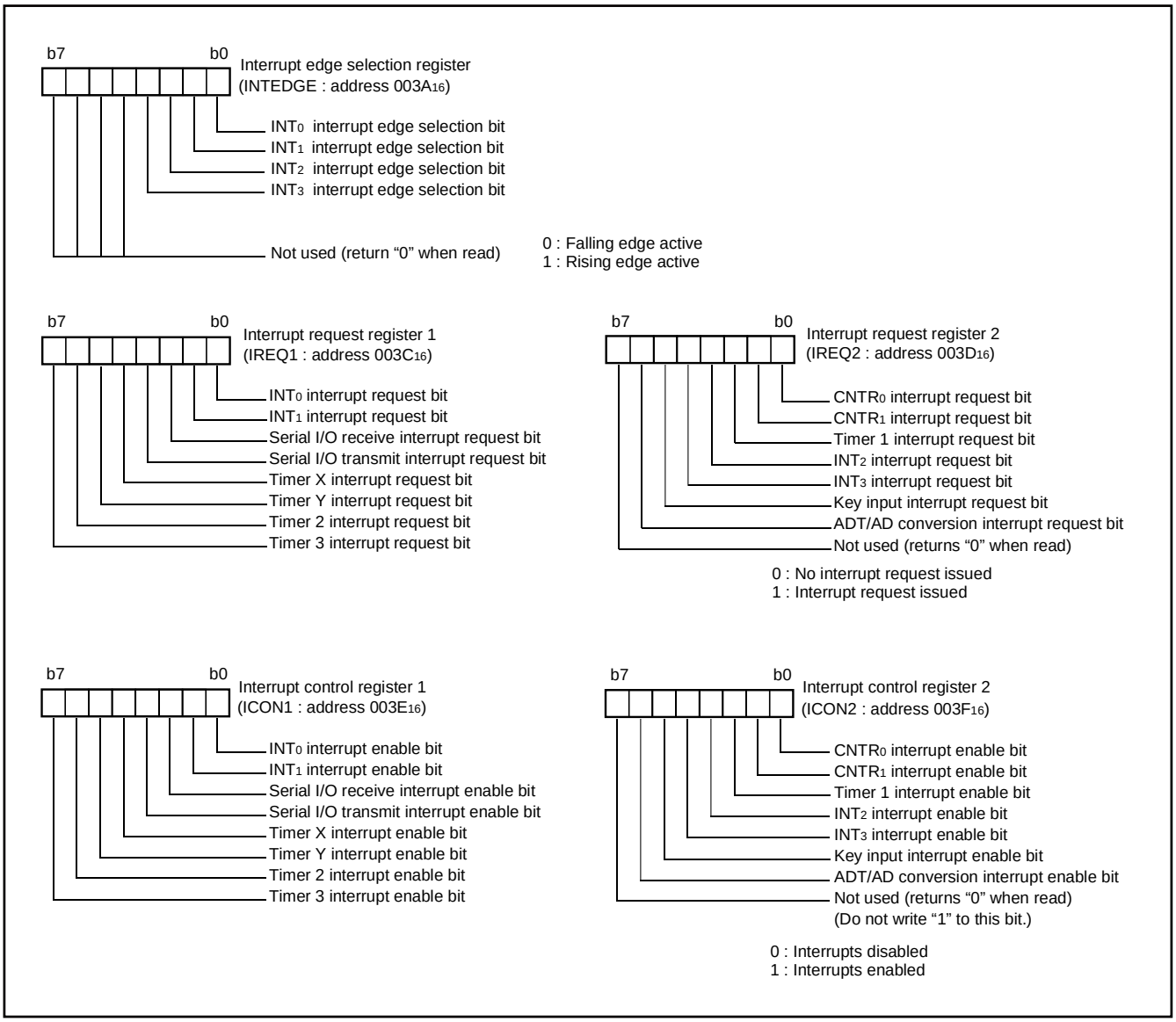
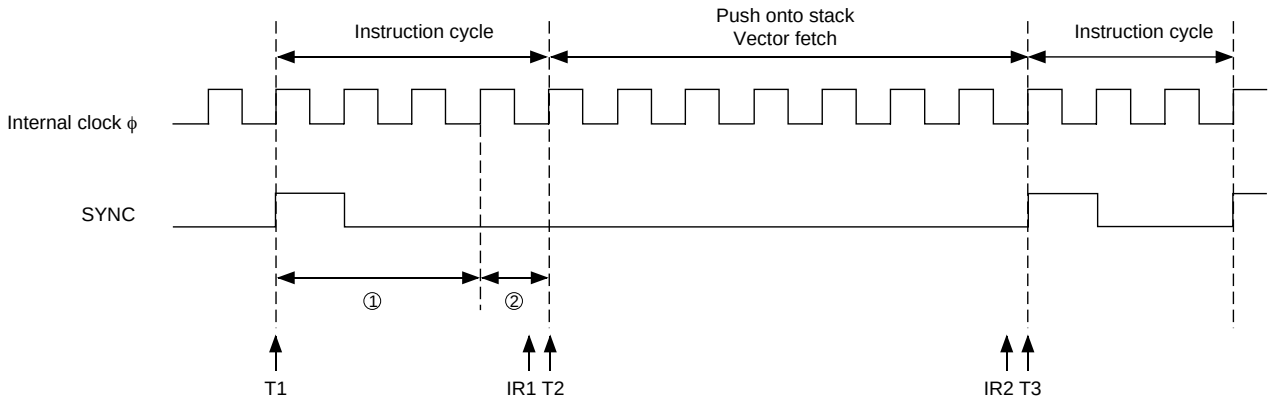


Fig. 17 Structure of interrupt-related registers



T1 T2 T3: Interrupt acceptance timing points
IR1 IR2: Timings points at which the interrupt request bit is set to “1”.

Note: Period 2 indicates the last ϕ cycle during one instruction cycle.

(1) The interrupt request bit for an interrupt request generated during period 1 is set to “1” at timing point IR1.
(2) The interrupt request bit for an interrupt request generated during period 2 is set to “1” at timing point IR1 or IR2. The timing point at which the bit is set to “1” varies depending on conditions. When two or more interrupt requests are generated during the period 2, each request bit may be set to “1” at timing point IR1 or IR2 separately.

Fig. 20 Timing of interrupt request generation, interrupt request bit, and interrupt acceptance

Timer X

Timer X is a 16-bit timer that can be selected in one of four modes and can be controlled the timer X write and the real time port by setting the timer X mode register.

(1) Timer Mode

The timer counts f(XIN)/16 (or f(SUB)/16 in low-speed mode).
f(SUB) is the source oscillation frequency in low-speed mode. f(SUB) shows the oscillation frequency of XCIN or the on-chip oscillator. Internal clock ϕ is f(XCIN)/2 in the low-speed mode.

(2) Pulse Output Mode

Each time the timer underflows, a signal output from the CNTR0 pin is inverted. Except for this, the operation in pulse output mode is the same as in timer mode. When using a timer in this mode, set the corresponding port P54 direction register to output mode.

(3) Event Counter Mode

The timer counts signals input through the CNTR0 pin.
Except for this, the operation in event counter mode is the same as in timer mode. When using a timer in this mode, set the corresponding port P54 direction register to input mode.

(4) Pulse Width Measurement Mode

The count source is f(XIN)/16 (or f(SUB)/16 in low-speed mode). If CNTR0 active edge switch bit is “0”, the timer counts while the input signal of CNTR0 pin is at “H”. If it is “1”, the timer counts while the input signal of CNTR0 pin is at “L”. When using a timer in this mode, set the corresponding port P54 direction register to input mode.

●Timer X write control

If the timer X write control bit is “0”, when the value is written in the address of timer X, the value is loaded in the timer X and the latch at the same time.
If the timer X write control bit is “1”, when the value is written in the address of timer X, the value is loaded only in the latch. The value in the latch is loaded in timer X after timer X underflows.
If the value is written in latch only, when writing in the timer latch at the timer underflow, the value is set in the timer and the latch at one time. Additionally, unexpected value may be set in the high-order counter when the writing in high-order latch and the underflow of timer X are performed at the same timing.

●Real time port control

While the real time port function is valid, data for the real time port are output from ports P52 and P53 each time the timer X underflows. (However, after rewriting a data for real time port, if the real time port control bit is changed from “0” to “1”, data are output independent of the timer X operation.) If the data for the real time port is changed while the real time port function is valid, the changed data are output at the next underflow of timer X.
Before using this function, set the corresponding port direction registers to output mode.

■Note on CNTR0 interrupt active edge selection

CNTR0 interrupt active edge depends on the CNTR0 active edge switch bit.

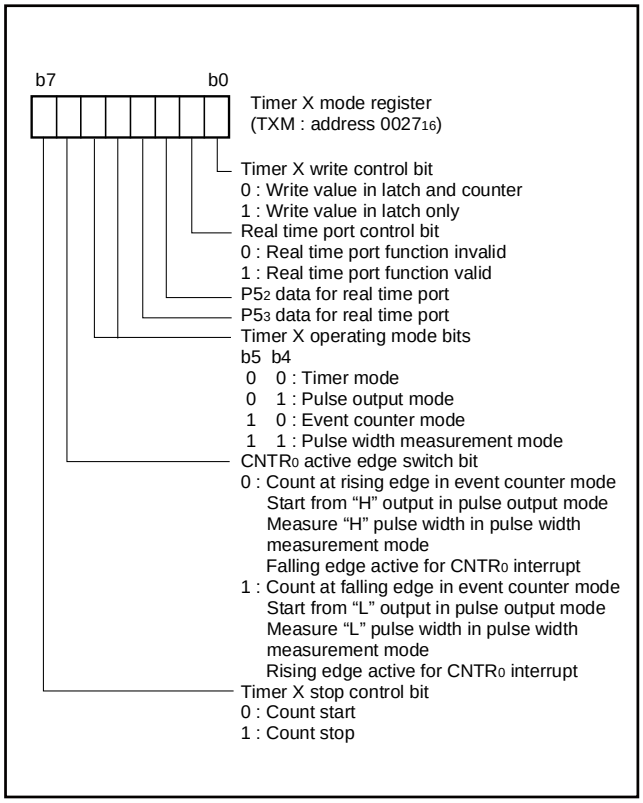


Fig. 23 Structure of timer X mode register

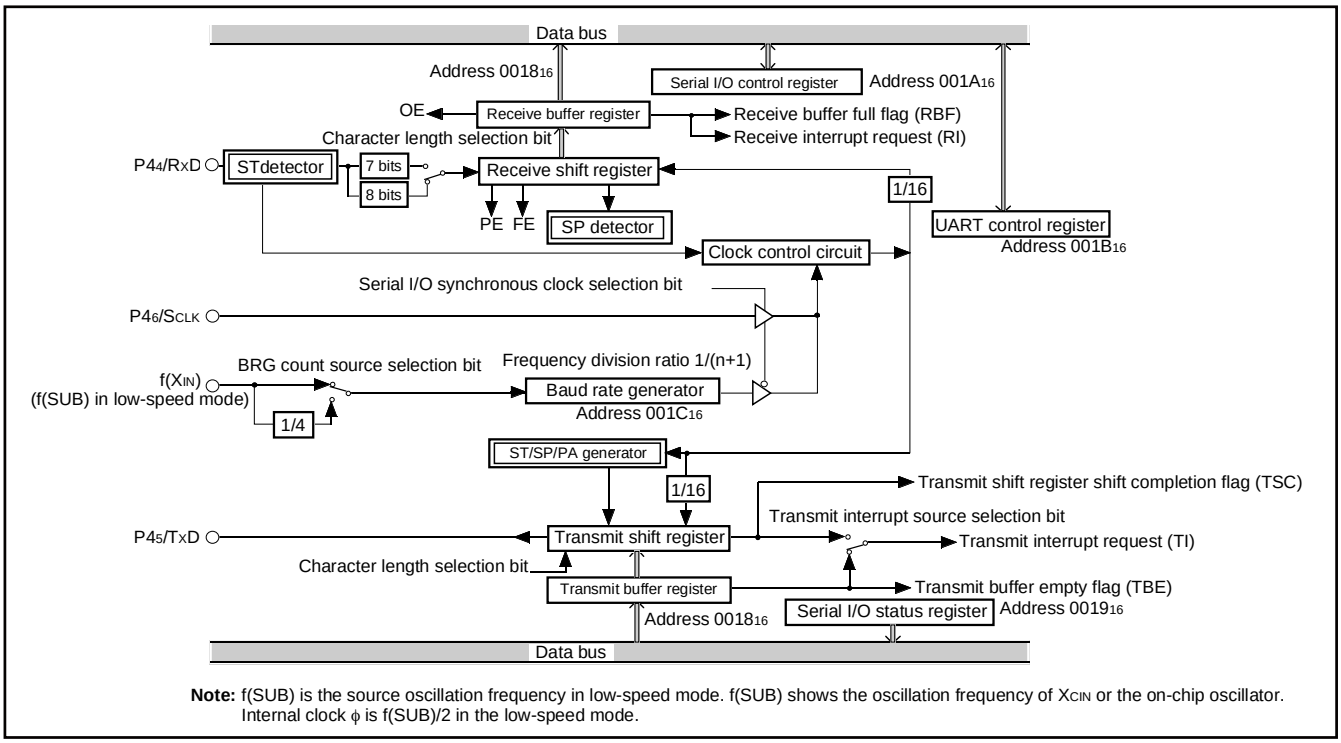
(2) Asynchronous Serial I/O (UART) Mode

Clock asynchronous serial I/O mode (UART) can be selected by clearing the serial I/O mode selection bit of the serial I/O control register to “0”.

Eight serial data transfer formats can be selected, and the transfer formats used by a transmitter and receiver must be identical.

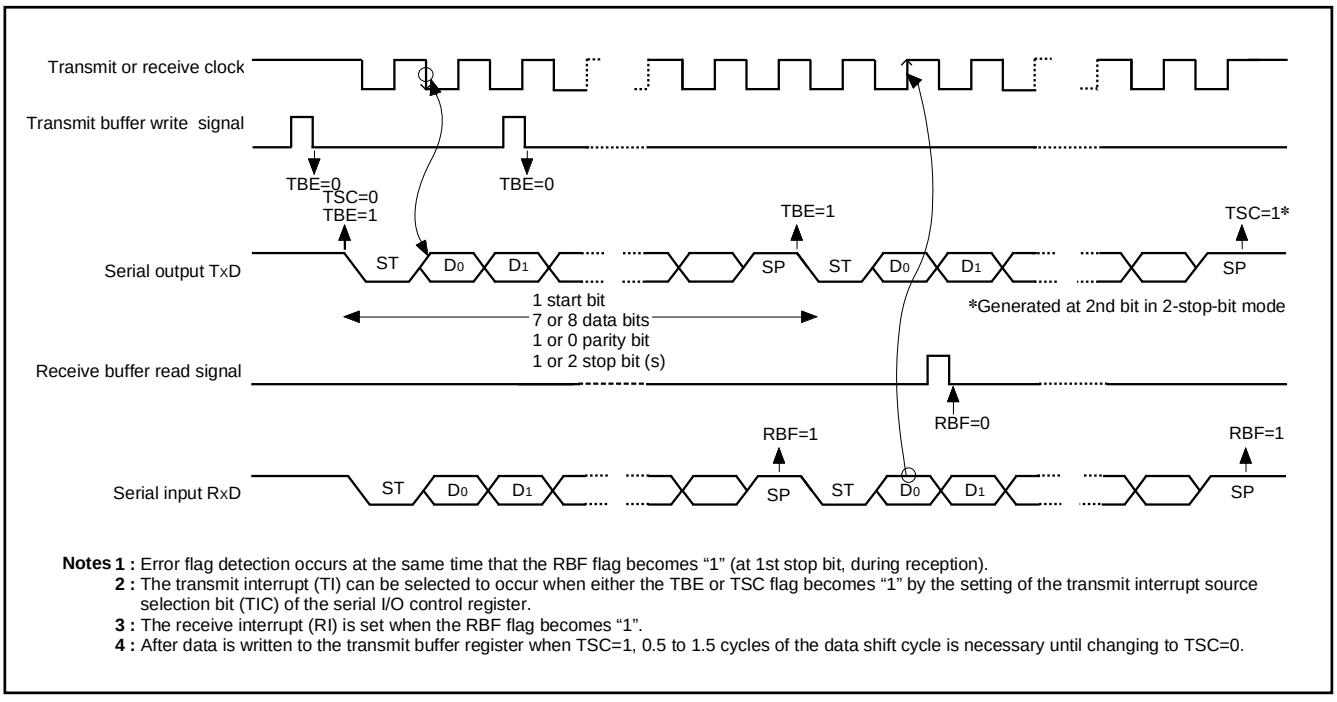
The transmit and receive shift registers each have a buffer register, but the two buffers have the same address in memory. Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer, and receive data is read from the receive buffer.

The transmit buffer can also hold the next data to be transmitted, and the receive buffer register can hold a character while the next character is being received.



Note: f(SUB) is the source oscillation frequency in low-speed mode. f(SUB) shows the oscillation frequency of XCIN or the on-chip oscillator. Internal clock ϕ is f(SUB)/2 in the low-speed mode.

Fig. 28 Block diagram of UART serial I/O



Notes 1 : Error flag detection occurs at the same time that the RBF flag becomes “1” (at 1st stop bit, during reception).
2 : The transmit interrupt (TI) can be selected to occur when either the TBE or TSC flag becomes “1” by the setting of the transmit interrupt source selection bit (TIC) of the serial I/O control register.
3 : The receive interrupt (RI) is set when the RBF flag becomes “1”.
4 : After data is written to the transmit buffer register when TSC=1, 0.5 to 1.5 cycles of the data shift cycle is necessary until changing to TSC=0.

Fig. 29 Operation of UART serial I/O function

[Transmit Buffer/Receive Buffer Register (TB/RB)] 0018$_{16}$

The transmit buffer register and the receive buffer register are located at the same address. The transmit buffer register is write-only and the receive buffer register is read-only. If a character bit length is 7 bits, the MSB of data stored in the receive buffer register is “0”.

[Serial I/O Status Register (SIOSTS)] 0019$_{16}$

The read-only serial I/O status register consists of seven flags (bits 0 to 6) which indicate the operating status of the serial I/O function and various errors.

Three of the flags (bits 4 to 6) are valid only in UART mode.

The receive buffer full flag (bit 1) is cleared to “0” when the receive buffer is read.

If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer register, and the receive buffer full flag is set. A write to the serial I/O status register clears all the error flags OE, PE, FE, and SE. Writing “0” to the serial I/O enable bit (SIOE) also clears all the status flags, including the error flags.

All bits of the serial I/O status register are initialized to “0” at reset, but if the transmit enable bit (bit 4) of the serial I/O control register has been set to “1”, the transmit shift register shift completion flag (bit 2) and the transmit buffer empty flag (bit 0) become “1”.

[Serial I/O Control Register (SIOCON)] 001A$_{16}$

The serial I/O control register contains eight control bits for the serial I/O function.

[UART Control Register (UARTCON)]001B$_{16}$

The UART control register consists of four control bits (bits 0 to 3) which are valid when asynchronous serial I/O is selected and set the data format of an data transfer. One bit in this register (bit 4) is always valid and sets the output structure of the P4$_5$/TxD pin.

[Baud Rate Generator (BRG)] 001C$_{16}$

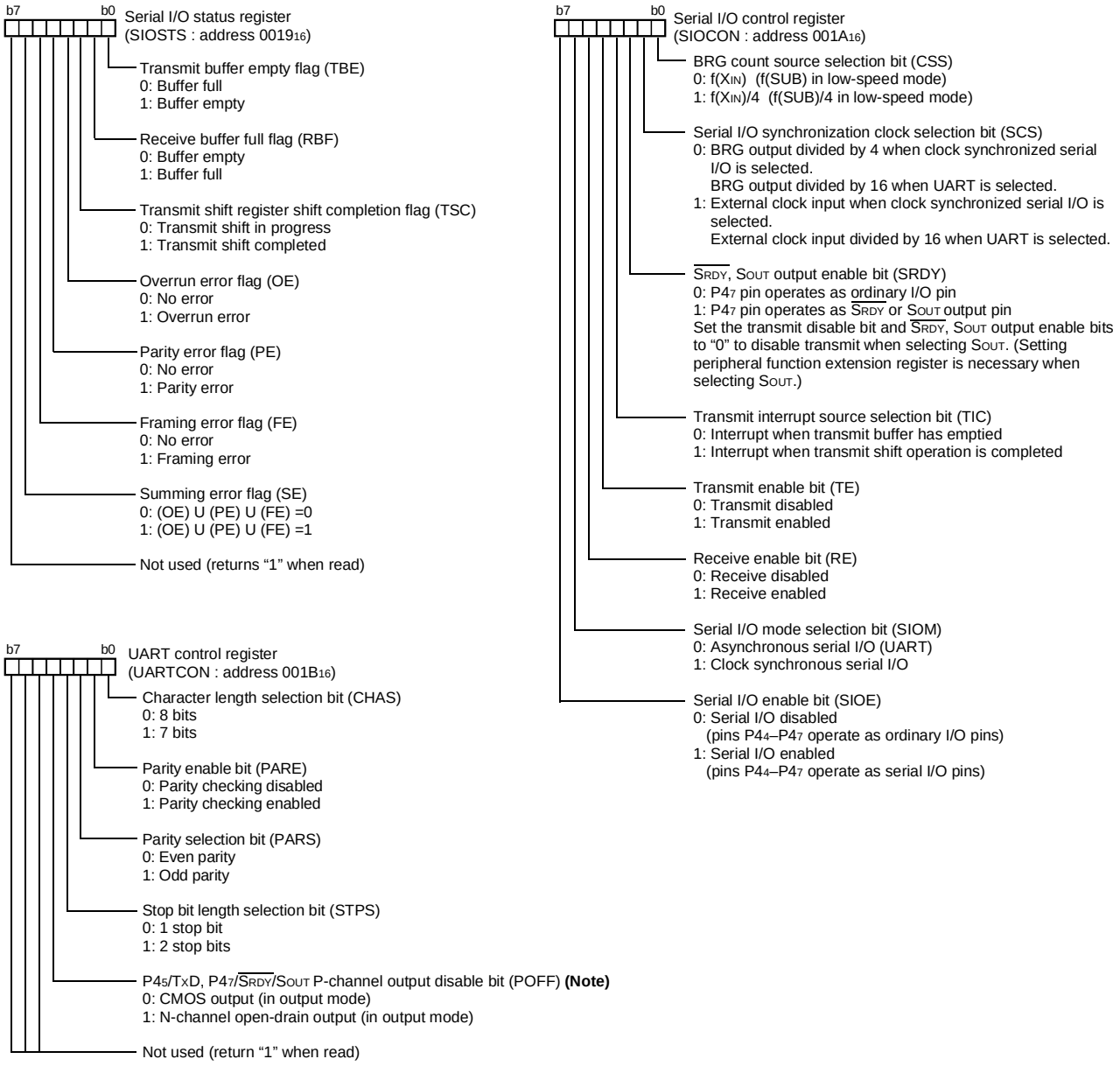
The baud rate generator determines the baud rate for serial transfer.

The baud rate generator divides the frequency of the count source by 1/(n + 1), where n is the value written to the baud rate generator.

■Notes on serial I/O

When setting the transmit enable bit to “1”, the serial I/O transmit interrupt request bit is automatically set to “1”. When not requiring the interrupt occurrence synchronized with the transmission enalbed, take the following sequence.

①Set the serial I/O transmit interrupt enable bit to “0” (disabled).
②Set the transmit enable bit to “1”.
③Set the serial I/O transmit interrupt request bit to “0” after 1 or more instructions have been executed.
④Set the serial I/O transmit interrupt enable bit to “1” (enabled).

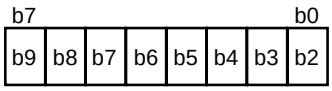


Notes 1 : The peripheral function extension register is used to choose P45/TxD, P47/SRDY/SOUT.
2 : f(SUB) is the source oscillation frequency in low-speed mode. f(SUB) shows the oscillation frequency of XCIN or the on-chip oscillator.

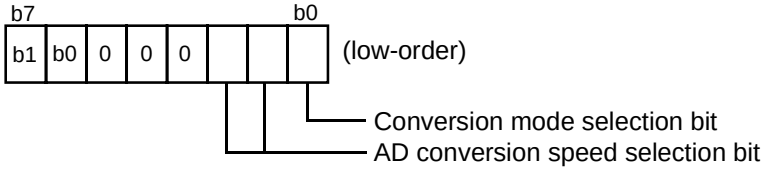
Fig. 32 Structure of serial I/O control registers

• 10 bit reading (Read address 0035$_{16}$ before 0036$_{16}$)

AD conversion high-order register (Address 0035$_{16}$) ADH



AD conversion low-order register (Address 0036$_{16}$) ADL



Note: The bit 5 to bit 3 of address 0036$_{16}$ become "0" at reading.

• 8 bit reading (Read only address 0035$_{16}$)

(Address 0035$_{16}$)

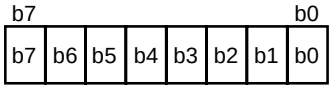


Fig. 34 A/D conversion register reading

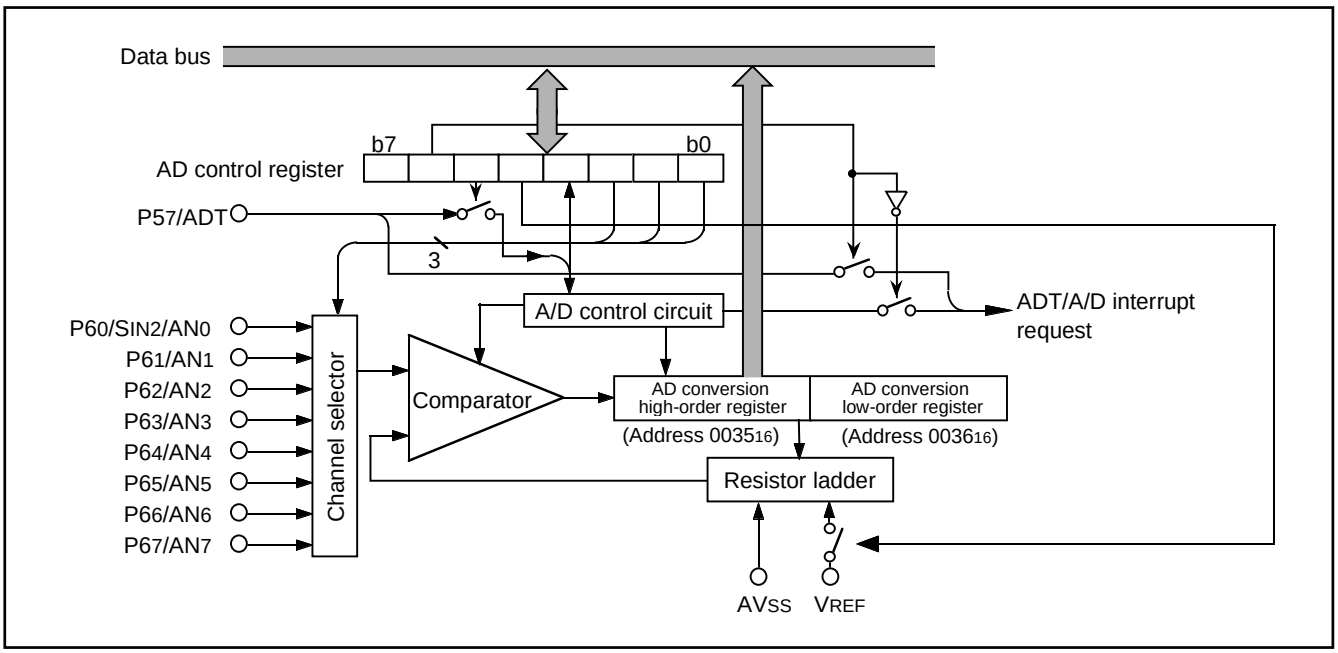


Fig. 35 A/D converter block diagram

Bias Control and Applied Voltage to LCD Power Input Pins

To the LCD power input pins (V_{L1}–V_{L3}), apply the voltage shown in Table 11 according to the bias value.

Select a bias value by the bias control bit (bit 2 of the LCD mode register).

Common Pin and Duty Ratio Control

The common pins (COM_0–COM_3) to be used are determined by duty ratio.

Select duty ratio by the duty ratio selection bits (bits 0 and 1 of the LCD mode register).

Table 11 Bias control and applied voltage to V_{L1}–V_{L3}

Bias value	Voltage value
1/3 bias	$V_{L3}=V_{LCD}$ $V_{L2}=2/3\ V_{LCD}$ $V_{L1}=1/3\ V_{LCD}$
1/2 bias	$V_{L3}=V_{LCD}$ $V_{L2}=V_{L1}=1/2\ V_{LCD}$

Note 1: V_{LCD} is the maximum value of supplied voltage for the LCD panel.

Table 12 Duty ratio control and common pins used

Duty ratio	Duty ratio selection bit		Common pins used
	Bit 1	Bit 0	
2	0	1	COM_0, COM_1 **(Note 1)**
3	1	0	COM_0–COM_2 **(Note 2)**
4	1	1	COM_0–COM_3

Notes1: COM_2 and COM_3 are open.
2: COM_3 is open.

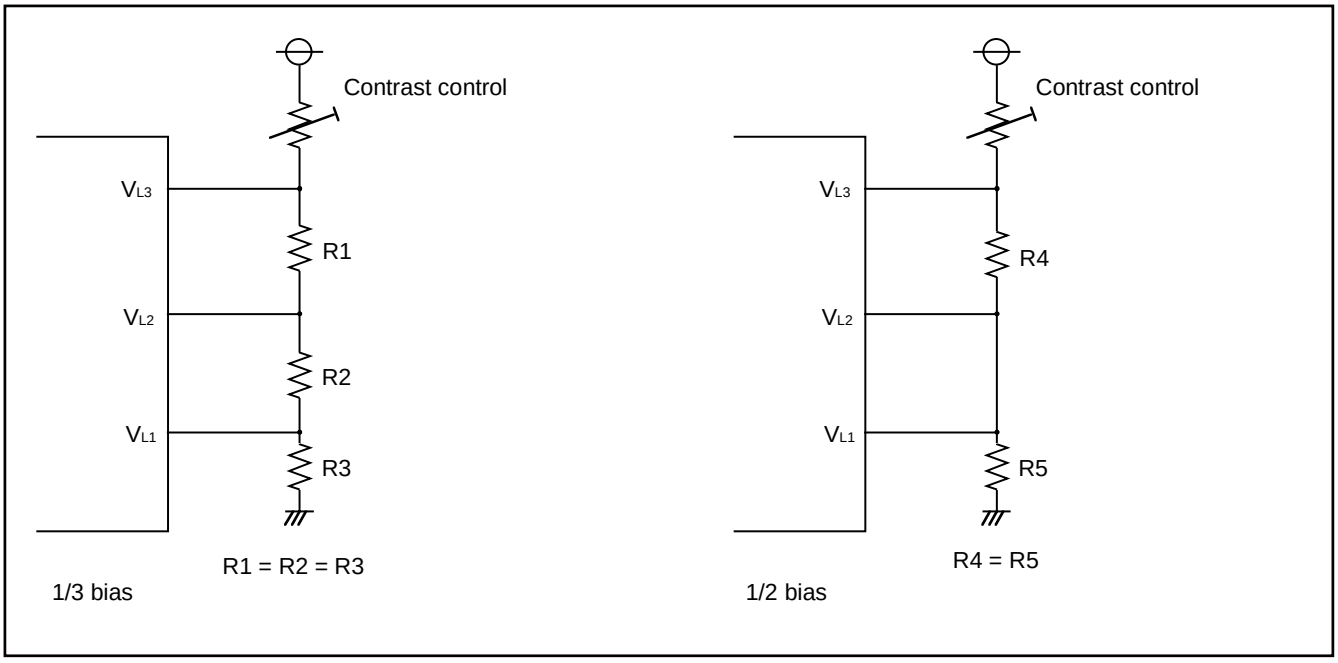


Fig. 38 Example of circuit at each bias

φ CLOCK SYSTEM OUTPUT FUNCTION

The internal system clock φ or XCIN frequency signal can be output from port P41 by setting the φ output control register. Set bit 1 of the port P4 direction register to "1" when outputting φ clock.

Set the bit 4 in the peripheral function expansion register to "1" when the XCIN frequency signal is output.

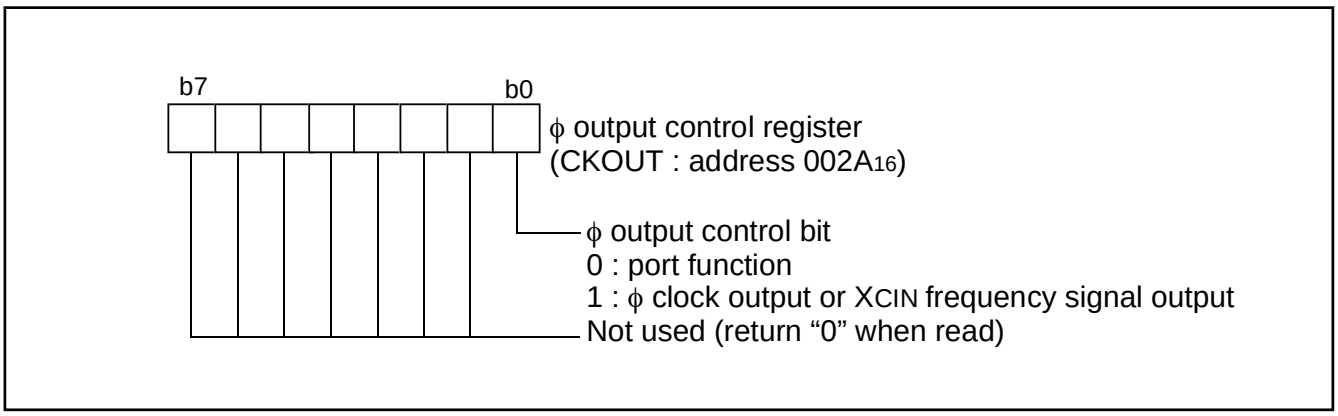


Fig. 45 Structure of φ output control register

Temporary data register

The temporary data register (addresses 002C16 to 002E16) is the 8-bit register and does not have the control function. It can be used to store data temporarily. It is initialized after reset.

RRF register

The RRF register (address 002F16)is the 8-bit register and does not have the control function. As for the value written in this register, high-order 4 bits and low-order 4 bits interchange. It is initialized after reset.

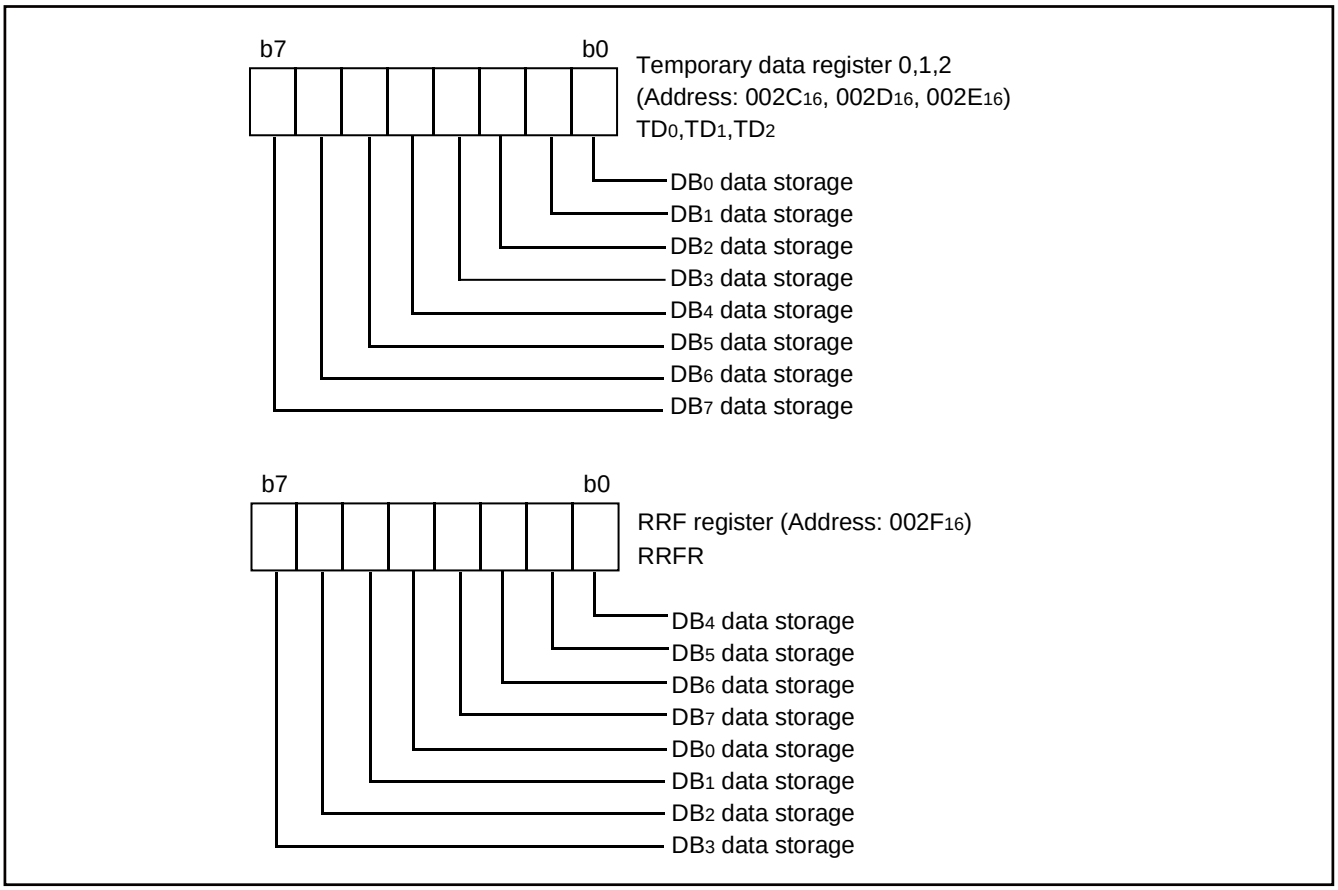


Fig. 46 Structure of temporary register, RPF register

RESET CIRCUIT

To reset the microcomputer, $\overline{\text{RESET}}$ pin should be held at an “L” level for 2 µs or more. Then the $\overline{\text{RESET}}$ pin is returned to an “H” level (the power source voltage should be between V_{CC}(min.) and 5.5 V, and the quartz-crystal oscillator should be stable), reset is released. After the reset is completed, the program starts from the address contained in address FFFD16 (high-order byte) and address FFFC16 (low-order byte). Make sure that the reset input voltage meets V_{IL} spec. when a power source voltage passes V_{CC}(min.).

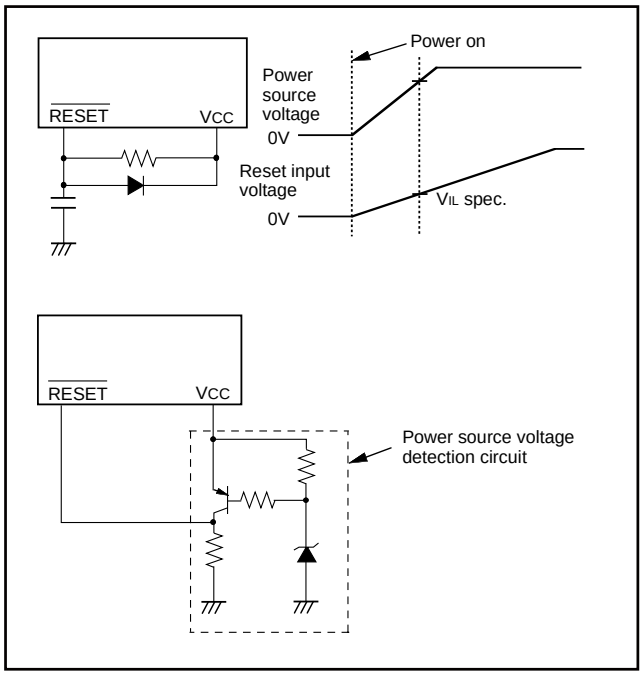
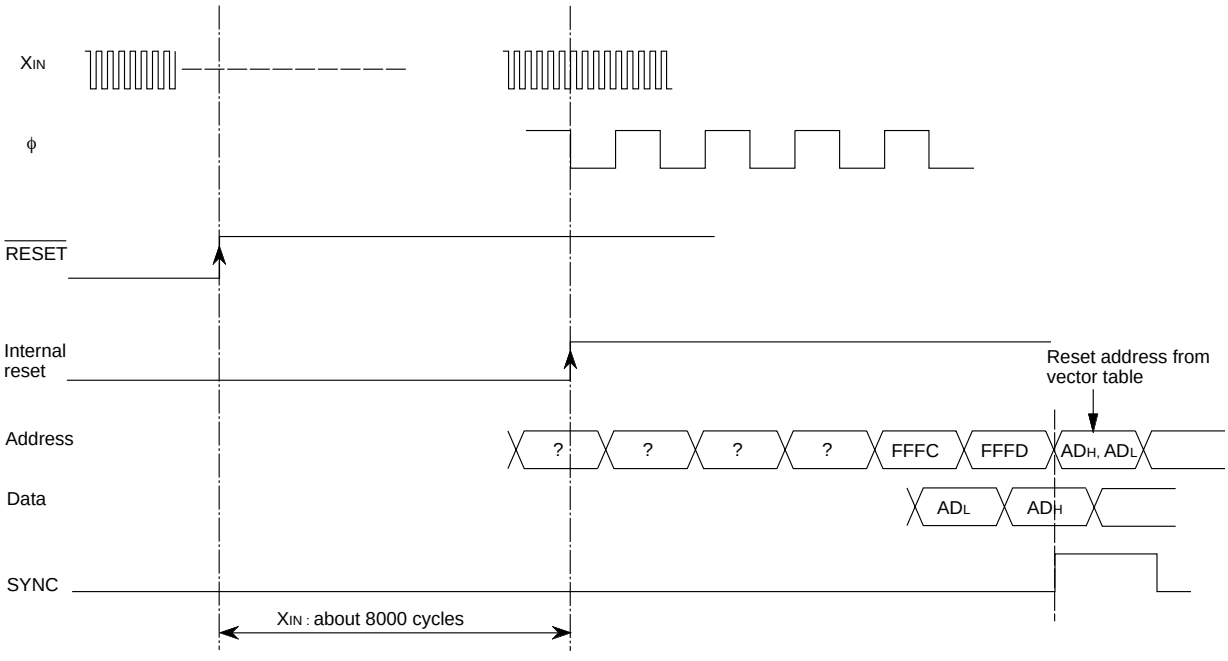


Fig. 51 Reset Circuit Example



Notes 1: The frequency relation of f(X_{IN}) and f(ϕ) is f(X_{IN}) =8•f(ϕ)
2: The question marks (?) indicate an undefined state that depends on the previous state.

Fig. 52 Reset Sequence

		Address	Register Contents
(1)	Port P0 direction register	000116	0016
(2)	Port P1 direction register	000316	0016
(3)	Port P2 direction register	000516	0016
(4)	Port P4 direction register	000916	0016
(5)	Port P5 direction register	000B16	0016
(6)	Port P6 direction register	000D16	0016
(7)	Port P7 direction register	000F16	0016
(8)	ROM correctoin enable register (RCR)	001416	0016
(9)	PULL register A	001616	0 0 0 0 1 0 1 1
(10)	PULL register B	001716	0016
(11)	Sirial I/O status register	001916	1 0 0 0 0 0 0 0
(12)	Sirial I/O control register	001A16	0016
(13)	UART control register	001B16	1 1 1 0 0 0 0 0
(14)	Timer X high-order register	002016	FF16
(15)	Timer X low-order register	002116	FF16
(16)	Timer Y high-order register	002216	FF16
(17)	Timer Y low-order register	002316	FF16
(18)	Timer 1 register	002416	FF16
(19)	Timer 2 register	002516	0116
(20)	Timer 3 register	002616	FF16
(21)	Timer X mode register	002716	0016
(22)	Timer Y mode register	002816	0016
(23)	Timer 123 mode register	002916	0016
(24)	ϕ output control register	002A16	0016
(25)	CPU mode extension register	002B16	0016
(26)	Temporary data register 0	002C16	0016
(27)	Temporary data register 1	002D16	0016
(28)	Temporary data register 2	002E16	0016
(29)	RRF register	002F16	0016
(30)	Peripheral function extension register	003016	0016
(31)	AD control register	003416	0 0 0 0 1 0 0 0
(32)	AD conversion low-order register	003616	X X 0 0 0 0 0 0
(33)	Watchdog timer control register	003716	0 0 1 1 1 1 1 1
(34)	Segment output enable register	003816	0016
(35)	LCD mode register	003916	0016
(36)	Interrupt edge selection register	003A16	0016
(37)	CPU mode register	003B16	0 1 0 0 1 0 0 0
(38)	Interrupt request register 1	003C16	0016
(39)	Interrupt request register 2	003D16	0016
(40)	Interrupt control register 1	003E16	0016
(41)	Interrupt control register 2	003F16	0016
(42)	Processor status register	(PS)	X X X X X 1 X X
(43)	Program counter	(PC_H)	Contents of address FFFD16
		(PC_L)	Contents of address FFFC16

Note: The contents of all other registers and RAM are undefined after reset, so they must be initialized by software.
X: undefined

Fig. 53 Initial status of microcomputer after reset

Oscillation Control

(1) Stop Mode

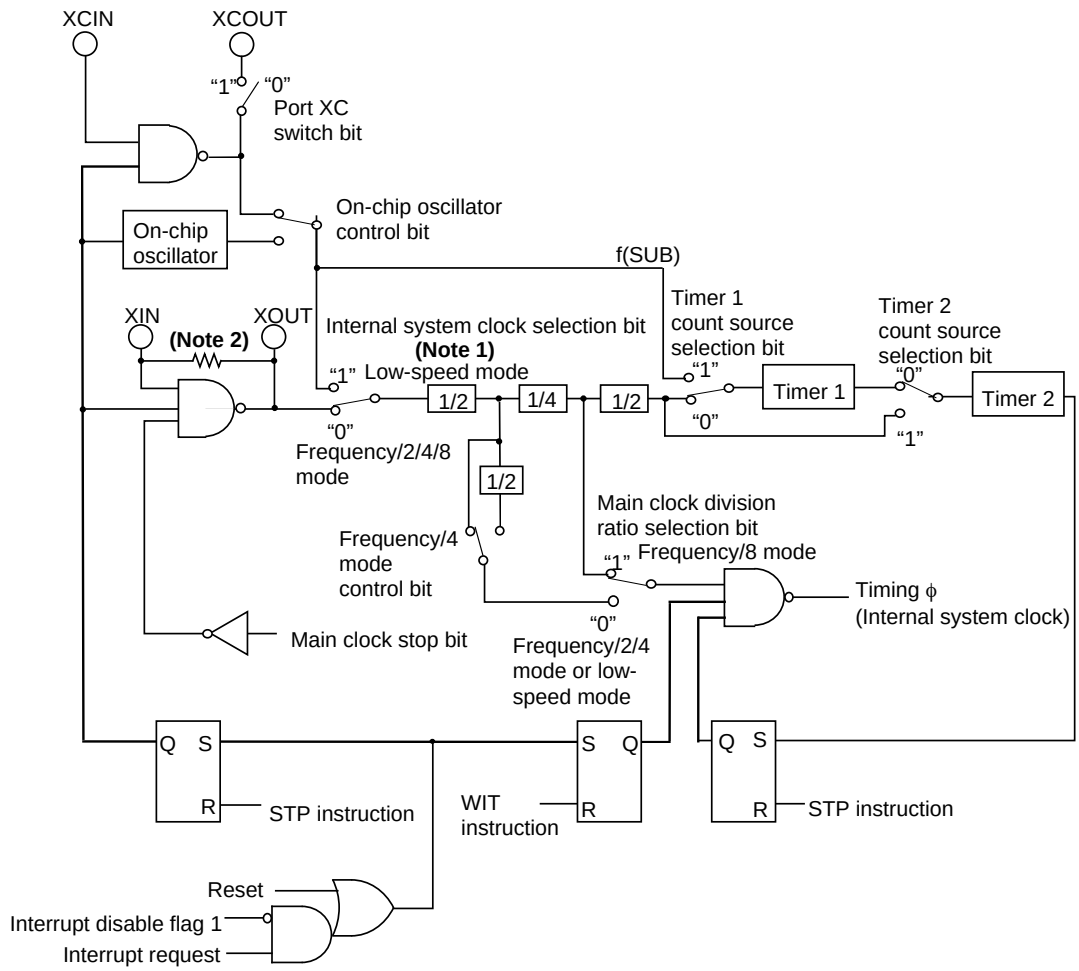
If the STP instruction is executed, the internal clock ϕ stops at an "H" level, and XIN and XCIN oscillators stop. Timer 1 is set to "FF16" and timer 2 is set to "0116".

Either XIN or XCIN divided by 16 is input to timer 1 as count source, and the output of timer 1 is connected to timer 2. The bits of the timer 123 mode register except bit 4 are cleared to "0". Set the timer 1 and timer 2 interrupt enable bits to disabled ("0") before executing the STP instruction. Oscillator restarts at reset or when an external interrupt is received, but the internal clock ϕ is not supplied to the CPU until timer 2 underflows. This allows timer for the clock circuit oscillation to stabilize.

Execution of the STP instruction sets the LCD enable bit (bit 3 of the LCD mode register) to "0" and the LCD panel turns off.To make the LCD panel turn on after returning from the stop mode, set the LCD enable bit to "1".

(2) Wait Mode

If the WIT instruction is executed, only the system clock ϕ stops at an "H" state. The states of main clock, on-chip oscillator and sub clock are the same as the state before executing the WIT instruction, and oscillation does not stop. Since supply of system clock ϕ is started immediately after the interrupt is received, the instruction can be executed immediately.



Notes 1: When using the low-speed mode, set the port XC switch bit to "1" .
2: Although a feed-back resistor exists on-chip, an external feed-back resistor may be needed depending on conditions.

Fig. 56 Clock generating circuit block diagram

Countermeasures against noise

(1) Shortest wiring length

① Wiring for RESET pin

Make the length of wiring which is connected to the RESET pin as short as possible. Especially, connect a capacitor across the RESET pin and the Vss pin with the shortest possible wiring (within 20mm).

● Reason

The width of a pulse input into the RESET pin is determined by the timing necessary conditions. If noise having a shorter pulse width than the standard is input to the RESET pin, the reset is released before the internal state of the microcomputer is completely initialized. This may cause a program runaway.

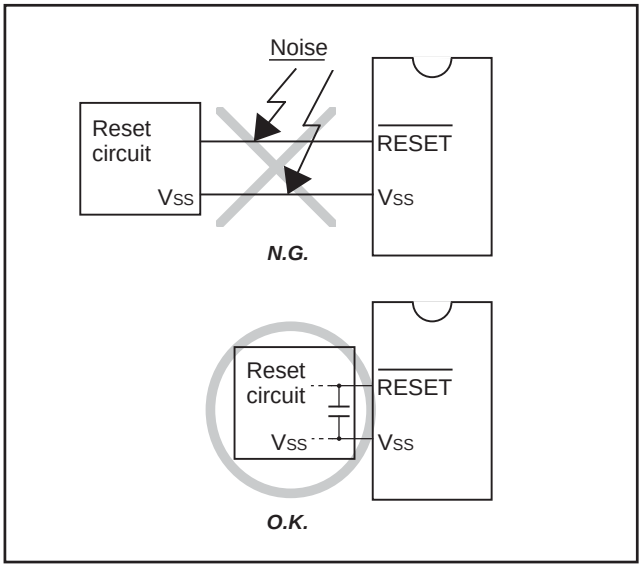


Fig. 62 Wiring for the RESET pin

② Wiring for clock input/output pins

- Make the length of wiring which is connected to clock I/O pins as short as possible.
- Make the length of wiring (within 20 mm) across the grounding lead of a capacitor which is connected to an oscillator and the Vss pin of a microcomputer as short as possible.
- Separate the Vss pattern only for oscillation from other Vss patterns.

● Reason

If noise enters clock I/O pins, clock waveforms may be deformed. This may cause a program failure or program runaway. Also, if a potential difference is caused by the noise between the Vss level of a microcomputer and the Vss level of an oscillator, the correct clock will not be input in the microcomputer.

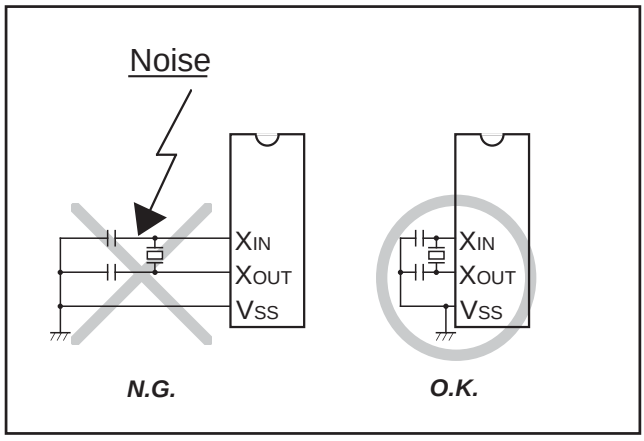


Fig. 63 Wiring for clock I/O pins

(2) Connection of bypass capacitor across Vss line and Vcc line

In order to stabilize the system operation and avoid the latch-up, connect an approximately 0.1 μF bypass capacitor across the Vss line and the Vcc line as follows:

- Connect a bypass capacitor across the Vss pin and the Vcc pin at equal length.
- Connect a bypass capacitor across the Vss pin and the Vcc pin with the shortest possible wiring.
- Use lines with a larger diameter than other signal lines for Vss line and Vcc line.
- Connect the power source wiring via a bypass capacitor to the Vss pin and the Vcc pin.

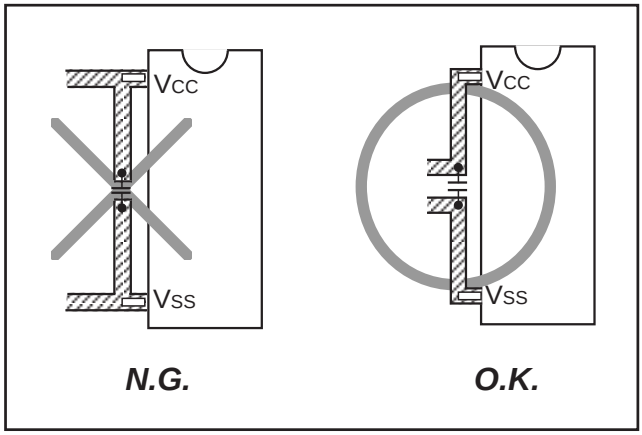


Fig. 64 Bypass capacitor across the Vss line and the Vcc line

REVISION HISTORY	3823 GROUP DATA SHEET

Rev.	Date	Description	
		Page	Summary
1.00	05/13/05		First edition
2.00	05/07/07	6 8 9 14 40 49 52 54 55 60	Table 3 is partly revised Fig.5 is partly added Table 4 is revised “ROM Code Protect Address” is added Fig.10 is revised “STP instruction Execution” is revised “Oscillation Control” (1) Stop Mode is partly revised “LCD drive Control Circuit” is revised “(6) Wiring to P40/(V_{PP}) pin” is revised Fig.59 is revised Fig.60 is partly deleted “NOTES ON QzROM” is added Table 18 is partly added
2.01	05/11/08	6 61 65-66	Table 3 is partly revised Table 19, 20 are partly revised PACKAGE OUTLINE revised
2.02	07/06/19	– 6 8 9 10 15 22 23-27 46 48 51 52 53 54 55-58 58 59 63 66	“RENESAS TECHNICAL UPDATE” reflected: TN-740-A111A/E Table 3: Function except a port function; •Serial I/O function pins → •Serial interface function pins Fig. 5 M38234G4, M38235G6: Under development → Mass production Note deleted Table 4: Under development deleted FUNCTIONAL DESCRIPTION CENTRAL PROCESSING UNIT (CPU): Description added Fig. 11: Note added CPU mode extension register ($002B_{16}$) → CPU mode expansion register Peripheral function extension register (0030_{16}) → Peripheral function expansion register Table 8: AV_{SS} added, Note revised INTERRUPTS: Description revised, Fig. 18-20 added ROM CORRECTION FUNCTION: Description added Initial Value of Watchdog Timer: Description added Standard Operation of Watchdog Timer: A part of description deleted Bit 6 and bit 7 of Watchdog Timer Control Register: added and revised Fig. 48 revised, Note added Fig. 53: Port P0 direction register (0000_{16}) → (0001_{16}) Frequency Control: Description revised Fig. 56: revised Fig. 57: revised QzROM Writing Mode: added Processor Status Register: added Overvoltage: Description revised and Fig. 68 added Table 15 V_{CC}: Frequency/4 mode → Frequency/8 mode V_{REF}: Limits Min. 2.0 → 1.8 Table 18: V_{RAM} added

Rev.	Date	Description	
		Page	Summary
2.02	07/06/19	67 72	Table 19 ROCO: Ta = 25 °C added Note added

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