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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	740
Core Size	8-Bit
Speed	10MHz
Connectivity	SIO, UART/USART
Peripherals	LCD, WDT
Number of I/O	49
Program Memory Size	60KB (60K x 8)
Program Memory Type	QzROM
EEPROM Size	-
RAM Size	2.5K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x8b, 8x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m3823agfhp-u0

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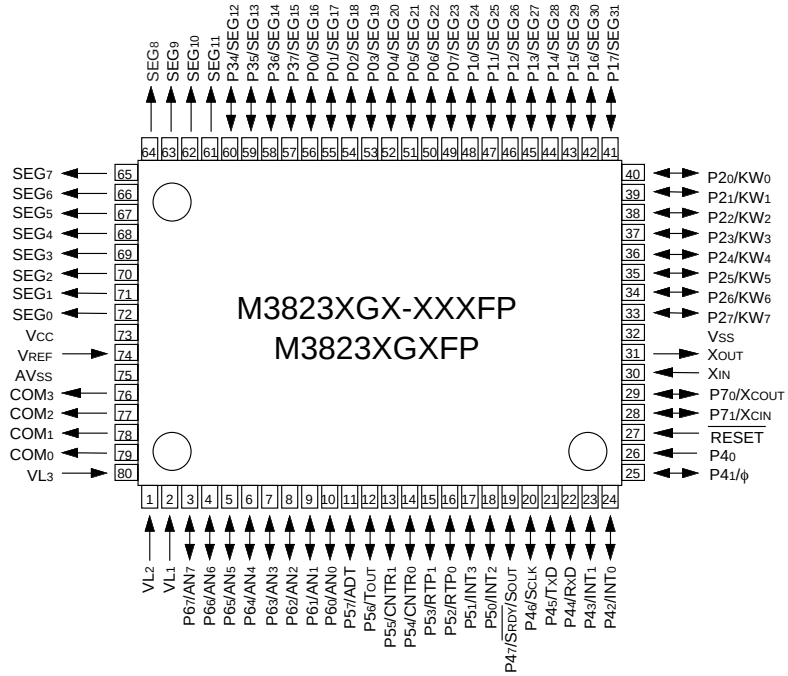
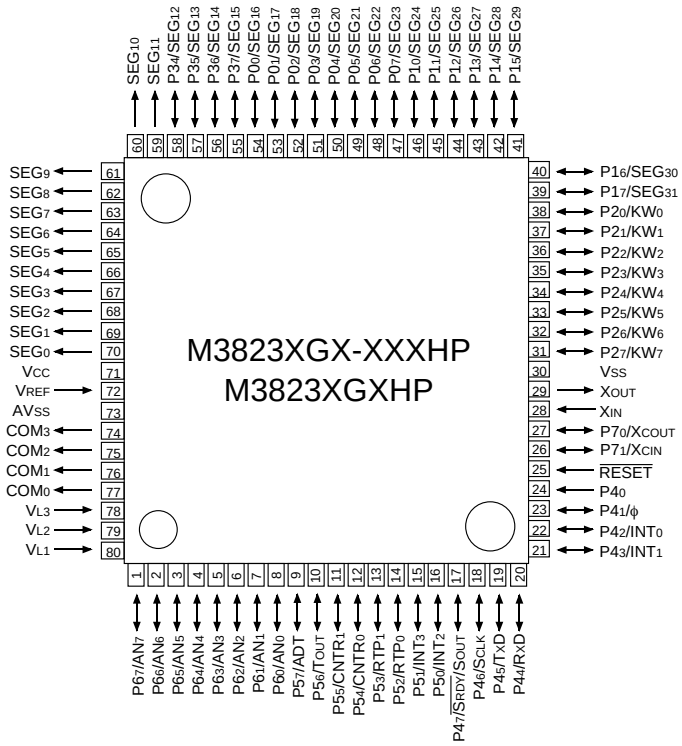
PIN CONFIGURATION (TOP VIEW)



Package code : PRQP0080GB-A (80P6N-A) (80-pin plastic-molded QFP)

Fig. 1 M3823XGX-XXXFP pin configuration

PIN CONFIGURATION (TOP VIEW)



Package code : PLQP0080KB-A (80P6Q-A) (80-pin plastic-molded LQFP)

Fig. 2 M3823XGX-XXXHP pin configuration

Table 1 Performance overview

Parameter		Function
Number of basic instructions		71
Instruction execution time		0.4 μs (Minimum instruction, f(XIN) 10 MHz, High-speed mode)
Oscillation frequency		10 MHz (Maximum)
Memory sizes	ROM	16 K to 60 K bytes
	RAM	640 to 2560 bytes
Input port	P34-P37, P40	4-bit × 1, 1-bit × 1 (4 pins sharing SEG)
I/O port	P0-P2, P41-P47, P5, P6, P70, P71	8-bit × 5, 7-bit × 1, 2 bit × 1 (16 pins sharing SEG)
Interrupt		17 sources, 16 vectors (includes key input interrupt)
Timer		8-bit × 3, 16-bit × 2
Serial interface		8-bit × 1 (UART or Clock-synchronized)
A/D converter		10-bit × 8 channels or 8 bit × 8 channels
Watchdog timer		8-bit × 1
ROM correction function		32 bytes × 2 blocks
LCD drive control circuit	Bias	1/2, 1/3
	Duty	2, 3, 4
	Common output	4
	Segment output	32
Main clock generating circuits		Built-in feedback resistor (connect to external ceramic rasonator or quartz-crystal oscillator)
Sub-clock generating circuits		Built-in feedback resistor (connect to external quartz-crystal oscillator or on-chip oscillator)
Power source voltage	In frequency/2 mode (f(XIN) ≤ 10MHz)	4.5 to 5.5V
	In frequency/2 mode (f(XIN) ≤ 8MHz)	4.0 to 5.5V
	In frequency/4 mode (f(XIN) ≤ 10MHz)	2.5 to 5.5V
	In frequency/4 mode (f(XIN) ≤ 8MHz)	2.0 to 5.5V
	In frequency/4 mode (f(XIN) ≤ 5MHz)	1.8 to 5.5V
	In frequency/8 mode (f(XIN) ≤ 10MHz)	2.5 to 5.5V
	In frequency/8 mode (f(XIN) ≤ 8MHz)	2.0 to 5.5V
	In frequency/8 mode (f(XIN) ≤ 5MHz)	1.8 to 5.5V
	In low-speed mode	1.8 to 5.5V
Power dissipation	In frequency/2 mode	Std. 18 mW (Vcc = 5V, f(XIN) = 8MHz, Ta = 25 °C)
	In low-speed mode at XCIN	Std. 18 μW (Vcc = 2.5V, f(XIN) = stopped, f(XCIN) = 32kHz, Ta = 25 °C)
	In low-speed mode at on-chip oscillator	Std. 35 μW (Vcc = 2.5V, f(XIN) = stopped, f(XCIN) = stopped, Ta = 25 °C)
Input/Output characteristics	Input/Output withstand voltage	VCC
	Output current	10mA
Operating temperature range		-20 to 85 °C
Device structure		CMOS sillicon gate
Package		80-pin plastic molded LQFP/QFP

GROUP EXPANSION

Mitsubishi plans to expand the 3823 group as follows:

Memory Type

Support for QzROM version.

Memory Size

ROM size ..... 16 K to 60 K bytes
RAM size ..... 640 to 2560 bytes

Package

PRQP0080GB-A ..... 0.8 mm-pitch plastic molded QFP
PLQP0080KB-A ..... 0.5 mm-pitch plastic molded LQFP

Memory Expansion Plan

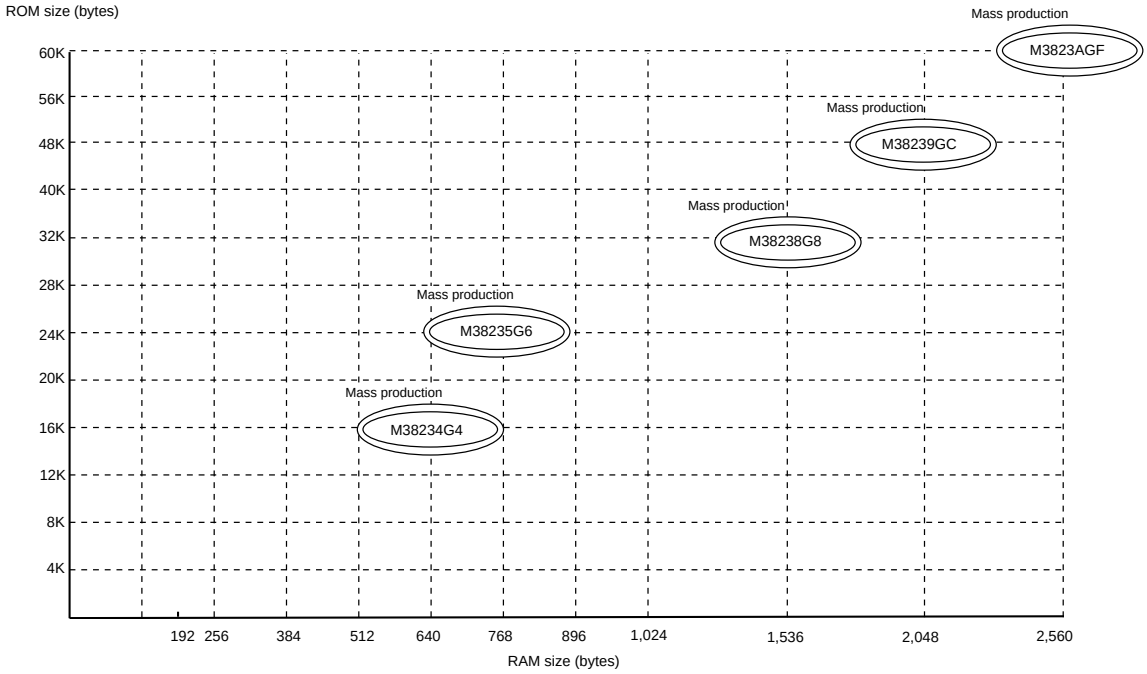


Fig. 5 Memory expansion plan

0000₁₆	Port P0 register (P0)
0001₁₆	Port P0 direction register (P0D)
0002₁₆	Port P1 register (P1)
0003₁₆	Port P1 direction register (P1D)
0004₁₆	Port P2 register (P2)
0005₁₆	Port P2 direction register (P2D)
0006₁₆	Port P3 register (P3)
0007₁₆	
0008₁₆	Port P4 register (P4)
0009₁₆	Port P4 direction register (P4D)
000A₁₆	Port P5 register (P5)
000B₁₆	Port P5 direction register (P5D)
000C₁₆	Port P6 register (P6)
000D₁₆	Port P6 direction register (P6D)
000E₁₆	Port P7 register (P7)
000F₁₆	Port P7 direction register (P7D)
0010₁₆	ROM correction address 1 high-order register (RCA1H)
0011₁₆	ROM correction address 1 low-order register (RCA1L)
0012₁₆	ROM correction address 2 high-order register (RCA2H)
0013₁₆	ROM correction address 2 low-order register (RCA2L)
0014₁₆	ROM correction enable register (RCR)
0015₁₆	
0016₁₆	PULL register A (PULLA)
0017₁₆	PULL register B (PULLB)
0018₁₆	Transmit/Receive buffer register(TB/RB)
0019₁₆	Serial I/O status register (SIOSTS)
001A₁₆	Serial I/O control register (SIO1CON)
001B₁₆	UART control register (UARTCON)
001C₁₆	Baud rate generator (BRG)
001D₁₆	
001E₁₆	
001F₁₆	

0020₁₆	Timer X low-order register (TXL)
0021₁₆	Timer X high-order register (TXH)
0022₁₆	Timer Y low-order register (TYL)
0023₁₆	Timer Y high-order register (TYH)
0024₁₆	Timer 1 register (T1)
0025₁₆	Timer 2 register (T2)
0026₁₆	Timer 3 register (T3)
0027₁₆	Timer X mode register (TXM)
0028₁₆	Timer Y mode register (TYM)
0029₁₆	Timer 123 mode register (T123M)
002A₁₆	ϕ output control register (CKOUT)
002B₁₆	CPU mode expansion register (EXPCM)
002C₁₆	Temporary data register 0 (TD0)
002D₁₆	Temporary data register 1 (TD1)
002E₁₆	Temporary data register 2 (TD2)
002F₁₆	RRF register (RRFR)
0030₁₆	Peripheral function expansion register (EXP)
0031₁₆	
0032₁₆	
0033₁₆	
0034₁₆	AD control register (ADCON)
0035₁₆	AD conversion high-order register (ADH)
0036₁₆	AD conversion low-order register (ADL)
0037₁₆	Watchdog timer register (WDT)
0038₁₆	Segment output enable register (SEG)
0039₁₆	LCD mode register (LM)
003A₁₆	Interrupt edge selection register (INTEDGE)
003B₁₆	CPU mode register (CPUM)
003C₁₆	Interrupt request register 1(IREQ1)
003D₁₆	Interrupt request register 2(IREQ2)
003E₁₆	Interrupt control register 1(ICON1)
003F₁₆	Interrupt control register 2(ICON2)

Note: Do not access to the SFR area including nothing.

Fig. 11 Memory map of special function register (SFR)

I/O PORTS

Direction Registers (ports P2, P41-P47, and P5-P7)

The 3823 group has 49 programmable I/O pins arranged in seven I/O ports (ports P0–P2, P41–P47 and P5-P7). The I/O ports P2, P41–P47 and P5-P7 have direction registers which determine the input/output direction of each individual pin. Each bit in a direction register corresponds to one pin, and each pin can be set to be input port or output port.

When “0” is written to the bit corresponding to a pin, that pin becomes an input pin. When “1” is written to that bit, that pin becomes an output pin.

If data is read from a pin set to output, the value of the port output latch is read, not the value of the pin itself. Pins set to input are floating. If a pin set to input is written to, only the port output latch is written to and the pin remains floating.

Direction Registers (ports P0 and P1)

Ports P0 and P1 have direction registers which determine the input/output direction of each individual port.

Each port in a direction register corresponds to one port, each port can be set to be input or output. When “0” is written to the bit 0 of a direction register, that port becomes an input port. When “1” is written to that port, that port becomes an output port. Bits 1 to 7 of ports P0 and P1 direction registers are not used.

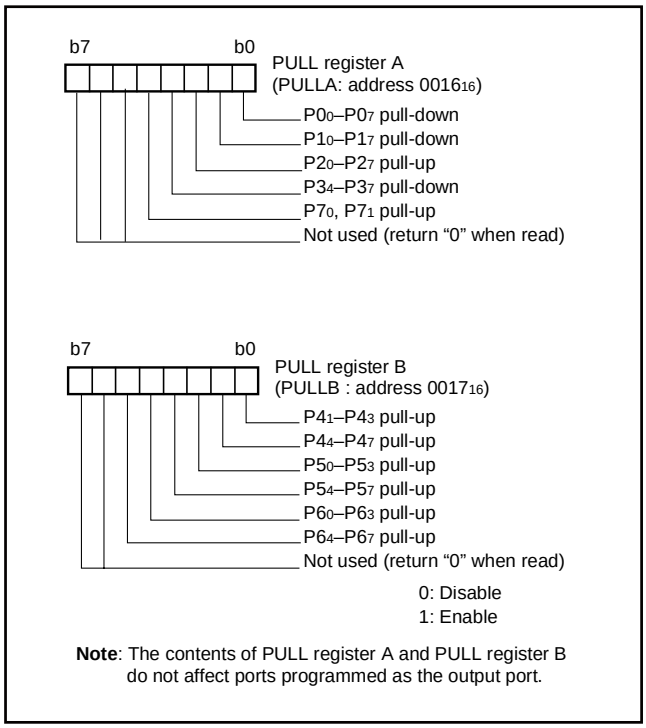
Ports P3 and P40

These ports are only for input.

Pull-up/Pull-down Control

By setting the PULL register A (address 0016$_{16}$) or the PULL register B (address 0017$_{16}$), ports except for port P40 can control either pull-down or pull-up (pins that are shared with the segment output pins for LCD are pull-down; all other pins are pull-up) with a program.

However, the contents of PULL register A and PULL register B do not affect ports programmed as the output ports.



Note: The contents of PULL register A and PULL register B do not affect ports programmed as the output port.

Fig. 12 Structure of PULL register A and PULL register B

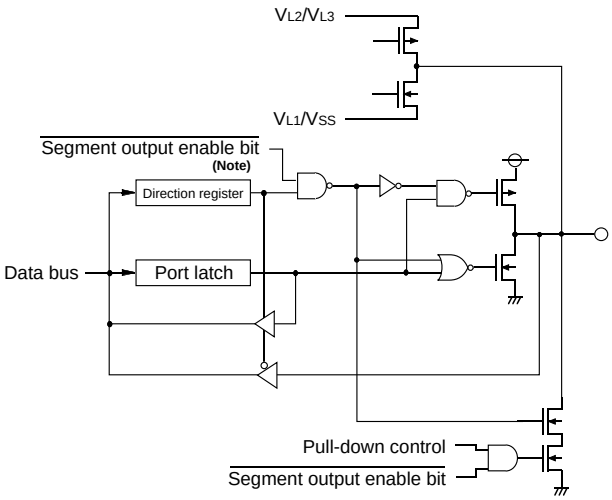
Table 7 List of I/O port function

Pin	Name	Input/Output	I/O Format	Non-Port Function	Related SFRs	Diagram No.
P0$_0$/SEG$_{16}$–P0$_7$/SEG$_{23}$	Port P0	Input/output, individual ports	CMOS compatible input level CMOS 3-state output	LCD segment output	PULL register A Segment output enable register	(1)
P1$_0$/SEG$_{24}$–P1$_7$/SEG$_{31}$	Port P1					
P2$_0$/KW$_0$–P2$_7$/KW$_7$	Port P2	Input/output, individual bits	CMOS compatible input level CMOS 3-state output	Key input (key-on wake-up) interrupt input	PULL register A Interrupt control register 2	(2)
P3$_4$/SEG$_{12}$–P3$_7$/SEG$_{15}$	Port P3	Input	CMOS compatible input level	LCD segment output	PULL register A Segment output enable register	(3)
P4$_0$	Port P4	Input	CMOS compatible input level	QzROM program power pin		(4)
P4$_1$/ϕ		Input/output, individual bits	CMOS compatible input level CMOS 3-state output	ϕ clock output X$_{CIN}$ frequency signal output	PULL register B ϕ output control register Peripheral function extension register	(5)
P4$_2$/INT$_0$, P4$_3$/INT$_1$				External interrupt input	PULL register B Interrupt edge selection register	(2)
P4$_4$/RxD				Serial I/O function input/output	PULL register B	(6)
P4$_5$/TxD					Serial I/O control register	(7)
P4$_6$/SCLK					Serial I/O status register	(8)
P4$_7$/$\overline{\text{SRDY}}$/SOUT					UART control register Peripheral function extension register	(9)
P5$_0$/INT$_2$, P5$_1$/INT$_3$	Port P5	Input/output, individual bits	CMOS compatible input level CMOS 3-state output	External interrupt input	PULL register B Interrupt edge selection register	(2)
P5$_2$/RTP$_0$, P5$_3$/RTP$_1$				Real time port function output	PULL register B Timer X mode register	(10)
P5$_4$/CNTR$_0$				Timer X function I/O	PULL register B Timer X mode register	(11)
P5$_5$/CNTR$_1$				Timer Y function input	PULL register B Timer Y mode register	(12)
P5$_6$/TOUT				Timer 2 function output	PULL register B Timer 123 mode register	(13)
P5$_7$/ADT				A/D trigger input	PULL register B	(12)
P6$_0$/AN$_0$–P6$_7$/AN$_7$	Port P6	Input/output, individual bits	CMOS compatible input level CMOS 3-state output	A/D conversion input	A/D control register	(14)
P7$_0$/XCOUT	Port P7	Input/output, individual bits	CMOS compatible input level CMOS 3-state output	Sub-clock generating circuit I/O	PULL register A CPU mode register	(15)
P7$_1$/XCIN						(16)
COM$_0$–COM$_3$	Common	Output	LCD common output		LCD mode register	(17)
SEG$_0$–SEG$_{11}$	Segment	Output	LCD segment output			(18)

Notes 1: For details of how to use double function ports as function I/O ports, refer to the applicable sections.

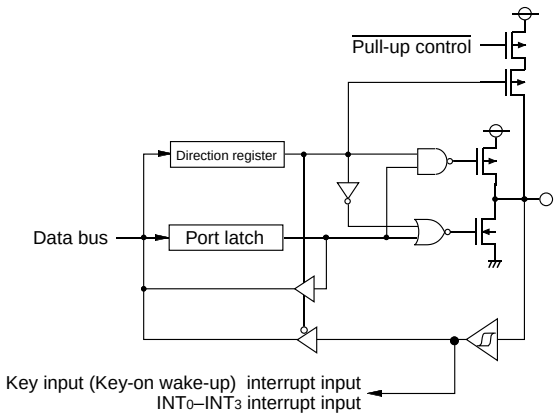
2: When an input level is at an intermediate potential, a current will flow from V_{CC} to V_{SS} through the input-stage gate. Especially, power source current may increase during execution of the STP and WIT instructions. Fix the unused input pins to "H" or "L" through a resistor.

(1) Ports P0, P1

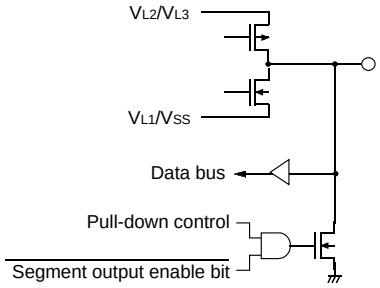


Note: Bit 0 of direction register.

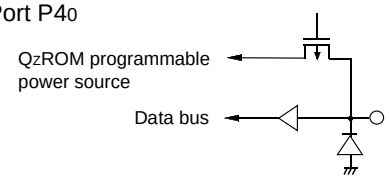
(2) Ports P2, P42, P43, P50, P51



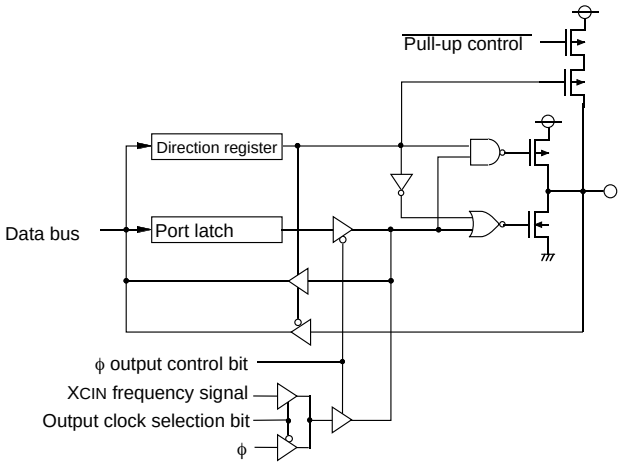
(3) Ports P34–P37



(4) Port P40



(5) Port P41



(6) Port P44

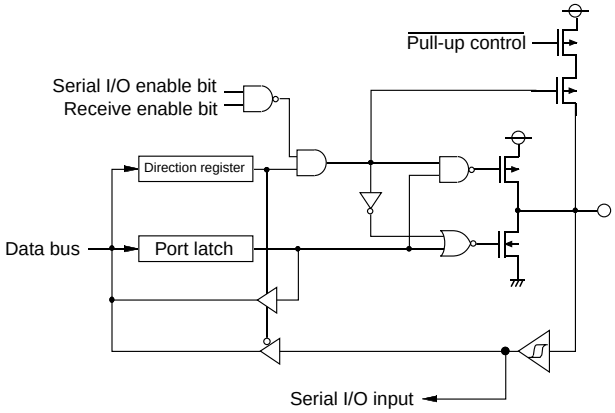


Fig. 13 Port block diagram (1)

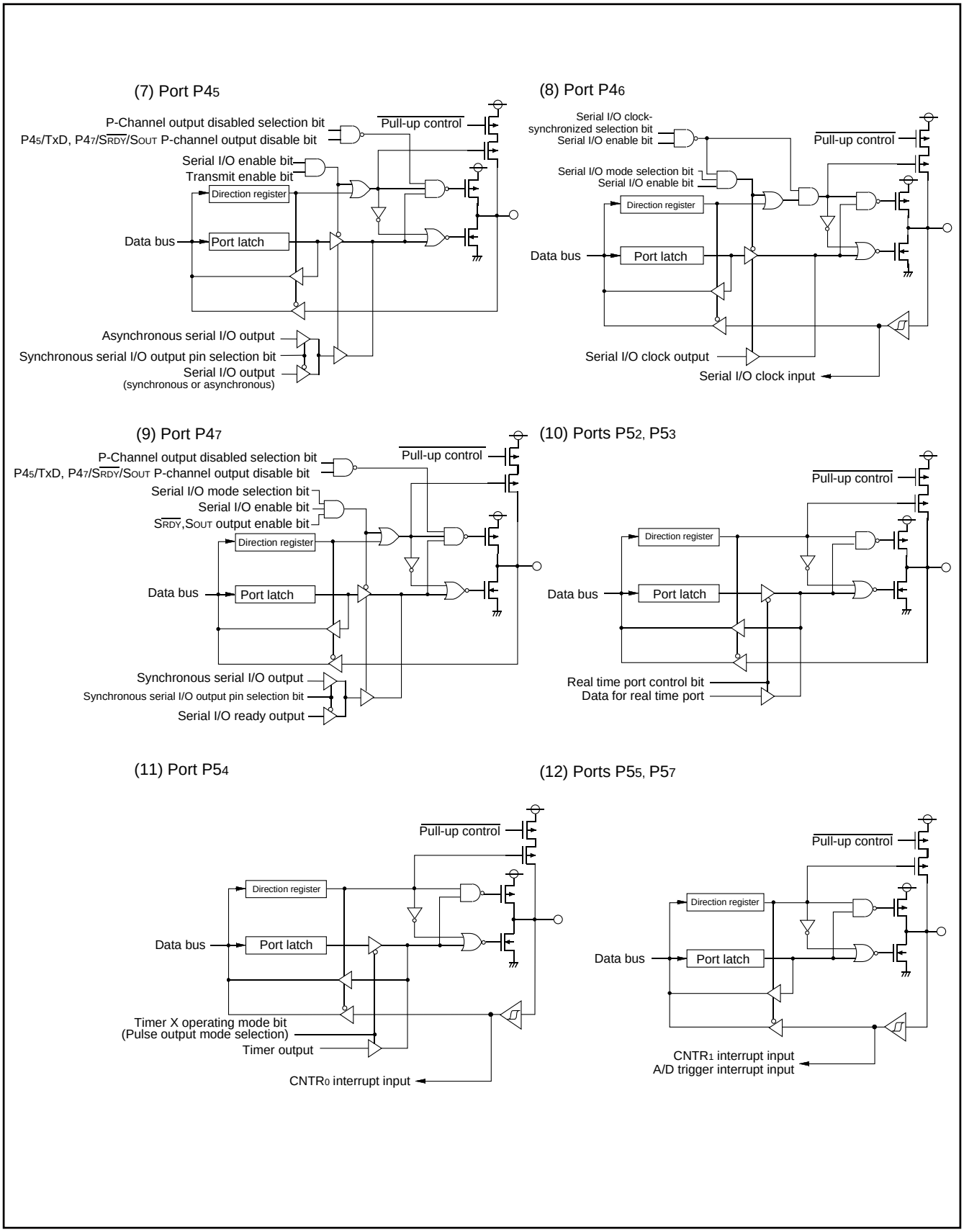
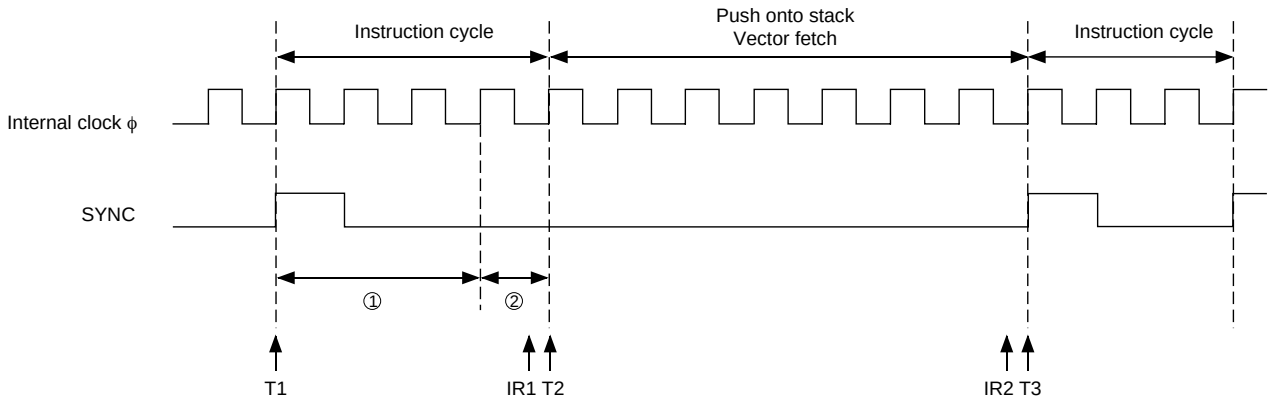


Fig. 14 Port block diagram (2)



T1 T2 T3: Interrupt acceptance timing points
IR1 IR2: Timings points at which the interrupt request bit is set to “1”.

Note: Period 2 indicates the last ϕ cycle during one instruction cycle.

(1) The interrupt request bit for an interrupt request generated during period 1 is set to “1” at timing point IR1.
(2) The interrupt request bit for an interrupt request generated during period 2 is set to “1” at timing point IR1 or IR2. The timing point at which the bit is set to “1” varies depending on conditions. When two or more interrupt requests are generated during the period 2, each request bit may be set to “1” at timing point IR1 or IR2 separately.

Fig. 20 Timing of interrupt request generation, interrupt request bit, and interrupt acceptance

[Transmit Buffer/Receive Buffer Register (TB/RB)] 0018$_{16}$

The transmit buffer register and the receive buffer register are located at the same address. The transmit buffer register is write-only and the receive buffer register is read-only. If a character bit length is 7 bits, the MSB of data stored in the receive buffer register is “0”.

[Serial I/O Status Register (SIOSTS)] 0019$_{16}$

The read-only serial I/O status register consists of seven flags (bits 0 to 6) which indicate the operating status of the serial I/O function and various errors.

Three of the flags (bits 4 to 6) are valid only in UART mode.

The receive buffer full flag (bit 1) is cleared to “0” when the receive buffer is read.

If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer register, and the receive buffer full flag is set. A write to the serial I/O status register clears all the error flags OE, PE, FE, and SE. Writing “0” to the serial I/O enable bit (SIOE) also clears all the status flags, including the error flags.

All bits of the serial I/O status register are initialized to “0” at reset, but if the transmit enable bit (bit 4) of the serial I/O control register has been set to “1”, the transmit shift register shift completion flag (bit 2) and the transmit buffer empty flag (bit 0) become “1”.

[Serial I/O Control Register (SIOCON)] 001A$_{16}$

The serial I/O control register contains eight control bits for the serial I/O function.

[UART Control Register (UARTCON)]001B$_{16}$

The UART control register consists of four control bits (bits 0 to 3) which are valid when asynchronous serial I/O is selected and set the data format of an data transfer. One bit in this register (bit 4) is always valid and sets the output structure of the P4$_5$/TxD pin.

[Baud Rate Generator (BRG)] 001C$_{16}$

The baud rate generator determines the baud rate for serial transfer.

The baud rate generator divides the frequency of the count source by 1/(n + 1), where n is the value written to the baud rate generator.

■Notes on serial I/O

When setting the transmit enable bit to “1”, the serial I/O transmit interrupt request bit is automatically set to “1”. When not requiring the interrupt occurrence synchronized with the transmission enalbed, take the following sequence.

①Set the serial I/O transmit interrupt enable bit to “0” (disabled).
②Set the transmit enable bit to “1”.
③Set the serial I/O transmit interrupt request bit to “0” after 1 or more instructions have been executed.
④Set the serial I/O transmit interrupt enable bit to “1” (enabled).

Fig. 34 A/D conversion register reading

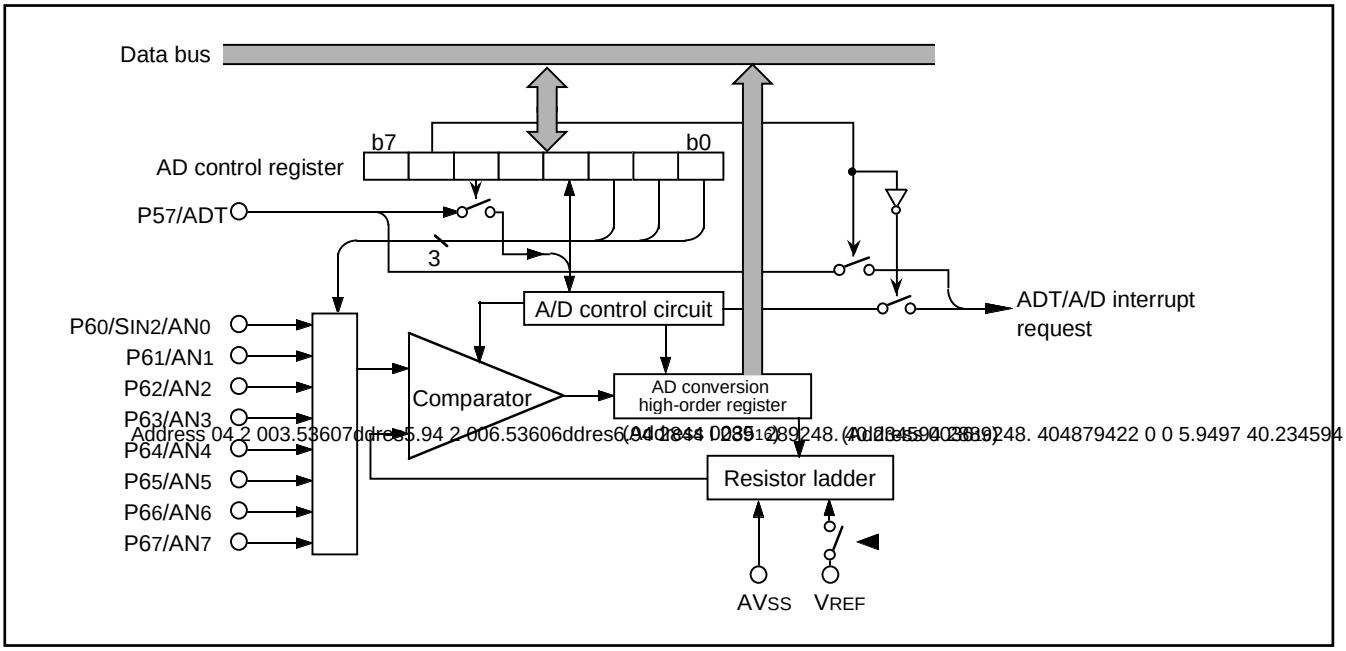


Fig. 35 A/D converter block diagram

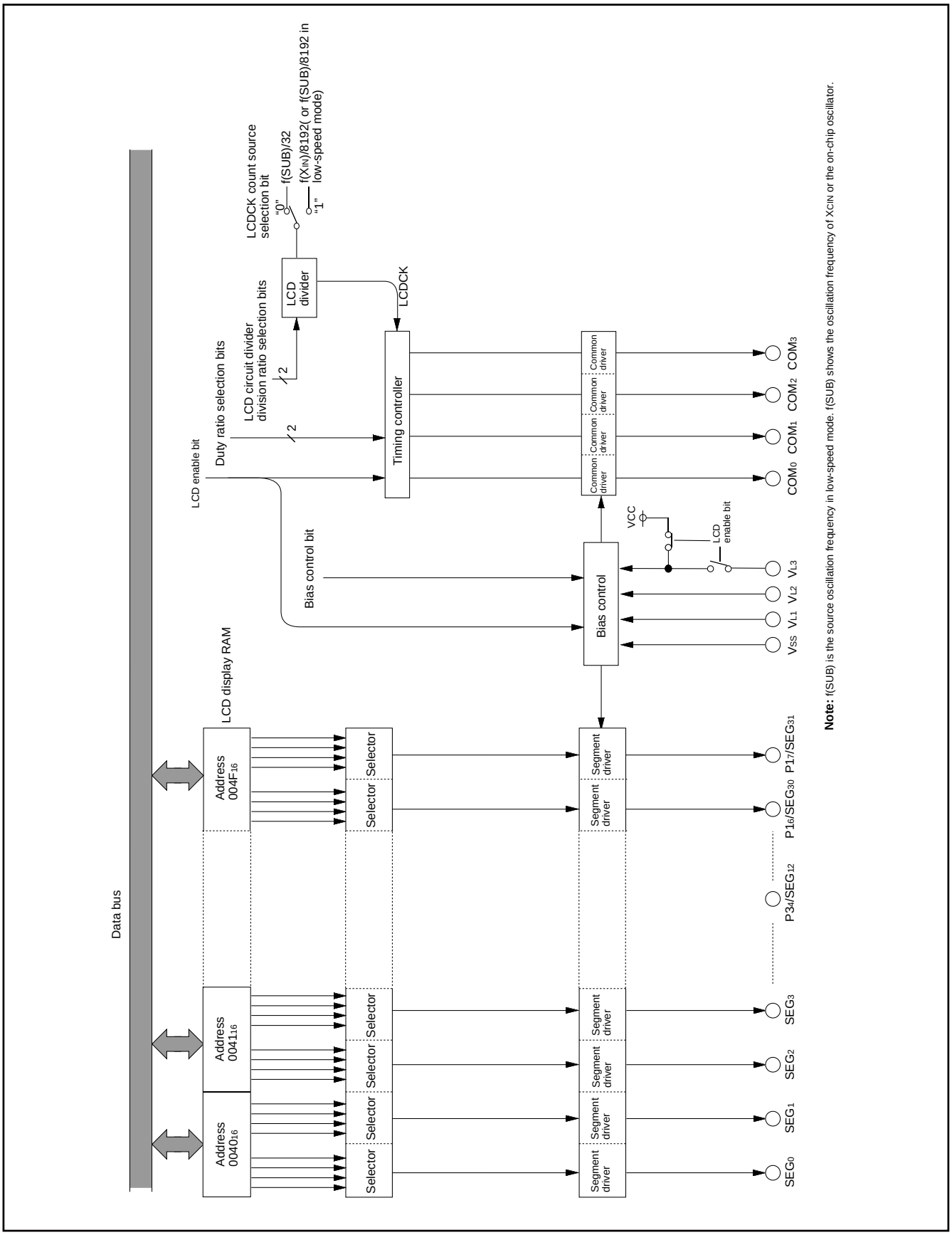


Fig. 37 Block diagram of LCD controller/driver

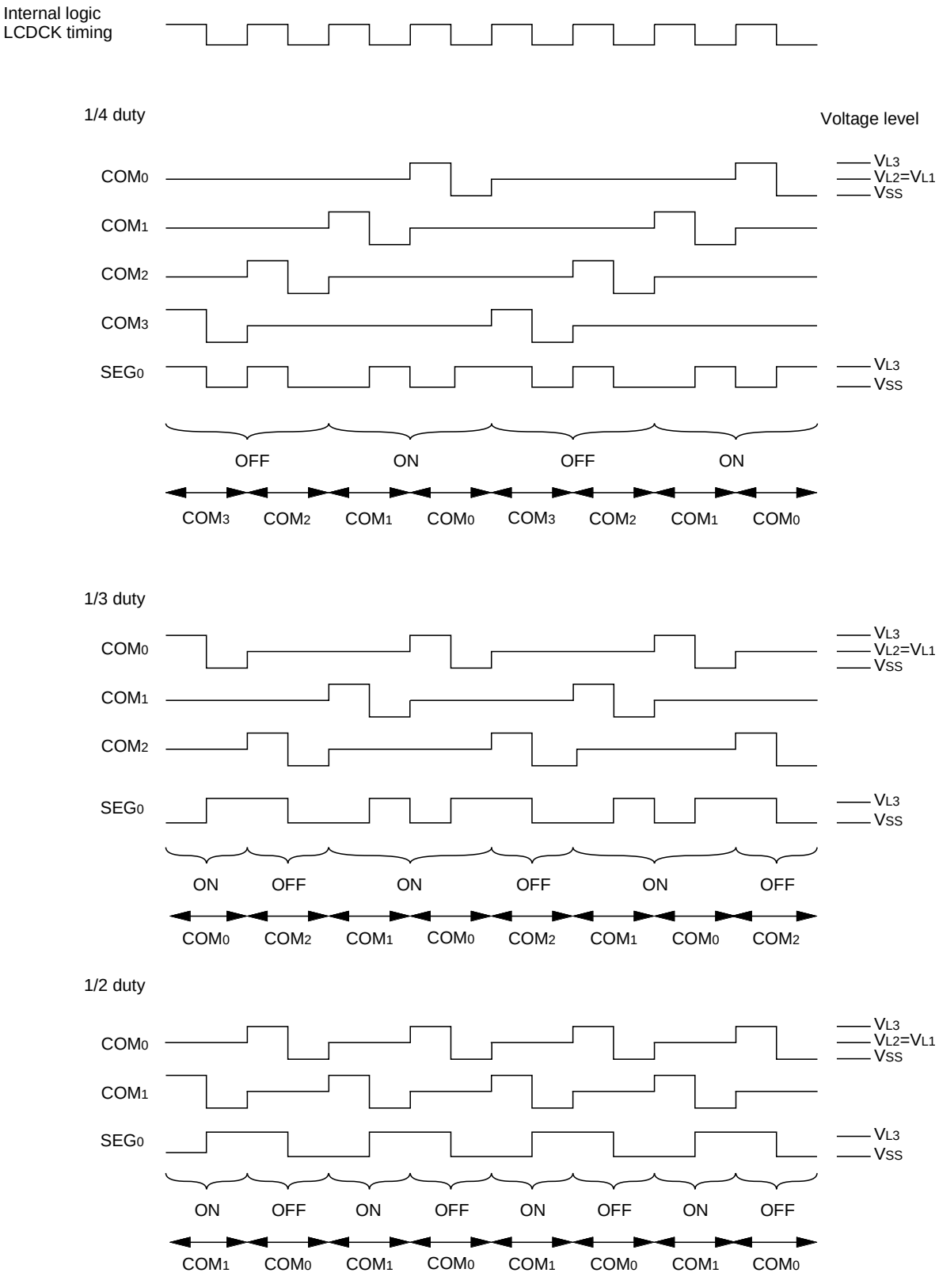


Fig. 40 LCD drive waveform (1/2 bias)

φ CLOCK SYSTEM OUTPUT FUNCTION

The internal system clock φ or XCIN frequency signal can be output from port P41 by setting the φ output control register. Set bit 1 of the port P4 direction register to "1" when outputting φ clock.

Set the bit 4 in the peripheral function expansion register to "1" when the XCIN frequency signal is output.

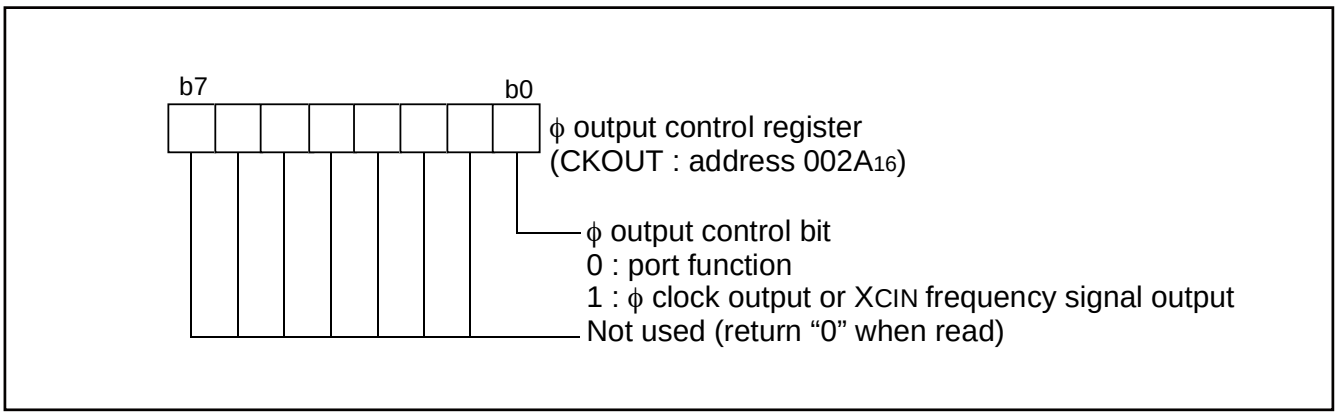


Fig. 45 Structure of φ output control register

Temporary data register

The temporary data register (addresses 002C16 to 002E16) is the 8-bit register and does not have the control function. It can be used to store data temporarily. It is initialized after reset.

RRF register

The RRF register (address 002F16)is the 8-bit register and does not have the control function. As for the value written in this register, high-order 4 bits and low-order 4 bits interchange. It is initialized after reset.

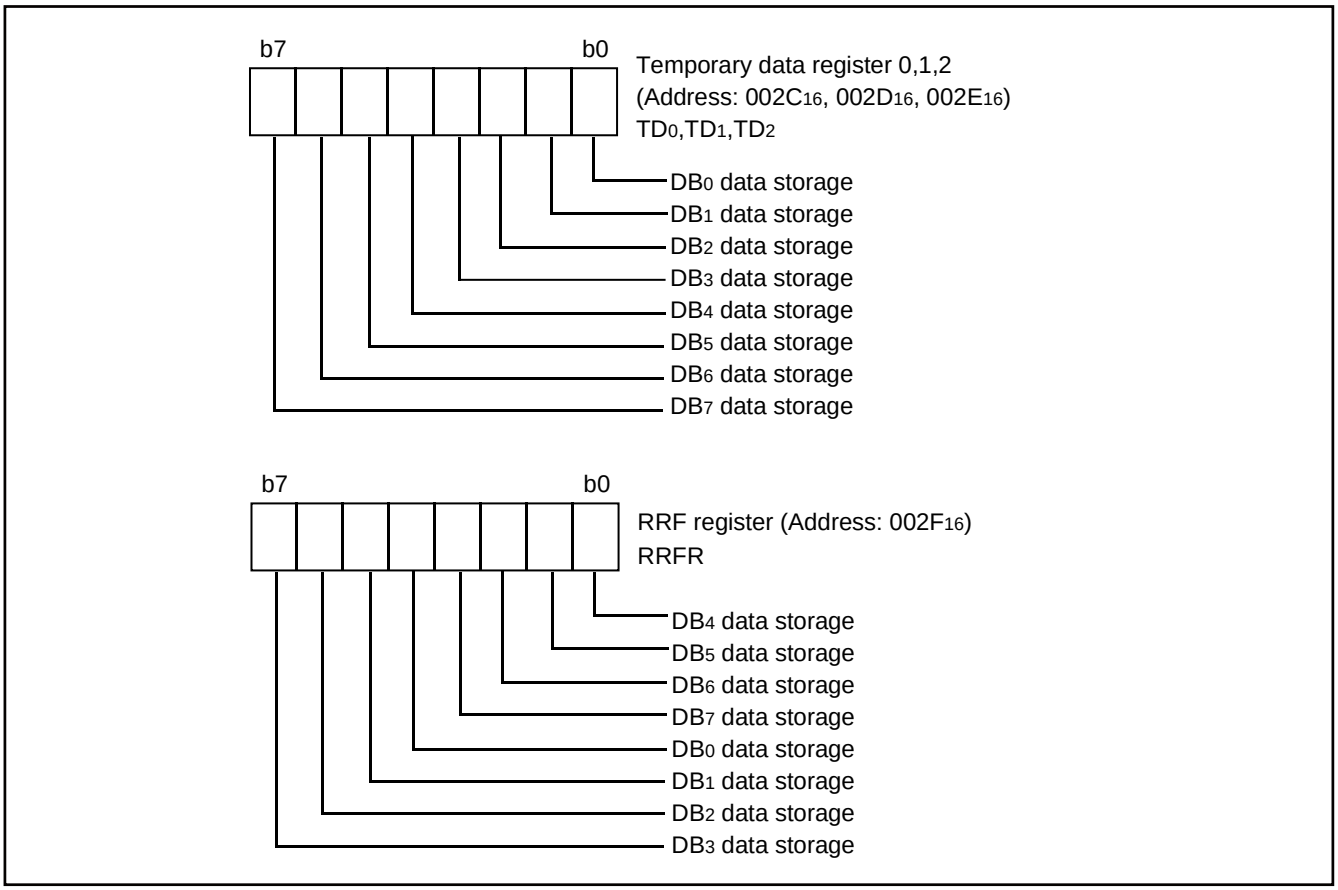


Fig. 46 Structure of temporary register, RPF register

PERIPHERAL FUNCTION EXTENSION REGISTER

The serial I/O transfer direction can be switched by setting the bit 0 in the peripheral function expansion register to “1”. This function is valid only when the bit 6 in the serial I/O control register is set to “1” (when the clock synchronous serial I/O is selected). P47 can be selected as the output pin of the clock synchronous serial I/O by setting the bit 1 in the peripheral function expansion register to “1”. When setting P47 to the SOUT pin, set the bit 7 in the port P4 direction register to “1”. This function is valid only when the bit 6 in the serial I/O control register to “1” (when the clock synchronous serial I/O is selected). P-channel output of TXD and SOUT can be disabled by the bits 2 and 3 in the peripheral function expansion register. Set the bit 4 in the UART control register to “1” after selecting the pin to disable the P-channel output. XCIN frequency signal can be output from the port P41 by setting the bit 4 in the peripheral function expansion register to “1”. Set the bit 0 in the ϕ output control register and the bit 1 in the port P4 direction register to “1” to output the XCIN frequency signal.

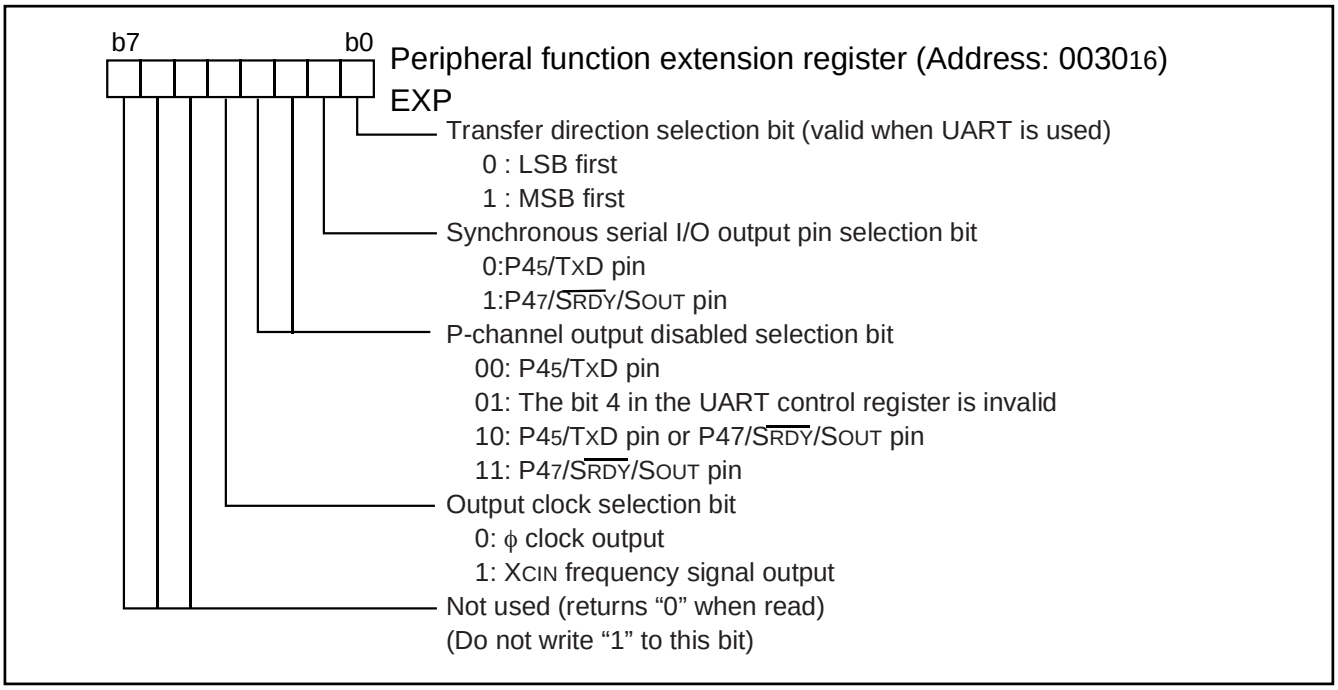
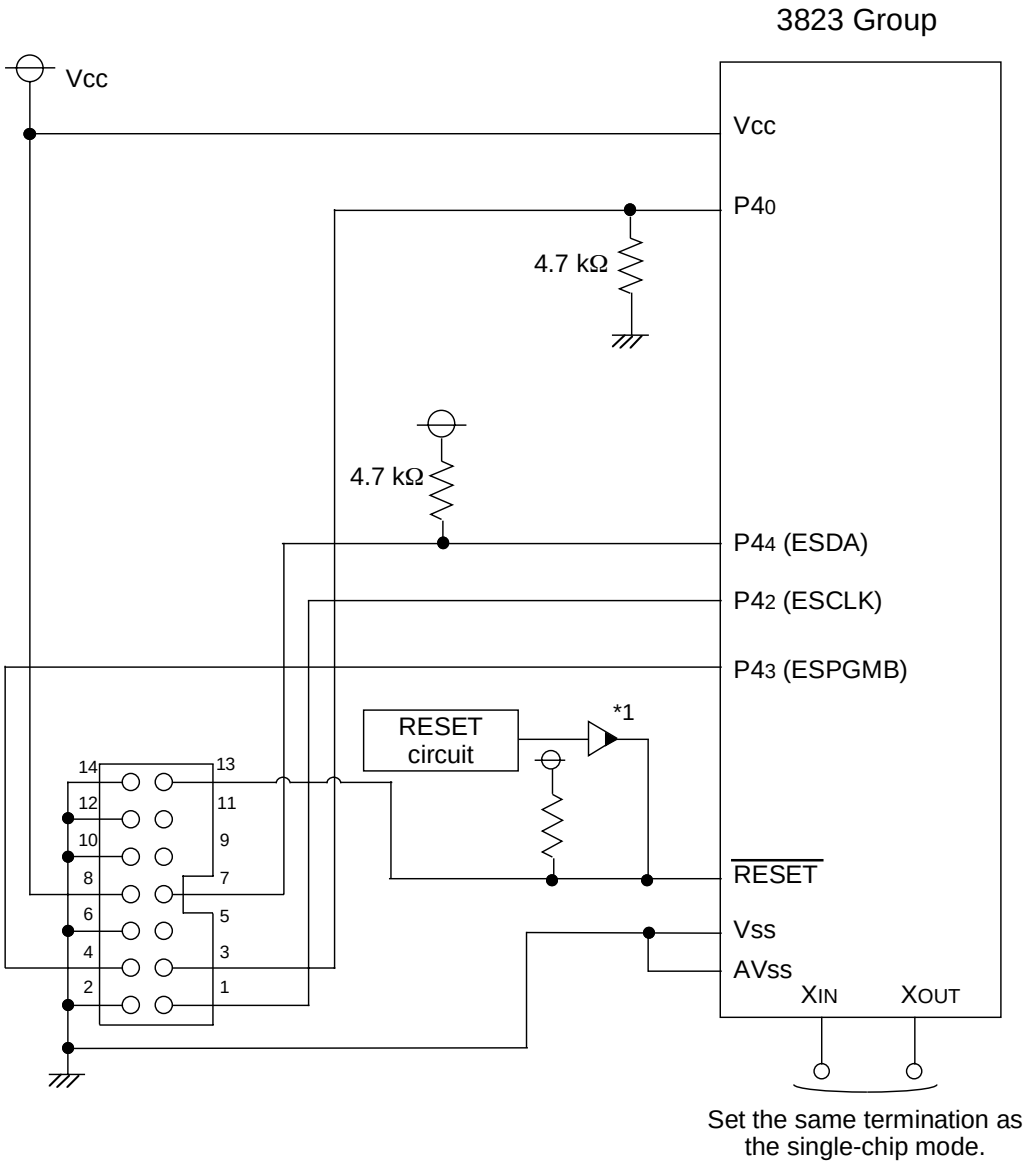


Fig. 50 Structure of peripheral function extension register



* 1 : Open-collector buffer

Note: For the programming circuit, the wiring capacity of each signal pin must not exceed 47 pF.

Fig. 60 When using E8 programmer, connection example

Table 22 Timing requirements (1)

(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
$t_{w(\overline{RESET})}$	Reset input “L” pulse width		2			µs
$t_{c(X_{IN})}$	Main clock input cycle time (X_{IN} input)	4.0 ≤ Vcc < 4.5 V	1000/(4 × V_{CC}–8)			ns
		4.5 ≤ Vcc ≤ 5.5 V	100			ns
$t_{wH(X_{IN})}$	Main clock input “H” pulse width	4.0 ≤ Vcc < 4.5 V	45			ns
		4.5 ≤ Vcc ≤ 5.5 V	40			ns
$t_{wL(X_{IN})}$	Main clock input “L” pulse width	4.0 ≤ Vcc < 4.5 V	45			ns
		4.5 ≤ Vcc ≤ 5.5 V	40			ns
$t_{c(CNTR)}$	$CNTR_0$, $CNTR_1$ input cycle time	4.0 ≤ Vcc < 4.5 V	1000/(2 × V_{CC}–4)			ns
		4.5 ≤ Vcc ≤ 5.5 V	200			ns
$t_{wH(CNTR)}$	$CNTR_0$, $CNTR_1$ input “H” pulse width	4.0 ≤ Vcc < 4.5 V	105			ns
		4.5 ≤ Vcc ≤ 5.5 V	85			ns
$t_{wL(CNTR)}$	$CNTR_0$, $CNTR_1$ input “L” pulse width	4.0 ≤ Vcc < 4.5 V	105			ns
		4.5 ≤ Vcc ≤ 5.5 V	85			ns
$t_{wH(INT)}$	INT_0 to INT_3 input “H” pulse width		80			ns
$t_{wL(INT)}$	INT_0 to INT_3 input “L” pulse width		80			ns
$t_{c(S_{CLK})}$	Serial I/O clock input cycle time **(Note)**		800			ns
$t_{wH(S_{CLK})}$	Serial I/O clock input “H” pulse width **(Note)**		370			ns
$t_{wL(S_{CLK})}$	Serial I/O clock input “L” pulse width **(Note)**		370			ns
$t_{su(R_{XD}–S_{CLK})}$	Serial I/O input set up time		220			ns
$t_{h(S_{CLK}–R_{XD})}$	Serial I/O input hold time		100			ns

Note: When bit 6 of address $001A_{16}$ is “1” (clock synchronous).
Divide this limits value by four when bit 6 of address $001A_{16}$ is “0” (UART).

Table 23 Timing requirements (2)

(V_{CC} = 1.8 to 4.0 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
$t_{w(\overline{RESET})}$	Reset input “L” pulse width		2			µs
$t_{c(X_{IN})}$	Main clock input cycle time (X_{IN} input)	2.0 ≤ Vcc ≤ 4.0 V	125			ns
		Vcc < 2.0 V	1000/(10 × V_{CC}–12)			ns
$t_{wH(X_{IN})}$	Main clock input “H” pulse width	2.0 ≤ Vcc ≤ 4.0 V	50			ns
		Vcc < 2.0 V	70			ns
$t_{wL(X_{IN})}$	Main clock input “L” pulse width	2.0 ≤ Vcc ≤ 4.0 V	50			ns
		Vcc < 2.0 V	70			ns
$t_{c(CNTR)}$	$CNTR_0$, $CNTR_1$ input cycle time	2.0 ≤ Vcc ≤ 4.0 V	1000/V_{CC}			ns
		Vcc < 2.0 V	1000/(5 × V_{CC}–8)			ns
$t_{wH(CNTR)}$	$CNTR_0$, $CNTR_1$ input “H” pulse width		$t_{c(CNTR)}$/2–20			ns
$t_{wL(CNTR)}$	$CNTR_0$, $CNTR_1$ input “L” pulse width		$t_{c(CNTR)}$/2–20			ns
$t_{wH(INT)}$	INT_0 to INT_3 input “H” pulse width		230			ns
$t_{wL(INT)}$	INT_0 to INT_3 input “L” pulse width		230			ns
$t_{c(S_{CLK})}$	Serial I/O clock input cycle time **(Note)**		2000			ns
$t_{wH(S_{CLK})}$	Serial I/O clock input “H” pulse width **(Note)**		950			ns
$t_{wL(S_{CLK})}$	Serial I/O clock input “L” pulse width **(Note)**		950			ns
$t_{su(R_{XD}–S_{CLK})}$	Serial I/O input set up time		400			ns
$t_{h(S_{CLK}–R_{XD})}$	Serial I/O input hold time		200			ns

Note: When bit 6 of address $001A_{16}$ is “1” (clock synchronous).
Divide this limits value by four when bit 6 of address $001A_{16}$ is “0” (UART).

Table 24 Switching characteristics (1)

(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{WH(SCLK)}$	Serial I/O clock output “H” pulse width	$t_{C(SCLK)}$/2–30			ns
$t_{WL(SCLK)}$	Serial I/O clock output “L” pulse width	$t_{C(SCLK)}$/2–30			ns
$t_{d(SCLK-TxD)}$	Serial I/O output delay time **(Note)**			140	ns
$t_{v(SCLK-TxD)}$	Serial I/O output valid time **(Note)**	–30			ns
$t_{r(SCLK)}$	Serial I/O clock output rising time			30	ns
$t_{f(SCLK)}$	Serial I/O clock output falling time			30	ns

Note : When the $P4_5$/TxD P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is “0”.

Table 25 Switching characteristics (2)

(V_{CC} = 1.8 to 4.0 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{WH(SCLK)}$	Serial I/O clock output “H” pulse width	$t_{C(SCLK)}$/2–100			ns
$t_{WL(SCLK)}$	Serial I/O clock output “L” pulse width	$t_{C(SCLK)}$/2–100			ns
$t_{d(SCLK-TxD)}$	Serial I/O output delay time **(Note)**			350	ns
$t_{v(SCLK-TxD)}$	Serial I/O output valid time **(Note)**	–30			ns
$t_{r(SCLK)}$	Serial I/O clock output rising time			100	ns
$t_{f(SCLK)}$	Serial I/O clock output falling time			100	ns

Note : When the $P4_5$/TxD P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is “0”.

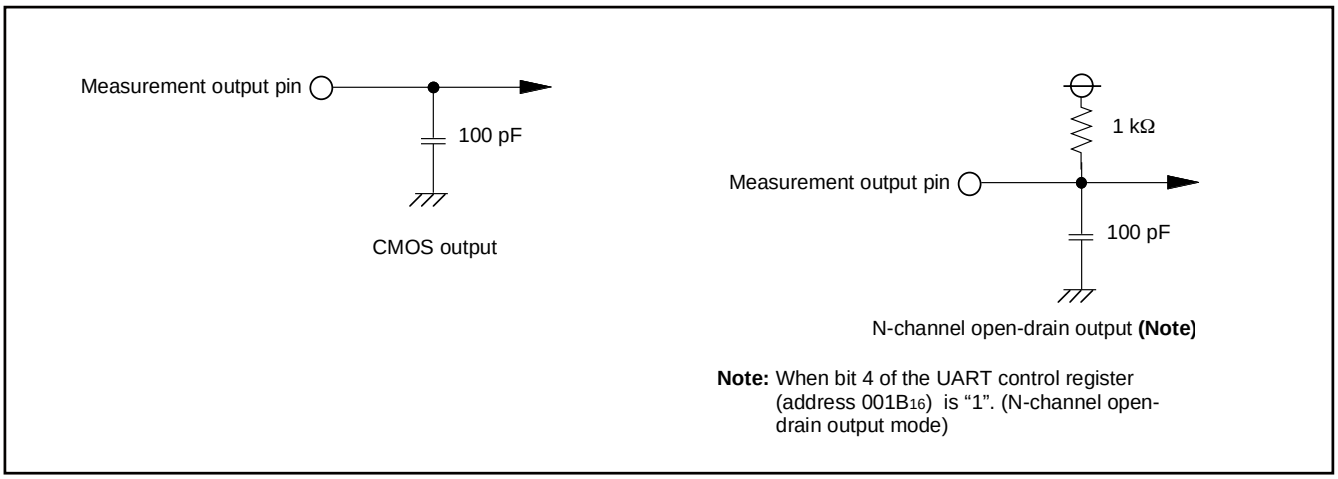


Fig. 69 Circuit for measuring output switching characteristics

REVISION HISTORY	3823 GROUP DATA SHEET

Rev.	Date	Description	
		Page	Summary
1.00	05/13/05		First edition
2.00	05/07/07	6 8 9 14 40 49 52 54 55 60	Table 3 is partly revised Fig.5 is partly added Table 4 is revised “ROM Code Protect Address” is added Fig.10 is revised “STP instruction Execution” is revised “Oscillation Control” (1) Stop Mode is partly revised “LCD drive Control Circuit” is revised “(6) Wiring to P40/(V_{PP}) pin” is revised Fig.59 is revised Fig.60 is partly deleted “NOTES ON QzROM” is added Table 18 is partly added
2.01	05/11/08	6 61 65-66	Table 3 is partly revised Table 19, 20 are partly revised PACKAGE OUTLINE revised
2.02	07/06/19	– 6 8 9 10 15 22 23-27 46 48 51 52 53 54 55-58 58 59 63 66	“RENESAS TECHNICAL UPDATE” reflected: TN-740-A111A/E Table 3: Function except a port function; •Serial I/O function pins → •Serial interface function pins Fig. 5 M38234G4, M38235G6: Under development → Mass production Note deleted Table 4: Under development deleted FUNCTIONAL DESCRIPTION CENTRAL PROCESSING UNIT (CPU): Description added Fig. 11: Note added CPU mode extension register ($002B_{16}$) → CPU mode expansion register Peripheral function extension register (0030_{16}) → Peripheral function expansion register Table 8: AV_{SS} added, Note revised INTERRUPTS: Description revised, Fig. 18-20 added ROM CORRECTION FUNCTION: Description added Initial Value of Watchdog Timer: Description added Standard Operation of Watchdog Timer: A part of description deleted Bit 6 and bit 7 of Watchdog Timer Control Register: added and revised Fig. 48 revised, Note added Fig. 53: Port P0 direction register (0000_{16}) → (0001_{16}) Frequency Control: Description revised Fig. 56: revised Fig. 57: revised QzROM Writing Mode: added Processor Status Register: added Overvoltage: Description revised and Fig. 68 added Table 15 V_{CC}: Frequency/4 mode → Frequency/8 mode V_{REF}: Limits Min. 2.0 → 1.8 Table 18: V_{RAM} added