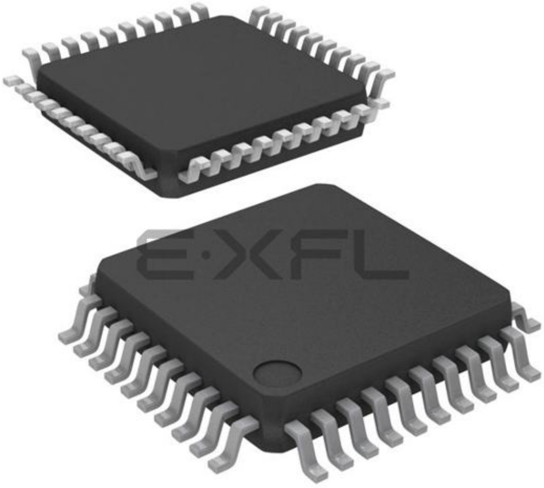

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	LINbus, SIO, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	25
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f212e4dfp-u0

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R8C/2E Group, R8C/2F Group

RENESAS MCU

REJ03B0222-0100
Rev.1.00
Dec 14, 2007

1. Overview

1.1 Features

The R8C/2E Group and R8C/2F Group of single-chip MCUs incorporates the R8C/Tiny Series CPU core, employing sophisticated instructions for a high level of efficiency. With 1 Mbyte of address space, and it is capable of executing instructions at high speed. In addition, the CPU core boasts a multiplier for high-speed operation processing.

Power consumption is low, and the supported operating modes allow additional power control. These MCUs also use an anti-noise configuration to reduce emissions of electromagnetic noise and are designed to withstand EMI.

Integration of many peripheral functions, including multifunction timer and serial interface, reduces the number of system components.

Furthermore, the R8C/2F Group has on-chip data flash (1 KB × 2 blocks).

The difference between the R8C/2E Group and R8C/2F Group is only the presence or absence of data flash. Their peripheral functions are the same.

1.1.1 Applications

Electronic household appliances, office equipment, audio equipment, consumer equipment, etc.

Table 1.3 Specifications for R8C/2F Group (1)

Item	Function	Specification
CPU	Central processing unit	R8C/Tiny series core • Number of fundamental instructions: 89 • Minimum instruction execution time: 50 ns (f(XIN) = 20 MHz, VCC = 3.0 to 5.5 V) 100 ns (f(XIN) = 10 MHz, VCC = 2.7 to 5.5 V) • Multiplier: 16 bits × 16 bits → 32 bits • Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits • Operation mode: Single-chip mode (address space: 1 Mbyte)
Memory	ROM, RAM	Refer to **Table 1.6 Product List for R8C/2F Group**.
Power Supply Voltage Detection	Voltage detection circuit	• Power-on reset • Voltage detection 2
I/O Ports	Programmable I/O ports	• Input-only: 3 pins • CMOS I/O ports: 25, selectable pull-up resistor • High current drive ports: 8
Clock	Clock generation circuits	2 circuits: XIN clock oscillation circuit (with on-chip feedback resistor), On-chip oscillator (high-speed, low-speed) (high-speed on-chip oscillator has a frequency adjustment function) • Oscillation stop detection: XIN clock oscillation stop detection function • Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16 • Low power consumption modes: Standard operating mode (high-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode
Interrupts		• External: 4 sources, Internal: 13 sources, Software: 4 sources • Priority levels: 7 levels
Watchdog Timer		15 bits × 1 (with prescaler), reset start selectable
Timer	Timer RA	8 bits × 1 (with 8-bit prescaler) Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
	Timer RB	8 bits × 1 (with 8-bit prescaler) Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode
	Timer RC	16 bits × 1 (with 4 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output 3 pins), PWM2 mode (PWM output pin)
	Timer RE	8 bits × 1 Output compare mode
Serial Interface	UART0	Clock synchronous serial I/O/UART × 1
LIN Module		Hardware LIN: 1 (timer RA, UART0)
A/D Converter		10-bit resolution × 12 channels, includes sample and hold function
D/A Converter		8-bit resolution × 2 circuits
Comparator		2 circuits

1.2 Product List

Table 1.5 lists Product List for R8C/2E Group, Figure 1.1 shows a Part Number, Memory Size, and Package of R8C/2E Group, Table 1.6 lists Product List for R8C/2F Group, and Figure 1.2 shows a Part Number, Memory Size, and Package of R8C/2F Group.

Table 1.5 Product List for R8C/2E Group **Current of Dec. 2007**

Part No.	ROM Capacity	RAM Capacity	Package Type	Remarks
R5F212E2NFP	8 Kbytes	512 bytes	PLQP0032GB-A	N version
R5F212E4NFP	16 Kbytes	1 Kbyte	PLQP0032GB-A	
R5F212E2DFP	8 Kbytes	512 bytes	PLQP0032GB-A	D version
R5F212E4DFP	16 Kbytes	1 Kbyte	PLQP0032GB-A	
R5F212E2NXXXFP	8 Kbytes	512 bytes	PLQP0032GB-A	N version Factory programming product(1)
R5F212E4NXXXFP	16 Kbytes	1 Kbyte	PLQP0032GB-A	
R5F212E2DXXXFP	8 Kbytes	512 bytes	PLQP0032GB-A	D version Factory programming product(1)
R5F212E4DXXXFP	16 Kbytes	1 Kbyte	PLQP0032GB-A	

NOTE:

1. The user ROM is programmed before shipment.

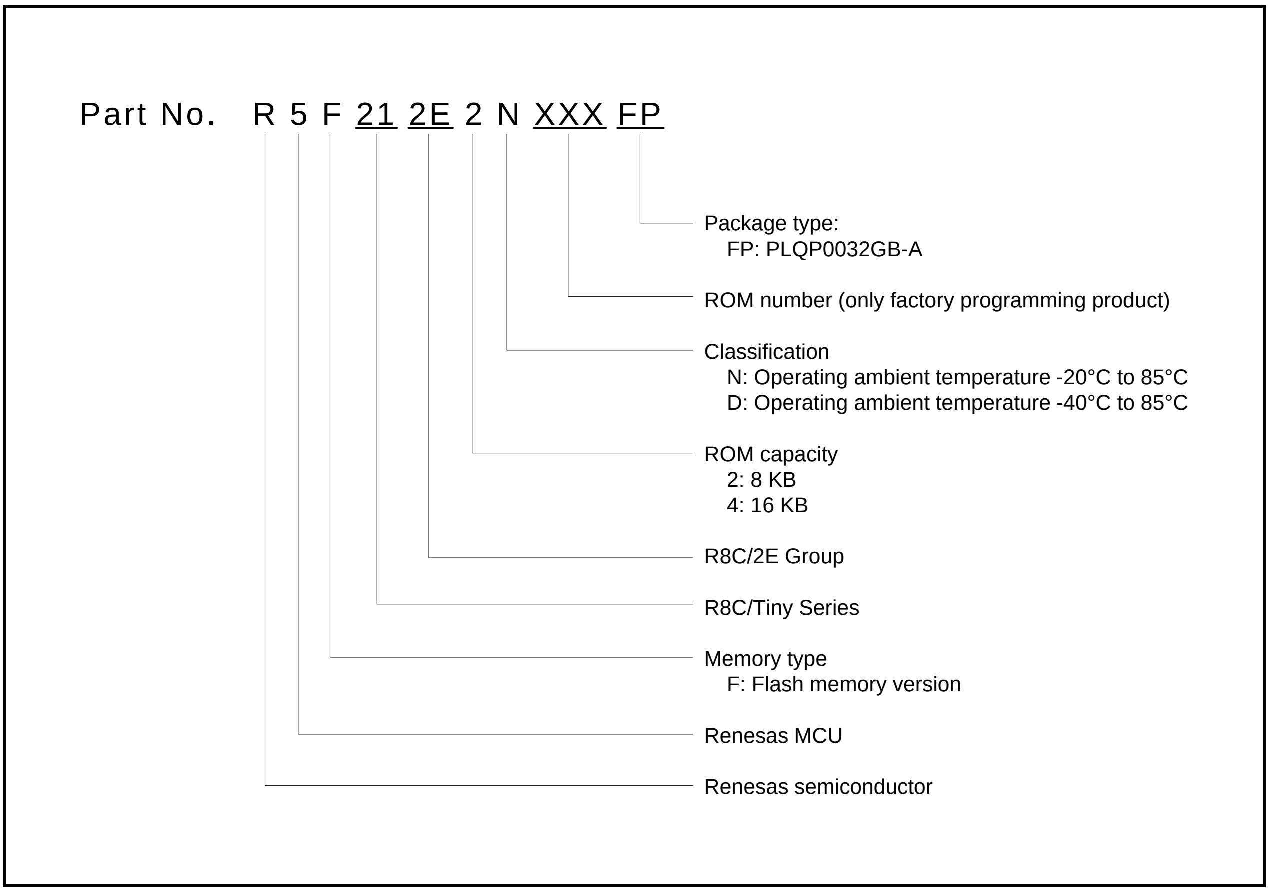


Figure 1.1 Part Number, Memory Size, and Package of R8C/2E Group

Table 1.6 Product List for R8C/2F Group **Current of Dec. 2007**

Part No.	ROM Capacity		RAM Capacity	Package Type	Remarks
	Program ROM	Data flash			
R5F212F2NFP	8 Kbytes	1 Kbyte × 2	512 bytes	PLQP0032GB-A	N version
R5F212F4NFP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLQP0032GB-A	
R5F212F2DFP	8 Kbytes	1 Kbyte × 2	512 bytes	PLQP0032GB-A	D version
R5F212F4DFP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLQP0032GB-A	
R5F212F2NXXXFP	8 Kbytes	1 Kbyte × 2	512 bytes	PLQP0032GB-A	N version Factory programming product(1)
R5F212F4NXXXFP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLQP0032GB-A	
R5F212F2DXXXFP	8 Kbytes	1 Kbyte × 2	512 bytes	PLQP0032GB-A	D version Factory programming product(1)
R5F212F4DXXXFP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLQP0032GB-A	

NOTE:

1. The user ROM is programmed before shipment.

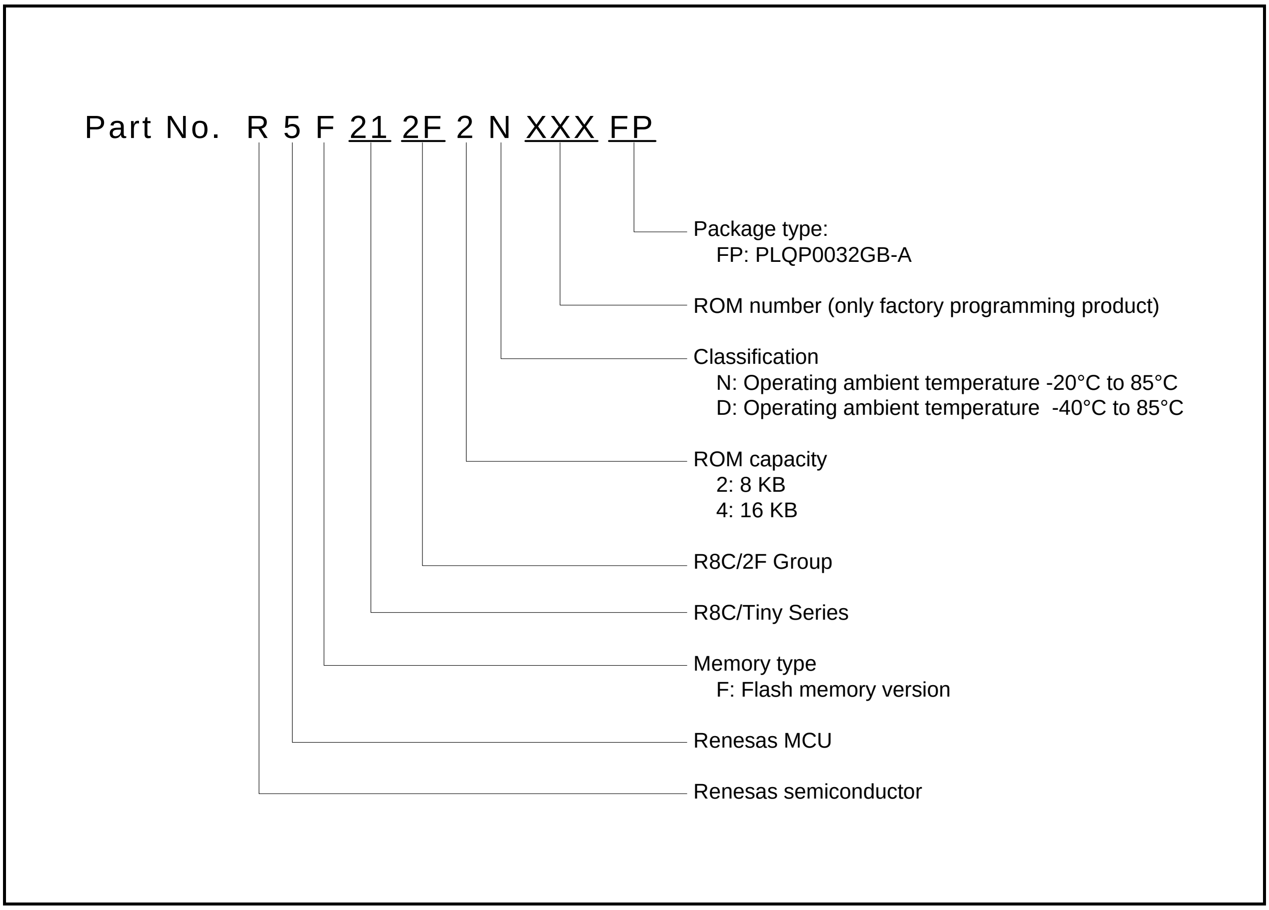


Figure 1.2 Part Number, Memory Size, and Package of R8C/2F Group

Table 1.7 Pin Name Information by Pin Number

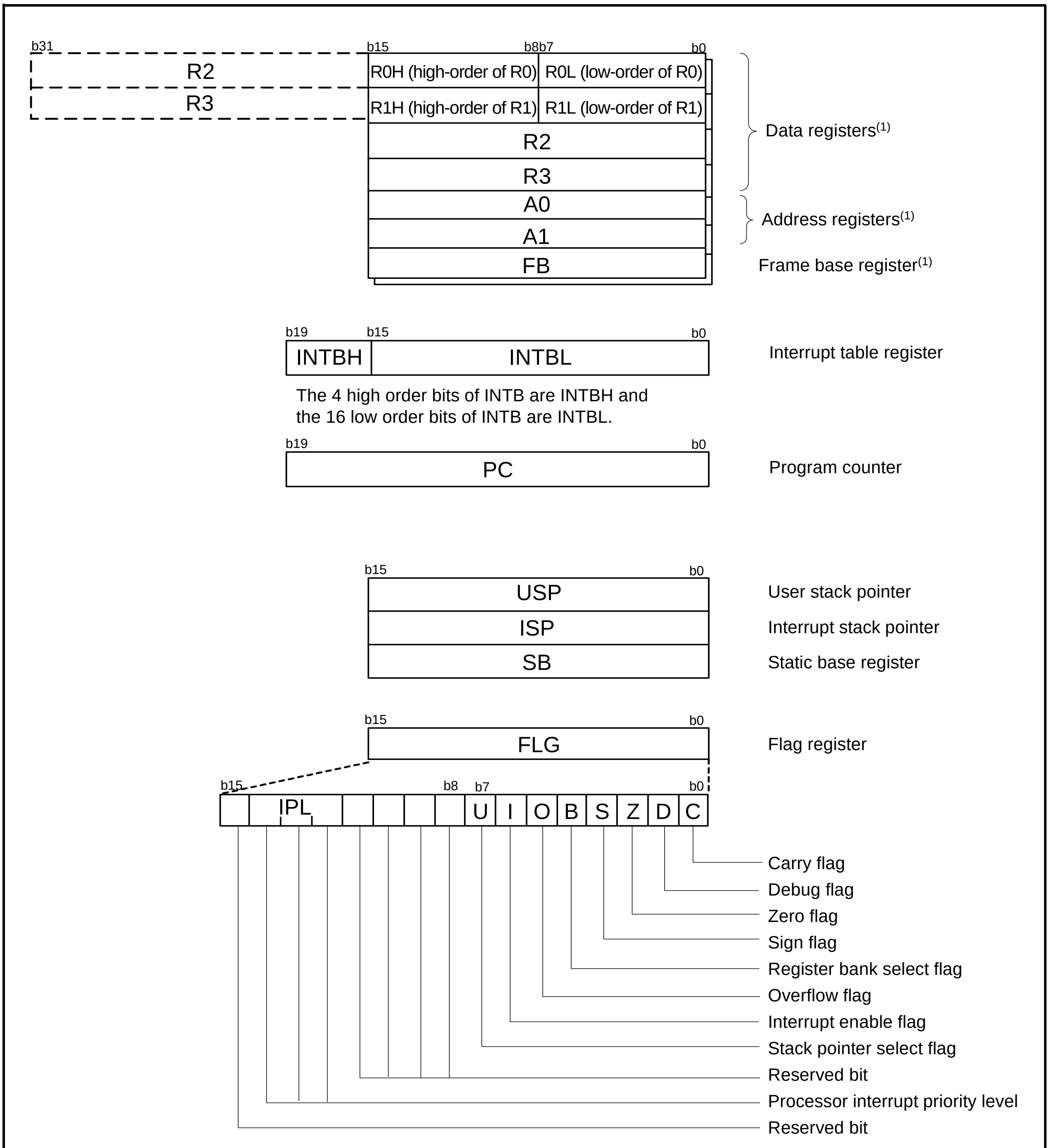
Pin Number	Control Pin	Port	I/O Pin Functions for of Peripheral Modules					
			Interrupt	Timer	Serial Interface	A/D Converter	D/A Converter	Comparator
1		P3_5		(TRCIOD)(1)				
2		P3_7		TRAO				
3	$\overline{\text{RESET}}$							
4	XOUT	P4_7						
5	VSS/AVSS							
6	XIN	P4_6						
7	VCC/AVCC							
8	MODE							
9		P4_5	$\overline{\text{INT0}}$					
10		P1_7	$\overline{\text{INT1}}$	TRAIO				
11		P3_6	($\overline{\text{INT1}}$)(1)					
12		P3_1		TRBO				
13		P5_4		TRCIOD				ACOUT1
14		P5_3		TRCIOC				ACOUT0
15		P1_6			CLK0			
16		P1_5	($\overline{\text{INT1}}$)(1)	(TRAIO)(1)	RXD0			
17		P1_4			TXD0			
18		P1_3	$\overline{\text{KI3}}$	(TRBO)(1)		AN11		
19		P1_2	$\overline{\text{KI2}}$	TRCIOB		AN10		
20	VREF	P4_2						
21		P1_1	$\overline{\text{KI1}}$	TRCIOA/TRCTRG		AN9		
22		P1_0	$\overline{\text{KI0}}$			AN8		
23		P3_3	$\overline{\text{INT3}}$	TRCCLK				
24		P3_4		(TRCIOC)(1)				
25		P0_7				AN0	DA1	
26		P0_6				AN1	DA0	
27		P0_5				AN2		AVREF0
28		P0_4		TREO		AN3		ACMP0
29		P0_3				AN4		AVREF1
30		P0_2				AN5		ACMP1
31		P0_1				AN6		
32		P0_0				AN7		

NOTE:

1. Can be assigned to the pin in parentheses by a program.

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register bank.



NOTE:
1. These registers comprise a register bank. There are two register banks.

Figure 2.1 CPU Registers

3. Memory

3.1 R8C/2E Group

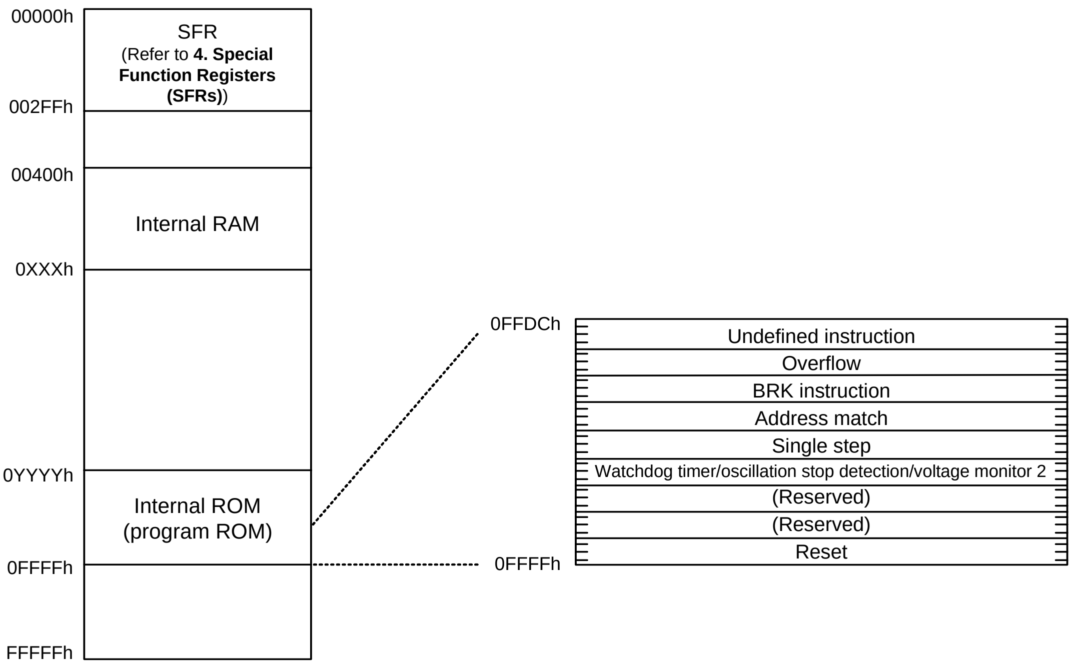
Figure 3.1 is a Memory Map of R8C/2E Group. The R8C/2E group has 1 Mbyte of address space from addresses 00000h to FFFFFh.

The internal ROM is allocated lower addresses, beginning with address 0FFFFh. For example, a 16-Kbyte internal ROM area is allocated addresses 0C000h to 0FFFFh.

The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.

The internal RAM is allocated higher addresses beginning with address 00400h. For example, a 1-Kbyte internal RAM area is allocated addresses 00400h to 007FFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.

Special function registers (SFRs) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated here. All addresses within the SFR, which have nothing allocated are reserved for future use and cannot be accessed by users.



NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Part Number	Internal ROM		Internal RAM	
	Size	Address 0YYYYh	Size	Address 0XXXXh
R5F212E2NFP, R5F212E2DFP, R5F212E2NXXXFP, R5F212E2DXXXFP	8 Kbytes	0E000h	512 bytes	005FFh
R5F212E4NFP, R5F212E4DFP, R5F212E4NXXXFP, R5F212E4DXXXFP	16 Kbytes	0C000h	1 Kbyte	007FFh

Figure 3.1 Memory Map of R8C/2E Group

4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.7 list the special function registers.

Table 4.1 SFR Information (1)(1)

Address	Register	Symbol	After reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	01101000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h			
0009h			
000Ah	Protect Register	PRCR	00h
000Bh			
000Ch	Oscillation Stop Detection Register	OCD	00000100b
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDC	00X11111b
0010h	Address Match Interrupt Register 0	RMAD0	00h
0011h			00h
0012h			00h
0013h	Address Match Interrupt Enable Register	AIER	00h
0014h	Address Match Interrupt Register 1	RMAD1	00h
0015h			00h
0016h			00h
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	00h 10000000b(4)
001Dh			
001Eh			
001Fh			
0020h			
0021h			
0022h			
0023h	High-Speed On-Chip Oscillator Control Register 0	FRA0	00h
0024h	High-Speed On-Chip Oscillator Control Register 1	FRA1	When shipping
0025h	High-Speed On-Chip Oscillator Control Register 2	FRA2	00h
0026h			
0027h			
0028h			
0029h			
002Ah			
002Bh			
002Ch	High-Speed On-Chip Oscillator Control Register 7	FRA7	When Shipping
0030h			
0031h	Voltage Detection Register 1 (2)	VCA1	00001000b
0032h	Voltage Detection Register 2 (2)	VCA2	00100000b
0033h			
0034h			
0035h			
0036h	Voltage Monitor 1 Circuit Control Register(3)	VW1C	00001000b
0037h	Voltage Monitor 2 Circuit Control Register(3)	VW2C	00h
0038h			
0039h			
003Ah			
003Bh			
003Ch			
003Dh			
003Eh			
003Fh			

X: Undefined

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. Software reset, watchdog timer reset, and voltage monitor 1 reset or voltage monitor 2 reset do not affect this register.
3. Software reset, watchdog timer reset, and voltage monitor 1 reset or voltage monitor 2 reset do not affect b2 and b3.
4. The CSPROINI bit in the OFS register is set to 0.

Table 4.4 SFR Information (4)[1]

Address	Register	Symbol	After reset
00C0h	A/D Register	AD	XXh
00C1h			XXh
00C2h			
00C3h			
00C4h			
00C5h			
00C6h			
00C7h			
00C8h			
00C9h			
00CAh			
00CBh			
00CCh			
00CDh			
00CEh			
00CFh			
00D0h			
00D1h			
00D2h			
00D3h			
00D4h	A/D Control Register 2	ADCON2	00h
00D5h			
00D6h	A/D Control Register 0	ADCON0	00h
00D7h	A/D Control Register 1	ADCON1	00h
00D8h	D/A Register 0	DA0	00h
00D9h			
00DAh	D/A Register 1	DA1	00h
00DBh			
00DCh	D/A Control Register	DACON	00h
00DDh			
00DEh			
00DFh			
00E0h	Port P0 Register	P0	00h
00E1h	Port P1 Register	P1	00h
00E2h	Port P0 Direction Register	PD0	00h
00E3h	Port P1 Direction Register	PD1	00h
00E4h			
00E5h	Port P3 Register	P3	00h
00E6h			
00E7h	Port P3 Direction Register	PD3	00h
00E8h	Port P4 Register	P4	00h
00E9h	Port P5 Register	P5	00h
00EAh	Port P4 Direction Register	PD4	00h
00EBh	Port P5 Direction Register	PD5	00h
00ECh			
00EDh			
00EEh			
00EFh			
00F0h			
00F1h			
00F2h			
00F3h			
00F4h			
00F5h			
00F6h	Pin Select Register 2	PINSR2	00h
00F7h	Pin Select Register 3	PINSR3	00h
00F8h	Port Mode Register	PMR	00h
00F9h	External Input Enable Register	INTEN	00h
00FAh	INT Input Filter Select Register	INTF	00h
00FBh	Key Input Enable Register	KIEN	00h
00FCh	Pull-Up Control Register 0	PUR0	00h
00FDh	Pull-Up Control Register 1	PUR1	00h
00FEh	Port P1 Drive Capacity Control Register	P1DRR	00h
00FFh			

X: Undefined
NOTE:
1. The blank regions are reserved. Do not access locations in these regions.

Table 4.5 SFR Information (5)[1]

Address	Register	Symbol	After reset
0100h	Timer RA Control Register	TRACR	00h
0101h	Timer RA I/O Control Register	TRAIOC	00h
0102h	Timer RA Mode Register	TRAMR	00h
0103h	Timer RA Prescaler Register	TRAPRE	FFh
0104h	Timer RA Register	TRA	FFh
0105h			
0106h	LIN Control Register	LINCR	00h
0107h	LIN Status Register	LINST	00h
0108h	Timer RB Control Register	TRBCR	00h
0109h	Timer RB One-Shot Control Register	TRBOCR	00h
010Ah	Timer RB I/O Control Register	TRBIOC	00h
010Bh	Timer RB Mode Register	TRBMR	00h
010Ch	Timer RB Prescaler Register	TRBPRE	FFh
010Dh	Timer RB Secondary Register	TRBSC	FFh
010Eh	Timer RB Primary Register	TRBPR	FFh
010Fh			
0110h			
0111h			
0112h			
0113h			
0114h			
0115h			
0116h			
0117h			
0118h	Timer RE Counter Data Register	TRESEC	00h
0119h	Timer RE Compare Data Register	TREMIN	00h
011Ah			
011Bh			
011Ch	Timer RE Control Register 1	TRECR1	00h
011Dh	Timer RE Control Register 2	TRECR2	00h
011Eh	Timer RE Clock Source Select Register	TRECSR	00001000b
011Fh			
0120h	Timer RC Mode Register	TRCMR	01001000b
0121h	Timer RC Control Register 1	TRCCR1	00h
0122h	Timer RC Interrupt Enable Register	TRCIER	01110000b
0123h	Timer RC Status Register	TRCSR	01110000b
0124h	Timer RC I/O Control Register 0	TRCIOR0	10001000b
0125h	Timer RC I/O Control Register 1	TRCIOR1	10001000b
0126h	Timer RC Counter	TRC	00h
0127h			00h
0128h	Timer RC General Register A	TRCGRA	FFh
0129h			FFh
012Ah	Timer RC General Register B	TRCGRB	FFh
012Bh			FFh
012Ch	Timer RC General Register C	TRCGRC	FFh
012Dh			FFh
012Eh	Timer RC General Register D	TRCGRD	FFh
012Fh			FFh
0130h	Timer RC Control Register 2	TRCCR2	00011111b
0131h	Timer RC Digital Filter Function Select Register	TRCDF	00h
0132h	Timer RC Output Master Enable Register	TRCOER	01111111b
0133h			
0134h			
0135h			
0136h			
0137h			
0138h			
0139h			
013Ah			
013Bh			
013Ch			
013Dh			
013Eh			
013Fh			

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 4.6 SFR Information (6)[1]

Address	Register	Symbol	After reset
0140h			
0141h			
0142h			
0143h			
0144h			
0145h			
0146h			
0147h			
0148h			
0149h			
014Ah			
014Bh			
014Ch			
014Dh			
014Eh			
014Fh			
0150h			
0151h			
0152h			
0153h			
0154h			
0155h			
0156h			
0157h			
0158h			
0159h			
015Ah			
015Bh			
015Ch			
015Dh			
015Eh			
015Fh			
0160h			
0161h			
0162h			
0163h			
0164h			
0165h			
0166h			
0167h			
0168h			
0169h			
016Ah			
016Bh			
016Ch			
016Dh			
016Eh			
016Fh			
0170h			
0171h			
0172h			
0173h			
0174h	Comparator 0 Control Register	ACCR0	00001000b
0175h	Comparator 1 Control Register	ACCR1	00001000b
0176h			
0177h	Comparator Mode Register	ACMR	00h
0178h			
0179h			
017Ah			
017Bh			
017Ch			
017Dh			
017Eh			
017Fh			

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 4.7 SFR Information (7)(1)

Address	Register	Symbol	After reset
0180h			
0181h			
0182h			
0183h			
0184h			
0185h			
0186h			
0187h			
0188h			
0189h			
018Ah			
018Bh			
018Ch			
018Dh			
018Eh			
018Fh			
0190h			
0191h			
0192h			
0193h			
0194h			
0195h			
0196h			
0197h			
0198h			
0199h			
019Ah			
019Bh			
019Ch			
019Dh			
019Eh			
019Fh			
01A0h			
01A1h			
01A2h			
01A3h			
01A4h			
01A5h			
01A6h			
01A7h			
01A8h			
01A9h			
01AAh			
01ABh			
01ACh			
01ADh			
01AEh			
01AFh			
01B0h			
01B1h			
01B2h			
01B3h	Flash Memory Control Register 4	FMR4	01000000b
01B4h			
01B5h	Flash Memory Control Register1	FMR1	1000000Xb
01B6h			
01B7h	Flash Memory Control Register 0	FMR0	00000001b
01B8h			
01B9h			
01BAh			
01BBh			
01BCh			
01BDh			
01BEh			
01BFh			

FFFFh	Option Function Select Register	OFS	(Note 2)

X: Undefined

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. The OFS register cannot be changed by a program. Use a flash programmer to write to it.

5. Electrical Characteristics

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated Value	Unit
VCC/AVCC	Supply voltage		–0.3 to 6.5	V
V_I	Input voltage		–0.3 to VCC + 0.3	V
V_O	Output voltage		–0.3 to VCC + 0.3	V
P_d	Power dissipation	T_{opr} = 25°C	500	mW
T_{opr}	Operating ambient temperature		–20 to 85 (N version) / –40 to 85 (D version)	°C
T_{stg}	Storage temperature		–65 to 150	°C

Table 5.2 Recommended Operating Conditions

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
VCC/AVCC	Supply voltage			2.7	–	5.5	V
VSS/AVSS	Supply voltage			–	0	–	V
V_{IH}	Input “H” voltage			0.8 VCC	–	VCC	V
V_{IL}	Input “L” voltage			0	–	0.2 VCC	V
$I_{OH(sum)}$	Peak sum output “H” current	Sum of all pins $I_{OH(peak)}$		–	–	–160	mA
$I_{OH(sum)}$	Average sum output “H” current	Sum of all pins $I_{OH(avg)}$		–	–	–80	mA
$I_{OH(peak)}$	Peak output “H” current	Except P1_0 to P1_7		–	–	–10	mA
		P1_0 to P1_7		–	–	–20	mA
$I_{OH(avg)}$	Average output “H” current	Except P1_0 to P1_7		–	–	–5	mA
		P1_0 to P1_7		–	–	–10	mA
$I_{OL(sum)}$	Peak sum output “L” currents	Sum of all pins $I_{OL(peak)}$		–	–	160	mA
$I_{OL(sum)}$	Average sum output “L” currents	Sum of all pins $I_{OL(avg)}$		–	–	80	mA
$I_{OL(peak)}$	Peak output “L” currents	Except P1_0 to P1_7		–	–	10	mA
		P1_0 to P1_7		–	–	20	mA
$I_{OL(avg)}$	Average output “L” current	Except P1_0 to P1_7		–	–	5	mA
		P1_0 to P1_7		–	–	10	mA
$f_{(XIN)}$	XIN clock input oscillation frequency		3.0 V ≤ VCC ≤ 5.5 V	0	–	20	MHz
			2.7 V ≤ VCC < 3.0 V	0	–	10	MHz
–	System clock	OCD2 = 0 XIN clock selected	3.0 V ≤ VCC ≤ 5.5 V	0	–	20	MHz
			2.7 V ≤ VCC < 3.0 V	0	–	10	MHz
		OCD2 = 1 On-chip oscillator clock selected	FRA01 = 0 Low-speed on-chip oscillator clock selected	–	125	–	kHz
			FRA01 = 1 High-speed on-chip oscillator clock selected 3.0 V ≤ VCC ≤ 5.5 V	–	–	20	MHz
			FRA01 = 1 High-speed on-chip oscillator clock selected 2.7 V ≤ VCC ≤ 5.5 V	–	–	10	MHz

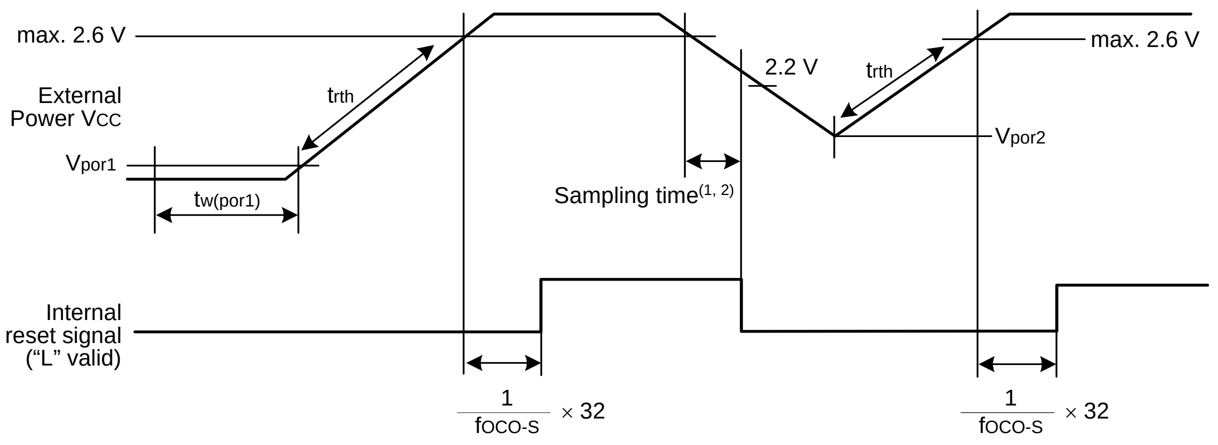
NOTES:

1. VCC = 2.7 to 5.5 V at T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.

Table 5.10 Power-on Reset Circuit, Voltage Monitor 0 Reset Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{por1}	Power-on reset valid voltage(3)		–	–	0.1	V
V_{por2}	Power-on reset valid voltage		0	–	2.6	V
t_{rth}	External power V_{CC} rise gradient(2)		20	–	–	mV/msec

NOTES:
1. The measurement condition is T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. This condition (external power V_{CC} rise gradient) does not apply if $V_{CC} \geq 1.0$ V.
3. $t_{w(por1)}$ indicates the duration the external power V_{CC} must be held below the effective voltage (V_{por1}) to enable a power on reset. When turning on the power for the first time, maintain $t_{w(por1)}$ for 30 s or more if $-20°C \leq T_{opr} \leq 85°C$, maintain $t_{w(por1)}$ for 3,000 s or more if $-40°C \leq T_{opr} < -20°C$.



NOTES:
1. Ensure that the voltage is 2.2 V or above during the sampling time.
2. The sampling time is fOCO-S divided by 1 × 4 cycles.

Figure 5.3 Reset Circuit Electrical Characteristics

Table 5.11 High-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO40M	High-speed on-chip oscillator frequency temperature • supply voltage dependence	V_{CC} = 4.75 V to 5.25 V 0°C ≤ T_{opr} ≤ 60°C(2)	39.2	40	40.8	MHz
		V_{CC} = 3.0 V to 5.5 V –20°C ≤ T_{opr} ≤ 85°C(2)	38.8	40	41.2	MHz
		V_{CC} = 3.0 V to 5.5 V –40°C ≤ T_{opr} ≤ 85°C(2)	38.4	40	41.6	MHz
		V_{CC} = 2.7 V to 5.5 V –20°C ≤ T_{opr} ≤ 85°C(2)	38	40	42	MHz
		V_{CC} = 2.7 V to 5.5 V –40°C ≤ T_{opr} ≤ 85°C(2)	37.6	40	42.4	MHz
		V_{CC} = 5.0 V ±10% –20°C ≤ T_{opr} ≤ 85°C(2)	38.8	40	40.8	MHz
		V_{CC} = 5.0 V ±10% –40°C ≤ T_{opr} ≤ 85°C(2)	38.4	40	40.8	MHz
	High-speed on-chip oscillator frequency when correction value in FRA7 register is written to FRA1 register	V_{CC} = 5.0 V, T_{opr} = 25°C	–	36.864	–	MHz
		V_{CC} = 2.7 V to 5.5 V –20°C ≤ T_{opr} ≤ 85°C	–3%	–	3%	%
–	Value in FRA1 register after reset		08h	–	F7h	–
–	Oscillation frequency adjustment unit of high-speed on-chip oscillator	Adjust FRA1 register (value after reset) to –1	–	+0.3	–	MHz
–	Oscillation stability time		–	10	100	µs
–	Self power consumption at oscillation	V_{CC} = 5.0 V, T_{opr} = 25°C	–	400	–	µA

NOTES:

1. V_{CC} = 2.7 to 5.5 V, T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. These standard values show when the FRA1 register value after reset is assumed.

Table 5.12 Low-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-S	Low-speed on-chip oscillator frequency		30	125	250	kHz
–	Oscillation stability time		–	10	100	µs
–	Self power consumption at oscillation	V_{CC} = 5.0 V, T_{opr} = 25°C	–	15	–	µA

NOTE:

1. V_{CC} = 2.7 to 5.5 V, T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.

Table 5.13 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for internal power supply stabilization during power-on(2)		1	–	2000	µs
$t_{d(R-S)}$	STOP exit time(3)		–	–	150	µs

NOTES:

1. The measurement condition is V_{CC} = 2.7 to 5.5 V and T_{opr} = 25°C.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.
3. Time until system clock supply starts after the interrupt is acknowledged to exit stop mode.

Table 5.14 Electrical Characteristics (1) [V_{CC} = 5 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output "H" voltage	Except P1_0 to P1_7, XOUT	I_{OH} = –5 mA		V_{CC} – 2.0	–	V_{CC}	V
			I_{OH} = –200 μA		V_{CC} – 0.5	–	V_{CC}	V
		P1_0 to P1_7	Drive capacity HIGH	I_{OH} = –10 mA	V_{CC} – 2.0	–	V_{CC}	V
			Drive capacity LOW	I_{OH} = –5 mA	V_{CC} – 2.0	–	V_{CC}	V
		XOUT	Drive capacity HIGH	I_{OH} = –1 mA	V_{CC} – 2.0	–	V_{CC}	V
			Drive capacity LOW	I_{OH} = –500 μA	V_{CC} – 2.0	–	V_{CC}	V
V_{OL}	Output "L" voltage	Except P1_0 to P1_7, XOUT	I_{OL} = 5 mA		–	–	2.0	V
			I_{OL} = 200 μA		–	–	0.45	V
		P1_0 to P1_7	Drive capacity HIGH	I_{OL} = 10 mA	–	–	2.0	V
			Drive capacity LOW	I_{OL} = 5 mA	–	–	2.0	V
		XOUT	Drive capacity HIGH	I_{OL} = 1 mA	–	–	2.0	V
			Drive capacity LOW	I_{OL} = 500 μA	–	–	2.0	V
V_{T+}-V_{T-}	Hysteresis	$\overline{\text{INT0}}$, $\overline{\text{INT1}}$, $\overline{\text{INT3}}$, KI0, KI1, KI2, KI3, TRAIO, RXD0, CLK0			0.1	0.5	–	V
		$\overline{\text{RESET}}$			0.1	1.0	–	V
I_{IH}	Input "H" current		VI = 5 V, V_{CC} = 5 V		–	–	5.0	μA
I_{IL}	Input "L" current		VI = 0 V, V_{CC} = 5 V		–	–	–5.0	μA
R_{PULLUP}	Pull-up resistance		VI = 0 V, V_{CC} = 5 V		30	50	167	kΩ
R_{fXIN}	Feedback resistance	XIN			–	1.0	–	MΩ
V_{RAM}	RAM hold voltage		During stop mode		1.8	–	–	V

NOTE:

1. V_{CC} = 4.2 to 5.5 V at T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), $f_{(XIN)}$ = 20 MHz, unless otherwise specified.

Table 5.18 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLK0 input cycle time	200	–	ns
$t_{W(CKH)}$	CLK0 input “H” width	100	–	ns
$t_{W(CKL)}$	CLK0 input “L” width	100	–	ns
$t_{d(C-Q)}$	TXD0 output delay time	–	50	ns
$t_{h(C-Q)}$	TXD0 hold time	0	–	ns
$t_{su(D-C)}$	RXD0 input setup time	50	–	ns
$t_{h(C-D)}$	RXD0 input hold time	90	–	ns

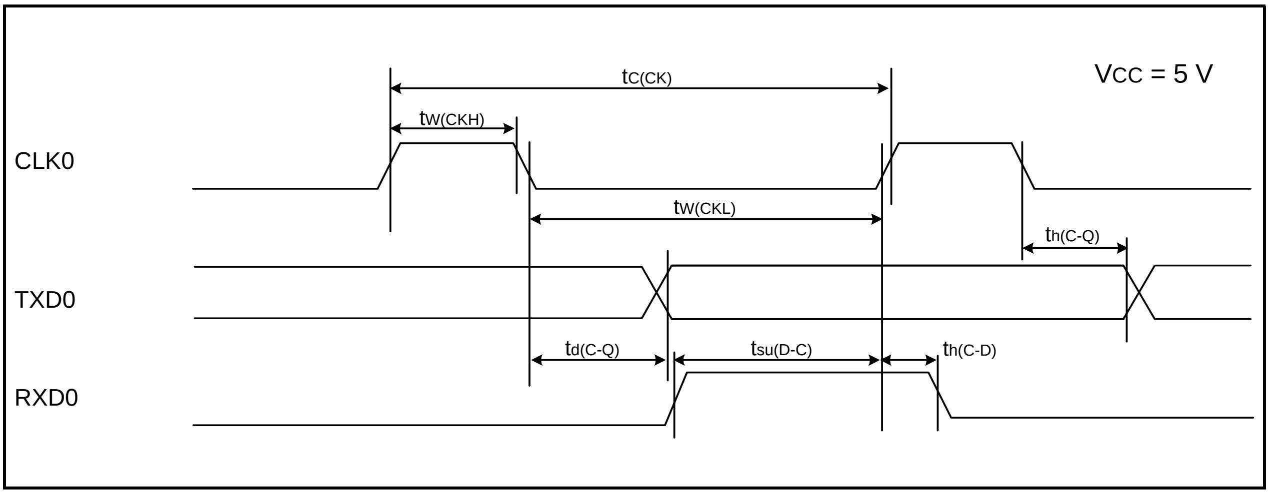


Figure 5.6 Serial Interface Timing Diagram when V_{CC} = 5 V

Table 5.19 External Interrupt $\overline{\text{INTi}}$ (i = 0, 1, 3) Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{\text{INTi}}$ input “H” width	250(1)	–	ns
$t_{W(INL)}$	$\overline{\text{INTi}}$ input “L” width	250(2)	–	ns

NOTES:

1. When selecting the digital filter by the $\overline{\text{INTi}}$ input filter select bit, use an $\overline{\text{INTi}}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{\text{INTi}}$ input filter select bit, use an $\overline{\text{INTi}}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

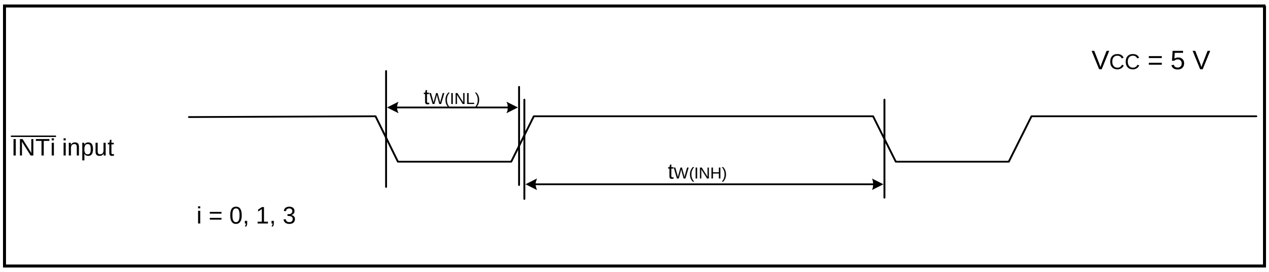


Figure 5.7 External Interrupt $\overline{\text{INTi}}$ Input Timing Diagram when V_{CC} = 5 V

Timing requirements
(Unless Otherwise Specified: V_{CC} = 3 V, V_{SS} = 0 V at T_{opr} = 25°C) [V_{CC} = 3 V]

Table 5.22 XIN Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	100	–	ns
$t_{WH(XIN)}$	XIN input “H” width	40	–	ns
$t_{WL(XIN)}$	XIN input “L” width	40	–	ns

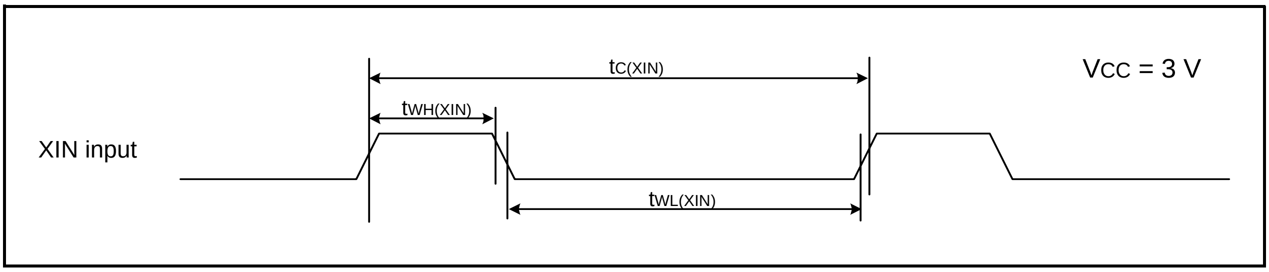


Figure 5.8 XIN Input Timing Diagram when V_{CC} = 3 V

Table 5.23 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	300	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	120	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	120	–	ns

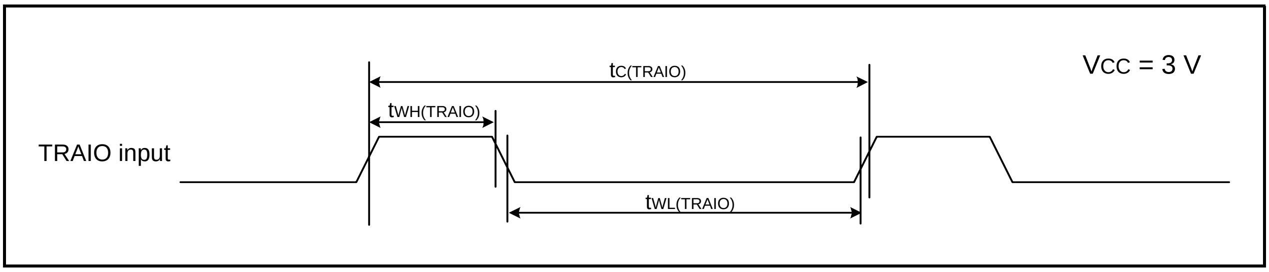


Figure 5.9 TRAIO Input Timing Diagram when V_{CC} = 3 V

Table 5.24 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLK0 input cycle time	300	–	ns
$t_{W(CKH)}$	CLK0 input “H” width	150	–	ns
$t_{W(CKL)}$	CLK0 Input “L” width	150	–	ns
$t_{d(C-Q)}$	TXD0 output delay time	–	80	ns
$t_{h(C-Q)}$	TXD0 hold time	0	–	ns
$t_{su(D-C)}$	RXD0 input setup time	70	–	ns
$t_{h(C-D)}$	RXD0 input hold time	90	–	ns

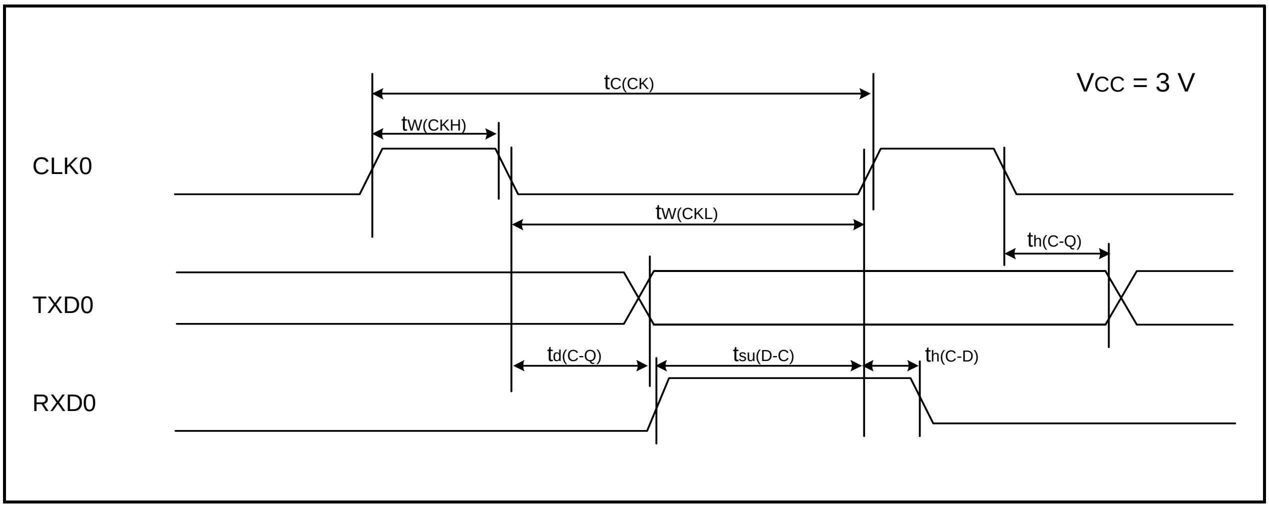


Figure 5.10 Serial Interface Timing Diagram when Vcc = 3 V

Table 5.25 External Interrupt $\overline{\text{INTi}}$ (i = 0, 1, 3) Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{\text{INTi}}$ input “H” width	380(1)	–	ns
$t_{W(INL)}$	$\overline{\text{INTi}}$ input “L” width	380(2)	–	ns

NOTES:

1. When selecting the digital filter by the $\overline{\text{INTi}}$ input filter select bit, use an $\overline{\text{INTi}}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{\text{INTi}}$ input filter select bit, use an $\overline{\text{INTi}}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

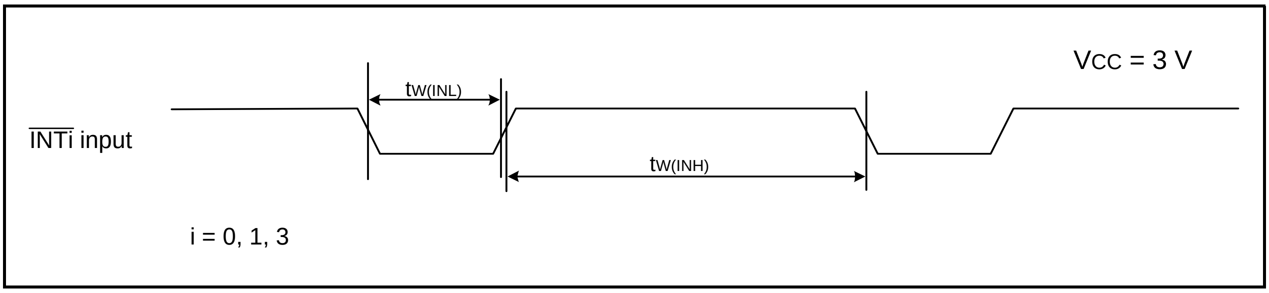


Figure 5.11 External Interrupt $\overline{\text{INTi}}$ Input Timing Diagram when Vcc = 3 V