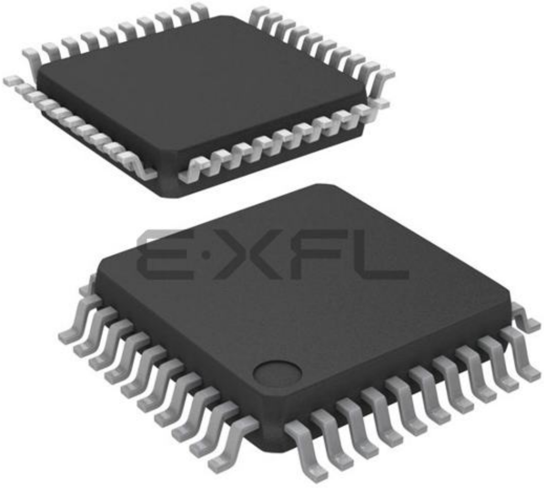

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| **Details** | |
|---|---|
| Product Status | Active |
| Core Processor | R8C |
| Core Size | 16-Bit |
| Speed | 20MHz |
| Connectivity | LINbus, SIO, UART/USART |
| Peripherals | POR, PWM, Voltage Detect, WDT |
| Number of I/O | 25 |
| Program Memory Size | 8KB (8K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 512 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 5.5V |
| Data Converters | A/D 12x10b; D/A 2x8b |
| Oscillator Type | Internal |
| Operating Temperature | -20°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 32-LQFP |
| Supplier Device Package | 32-LQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f212f2nfp-w4 |

### 1.1.2 Specifications

Tables 1.1 and 1.2 outlines the Specifications for R8C/2E Group and Tables 1.3 and 1.4 outlines the Specifications for R8C/2F Group.

**Table 1.1 Specifications for R8C/2E Group (1)**

| Item | Function | Specification |
|---|---|---|
| CPU | Central processing unit | R8C/Tiny series core<br>• Number of fundamental instructions: 89<br>• Minimum instruction execution time:<br>50 ns (f(XIN) = 20 MHz, VCC = 3.0 to 5.5 V)<br>100 ns (f(XIN) = 10 MHz, VCC = 2.7 to 5.5 V)<br>• Multiplier: 16 bits × 16 bits → 32 bits<br>• Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits<br>• Operation mode: Single-chip mode (address space: 1 Mbyte) |
| Memory | ROM, RAM | Refer to **Table 1.5 Product List for R8C/2E Group**. |
| Power Supply Voltage Detection | Voltage detection circuit | • Power-on reset<br>• Voltage detection 2 |
| I/O Ports | Programmable I/O ports | • Input-only: 3 pins<br>• CMOS I/O ports: 25, selectable pull-up resistor<br>• High current drive ports: 8 |
| Clock | Clock generation circuits | 2 circuits: XIN clock oscillation circuit (with on-chip feedback resistor),<br>On-chip oscillator (high-speed, low-speed)<br>(high-speed on-chip oscillator has a frequency adjustment function)<br>• Oscillation stop detection: XIN clock oscillation stop detection function<br>• Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16<br>• Low power consumption modes:<br>Standard operating mode (high-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode |
| Interrupts | | • External: 4 sources, Internal: 13 sources, Software: 4 sources<br>• Priority levels: 7 levels |
| Watchdog Timer | | 15 bits × 1 (with prescaler), reset start selectable |
| Timer | Timer RA | 8 bits × 1 (with 8-bit prescaler)<br>Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode |
| | Timer RB | 8 bits × 1 (with 8-bit prescaler)<br>Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode |
| | Timer RC | 16 bits × 1 (with 4 capture/compare registers)<br>Timer mode (input capture function, output compare function), PWM mode (output 3 pins), PWM2 mode (PWM output pin) |
| | Timer RE | 8 bits × 1<br>Output compare mode |
| Serial Interface | UART0 | Clock synchronous serial I/O/UART × 1 |
| LIN Module | | Hardware LIN: 1 (timer RA, UART0) |
| A/D Converter | | 10-bit resolution × 12 channels, includes sample and hold function |
| D/A Converter | | 8-bit resolution × 2 circuits |
| Comparator | | 2 circuits |

**Table 1.3 Specifications for R8C/2F Group (1)**

| Item | Function | Specification |
|---|---|---|
| CPU | Central processing unit | R8C/Tiny series core<br>• Number of fundamental instructions: 89<br>• Minimum instruction execution time:<br>50 ns (f(XIN) = 20 MHz, VCC = 3.0 to 5.5 V)<br>100 ns (f(XIN) = 10 MHz, VCC = 2.7 to 5.5 V)<br>• Multiplier: 16 bits × 16 bits → 32 bits<br>• Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits<br>• Operation mode: Single-chip mode (address space: 1 Mbyte) |
| Memory | ROM, RAM | Refer to **Table 1.6 Product List for R8C/2F Group**. |
| Power Supply Voltage Detection | Voltage detection circuit | • Power-on reset<br>• Voltage detection 2 |
| I/O Ports | Programmable I/O ports | • Input-only: 3 pins<br>• CMOS I/O ports: 25, selectable pull-up resistor<br>• High current drive ports: 8 |
| Clock | Clock generation circuits | 2 circuits: XIN clock oscillation circuit (with on-chip feedback resistor), On-chip oscillator (high-speed, low-speed) (high-speed on-chip oscillator has a frequency adjustment function)<br>• Oscillation stop detection: XIN clock oscillation stop detection function<br>• Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16<br>• Low power consumption modes:<br>Standard operating mode (high-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode |
| Interrupts | | • External: 4 sources, Internal: 13 sources, Software: 4 sources<br>• Priority levels: 7 levels |
| Watchdog Timer | | 15 bits × 1 (with prescaler), reset start selectable |
| Timer | Timer RA | 8 bits × 1 (with 8-bit prescaler)<br>Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode |
| | Timer RB | 8 bits × 1 (with 8-bit prescaler)<br>Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode |
| | Timer RC | 16 bits × 1 (with 4 capture/compare registers)<br>Timer mode (input capture function, output compare function), PWM mode (output 3 pins), PWM2 mode (PWM output pin) |
| | Timer RE | 8 bits × 1<br>Output compare mode |
| Serial Interface | UART0 | Clock synchronous serial I/O/UART × 1 |
| LIN Module | | Hardware LIN: 1 (timer RA, UART0) |
| A/D Converter | | 10-bit resolution × 12 channels, includes sample and hold function |
| D/A Converter | | 8-bit resolution × 2 circuits |
| Comparator | | 2 circuits |

## 1.2 Product List

Table 1.5 lists Product List for R8C/2E Group, Figure 1.1 shows a Part Number, Memory Size, and Package of R8C/2E Group, Table 1.6 lists Product List for R8C/2F Group, and Figure 1.2 shows a Part Number, Memory Size, and Package of R8C/2F Group.

**Table 1.5 Product List for R8C/2E Group** **Current of Dec. 2007**

| Part No. | ROM Capacity | RAM Capacity | Package Type | Remarks |
|---|---|---|---|---|
| R5F212E2NFP | 8 Kbytes | 512 bytes | PLQP0032GB-A | N version |
| R5F212E4NFP | 16 Kbytes | 1 Kbyte | PLQP0032GB-A | |
| R5F212E2DFP | 8 Kbytes | 512 bytes | PLQP0032GB-A | D version |
| R5F212E4DFP | 16 Kbytes | 1 Kbyte | PLQP0032GB-A | |
| R5F212E2NXXXFP | 8 Kbytes | 512 bytes | PLQP0032GB-A | N version<br>Factory programming product(1) |
| R5F212E4NXXXFP | 16 Kbytes | 1 Kbyte | PLQP0032GB-A | |
| R5F212E2DXXXFP | 8 Kbytes | 512 bytes | PLQP0032GB-A | D version<br>Factory programming product(1) |
| R5F212E4DXXXFP | 16 Kbytes | 1 Kbyte | PLQP0032GB-A | |

NOTE:

1. The user ROM is programmed before shipment.

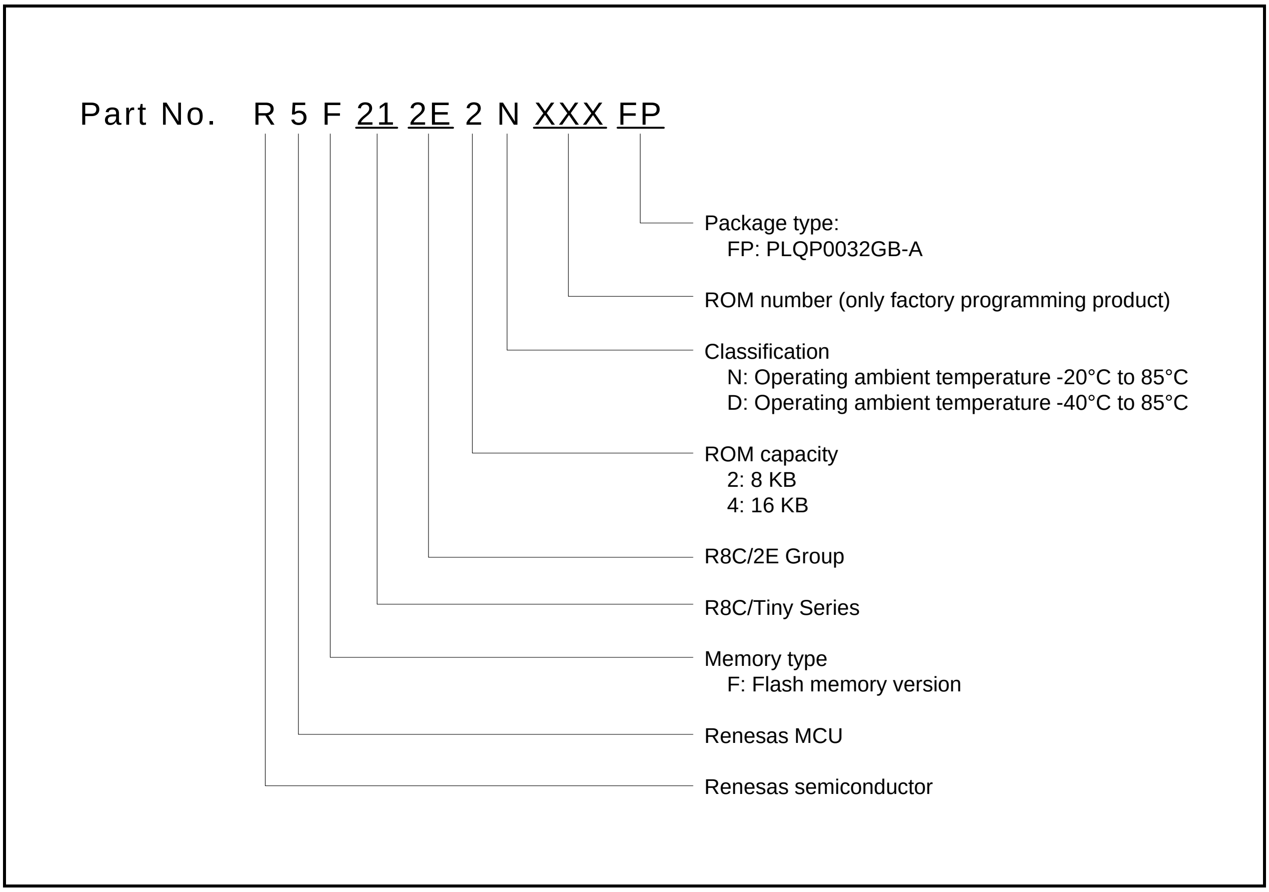


**Figure 1.1 Part Number, Memory Size, and Package of R8C/2E Group**

**Table 1.6 Product List for R8C/2F Group** **Current of Dec. 2007**

| Part No. | ROM Capacity | | RAM Capacity | Package Type | Remarks |
|---|---|---|---|---|---|
| | Program ROM | Data flash | | | |
| R5F212F2NFP | 8 Kbytes | 1 Kbyte × 2 | 512 bytes | PLQP0032GB-A | N version |
| R5F212F4NFP | 16 Kbytes | 1 Kbyte × 2 | 1 Kbyte | PLQP0032GB-A | |
| R5F212F2DFP | 8 Kbytes | 1 Kbyte × 2 | 512 bytes | PLQP0032GB-A | D version |
| R5F212F4DFP | 16 Kbytes | 1 Kbyte × 2 | 1 Kbyte | PLQP0032GB-A | |
| R5F212F2NXXXFP | 8 Kbytes | 1 Kbyte × 2 | 512 bytes | PLQP0032GB-A | N version<br>Factory programming product(1) |
| R5F212F4NXXXFP | 16 Kbytes | 1 Kbyte × 2 | 1 Kbyte | PLQP0032GB-A | |
| R5F212F2DXXXFP | 8 Kbytes | 1 Kbyte × 2 | 512 bytes | PLQP0032GB-A | D version<br>Factory programming product(1) |
| R5F212F4DXXXFP | 16 Kbytes | 1 Kbyte × 2 | 1 Kbyte | PLQP0032GB-A | |

NOTE:

1. The user ROM is programmed before shipment.

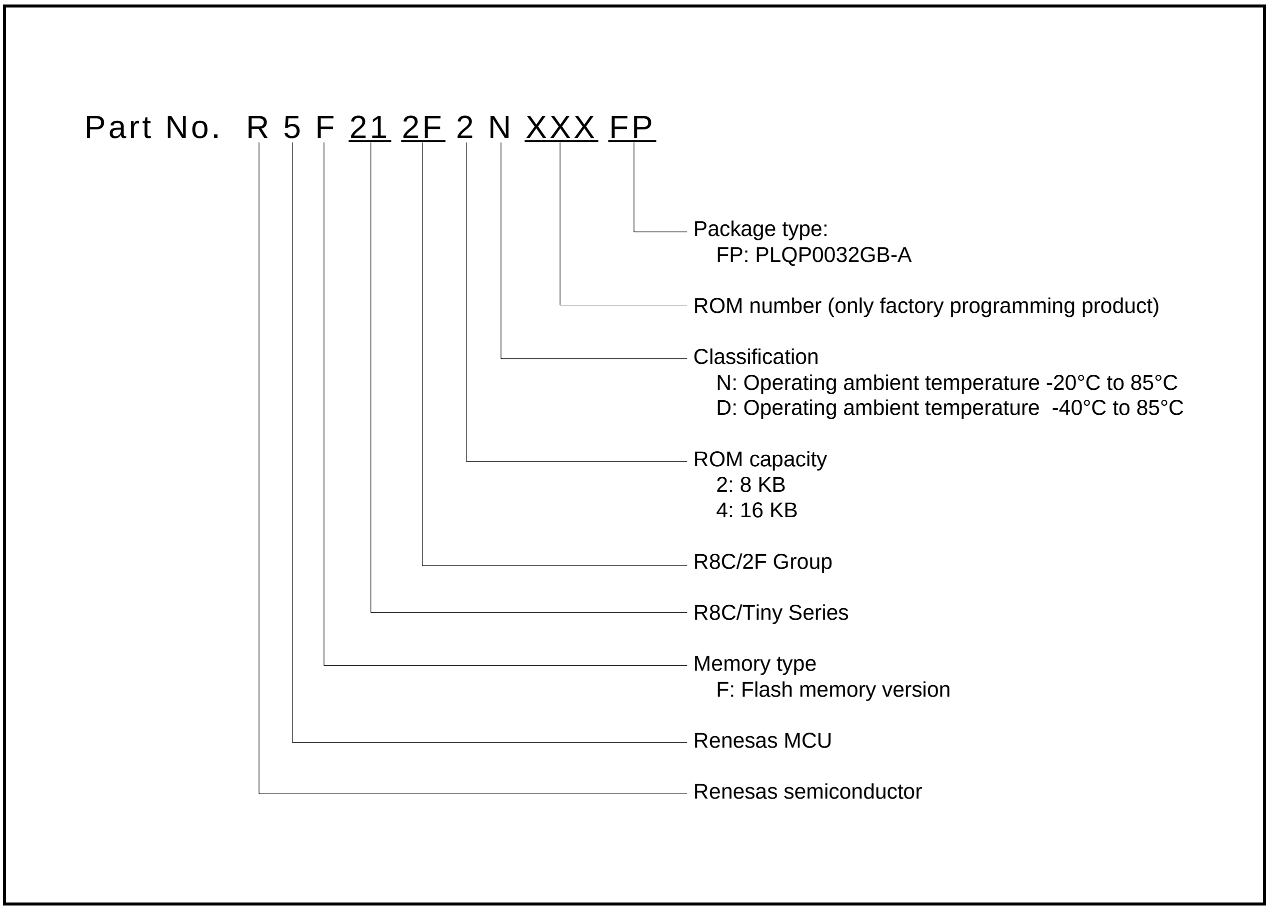
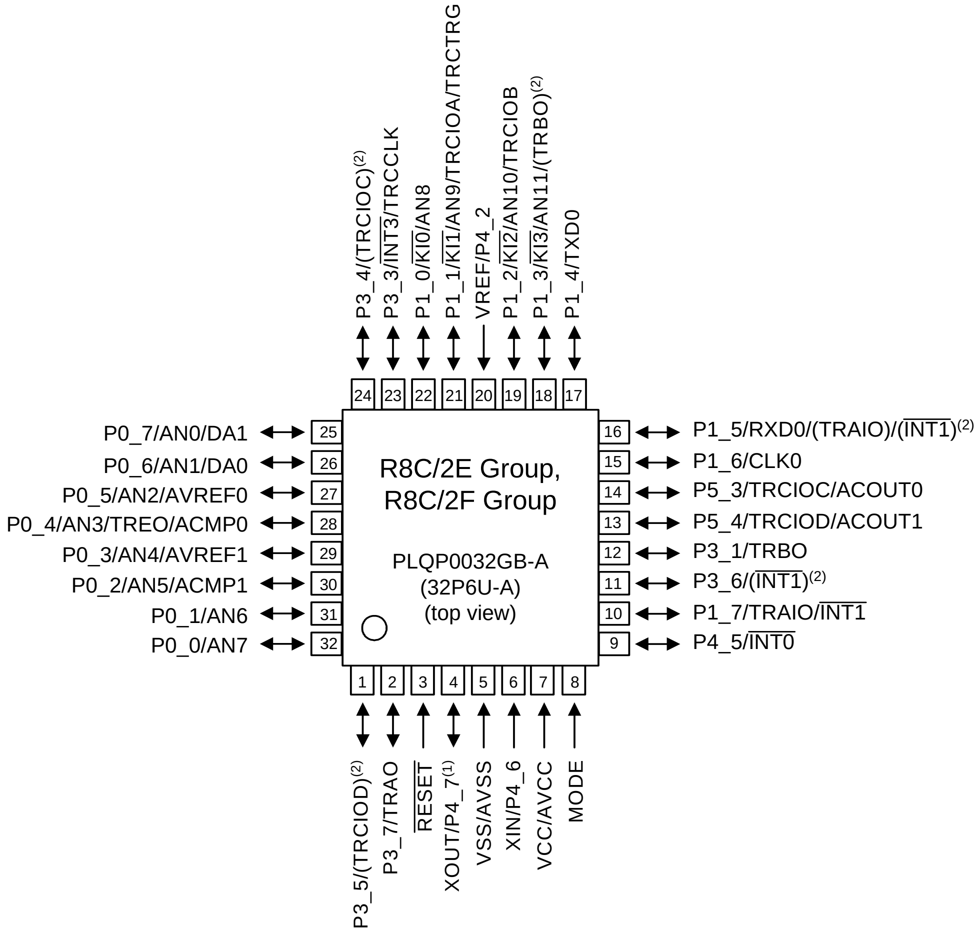


**Figure 1.2 Part Number, Memory Size, and Package of R8C/2F Group**

## 1.4 Pin Assignment

Figure 1.4 shows Pin Assignments (Top View). Table 1.7 outlines the Pin Name Information by Pin Number.



NOTES:
1. P4_7 is an input-only port.
2. Can be assigned to the pin in parentheses by a program.
3. Confirm the pin 1 position on the package by referring to the package dimensions.

**Figure 1.4 Pin Assignments (Top View)**

**Table 1.7 Pin Name Information by Pin Number**

| Pin Number | Control Pin | Port | I/O Pin Functions for of Peripheral Modules | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | Interrupt | Timer | Serial Interface | A/D Converter | D/A Converter | Comparator |
| 1 | | P3_5 | | (TRCIOD)(1) | | | | |
| 2 | | P3_7 | | TRAO | | | | |
| 3 | $\overline{\mathrm{RESET}}$ | | | | | | | |
| 4 | XOUT | P4_7 | | | | | | |
| 5 | VSS/AVSS | | | | | | | |
| 6 | XIN | P4_6 | | | | | | |
| 7 | VCC/AVCC | | | | | | | |
| 8 | MODE | | | | | | | |
| 9 | | P4_5 | $\overline{\mathrm{INT0}}$ | | | | | |
| 10 | | P1_7 | $\overline{\mathrm{INT1}}$ | TRAIO | | | | |
| 11 | | P3_6 | ($\overline{\mathrm{INT1}}$)(1) | | | | | |
| 12 | | P3_1 | | TRBO | | | | |
| 13 | | P5_4 | | TRCIOD | | | | ACOUT1 |
| 14 | | P5_3 | | TRCIOC | | | | ACOUT0 |
| 15 | | P1_6 | | | CLK0 | | | |
| 16 | | P1_5 | ($\overline{\mathrm{INT1}}$)(1) | (TRAIO)(1) | RXD0 | | | |
| 17 | | P1_4 | | | TXD0 | | | |
| 18 | | P1_3 | $\overline{\mathrm{KI3}}$ | (TRBO)(1) | | AN11 | | |
| 19 | | P1_2 | $\overline{\mathrm{KI2}}$ | TRCIOB | | AN10 | | |
| 20 | VREF | P4_2 | | | | | | |
| 21 | | P1_1 | $\overline{\mathrm{KI1}}$ | TRCIOA/TRCTRG | | AN9 | | |
| 22 | | P1_0 | $\overline{\mathrm{KI0}}$ | | | AN8 | | |
| 23 | | P3_3 | $\overline{\mathrm{INT3}}$ | TRCCLK | | | | |
| 24 | | P3_4 | | (TRCIOC)(1) | | | | |
| 25 | | P0_7 | | | | AN0 | DA1 | |
| 26 | | P0_6 | | | | AN1 | DA0 | |
| 27 | | P0_5 | | | | AN2 | | AVREF0 |
| 28 | | P0_4 | | TREO | | AN3 | | ACMP0 |
| 29 | | P0_3 | | | | AN4 | | AVREF1 |
| 30 | | P0_2 | | | | AN5 | | ACMP1 |
| 31 | | P0_1 | | | | AN6 | | |
| 32 | | P0_0 | | | | AN7 | | |

NOTE:

1. Can be assigned to the pin in parentheses by a program.

## 2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

## 2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 to be used as a 32-bit address register (A1A0).

## 2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

## 2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the start address of an interrupt vector table.

## 2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

## 2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP, and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

## 2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

## 2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

### 2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

### 2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

### 2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

### 2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

### 2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

### 2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

# 3. Memory

## 3.1 R8C/2E Group

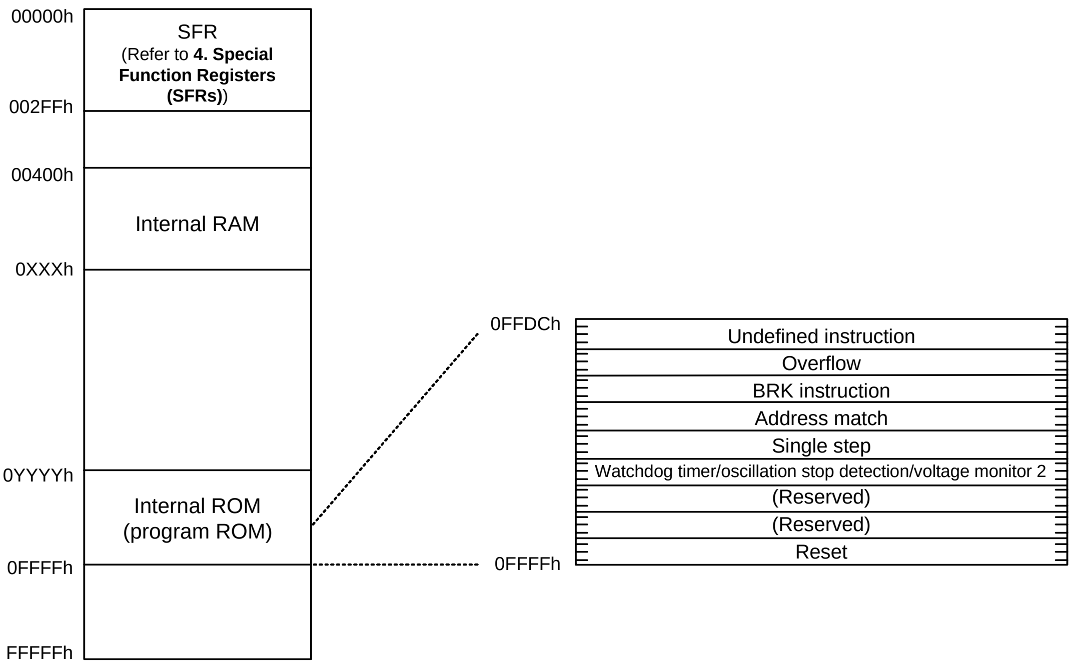
Figure 3.1 is a Memory Map of R8C/2E Group. The R8C/2E group has 1 Mbyte of address space from addresses 00000h to FFFFFh.

The internal ROM is allocated lower addresses, beginning with address 0FFFFh. For example, a 16-Kbyte internal ROM area is allocated addresses 0C000h to 0FFFFh.

The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.

The internal RAM is allocated higher addresses beginning with address 00400h. For example, a 1-Kbyte internal RAM area is allocated addresses 00400h to 007FFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.

Special function registers (SFRs) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated here. All addresses within the SFR, which have nothing allocated are reserved for future use and cannot be accessed by users.



NOTE:
1. The blank regions are reserved. Do not access locations in these regions.

| Part Number | Internal ROM | | Internal RAM | |
|---|---|---|---|---|
| | Size | Address 0YYYYh | Size | Address 0XXXXh |
| R5F212E2NFP, R5F212E2DFP,<br>R5F212E2NXXXFP, R5F212E2DXXXFP | 8 Kbytes | 0E000h | 512 bytes | 005FFh |
| R5F212E4NFP, R5F212E4DFP,<br>R5F212E4NXXXFP, R5F212E4DXXXFP | 16 Kbytes | 0C000h | 1 Kbyte | 007FFh |

**Figure 3.1 Memory Map of R8C/2E Group**

### Table 4.2 SFR Information (2)(1)

| Address | Register | Symbol | After reset |
|---|---|---|---|
| 0040h | | | |
| 0041h | | | |
| 0042h | | | |
| 0043h | | | |
| 0044h | | | |
| 0045h | | | |
| 0046h | | | |
| 0047h | Timer RC Interrupt Control Register | TRCIC | XXXXX000b |
| 0048h | | | |
| 0049h | | | |
| 004Ah | Timer RE Interrupt Control Register | TREIC | XXXXX000b |
| 004Bh | | | |
| 004Ch | | | |
| 004Dh | Key Input Interrupt Control Register | KUPIC | XXXXX000b |
| 004Eh | A/D Conversion Interrupt Control Register | ADIC | XXXXX000b |
| 004Fh | | | |
| 0050h | | | |
| 0051h | UART0 Transmit Interrupt Control Register | S0TIC | XXXXX000b |
| 0052h | UART0 Receive Interrupt Control Register | S0RIC | XXXXX000b |
| 0053h | | | |
| 0054h | | | |
| 0055h | | | |
| 0056h | Timer RA Interrupt Control Register | TRAIC | XXXXX000b |
| 0057h | | | |
| 0058h | Timer RB Interrupt Control Register | TRBIC | XXXXX000b |
| 0059h | INT1 Interrupt Control Register | INT1IC | XX00X000b |
| 005Ah | INT3 Interrupt Control Register | INT3IC | XX00X000b |
| 005Bh | Comparator 0 Interrupt Control Register | CM0IC | XXXXX000b |
| 005Ch | Comparator 1 Interrupt Control Register | CM1IC | XXXXX000b |
| 005Dh | INT0 Interrupt Control Register | INT0IC | XX00X000b |
| 005Eh | | | |
| 005Fh | | | |
| 0060h | | | |
| 0061h | | | |
| 0062h | | | |
| 0063h | | | |
| 0064h | | | |
| 0065h | | | |
| 0066h | | | |
| 0067h | | | |
| 0068h | | | |
| 0069h | | | |
| 006Ah | | | |
| 006Bh | | | |
| 006Ch | | | |
| 006Dh | | | |
| 006Eh | | | |
| 006Fh | | | |
| 0070h | | | |
| 0071h | | | |
| 0072h | | | |
| 0073h | | | |
| 0074h | | | |
| 0075h | | | |
| 0076h | | | |
| 0077h | | | |
| 0078h | | | |
| 0079h | | | |
| 007Ah | | | |
| 007Bh | | | |
| 007Ch | | | |
| 007Dh | | | |
| 007Eh | | | |
| 007Fh | | | |

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

### Table 4.4 SFR Information (4)[1]

| Address | Register | Symbol | After reset |
|---|---|---|---|
| 00C0h | A/D Register | AD | XXh |
| 00C1h | | | XXh |
| 00C2h | | | |
| 00C3h | | | |
| 00C4h | | | |
| 00C5h | | | |
| 00C6h | | | |
| 00C7h | | | |
| 00C8h | | | |
| 00C9h | | | |
| 00CAh | | | |
| 00CBh | | | |
| 00CCh | | | |
| 00CDh | | | |
| 00CEh | | | |
| 00CFh | | | |
| 00D0h | | | |
| 00D1h | | | |
| 00D2h | | | |
| 00D3h | | | |
| 00D4h | A/D Control Register 2 | ADCON2 | 00h |
| 00D5h | | | |
| 00D6h | A/D Control Register 0 | ADCON0 | 00h |
| 00D7h | A/D Control Register 1 | ADCON1 | 00h |
| 00D8h | D/A Register 0 | DA0 | 00h |
| 00D9h | | | |
| 00DAh | D/A Register 1 | DA1 | 00h |
| 00DBh | | | |
| 00DCh | D/A Control Register | DACON | 00h |
| 00DDh | | | |
| 00DEh | | | |
| 00DFh | | | |
| 00E0h | Port P0 Register | P0 | 00h |
| 00E1h | Port P1 Register | P1 | 00h |
| 00E2h | Port P0 Direction Register | PD0 | 00h |
| 00E3h | Port P1 Direction Register | PD1 | 00h |
| 00E4h | | | |
| 00E5h | Port P3 Register | P3 | 00h |
| 00E6h | | | |
| 00E7h | Port P3 Direction Register | PD3 | 00h |
| 00E8h | Port P4 Register | P4 | 00h |
| 00E9h | Port P5 Register | P5 | 00h |
| 00EAh | Port P4 Direction Register | PD4 | 00h |
| 00EBh | Port P5 Direction Register | PD5 | 00h |
| 00ECh | | | |
| 00EDh | | | |
| 00EEh | | | |
| 00EFh | | | |
| 00F0h | | | |
| 00F1h | | | |
| 00F2h | | | |
| 00F3h | | | |
| 00F4h | | | |
| 00F5h | | | |
| 00F6h | Pin Select Register 2 | PINSR2 | 00h |
| 00F7h | Pin Select Register 3 | PINSR3 | 00h |
| 00F8h | Port Mode Register | PMR | 00h |
| 00F9h | External Input Enable Register | INTEN | 00h |
| 00FAh | INT Input Filter Select Register | INTF | 00h |
| 00FBh | Key Input Enable Register | KIEN | 00h |
| 00FCh | Pull-Up Control Register 0 | PUR0 | 00h |
| 00FDh | Pull-Up Control Register 1 | PUR1 | 00h |
| 00FEh | Port P1 Drive Capacity Control Register | P1DRR | 00h |
| 00FFh | | | |

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

### Table 4.5 SFR Information (5)(1)

| Address | Register | Symbol | After reset |
|---|---|---|---|
| 0100h | Timer RA Control Register | TRACR | 00h |
| 0101h | Timer RA I/O Control Register | TRAIOC | 00h |
| 0102h | Timer RA Mode Register | TRAMR | 00h |
| 0103h | Timer RA Prescaler Register | TRAPRE | FFh |
| 0104h | Timer RA Register | TRA | FFh |
| 0105h | | | |
| 0106h | LIN Control Register | LINCR | 00h |
| 0107h | LIN Status Register | LINST | 00h |
| 0108h | Timer RB Control Register | TRBCR | 00h |
| 0109h | Timer RB One-Shot Control Register | TRBOCR | 00h |
| 010Ah | Timer RB I/O Control Register | TRBIOC | 00h |
| 010Bh | Timer RB Mode Register | TRBMR | 00h |
| 010Ch | Timer RB Prescaler Register | TRBPRE | FFh |
| 010Dh | Timer RB Secondary Register | TRBSC | FFh |
| 010Eh | Timer RB Primary Register | TRBPR | FFh |
| 010Fh | | | |
| 0110h | | | |
| 0111h | | | |
| 0112h | | | |
| 0113h | | | |
| 0114h | | | |
| 0115h | | | |
| 0116h | | | |
| 0117h | | | |
| 0118h | Timer RE Counter Data Register | TRESEC | 00h |
| 0119h | Timer RE Compare Data Register | TREMIN | 00h |
| 011Ah | | | |
| 011Bh | | | |
| 011Ch | Timer RE Control Register 1 | TRECR1 | 00h |
| 011Dh | Timer RE Control Register 2 | TRECR2 | 00h |
| 011Eh | Timer RE Clock Source Select Register | TRECSR | 00001000b |
| 011Fh | | | |
| 0120h | Timer RC Mode Register | TRCMR | 01001000b |
| 0121h | Timer RC Control Register 1 | TRCCR1 | 00h |
| 0122h | Timer RC Interrupt Enable Register | TRCIER | 01110000b |
| 0123h | Timer RC Status Register | TRCSR | 01110000b |
| 0124h | Timer RC I/O Control Register 0 | TRCIOR0 | 10001000b |
| 0125h | Timer RC I/O Control Register 1 | TRCIOR1 | 10001000b |
| 0126h | Timer RC Counter | TRC | 00h |
| 0127h | | | 00h |
| 0128h | Timer RC General Register A | TRCGRA | FFh |
| 0129h | | | FFh |
| 012Ah | Timer RC General Register B | TRCGRB | FFh |
| 012Bh | | | FFh |
| 012Ch | Timer RC General Register C | TRCGRC | FFh |
| 012Dh | | | FFh |
| 012Eh | Timer RC General Register D | TRCGRD | FFh |
| 012Fh | | | FFh |
| 0130h | Timer RC Control Register 2 | TRCCR2 | 00011111b |
| 0131h | Timer RC Digital Filter Function Select Register | TRCDF | 00h |
| 0132h | Timer RC Output Master Enable Register | TRCOER | 01111111b |
| 0133h | | | |
| 0134h | | | |
| 0135h | | | |
| 0136h | | | |
| 0137h | | | |
| 0138h | | | |
| 0139h | | | |
| 013Ah | | | |
| 013Bh | | | |
| 013Ch | | | |
| 013Dh | | | |
| 013Eh | | | |
| 013Fh | | | |

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

### Table 5.7 Flash Memory (Data flash Block A, Block B) Electrical Characteristics[4]

| Symbol | Parameter | Conditions | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| – | Program/erase endurance[2] | | 10,000[3] | – | – | times |
| – | Byte program time<br>(program/erase endurance ≤ 1,000 times) | | – | 50 | 400 | µs |
| – | Byte program time<br>(program/erase endurance > 1,000 times) | | – | 65 | – | µs |
| – | Block erase time<br>(program/erase endurance ≤ 1,000 times) | | – | 0.2 | 9 | s |
| – | Block erase time<br>(program/erase endurance > 1,000 times) | | – | 0.3 | – | s |
| $t_{d(SR-SUS)}$ | Time delay from suspend request until suspend | | – | – | 97+CPU clock × 6 cycles | µs |
| – | Interval from erase start/restart until following suspend request | | 650 | – | – | µs |
| – | Interval from program start/restart until following suspend request | | 0 | – | – | ns |
| – | Time from suspend until program/erase restart | | – | – | 3+CPU clock × 4 cycles | µs |
| – | Program, erase voltage | | 2.7 | – | 5.5 | V |
| – | Read voltage | | 2.7 | – | 5.5 | V |
| – | Program, erase temperature | | –20[8] | – | 85 | °C |
| – | Data hold time[9] | Ambient temperature = 55 °C | 20 | – | – | year |

NOTES:

1. $V_{CC}$ = 2.7 to 5.5 V at $T_{opr}$ = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 100 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
   However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. Standard of block A and block B when program and erase endurance exceeds 1,000 times. Byte program time to 1,000 times is the same as that in program ROM.
5. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erase count of each block and limit the number of erase operations to a certain number.
6. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
7. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
8. –40°C for D version.
9. The data hold time includes time that the power supply is off or the clock is not supplied.

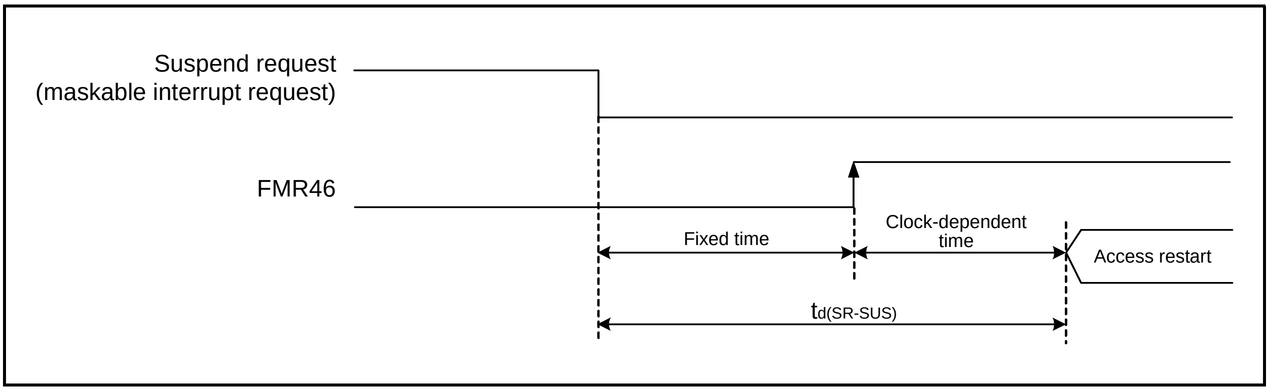


**Figure 5.2 Time delay until Suspend**

**Table 5.8 Voltage Detection 1 Circuit Electrical Characteristics**

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{det1}$ | Voltage detection level[4] | | 2.7 | 2.85 | 3.00 | V |
| – | Voltage monitor 1 interrupt request generation time[2] | | – | 40 | – | µs |
| – | Voltage detection circuit self power consumption | VCA26 = 1, $V_{CC}$ = 5.0 V | – | 0.6 | – | µA |
| $t_{d(E-A)}$ | Waiting time until voltage detection circuit operation starts[3] | | – | – | 100 | µs |
| Vccmin | MCU operating voltage minimum value | | 2.7 | – | – | V |

NOTES:
1. The measurement condition is $V_{CC}$ = 2.7 V to 5.5 V and $T_{opr}$ = –20 to 85°C (N version) / –40 to 85°C (D version).
2. Time until the voltage monitor 1 interrupt request is generated after the voltage passes $V_{det1}$.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.
4. This parameter shows the voltage detection level when the power supply drops.
   The voltage detection level when the power supply rises is higher than the voltage detection level when the power supply drops by approximately 0.1 V.

**Table 5.9 Voltage Detection 2 Circuit Electrical Characteristics**

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{det2}$ | Voltage detection level | | 3.3 | 3.6 | 3.9 | V |
| – | Voltage monitor 2 interrupt request generation time[2] | | – | 40 | – | µs |
| – | Voltage detection circuit self power consumption | VCA27 = 1, $V_{CC}$ = 5.0 V | – | 0.6 | – | µA |
| $t_{d(E-A)}$ | Waiting time until voltage detection circuit operation starts[3] | | – | – | 100 | µs |

NOTES:
1. The measurement condition is $V_{CC}$ = 2.7 V to 5.5 V and $T_{opr}$ = –20 to 85°C (N version) / –40 to 85°C (D version).
2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes $V_{det2}$.
3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

### Table 5.11 High-speed On-Chip Oscillator Circuit Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $f_{OCO40M}$ | High-speed on-chip oscillator frequency temperature • supply voltage dependence | $V_{CC}$ = 4.75 V to 5.25 V<br>0°C ≤ $T_{opr}$ ≤ 60°C(2) | 39.2 | 40 | 40.8 | MHz |
| | | $V_{CC}$ = 3.0 V to 5.5 V<br>–20°C ≤ $T_{opr}$ ≤ 85°C(2) | 38.8 | 40 | 41.2 | MHz |
| | | $V_{CC}$ = 3.0 V to 5.5 V<br>–40°C ≤ $T_{opr}$ ≤ 85°C(2) | 38.4 | 40 | 41.6 | MHz |
| | | $V_{CC}$ = 2.7 V to 5.5 V<br>–20°C ≤ $T_{opr}$ ≤ 85°C(2) | 38 | 40 | 42 | MHz |
| | | $V_{CC}$ = 2.7 V to 5.5 V<br>–40°C ≤ $T_{opr}$ ≤ 85°C(2) | 37.6 | 40 | 42.4 | MHz |
| | | $V_{CC}$ = 5.0 V ±10%<br>–20°C ≤ $T_{opr}$ ≤ 85°C(2) | 38.8 | 40 | 40.8 | MHz |
| | | $V_{CC}$ = 5.0 V ±10%<br>–40°C ≤ $T_{opr}$ ≤ 85°C(2) | 38.4 | 40 | 40.8 | MHz |
| | High-speed on-chip oscillator frequency when correction value in FRA7 register is written to FRA1 register | $V_{CC}$ = 5.0 V, $T_{opr}$ = 25°C | – | 36.864 | – | MHz |
| | | $V_{CC}$ = 2.7 V to 5.5 V<br>–20°C ≤ $T_{opr}$ ≤ 85°C | –3% | – | 3% | % |
| – | Value in FRA1 register after reset | | 08h | – | F7h | – |
| – | Oscillation frequency adjustment unit of high-speed on-chip oscillator | Adjust FRA1 register (value after reset) to –1 | – | +0.3 | – | MHz |
| – | Oscillation stability time | | – | 10 | 100 | µs |
| – | Self power consumption at oscillation | $V_{CC}$ = 5.0 V, $T_{opr}$ = 25°C | – | 400 | – | µA |

NOTES:
1. $V_{CC}$ = 2.7 to 5.5 V, $T_{opr}$ = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. These standard values show when the FRA1 register value after reset is assumed.

### Table 5.12 Low-speed On-Chip Oscillator Circuit Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $f_{OCO-S}$ | Low-speed on-chip oscillator frequency | | 30 | 125 | 250 | kHz |
| – | Oscillation stability time | | – | 10 | 100 | µs |
| – | Self power consumption at oscillation | $V_{CC}$ = 5.0 V, $T_{opr}$ = 25°C | – | 15 | – | µA |

NOTE:
1. $V_{CC}$ = 2.7 to 5.5 V, $T_{opr}$ = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.

### Table 5.13 Power Supply Circuit Timing Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $t_{d(P-R)}$ | Time for internal power supply stabilization during power-on(2) | | 1 | – | 2000 | µs |
| $t_{d(R-S)}$ | STOP exit time(3) | | – | – | 150 | µs |

NOTES:
1. The measurement condition is $V_{CC}$ = 2.7 to 5.5 V and $T_{opr}$ = 25°C.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.
3. Time until system clock supply starts after the interrupt is acknowledged to exit stop mode.

### Table 5.14 Electrical Characteristics (1) [$V_{CC}$ = 5 V]

| Symbol | Parameter | | Condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min. | Typ. | Max. | |
| $V_{OH}$ | Output “H” voltage | Except P1_0 to P1_7, XOUT | $I_{OH}$ = –5 mA | | $V_{CC}$ – 2.0 | – | $V_{CC}$ | V |
| | | | $I_{OH}$ = –200 µA | | $V_{CC}$ – 0.5 | – | $V_{CC}$ | V |
| | | P1_0 to P1_7 | Drive capacity HIGH | $I_{OH}$ = –10 mA | $V_{CC}$ – 2.0 | – | $V_{CC}$ | V |
| | | | Drive capacity LOW | $I_{OH}$ = –5 mA | $V_{CC}$ – 2.0 | – | $V_{CC}$ | V |
| | | XOUT | Drive capacity HIGH | $I_{OH}$ = –1 mA | $V_{CC}$ – 2.0 | – | $V_{CC}$ | V |
| | | | Drive capacity LOW | $I_{OH}$ = –500 µA | $V_{CC}$ – 2.0 | – | $V_{CC}$ | V |
| $V_{OL}$ | Output “L” voltage | Except P1_0 to P1_7, XOUT | $I_{OL}$ = 5 mA | | – | – | 2.0 | V |
| | | | $I_{OL}$ = 200 µA | | – | – | 0.45 | V |
| | | P1_0 to P1_7 | Drive capacity HIGH | $I_{OL}$ = 10 mA | – | – | 2.0 | V |
| | | | Drive capacity LOW | $I_{OL}$ = 5 mA | – | – | 2.0 | V |
| | | XOUT | Drive capacity HIGH | $I_{OL}$ = 1 mA | – | – | 2.0 | V |
| | | | Drive capacity LOW | $I_{OL}$ = 500 µA | – | – | 2.0 | V |
| $V_{T+}$-$V_{T-}$ | Hysteresis | $\overline{INT0}$, $\overline{INT1}$, $\overline{INT3}$, KI0, KI1, KI2, KI3, TRAIO, RXD0, CLK0 | | | 0.1 | 0.5 | – | V |
| | | $\overline{RESET}$ | | | 0.1 | 1.0 | – | V |
| $I_{IH}$ | Input “H” current | | VI = 5 V, $V_{CC}$ = 5 V | | – | – | 5.0 | µA |
| $I_{IL}$ | Input “L” current | | VI = 0 V, $V_{CC}$ = 5 V | | – | – | –5.0 | µA |
| $R_{PULLUP}$ | Pull-up resistance | | VI = 0 V, $V_{CC}$ = 5 V | | 30 | 50 | 167 | kΩ |
| $R_{fXIN}$ | Feedback resistance | XIN | | | – | 1.0 | – | MΩ |
| $V_{RAM}$ | RAM hold voltage | | During stop mode | | 1.8 | – | – | V |

NOTE:

1. $V_{CC}$ = 4.2 to 5.5 V at $T_{opr}$ = –20 to 85°C (N version) / –40 to 85°C (D version), $f_{(XIN)}$ = 20 MHz, unless otherwise specified.

### Table 5.15 Electrical Characteristics (2) [Vcc = 5 V]
### (Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

| Symbol | Parameter | Condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| ICC | Power supply current (VCC = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are VSS | High-speed clock mode | XIN = 20 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>No division | – | 10 | 17 | mA |
| | | | XIN = 16 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>No division | – | 9 | 15 | mA |
| | | | XIN = 10 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>No division | – | 6 | – | mA |
| | | | XIN = 20 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8 | – | 5 | – | mA |
| | | | XIN = 16 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8 | – | 4 | – | mA |
| | | | XIN = 10 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8 | – | 2.5 | – | mA |
| | | High-speed on-chip oscillator mode | XIN clock off<br>High-speed on-chip oscillator on fOCO = 20 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>No division | – | 10 | 15 | mA |
| | | | XIN clock off<br>High-speed on-chip oscillator on fOCO = 20 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8 | – | 4 | – | mA |
| | | | XIN clock off<br>High-speed on-chip oscillator on fOCO = 10 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>No division | – | 5.5 | 10 | mA |
| | | | XIN clock off<br>High-speed on-chip oscillator on fOCO = 10 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8 | – | 2.5 | – | mA |
| | | Low-speed on-chip oscillator mode | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8, FMR47 = 1 | – | 130 | 300 | µA |
| | | Wait mode | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>While a WAIT instruction is executed<br>Peripheral clock operation<br>VCA27 = VCA26 = 0<br>VCA20 = 1 | – | 25 | 75 | µA |
| | | | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>While a WAIT instruction is executed<br>Peripheral clock off<br>VCA27 = VCA26 = 0<br>VCA20 = 1 | – | 23 | 60 | µA |
| | | Stop mode | XIN clock off, Topr = 25°C<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>CM10 = 1<br>Peripheral clock off<br>VCA27 = VCA26 = 0 | – | 0.8 | 3.0 | µA |
| | | | XIN clock off, Topr = 85°C<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>CM10 = 1<br>Peripheral clock off<br>VCA27 = VCA26 = 0 | – | 1.2 | – | µA |

## Timing Requirements
## (Unless Otherwise Specified: VCC = 5 V, VSS = 0 V at Topr = 25°C) [VCC = 5 V]

**Table 5.16 XIN Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(XIN)}$ | XIN input cycle time | 50 | – | ns |
| $t_{WH(XIN)}$ | XIN input “H” width | 25 | – | ns |
| $t_{WL(XIN)}$ | XIN input “L” width | 25 | – | ns |

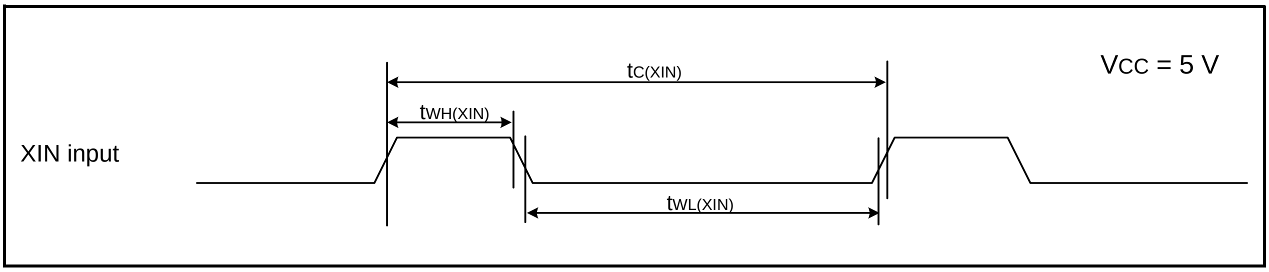


Figure 5.4 XIN Input Timing Diagram when VCC = 5 V

**Table 5.17 TRAIO Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TRAIO)}$ | TRAIO input cycle time | 100 | – | ns |
| $t_{WH(TRAIO)}$ | TRAIO input “H” width | 40 | – | ns |
| $t_{WL(TRAIO)}$ | TRAIO input “L” width | 40 | – | ns |

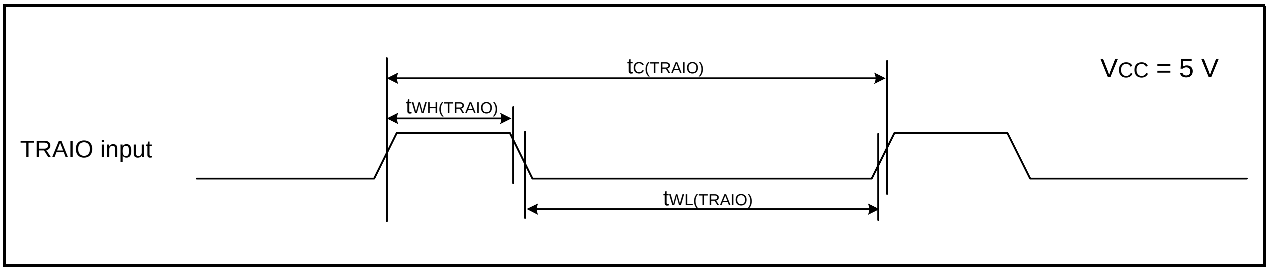


Figure 5.5 TRAIO Input Timing Diagram when VCC = 5 V

### Table 5.20 Electrical Characteristics (3) [$V_{CC}$ = 3 V]

| Symbol | Parameter | | Condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min. | Typ. | Max. | |
| $V_{OH}$ | Output “H” voltage | Except P1_0 to P1_7, XOUT | $I_{OH}$ = –1 mA | | $V_{CC}$ – 0.5 | – | $V_{CC}$ | V |
| | | P1_0 to P1_7 | Drive capacity HIGH | $I_{OH}$ = –2 mA | $V_{CC}$ – 0.5 | – | $V_{CC}$ | V |
| | | | Drive capacity LOW | $I_{OH}$ = –1 mA | $V_{CC}$ – 0.5 | – | $V_{CC}$ | V |
| | | XOUT | Drive capacity HIGH | $I_{OH}$ = –0.1 mA | $V_{CC}$ – 0.5 | – | $V_{CC}$ | V |
| | | | Drive capacity LOW | $I_{OH}$ = –50 μA | $V_{CC}$ – 0.5 | – | $V_{CC}$ | V |
| $V_{OL}$ | Output “L” voltage | Except P1_0 to P1_7, XOUT | $I_{OL}$ = 1 mA | | – | – | 0.5 | V |
| | | P1_0 to P1_7 | Drive capacity HIGH | $I_{OL}$ = 2 mA | – | – | 0.5 | V |
| | | | Drive capacity LOW | $I_{OL}$ = 1 mA | – | – | 0.5 | V |
| | | XOUT | Drive capacity HIGH | $I_{OL}$ = 0.1 mA | – | – | 0.5 | V |
| | | | Drive capacity LOW | $I_{OL}$ = 50 μA | – | – | 0.5 | V |
| $V_{T+}$-$V_{T-}$ | Hysteresis | $\overline{\text{INT0}}$, $\overline{\text{INT1}}$, $\overline{\text{INT3}}$, $\overline{\text{KI0}}$, $\overline{\text{KI1}}$, $\overline{\text{KI2}}$, $\overline{\text{KI3}}$, TRAIO, RXD0, CLK0 | | | 0.1 | 0.3 | – | V |
| | | $\overline{\text{RESET}}$ | | | 0.1 | 0.4 | – | V |
| $I_{IH}$ | Input “H” current | | VI = 3 V, $V_{CC}$ = 3 V | | – | – | 4.0 | μA |
| $I_{IL}$ | Input “L” current | | VI = 0 V, $V_{CC}$ = 3 V | | – | – | –4.0 | μA |
| $R_{PULLUP}$ | Pull-up resistance | | VI = 0 V, $V_{CC}$ = 3 V | | 66 | 160 | 500 | kΩ |
| $R_{fXIN}$ | Feedback resistance | XIN | | | – | 3.0 | – | MΩ |
| $V_{RAM}$ | RAM hold voltage | | During stop mode | | 1.8 | – | – | V |

NOTE:

1. $V_{CC}$ =2.7 to 3.3 V at $T_{opr}$ = –20 to 85°C (N version) / –40 to 85°C (D version), $f_{(XIN)}$ = 10 MHz, unless otherwise specified.

### Timing requirements
### (Unless Otherwise Specified: $V_{CC}$ = 3 V, $V_{SS}$ = 0 V at $T_{opr}$ = 25°C) [$V_{CC}$ = 3 V]

**Table 5.22 XIN Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(XIN)}$ | XIN input cycle time | 100 | – | ns |
| $t_{WH(XIN)}$ | XIN input “H” width | 40 | – | ns |
| $t_{WL(XIN)}$ | XIN input “L” width | 40 | – | ns |

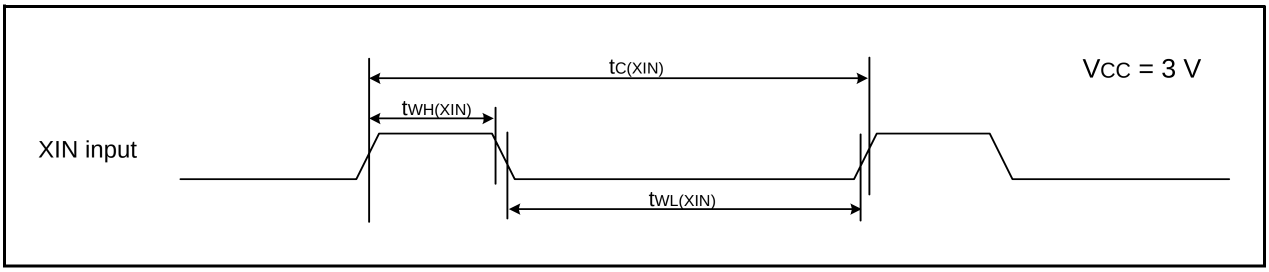


**Figure 5.8 XIN Input Timing Diagram when $V_{CC}$ = 3 V**

**Table 5.23 TRAIO Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TRAIO)}$ | TRAIO input cycle time | 300 | – | ns |
| $t_{WH(TRAIO)}$ | TRAIO input “H” width | 120 | – | ns |
| $t_{WL(TRAIO)}$ | TRAIO input “L” width | 120 | – | ns |

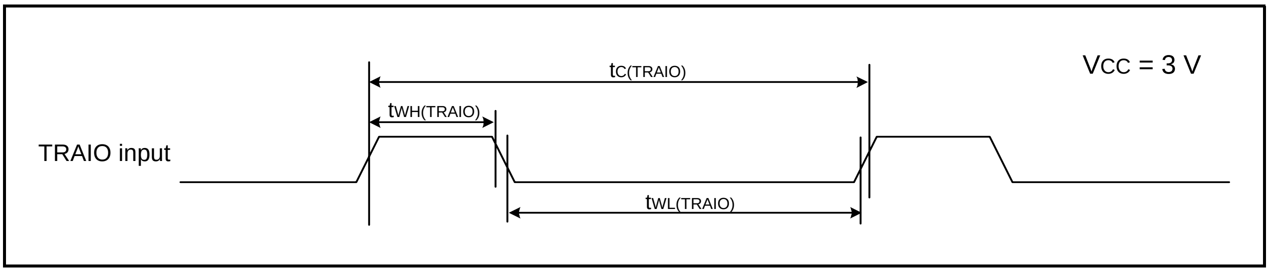


**Figure 5.9 TRAIO Input Timing Diagram when $V_{CC}$ = 3 V**

| REVISION HISTORY | R8C/2E Group, R8C/2F Group Datasheet |
|---|---|

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 0.10 | Aug 01, 2007 | – | First Edition issued |
| 1.00 | Dec 14, 2007 | All pages | “Under development” deleted |
| | | 2, 4 | Table 1.1, Table 1.3: “Interrupts” revised |
| | | 6, 7 | Table 1.5, Table 1.6: “(D)” deleted |
| | | 15, 16 | Figure 3.1, Figure 3.2: “Expanded area” deleted |
| | | 17 | Table 4.1: “002Ch” added |
| | | 24 | Table 5.2: $I_{OH(sum)}$, NOTE2 revised |
| | | 30 | Table 5.11: Symbol “fOCO40M”; Parameter added |
| | | | |