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## What is "**Embedded - Microcontrollers**"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "**Embedded - Microcontrollers**"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | R8C |
| Core Size | 16-Bit |
| Speed | 20MHz |
| Connectivity | LINbus, SIO, UART/USART |
| Peripherals | POR, PWM, Voltage Detect, WDT |
| Number of I/O | 25 |
| Program Memory Size | 16KB (16K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 1K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 5.5V |
| Data Converters | A/D 12x10b; D/A 2x8b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 32-LQFP |
| Supplier Device Package | 32-LQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f212f4dfp-u0 |

# 1. Overview

## 1.1 Features

The R8C/2E Group and R8C/2F Group of single-chip MCUs incorporates the R8C/Tiny Series CPU core, employing sophisticated instructions for a high level of efficiency. With 1 Mbyte of address space, and it is capable of executing instructions at high speed. In addition, the CPU core boasts a multiplier for high-speed operation processing.

Power consumption is low, and the supported operating modes allow additional power control. These MCUs also use an anti-noise configuration to reduce emissions of electromagnetic noise and are designed to withstand EMI.

Integration of many peripheral functions, including multifunction timer and serial interface, reduces the number of system components.

Furthermore, the R8C/2F Group has on-chip data flash (1 KB × 2 blocks).

The difference between the R8C/2E Group and R8C/2F Group is only the presence or absence of data flash. Their peripheral functions are the same.

### 1.1.1 Applications

Electronic household appliances, office equipment, audio equipment, consumer equipment, etc.

### 1.1.2    Specifications

Tables 1.1 and 1.2 outlines the Specifications for R8C/2E Group and Tables 1.3 and 1.4 outlines the Specifications for R8C/2F Group.

**Table 1.1      Specifications for R8C/2E Group (1)**

| Item | Function | Specification |
|---|---|---|
| CPU | Central processing unit | R8C/Tiny series core<br>• Number of fundamental instructions: 89<br>• Minimum instruction execution time:<br>    50 ns (f(XIN) = 20 MHz, VCC = 3.0 to 5.5 V)<br>    100 ns (f(XIN) = 10 MHz, VCC = 2.7 to 5.5 V)<br>• Multiplier: 16 bits × 16 bits → 32 bits<br>• Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits<br>• Operation mode: Single-chip mode (address space: 1 Mbyte) |
| Memory | ROM, RAM | Refer to **Table 1.5 Product List for R8C/2E Group**. |
| Power Supply Voltage Detection | Voltage detection circuit | • Power-on reset<br>• Voltage detection 2 |
| I/O Ports | Programmable I/O ports | • Input-only: 3 pins<br>• CMOS I/O ports: 25, selectable pull-up resistor<br>• High current drive ports: 8 |
| Clock | Clock generation circuits | 2 circuits: XIN clock oscillation circuit (with on-chip feedback resistor),<br>            On-chip oscillator (high-speed, low-speed)<br>            (high-speed on-chip oscillator has a frequency adjustment<br>            function)<br>• Oscillation stop detection: XIN clock oscillation stop detection<br>                function<br>• Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16<br>• Low power consumption modes:<br>   Standard operating mode (high-speed clock, high-speed on-chip<br>   oscillator, low-speed on-chip oscillator), wait mode, stop mode |
| Interrupts | | • External: 4 sources, Internal: 13 sources, Software: 4 sources<br>• Priority levels: 7 levels |
| Watchdog Timer | | 15 bits × 1 (with prescaler), reset start selectable |
| Timer | Timer RA | 8 bits × 1 (with 8-bit prescaler)<br>   Timer mode (period timer), pulse output mode (output level inverted<br>   every period), event counter mode, pulse width measurement mode,<br>   pulse period measurement mode |
| | Timer RB | 8 bits × 1 (with 8-bit prescaler)<br>   Timer mode (period timer), programmable waveform generation<br>   mode (PWM output), programmable one-shot generation mode,<br>   programmable wait one-shot generation mode |
| | Timer RC | 16 bits × 1 (with 4 capture/compare registers)<br>   Timer mode (input capture function, output compare function), PWM<br>   mode (output 3 pins), PWM2 mode (PWM output pin) |
| | Timer RE | 8 bits × 1<br>   Output compare mode |
| Serial Interface | UART0 | Clock synchronous serial I/O/UART × 1 |
| LIN Module | | Hardware LIN: 1 (timer RA, UART0) |
| A/D Converter | | 10-bit resolution × 12 channels, includes sample and hold function |
| D/A Converter | | 8-bit resolution × 2 circuits |
| Comparator | | 2 circuits |

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**Table 1.7      Pin Name Information by Pin Number**

| Pin Number | Control Pin | Port | I/O Pin Functions for of Peripheral Modules | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | Interrupt | Timer | Serial Interface | A/D Converter | D/A Converter | Comparator |
| 1 | | P3_5 | | (TRCIOD)[1] | | | | |
| 2 | | P3_7 | | TRAO | | | | |
| 3 | $\overline{\text{RESET}}$ | | | | | | | |
| 4 | XOUT | P4_7 | | | | | | |
| 5 | VSS/AVSS | | | | | | | |
| 6 | XIN | P4_6 | | | | | | |
| 7 | VCC/AVCC | | | | | | | |
| 8 | MODE | | | | | | | |
| 9 | | P4_5 | $\overline{\text{INT0}}$ | | | | | |
| 10 | | P1_7 | $\overline{\text{INT1}}$ | TRAIO | | | | |
| 11 | | P3_6 | $(\overline{\text{INT1}})$[1] | | | | | |
| 12 | | P3_1 | | TRBO | | | | |
| 13 | | P5_4 | | TRCIOD | | | | ACOUT1 |
| 14 | | P5_3 | | TRCIOC | | | | ACOUT0 |
| 15 | | P1_6 | | | CLK0 | | | |
| 16 | | P1_5 | $(\overline{\text{INT1}})$[1] | (TRAIO)[1] | RXD0 | | | |
| 17 | | P1_4 | | | TXD0 | | | |
| 18 | | P1_3 | $\overline{\text{KI3}}$ | (TRBO)[1] | | AN11 | | |
| 19 | | P1_2 | $\overline{\text{KI2}}$ | TRCIOB | | AN10 | | |
| 20 | VREF | P4_2 | | | | | | |
| 21 | | P1_1 | $\overline{\text{KI1}}$ | TRCIOA/ TRCTRG | | AN9 | | |
| 22 | | P1_0 | $\overline{\text{KI0}}$ | | | AN8 | | |
| 23 | | P3_3 | $\overline{\text{INT3}}$ | TRCCLK | | | | |
| 24 | | P3_4 | | (TRCIOC)[1] | | | | |
| 25 | | P0_7 | | | | AN0 | DA1 | |
| 26 | | P0_6 | | | | AN1 | DA0 | |
| 27 | | P0_5 | | | | AN2 | | AVREF0 |
| 28 | | P0_4 | | TREO | | AN3 | | ACMP0 |
| 29 | | P0_3 | | | | AN4 | | AVREF1 |
| 30 | | P0_2 | | | | AN5 | | ACMP1 |
| 31 | | P0_1 | | | | AN6 | | |
| 32 | | P0_0 | | | | AN7 | | |

NOTE:
  1.  Can be assigned to the pin in parentheses by a program.

## 1.5 Pin Functions

Table 1.8 list Pin Functions.

**Table 1.8      Pin Functions**

| Type | Symbol | I/O Type | Description |
|---|---|---|---|
| Power supply input | VCC, VSS | I | Apply 2.7 V to 5.5 V to the VCC pin. Apply 0 V to the VSS pin. |
| Analog power supply input | AVCC, AVSS | I | Power supply for the A/D converter. Connect a capacitor between AVCC and AVSS. |
| Reset input | $\overline{\text{RESET}}$ | I | Input "L" on this pin resets the MCU. |
| MODE | MODE | I | Connect this pin to VCC via a resistor. |
| XIN clock input | XIN | I | These pins are provided for XIN clock generation circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins.[1] To use an external clock, input it to the XIN pin and leave the XOUT pin open. |
| XIN clock output | XOUT | O | |
| $\overline{\text{INT}}$ interrupt input | $\overline{\text{INT0}}$, $\overline{\text{INT1}}$, $\overline{\text{INT3}}$ | I | $\overline{\text{INT}}$ interrupt input pins |
| Key input interrupt | $\overline{\text{KI0}}$ to $\overline{\text{KI3}}$ | I | Key input interrupt input pins |
| Timer RA | TRAO | O | Timer RA output pin |
| | TRAIO | I/O | Timer RA I/O pin |
| Timer RB | TRBO | O | Timer RB output pin |
| Timer RC | TRCCLK | I | External clock input pin |
| | TRCTRG | I | External trigger input pin |
| | TRCIOA, TRCIOB, TRCIOC, TRCIOD | I/O | Sharing output-compare output / input-capture input / PWM / PWM2 output pins |
| Timer RE | TREO | O | Timer RE output pin |
| Serial interface | CLK0 | I/O | Clock I/O pin |
| | RXD0 | I | Receive data input pin |
| | TXD0 | O | Transmit data output pin |
| Reference voltage input | VREF | I | Reference voltage input pin to A/D converter |
| A/D converter | AN0 to AN11 | I | Analog input pins to A/D converter |
| D/A converter | DA0 to DA1 | O | Output pins from D/A converter |
| Comparator | AVREF0 to AVREF1 | I | Reference voltage input pins to comparator |
| | ACMP0 to ACMP1 | I | Analog voltage input pins to comparator |
| | ACOUT0 to ACOUT1 | O | Comparison result output pins of comparator |
| I/O port | P0_0 to P0_7, P1_0 to P1_7, P3_1, P3_3 to P3_7, P4_5, P5_3, P5_4 | I/O | CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program. P1_0 to P1_7 also function as LED drive ports. |
| Input port | P4_2, P4_6, P4_7 | I | Input-only ports |

I: Input          O: Output          I/O: Input and output
NOTE:
   1.  Refer to the oscillator manufacturer for oscillation characteristics.

# 2.    Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register bank.
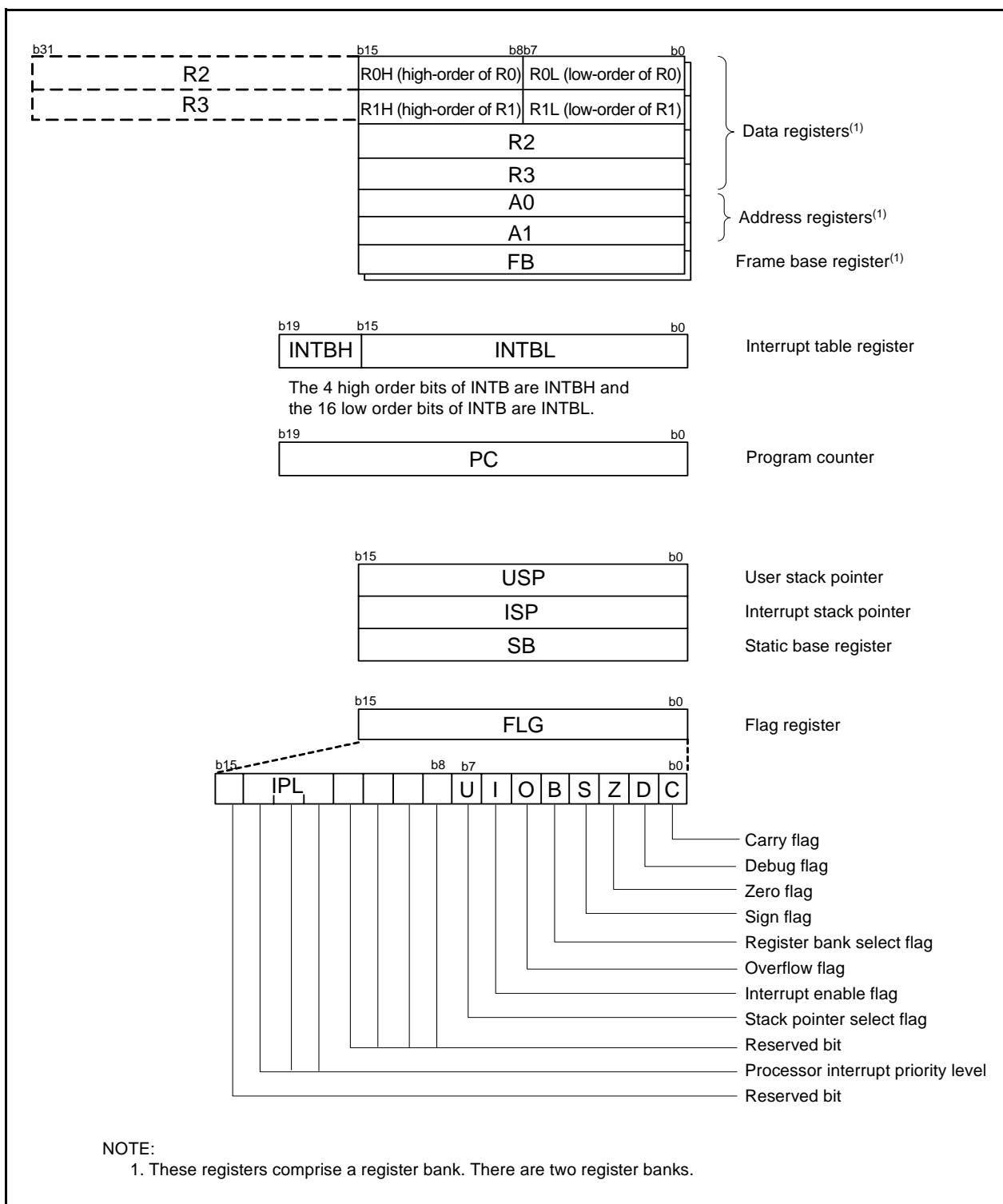


**Figure 2.1        CPU Registers**

## 2.1    Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

## 2.2    Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 to be used as a 32-bit address register (A1A0).

## 2.3    Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

## 2.4    Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the start address of an interrupt vector table.

## 2.5    Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

## 2.6    User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP, and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

## 2.7    Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

## 2.8    Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

### 2.8.1    Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

### 2.8.2    Debug Flag (D)

The D flag is for debugging only. Set it to 0.

### 2.8.3    Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

### 2.8.4    Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

### 2.8.5    Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

### 2.8.6    Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

### 2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.
Interrupt are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

### 2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.
The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

### 2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has higher priority than IPL, the interrupt is enabled.

### 2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

# 3.    Memory

## 3.1    R8C/2E Group

Figure 3.1 is a Memory Map of R8C/2E Group. The R8C/2E group has 1 Mbyte of address space from addresses 00000h to FFFFFh.

The internal ROM is allocated lower addresses, beginning with address 0FFFFFh. For example, a 16-Kbyte internal ROM area is allocated addresses 0C000h to 0FFFFFh.

The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFFh. They store the starting address of each interrupt routine.

The internal RAM is allocated higher addresses beginning with address 00400h. For example, a 1-Kbyte internal RAM area is allocated addresses 00400h to 007FFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.

Special function registers (SFRs) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated here. All addresses within the SFR, which have nothing allocated are reserved for future use and cannot be accessed by users.



**Figure 3.1      Memory Map of R8C/2E Group**

NOTE:
    1. The blank regions are reserved. Do not access locations in these regions.

| Part Number | Internal ROM | | Internal RAM | |
|---|---|---|---|---|
| | Size | Address 0YYYYh | Size | Address 0XXXXh |
| R5F212E2NFP, R5F212E2DFP, R5F212E2NXXXFP, R5F212E2DXXXFP | 8 Kbytes | 0E000h | 512 bytes | 005FFh |
| R5F212E4NFP, R5F212E4DFP, R5F212E4NXXXFP, R5F212E4DXXXFP | 16 Kbytes | 0C000h | 1 Kbyte | 007FFh |

## 3.2    R8C/2F Group

Figure 3.2 is a Memory Map of R8C/2F Group. The R8C/2F group has 1 Mbyte of address space from addresses 00000h to FFFFFh.

The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 16-Kbyte internal ROM area is allocated addresses 0C000h to 0FFFFh.

The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.

The internal ROM (data flash) is allocated addresses 02400h to 02BFFh.

The internal RAM area is allocated higher addresses, beginning with address 00400h. For example, a 1-Kbyte internal RAM is allocated addresses 00400h to 007FFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.

Special function registers (SFRs) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated here. All addresses within the SFR, which have nothing allocated are reserved for future use and cannot be accessed by users.
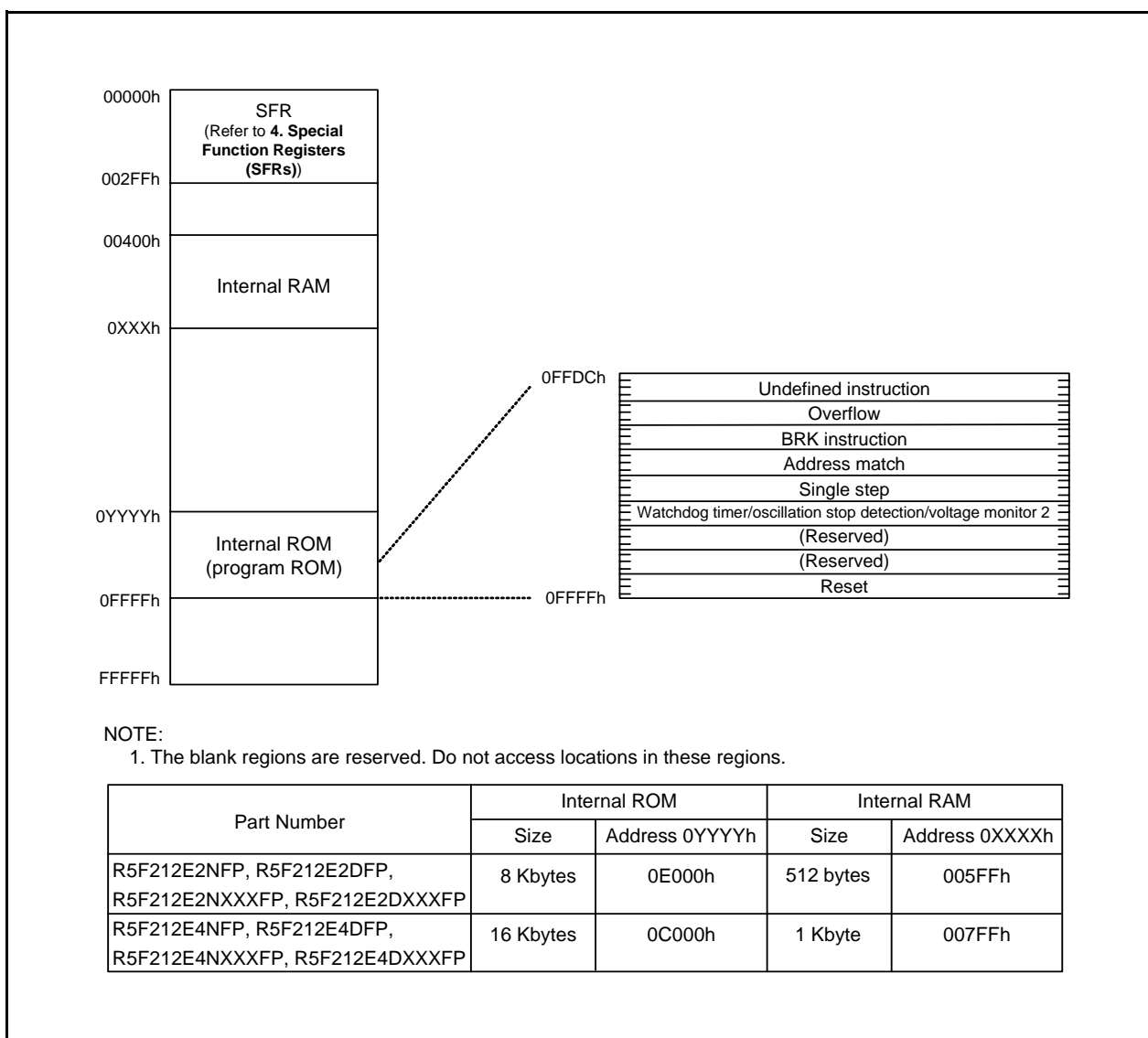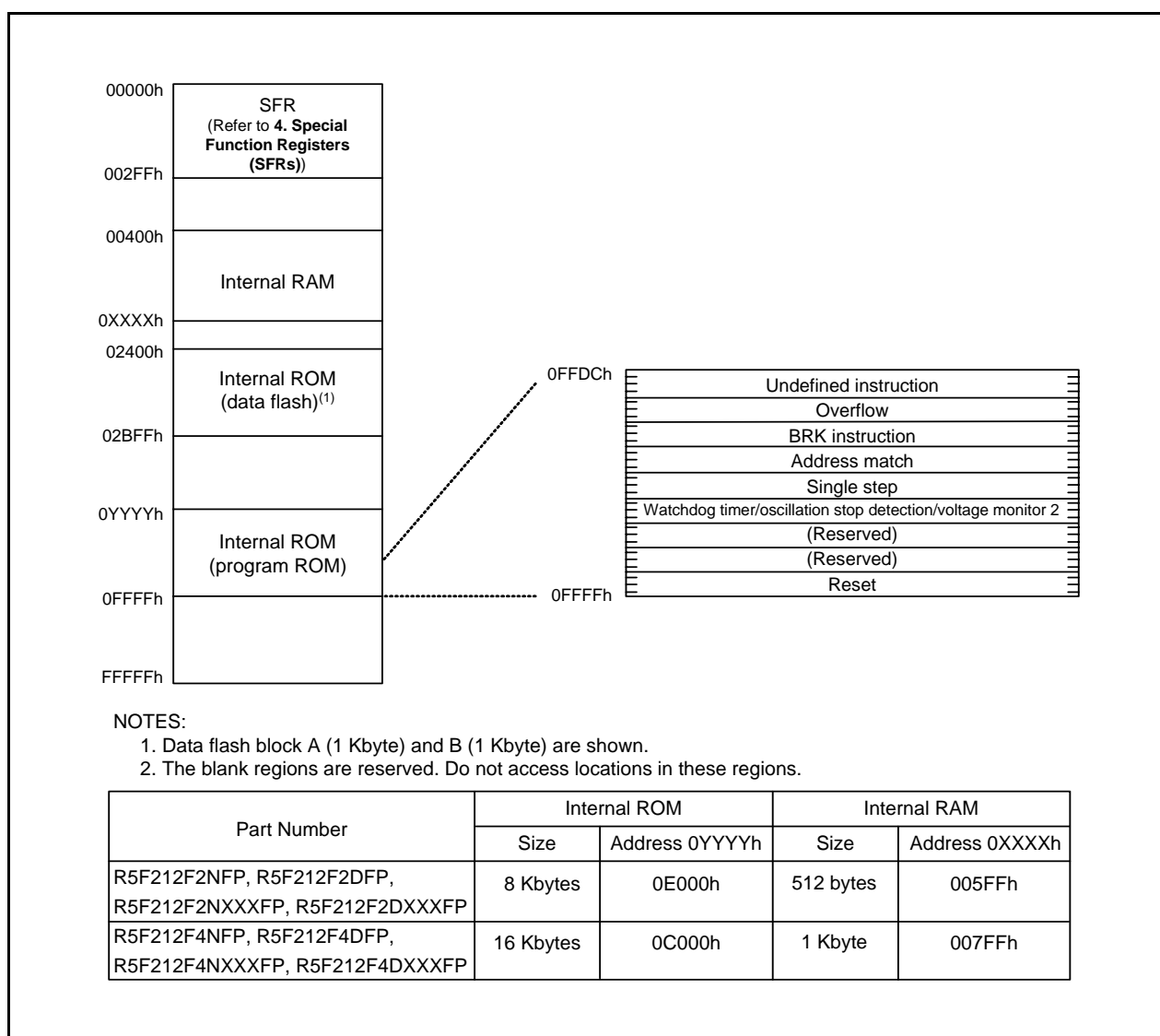


NOTES:
1. Data flash block A (1 Kbyte) and B (1 Kbyte) are shown.
2. The blank regions are reserved. Do not access locations in these regions.

| Part Number | Internal ROM | | Internal RAM | |
| --- | --- | --- | --- | --- |
| | Size | Address 0YYYYh | Size | Address 0XXXXh |
| R5F212F2NFP, R5F212F2DFP, R5F212F2NXXXFP, R5F212F2DXXXFP | 8 Kbytes | 0E000h | 512 bytes | 005FFh |
| R5F212F4NFP, R5F212F4DFP, R5F212F4NXXXFP, R5F212F4DXXXFP | 16 Kbytes | 0C000h | 1 Kbyte | 007FFh |

**Figure 3.2      Memory Map of R8C/2F Group**

**Table 4.2     SFR Information (2)[1]**

| Address | Register | Symbol | After reset |
|---|---|---|---|
| 0040h | | | |
| 0041h | | | |
| 0042h | | | |
| 0043h | | | |
| 0044h | | | |
| 0045h | | | |
| 0046h | | | |
| 0047h | Timer RC Interrupt Control Register | TRCIC | XXXXX000b |
| 0048h | | | |
| 0049h | | | |
| 004Ah | Timer RE Interrupt Control Register | TREIC | XXXXX000b |
| 004Bh | | | |
| 004Ch | | | |
| 004Dh | Key Input Interrupt Control Register | KUPIC | XXXXX000b |
| 004Eh | A/D Conversion Interrupt Control Register | ADIC | XXXXX000b |
| 004Fh | | | |
| 0050h | | | |
| 0051h | UART0 Transmit Interrupt Control Register | S0TIC | XXXXX000b |
| 0052h | UART0 Receive Interrupt Control Register | S0RIC | XXXXX000b |
| 0053h | | | |
| 0054h | | | |
| 0055h | | | |
| 0056h | Timer RA Interrupt Control Register | TRAIC | XXXXX000b |
| 0057h | | | |
| 0058h | Timer RB Interrupt Control Register | TRBIC | XXXXX000b |
| 0059h | INT1 Interrupt Control Register | INT1IC | XX00X000b |
| 005Ah | INT3 Interrupt Control Register | INT3IC | XX00X000b |
| 005Bh | Comparator 0 Interrupt Control Register | CM0IC | XXXXX000b |
| 005Ch | Comparator 1 Interrupt Control Register | CM1IC | XXXXX000b |
| 005Dh | INT0 Interrupt Control Register | INT0IC | XX00X000b |
| 005Eh | | | |
| 005Fh | | | |
| 0060h | | | |
| 0061h | | | |
| 0062h | | | |
| 0063h | | | |
| 0064h | | | |
| 0065h | | | |
| 0066h | | | |
| 0067h | | | |
| 0068h | | | |
| 0069h | | | |
| 006Ah | | | |
| 006Bh | | | |
| 006Ch | | | |
| 006Dh | | | |
| 006Eh | | | |
| 006Fh | | | |
| 0070h | | | |
| 0071h | | | |
| 0072h | | | |
| 0073h | | | |
| 0074h | | | |
| 0075h | | | |
| 0076h | | | |
| 0077h | | | |
| 0078h | | | |
| 0079h | | | |
| 007Ah | | | |
| 007Bh | | | |
| 007Ch | | | |
| 007Dh | | | |
| 007Eh | | | |
| 007Fh | | | |

X: Undefined
NOTE:
1.   The blank regions are reserved. Do not access locations in these regions.

**Table 4.3　　　SFR Information (3)[1]**

| Address | Register | Symbol | After reset |
|---|---|---|---|
| 0080h | | | |
| 0081h | | | |
| 0082h | | | |
| 0083h | | | |
| 0084h | | | |
| 0085h | | | |
| 0086h | | | |
| 0087h | | | |
| 0088h | | | |
| 0089h | | | |
| 008Ah | | | |
| 008Bh | | | |
| 008Ch | | | |
| 008Dh | | | |
| 008Eh | | | |
| 008Fh | | | |
| 0090h | | | |
| 0091h | | | |
| 0092h | | | |
| 0093h | | | |
| 0094h | | | |
| 0095h | | | |
| 0096h | | | |
| 0097h | | | |
| 0098h | | | |
| 0099h | | | |
| 009Ah | | | |
| 009Bh | | | |
| 009Ch | | | |
| 009Dh | | | |
| 009Eh | | | |
| 009Fh | | | |
| 00A0h | UART0 Transmit/Receive Mode Register | U0MR | 00h |
| 00A1h | UART0 Bit Rate Register | U0BRG | XXh |
| 00A2h | UART0 Transmit Buffer Register | U0TB | XXh |
| 00A3h | | | XXh |
| 00A4h | UART0 Transmit/Receive Control Register 0 | U0C0 | 00001000b |
| 00A5h | UART0 Transmit/Receive Control Register 1 | U0C1 | 00000010b |
| 00A6h | UART0 Receive Buffer Register | U0RB | XXh |
| 00A7h | | | XXh |
| 00A8h | | | |
| 00A9h | | | |
| 00AAh | | | |
| 00ABh | | | |
| 00ACh | | | |
| 00ADh | | | |
| 00AEh | | | |
| 00AFh | | | |
| 00B0h | | | |
| 00B1h | | | |
| 00B2h | | | |
| 00B3h | | | |
| 00B4h | | | |
| 00B5h | | | |
| 00B6h | | | |
| 00B7h | | | |
| 00B8h | | | |
| 00B9h | | | |
| 00BAh | | | |
| 00BBh | | | |
| 00BCh | | | |
| 00BDh | | | |
| 00BEh | | | |
| 00BFh | | | |

X: Undefined
NOTE:
1.　The blank regions are reserved. Do not access locations in these regions.

**Table 4.5      SFR Information (5)[1]**

| Address | Register | Symbol | After reset |
|---------|----------|--------|-------------|
| 0100h | Timer RA Control Register | TRACR | 00h |
| 0101h | Timer RA I/O Control Register | TRAIOC | 00h |
| 0102h | Timer RA Mode Register | TRAMR | 00h |
| 0103h | Timer RA Prescaler Register | TRAPRE | FFh |
| 0104h | Timer RA Register | TRA | FFh |
| 0105h | | | |
| 0106h | LIN Control Register | LINCR | 00h |
| 0107h | LIN Status Register | LINST | 00h |
| 0108h | Timer RB Control Register | TRBCR | 00h |
| 0109h | Timer RB One-Shot Control Register | TRBOCR | 00h |
| 010Ah | Timer RB I/O Control Register | TRBIOC | 00h |
| 010Bh | Timer RB Mode Register | TRBMR | 00h |
| 010Ch | Timer RB Prescaler Register | TRBPRE | FFh |
| 010Dh | Timer RB Secondary Register | TRBSC | FFh |
| 010Eh | Timer RB Primary Register | TRBPR | FFh |
| 010Fh | | | |
| 0110h | | | |
| 0111h | | | |
| 0112h | | | |
| 0113h | | | |
| 0114h | | | |
| 0115h | | | |
| 0116h | | | |
| 0117h | | | |
| 0118h | Timer RE Counter Data Register | TRESEC | 00h |
| 0119h | Timer RE Compare Data Register | TREMIN | 00h |
| 011Ah | | | |
| 011Bh | | | |
| 011Ch | Timer RE Control Register 1 | TRECR1 | 00h |
| 011Dh | Timer RE Control Register 2 | TRECR2 | 00h |
| 011Eh | Timer RE Clock Source Select Register | TRECSR | 00001000b |
| 011Fh | | | |
| 0120h | Timer RC Mode Register | TRCMR | 01001000b |
| 0121h | Timer RC Control Register 1 | TRCCR1 | 00h |
| 0122h | Timer RC Interrupt Enable Register | TRCIER | 01110000b |
| 0123h | Timer RC Status Register | TRCSR | 01110000b |
| 0124h | Timer RC I/O Control Register 0 | TRCIOR0 | 10001000b |
| 0125h | Timer RC I/O Control Register 1 | TRCIOR1 | 10001000b |
| 0126h | Timer RC Counter | TRC | 00h |
| 0127h | | | 00h |
| 0128h | Timer RC General Register A | TRCGRA | FFh |
| 0129h | | | FFh |
| 012Ah | Timer RC General Register B | TRCGRB | FFh |
| 012Bh | | | FFh |
| 012Ch | Timer RC General Register C | TRCGRC | FFh |
| 012Dh | | | FFh |
| 012Eh | Timer RC General Register D | TRCGRD | FFh |
| 012Fh | | | FFh |
| 0130h | Timer RC Control Register 2 | TRCCR2 | 00011111b |
| 0131h | Timer RC Digital Filter Function Select Register | TRCDF | 00h |
| 0132h | Timer RC Output Master Enable Register | TRCOER | 01111111b |
| 0133h | | | |
| 0134h | | | |
| 0135h | | | |
| 0136h | | | |
| 0137h | | | |
| 0138h | | | |
| 0139h | | | |
| 013Ah | | | |
| 013Bh | | | |
| 013Ch | | | |
| 013Dh | | | |
| 013Eh | | | |
| 013Fh | | | |

X: Undefined
NOTE:
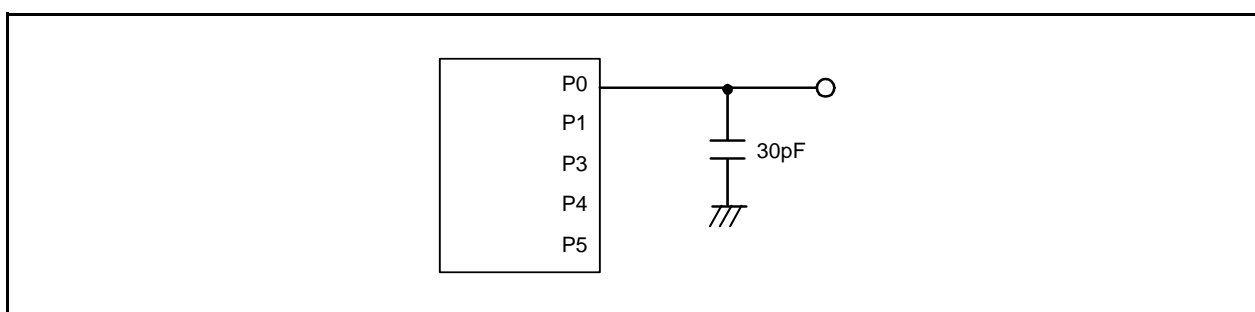  1.  The blank regions are reserved. Do not access locations in these regions.

**Figure 5.1    Ports P0, P1, and P3 to P5 Timing Measurement Circuit**

**Table 5.3    A/D Converter Characteristics**

| Symbol | Parameter | | Conditions | Standard | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| – | Resolution | | $V_{ref}$ = AVCC | – | – | 10 | Bits |
| – | Absolute accuracy | 10-bit mode | $\phi$AD = 10 MHz, $V_{ref}$ = AVCC = 5.0 V | – | – | ±3 | LSB |
| | | 8-bit mode | $\phi$AD = 10 MHz, $V_{ref}$ = AVCC = 5.0 V | – | – | ±2 | LSB |
| | | 10-bit mode | $\phi$AD = 10 MHz, $V_{ref}$ = AVCC = 3.3 V | – | – | ±5 | LSB |
| | | 8-bit mode | $\phi$AD = 10 MHz, $V_{ref}$ = AVCC = 3.3 V | – | – | ±2 | LSB |
| $R_{ladder}$ | Resistor ladder | | $V_{ref}$ = AVCC | 10 | – | 40 | k$\Omega$ |
| $t_{conv}$ | Conversion time | 10-bit mode | $\phi$AD = 10 MHz, $V_{ref}$ = AVCC = 5.0 V | 3.3 | – | – | $\mu$s |
| | | 8-bit mode | $\phi$AD = 10 MHz, $V_{ref}$ = AVCC = 5.0 V | 2.8 | – | – | $\mu$s |
| $V_{ref}$ | Reference voltage | | | 2.7 | – | AVCC | V |
| $V_{IA}$ | Analog input voltage[2] | | | 0 | – | AVCC | V |
| – | A/D operating clock frequency | Without sample and hold | $V_{ref}$ = AVCC = 2.7 to 5.5 V | 0.25 | – | 10 | MHz |
| | | With sample and hold | $V_{ref}$ = AVCC = 2.7 to 5.5 V | 1 | – | 10 | MHz |

NOTES:
1.  AVCC = 2.7 to 5.5 V at $T_{opr}$ = −20 to 85°C (N version) / −40 to 85°C (D version), unless otherwise specified.
2.  When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

**Table 5.4    D/A Converter Characteristics**

| Symbol | Parameter | Conditions | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| – | Resolution | | – | – | 8 | Bit |
| – | Absolute accuracy | | – | – | 1.0 | % |
| $t_{su}$ | Setup time | | – | – | 3 | $\mu$s |
| $R_O$ | Output resistor | | 4 | 10 | 20 | k$\Omega$ |
| $I_{Vref}$ | Reference power input current | (NOTE 2) | – | – | 1.5 | mA |

NOTES:
1.  AVCC = 2.7 to 5.5 V at $T_{opr}$ = −20 to 85°C (N version) / −40 to 85°C (D version), unless otherwise specified.
2.  This applies when one D/A converter is used and the value of the DAi register (i = 0 or 1) for the unused D/A converter is 00h. The resistor ladder of the A/D converter is not included. Also, even if the VCUT bit in the ADCON1 register is set to 0 (VREF not connected), $I_{Vref}$ flows into the D/A converters.

**Table 5.5 Comparator Characteristics[1]**

| Symbol | Parameter | Conditions | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| Vcref | Comparator reference voltage | | 0 | – | Vcc−1.2 | V |
| Vcin | Comparator input voltage | | −0.3 | – | Vcc+0.3 | V |
| Vofs | Input offset voltage | | – | – | ±100 | mV |
| Tcrsp | Response time | | – | – | 200 | ns |

NOTE:
1. Vcc = 2.7 to 5.5 V at Topr = −20 to 85°C (N version) / −40 to 85°C (D version), unless otherwise specified.

**Table 5.6 Flash Memory (Program ROM) Electrical Characteristics**

| Symbol | Parameter | Conditions | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| – | Program/erase endurance[2] | R8C/2E Group | 100[3] | – | – | times |
| | | R8C/2F Group | 1,000[3] | – | – | times |
| – | Byte program time | | – | 50 | 400 | μs |
| – | Block erase time | | – | 0.4 | 9 | s |
| td(SR-SUS) | Time delay from suspend request until suspend | | – | – | 97+CPU clock × 6 cycles | μs |
| – | Interval from erase start/restart until following suspend request | | 650 | – | – | μs |
| – | Interval from program start/restart until following suspend request | | 0 | – | – | ns |
| – | Time from suspend until program/erase restart | | – | – | 3+CPU clock × 4 cycles | μs |
| – | Program, erase voltage | | 2.7 | – | 5.5 | V |
| – | Read voltage | | 2.7 | – | 5.5 | V |
| – | Program, erase temperature | | 0 | – | 60 | °C |
| – | Data hold time[7] | Ambient temperature = 55°C | 20 | – | – | year |

NOTES:
1. Vcc = 2.7 to 5.5 V at Topr = 0 to 60°C, unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 100 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
   However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erase count of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

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**Table 5.11    High-speed On-Chip Oscillator Circuit Electrical Characteristics**

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| fOCO40M | High-speed on-chip oscillator frequency temperature • supply voltage dependence | $V_{CC}$ = 4.75 V to 5.25 V $0°C \leq T_{opr} \leq 60°C$[2] | 39.2 | 40 | 40.8 | MHz |
| | | $V_{CC}$ = 3.0 V to 5.5 V $-20°C \leq T_{opr} \leq 85°C$[2] | 38.8 | 40 | 41.2 | MHz |
| | | $V_{CC}$ = 3.0 V to 5.5 V $-40°C \leq T_{opr} \leq 85°C$[2] | 38.4 | 40 | 41.6 | MHz |
| | | $V_{CC}$ = 2.7 V to 5.5 V $-20°C \leq T_{opr} \leq 85°C$[2] | 38 | 40 | 42 | MHz |
| | | $V_{CC}$ = 2.7 V to 5.5 V $-40°C \leq T_{opr} \leq 85°C$[2] | 37.6 | 40 | 42.4 | MHz |
| | | $V_{CC}$ = 5.0 V ±10% $-20°C \leq T_{opr} \leq 85°C$[2] | 38.8 | 40 | 40.8 | MHz |
| | | $V_{CC}$ = 5.0 V ±10% $-40°C \leq T_{opr} \leq 85°C$[2] | 38.4 | 40 | 40.8 | MHz |
| | High-speed on-chip oscillator frequency when correction value in FRA7 register is written to FRA1 register | $V_{CC}$ = 5.0 V, $T_{opr}$ = 25°C | – | 36.864 | – | MHz |
| | | $V_{CC}$ = 2.7 V to 5.5 V $-20°C \leq T_{opr} \leq 85°C$ | –3% | – | 3% | % |
| – | Value in FRA1 register after reset | | 08h | – | F7h | – |
| – | Oscillation frequency adjustment unit of high-speed on-chip oscillator | Adjust FRA1 register (value after reset) to –1 | – | +0.3 | – | MHz |
| – | Oscillation stability time | | – | 10 | 100 | μs |
| – | Self power consumption at oscillation | $V_{CC}$ = 5.0 V, $T_{opr}$ = 25°C | – | 400 | – | μA |

NOTES:
1. $V_{CC}$ = 2.7 to 5.5 V, $T_{opr}$ = −20 to 85°C (N version) / −40 to 85°C (D version), unless otherwise specified.
2. These standard values show when the FRA1 register value after reset is assumed.

**Table 5.12    Low-speed On-Chip Oscillator Circuit Electrical Characteristics**

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| fOCO-S | Low-speed on-chip oscillator frequency | | 30 | 125 | 250 | kHz |
| – | Oscillation stability time | | – | 10 | 100 | μs |
| – | Self power consumption at oscillation | $V_{CC}$ = 5.0 V, $T_{opr}$ = 25°C | – | 15 | – | μA |

NOTE:
1. $V_{CC}$ = 2.7 to 5.5 V, $T_{opr}$ = −20 to 85°C (N version) / −40 to 85°C (D version), unless otherwise specified.

**Table 5.13    Power Supply Circuit Timing Characteristics**

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| td(P-R) | Time for internal power supply stabilization during power-on[2] | | 1 | – | 2000 | μs |
| td(R-S) | STOP exit time[3] | | – | – | 150 | μs |

NOTES:
1. The measurement condition is $V_{CC}$ = 2.7 to 5.5 V and $T_{opr}$ = 25°C.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.
3. Time until system clock supply starts after the interrupt is acknowledged to exit stop mode.

**Table 5.15    Electrical Characteristics (2) [Vcc = 5 V]**
**(T$_{opr}$ = −20 to 85°C (N version) / −40 to 85°C (D version), unless otherwise specified.)**

| Symbol | Parameter | Condition | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Icc | Power supply current (Vcc = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are Vss | High-speed clock mode | XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division | − | 10 | 17 | mA |
| | | | XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division | − | 9 | 15 | mA |
| | | | XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division | − | 6 | − | mA |
| | | | XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8 | − | 5 | − | mA |
| | | | XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8 | − | 4 | − | mA |
| | | | XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8 | − | 2.5 | − | mA |
| | | High-speed on-chip oscillator mode | XIN clock off High-speed on-chip oscillator on fOCO = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division | − | 10 | 15 | mA |
| | | | XIN clock off High-speed on-chip oscillator on fOCO = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8 | − | 4 | − | mA |
| | | | XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division | − | 5.5 | 10 | mA |
| | | | XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8 | − | 2.5 | − | mA |
| | | Low-speed on-chip oscillator mode | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1 | − | 130 | 300 | μA |
| | | Wait mode | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = 0 VCA20 = 1 | − | 25 | 75 | μA |
| | | | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = 0 VCA20 = 1 | − | 23 | 60 | μA |
| | | Stop mode | XIN clock off, T$_{opr}$ = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = 0 | − | 0.8 | 3.0 | μA |
| | | | XIN clock off, T$_{opr}$ = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = 0 | − | 1.2 | − | μA |

**Timing Requirements**
**(Unless Otherwise Specified: $V_{CC}$ = 5 V, $V_{SS}$ = 0 V at $T_{opr}$ = 25°C) [$V_{CC}$ = 5 V]**

**Table 5.16      XIN Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(XIN)}$ | XIN input cycle time | 50 | – | ns |
| $t_{WH(XIN)}$ | XIN input "H" width | 25 | – | ns |
| $t_{WL(XIN)}$ | XIN input "L" width | 25 | – | ns |
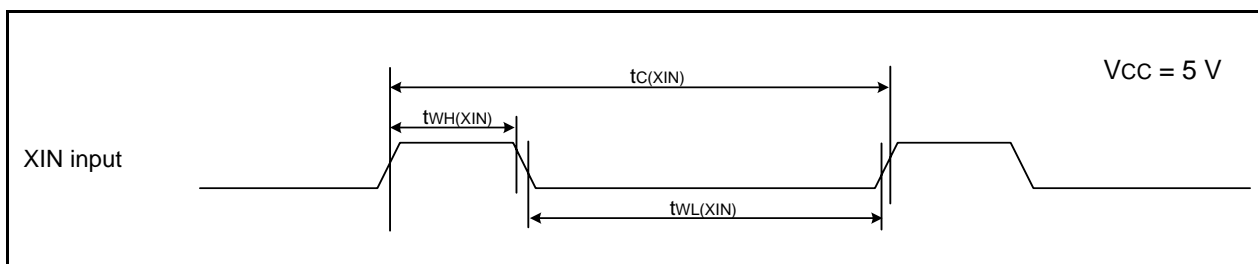


**Figure 5.4      XIN Input Timing Diagram when $V_{CC}$ = 5 V**

**Table 5.17      TRAIO Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TRAIO)}$ | TRAIO input cycle time | 100 | – | ns |
| $t_{WH(TRAIO)}$ | TRAIO input "H" width | 40 | – | ns |
| $t_{WL(TRAIO)}$ | TRAIO input "L" width | 40 | – | ns |
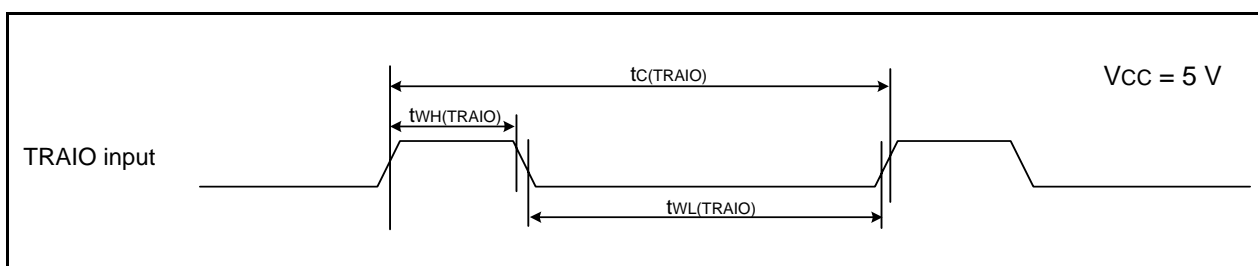


**Figure 5.5      TRAIO Input Timing Diagram when $V_{CC}$ = 5 V**

**Table 5.18     Serial Interface**

| Symbol | Parameter | Standard Min. | Standard Max. | Unit |
|--------|-----------|:---:|:---:|:---:|
| $t_{C(CK)}$ | CLK0 input cycle time | 200 | – | ns |
| $t_{W(CKH)}$ | CLK0 input "H" width | 100 | – | ns |
| $t_{W(CKL)}$ | CLK0 input "L" width | 100 | – | ns |
| $t_{d(C-Q)}$ | TXD0 output delay time | – | 50 | ns |
| $t_{h(C-Q)}$ | TXD0 hold time | 0 | – | ns |
| $t_{su(D-C)}$ | RXD0 input setup time | 50 | – | ns |
| $t_{h(C-D)}$ | RXD0 input hold time | 90 | – | ns |
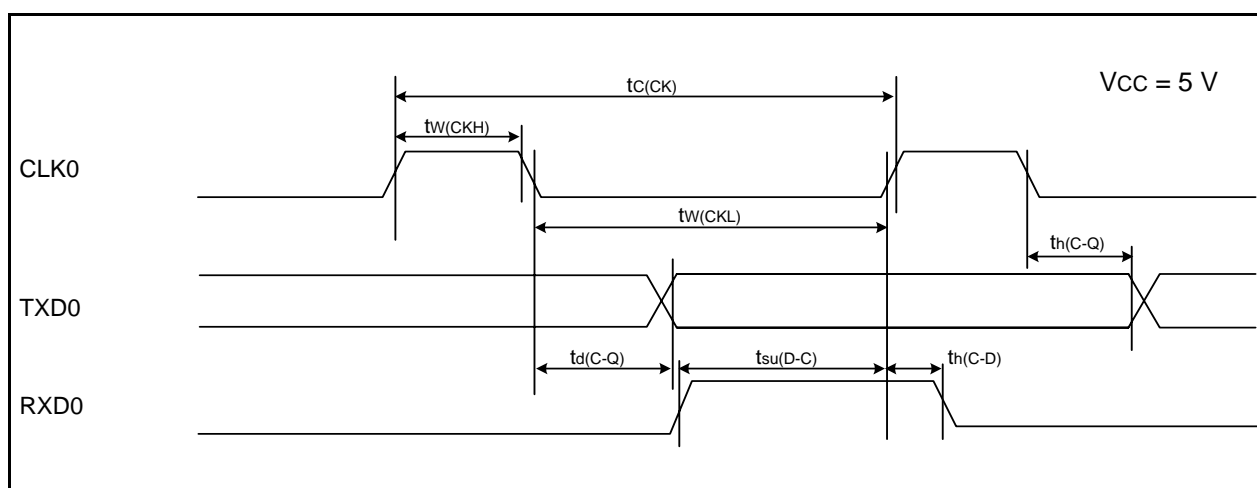


**Figure 5.6     Serial Interface Timing Diagram when $V_{CC}$ = 5 V**

**Table 5.19     External Interrupt $\overline{INTi}$ (i = 0, 1, 3) Input**

| Symbol | Parameter | Standard Min. | Standard Max. | Unit |
|--------|-----------|:---:|:---:|:---:|
| $t_{W(INH)}$ | $\overline{INTi}$ input "H" width | 250[1] | – | ns |
| $t_{W(INL)}$ | $\overline{INTi}$ input "L" width | 250[2] | – | ns |

NOTES:
1.  When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2.  When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
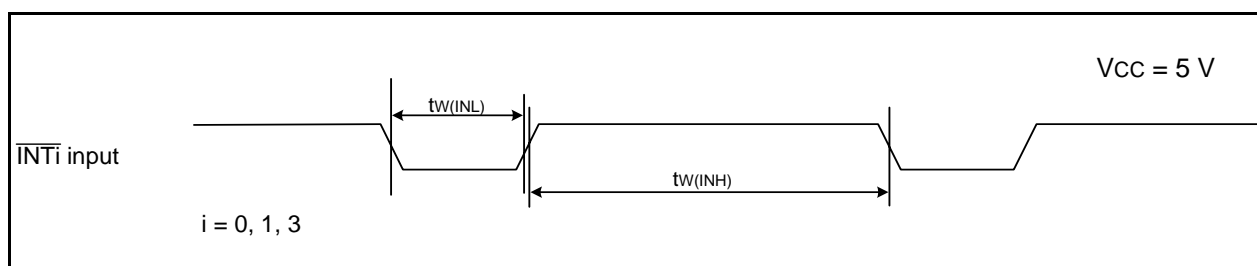


**Figure 5.7     External Interrupt $\overline{INTi}$ Input Timing Diagram when $V_{CC}$ = 5 V**

**Table 5.20     Electrical Characteristics (3) [V$_{CC}$ = 3 V]**

| Symbol | Parameter | | Condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min. | Typ. | Max. | |
| V$_{OH}$ | Output "H" voltage | Except P1_0 to P1_7, XOUT | I$_{OH}$ = −1 mA | | V$_{CC}$ − 0.5 | − | V$_{CC}$ | V |
| | | P1_0 to P1_7 | Drive capacity HIGH | I$_{OH}$ = −2 mA | V$_{CC}$ − 0.5 | − | V$_{CC}$ | V |
| | | | Drive capacity LOW | I$_{OH}$ = −1 mA | V$_{CC}$ − 0.5 | − | V$_{CC}$ | V |
| | | XOUT | Drive capacity HIGH | I$_{OH}$ = −0.1 mA | V$_{CC}$ − 0.5 | − | V$_{CC}$ | V |
| | | | Drive capacity LOW | I$_{OH}$ = −50 μA | V$_{CC}$ − 0.5 | − | V$_{CC}$ | V |
| V$_{OL}$ | Output "L" voltage | Except P1_0 to P1_7, XOUT | I$_{OL}$ = 1 mA | | − | − | 0.5 | V |
| | | P1_0 to P1_7 | Drive capacity HIGH | I$_{OL}$ = 2 mA | − | − | 0.5 | V |
| | | | Drive capacity LOW | I$_{OL}$ = 1 mA | − | − | 0.5 | V |
| | | XOUT | Drive capacity HIGH | I$_{OL}$ = 0.1 mA | − | − | 0.5 | V |
| | | | Drive capacity LOW | I$_{OL}$ = 50 μA | − | − | 0.5 | V |
| V$_{T+}$-V$_{T-}$ | Hysteresis | $\overline{INT0}$, $\overline{INT1}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRAIO, RXD0, CLK0 | | | 0.1 | 0.3 | − | V |
| | | $\overline{RESET}$ | | | 0.1 | 0.4 | − | V |
| I$_{IH}$ | Input "H" current | | VI = 3 V, V$_{CC}$ = 3 V | | − | − | 4.0 | μA |
| I$_{IL}$ | Input "L" current | | VI = 0 V, V$_{CC}$ = 3 V | | − | − | −4.0 | μA |
| R$_{PULLUP}$ | Pull-up resistance | | VI = 0 V, V$_{CC}$ = 3 V | | 66 | 160 | 500 | kΩ |
| R$_{fXIN}$ | Feedback resistance | XIN | | | − | 3.0 | − | MΩ |
| V$_{RAM}$ | RAM hold voltage | | During stop mode | | 1.8 | − | − | V |

NOTE:
1.  V$_{CC}$ =2.7 to 3.3 V at T$_{opr}$ = −20 to 85°C (N version) / −40 to 85°C (D version), f$_{(XIN)}$ = 10 MHz, unless otherwise specified.

**Table 5.21    Electrical Characteristics (4) [Vcc = 3 V]**
**(T$_{opr}$ = −20 to 85°C (N version) / −40 to 85°C (D version), unless otherwise specified.)**

| Symbol | Parameter | Condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| Icc | Power supply current (Vcc = 2.7 to 3.3 V) Single-chip mode, output pins are open, other pins are Vss | High-speed clock mode | XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division | − | 6 | − | mA |
| | | | XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8 | − | 2 | − | mA |
| | | High-speed on-chip oscillator mode | XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division | − | 5 | 9 | mA |
| | | | XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8 | − | 2 | − | mA |
| | | Low-speed on-chip oscillator mode | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1 | − | 130 | 300 | μA |
| | | Wait mode | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = 0 VCA20 = 1 | − | 25 | 70 | μA |
| | | | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = 0 VCA20 = 1 | − | 23 | 55 | μA |
| | | Stop mode | XIN clock off, T$_{opr}$ = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = 0 | − | 0.7 | 3.0 | μA |
| | | | XIN clock off, T$_{opr}$ = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = 0 | − | 1.1 | − | μA |