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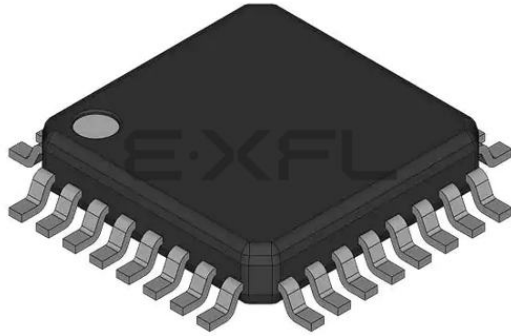
What is "**Embedded - Microcontrollers**"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "**Embedded - Microcontrollers**"

Details	
Product Status	Active
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	LINbus, SIO, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	25
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f212f4dfp-w4

Table 1.3   Specifications for R8C/2F Group (1)

Item	Function	Specification

CPU	Central processing unit	R8C/Tiny series core
		• Number of fundamental instructions: 89
		• Minimum instruction execution time:
		    50 ns (f(XIN) = 20 MHz, VCC = 3.0 to 5.5 V)
		    100 ns (f(XIN) = 10 MHz, VCC = 2.7 to 5.5 V)
		• Multiplier: 16 bits × 16 bits → 32 bits
		• Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits
		• Operation mode: Single-chip mode (address space: 1 Mbyte)

Memory	ROM, RAM	Refer to **Table 1.6 Product List for R8C/2F Group**.
Power Supply Voltage Detection	Voltage detection circuit	• Power-on reset • Voltage detection 2
I/O Ports	Programmable I/O ports	• Input-only: 3 pins • CMOS I/O ports: 25, selectable pull-up resistor • High current drive ports: 8

Clock	Clock generation circuits	2 circuits: XIN clock oscillation circuit (with on-chip feedback resistor),
		                On-chip oscillator (high-speed, low-speed)
		                (high-speed on-chip oscillator has a frequency adjustment
		                function)
		• Oscillation stop detection: XIN clock oscillation stop detection
		                function
		• Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16
		• Low power consumption modes:
		    Standard operating mode (high-speed clock, high-speed on-chip
		    oscillator, low-speed on-chip oscillator), wait mode, stop mode

Interrupts		• External: 4 sources, Internal: 13 sources, Software: 4 sources • Priority levels: 7 levels
Watchdog Timer		15 bits × 1 (with prescaler), reset start selectable

Timer	Timer RA	8 bits × 1 (with 8-bit prescaler)
		    Timer mode (period timer), pulse output mode (output level inverted
		    every period), event counter mode, pulse width measurement mode,
		    pulse period measurement mode

	Timer RB	8 bits × 1 (with 8-bit prescaler)
		    Timer mode (period timer), programmable waveform generation
		    mode (PWM output), programmable one-shot generation mode,
		    programmable wait one-shot generation mode

	Timer RC	16 bits × 1 (with 4 capture/compare registers)
		    Timer mode (input capture function, output compare function), PWM
		    mode (output 3 pins), PWM2 mode (PWM output pin)

	Timer RE	8 bits × 1 Output compare mode
Serial Interface	UART0	Clock synchronous serial I/O/UART × 1
LIN Module		Hardware LIN: 1 (timer RA, UART0)
A/D Converter		10-bit resolution × 12 channels, includes sample and hold function
D/A Converter		8-bit resolution × 2 circuits
Comparator		2 circuits

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1.3　　Block Diagram

Figure 1.3 shows a Block Diagram.
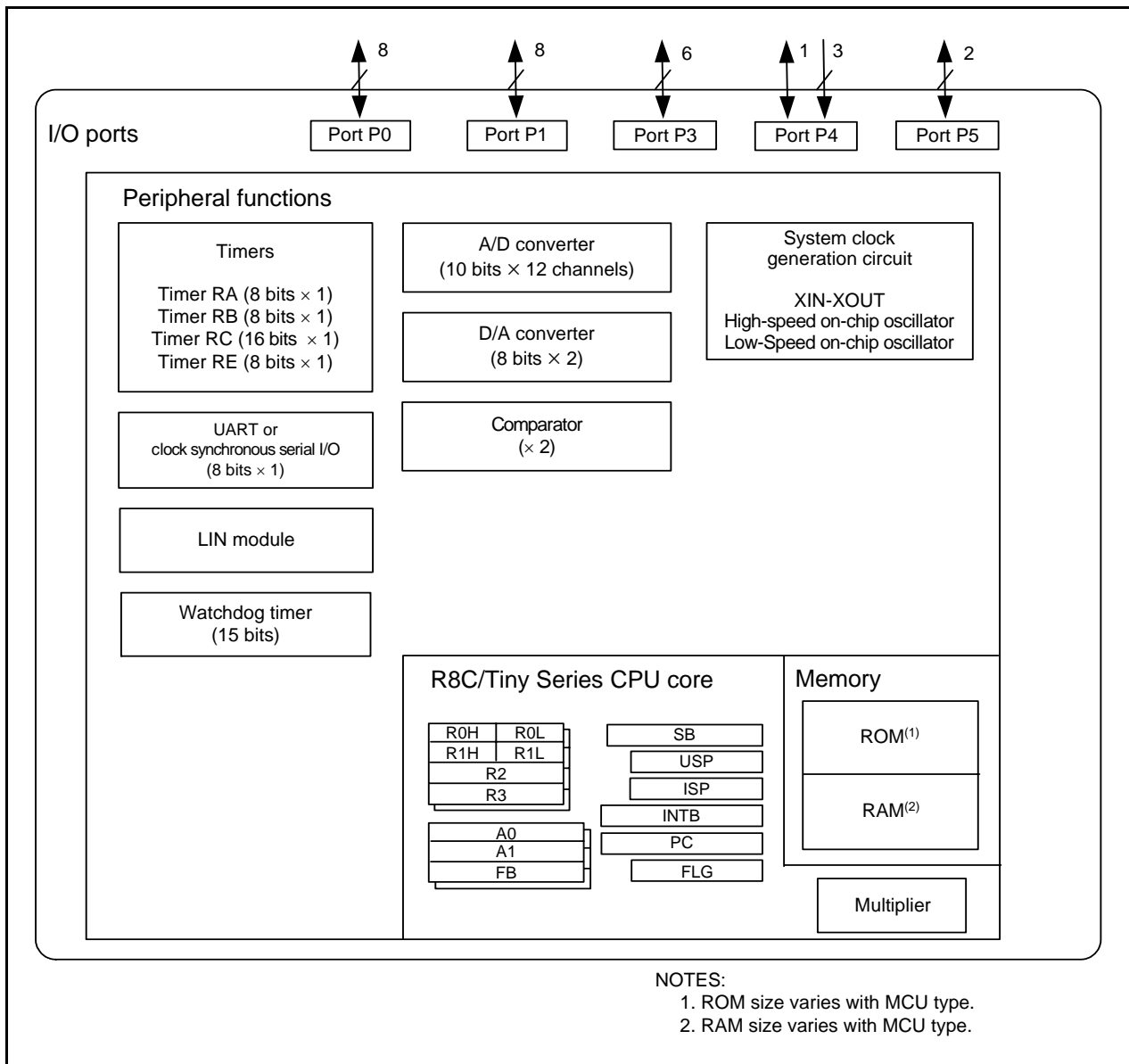
Figure 1.3　　Block Diagram

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1.4   Pin Assignment

Figure 1.4 shows Pin Assignments (Top View). Table 1.7 outlines the Pin Name Information by Pin Number.
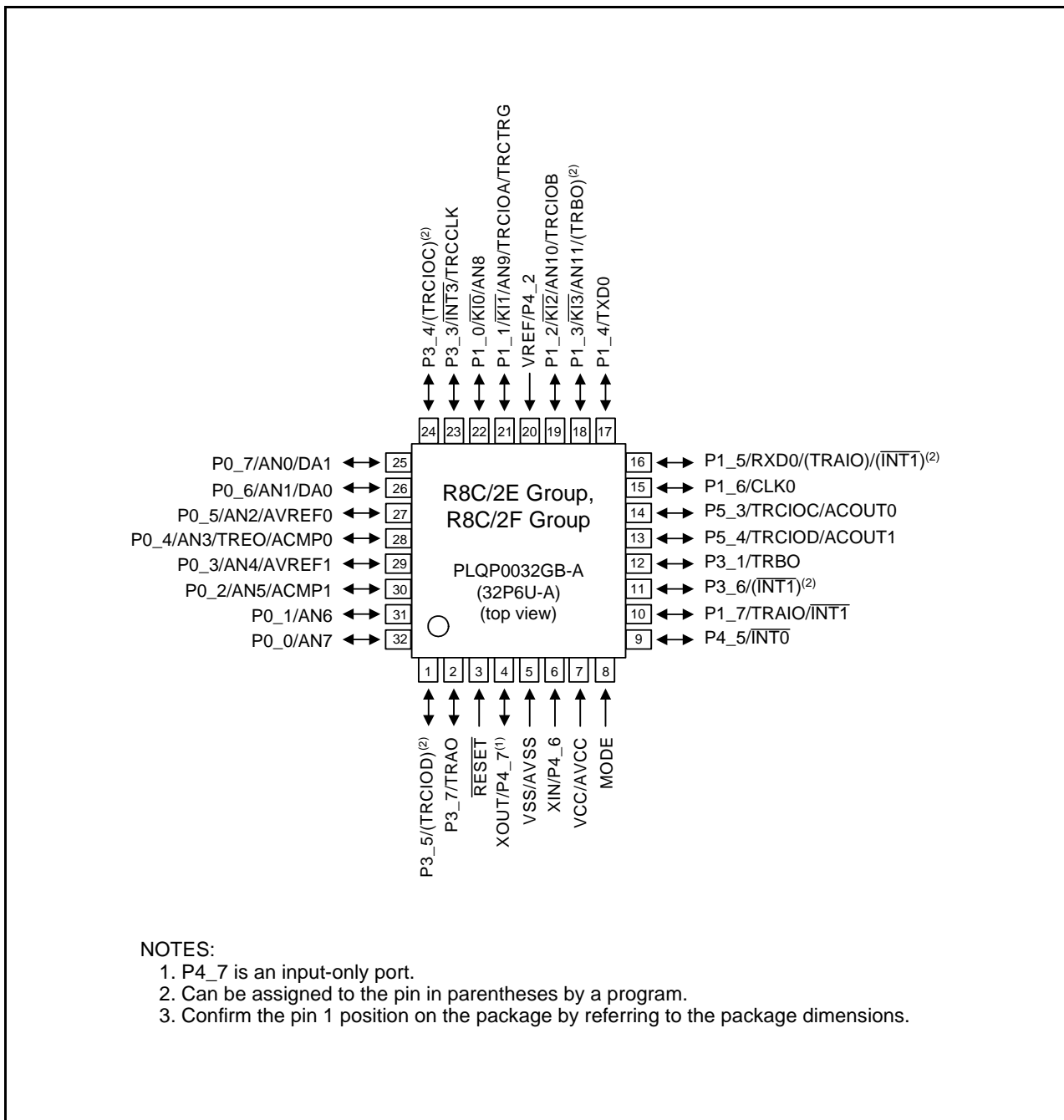
Figure 1.4   Pin Assignments (Top View)

NOTES:
1. P4_7 is an input-only port.
2. Can be assigned to the pin in parentheses by a program.
3. Confirm the pin 1 position on the package by referring to the package dimensions.

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Table 1.7   Pin Name Information by Pin Number

Pin Number	Control Pin	Port	I/O Pin Functions for of Peripheral Modules					
			Interrupt	Timer	Serial Interface	A/D Converter	D/A Converter	Comparator
1		P3_5		(TRCIOD)[1]				
2		P3_7		TRAO				
3	$\overline{\text{RESET}}$							
4	XOUT	P4_7						
5	VSS/AVSS							
6	XIN	P4_6						
7	VCC/AVCC							
8	MODE							
9		P4_5	$\overline{\text{INT0}}$					
10		P1_7	$\overline{\text{INT1}}$	TRAIO				
11		P3_6	$(\overline{\text{INT1}})$[1]					
12		P3_1		TRBO				
13		P5_4		TRCIOD				ACOUT1
14		P5_3		TRCIOC				ACOUT0
15		P1_6			CLK0			
16		P1_5	$(\overline{\text{INT1}})$[1]	(TRAIO)[1]	RXD0			
17		P1_4			TXD0			
18		P1_3	$\overline{\text{KI3}}$	(TRBO)[1]		AN11		
19		P1_2	$\overline{\text{KI2}}$	TRCIOB		AN10		
20	VREF	P4_2						
21		P1_1	$\overline{\text{KI1}}$	TRCIOA/ TRCTRG		AN9		
22		P1_0	$\overline{\text{KI0}}$			AN8		
23		P3_3	$\overline{\text{INT3}}$	TRCCLK				
24		P3_4		(TRCIOC)[1]				
25		P0_7				AN0	DA1	
26		P0_6				AN1	DA0	
27		P0_5				AN2		AVREF0
28		P0_4		TREO		AN3		ACMP0
29		P0_3				AN4		AVREF1
30		P0_2				AN5		ACMP1
31		P0_1				AN6		
32		P0_0				AN7		

NOTE:
1. Can be assigned to the pin in parentheses by a program.

1.5   Pin Functions

Table 1.8 list Pin Functions.

Table 1.8   Pin Functions

Type	Symbol	I/O Type	Description
Power supply input	VCC, VSS	I	Apply 2.7 V to 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Analog power supply input	AVCC, AVSS	I	Power supply for the A/D converter. Connect a capacitor between AVCC and AVSS.
Reset input	$\overline{\text{RESET}}$	I	Input "L" on this pin resets the MCU.
MODE	MODE	I	Connect this pin to VCC via a resistor.
XIN clock input	XIN	I	These pins are provided for XIN clock generation circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins.[1] To use an external clock, input it to the XIN pin and leave the XOUT pin open.
XIN clock output	XOUT	O	
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$, $\overline{\text{INT1}}$, $\overline{\text{INT3}}$	I	$\overline{\text{INT}}$ interrupt input pins
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Key input interrupt input pins
Timer RA	TRAO	O	Timer RA output pin
	TRAIO	I/O	Timer RA I/O pin
Timer RB	TRBO	O	Timer RB output pin
Timer RC	TRCCLK	I	External clock input pin
	TRCTRG	I	External trigger input pin
	TRCIOA, TRCIOB, TRCIOC, TRCIOD	I/O	Sharing output-compare output / input-capture input / PWM / PWM2 output pins
Timer RE	TREO	O	Timer RE output pin
Serial interface	CLK0	I/O	Clock I/O pin
	RXD0	I	Receive data input pin
	TXD0	O	Transmit data output pin
Reference voltage input	VREF	I	Reference voltage input pin to A/D converter
A/D converter	AN0 to AN11	I	Analog input pins to A/D converter
D/A converter	DA0 to DA1	O	Output pins from D/A converter
Comparator	AVREF0 to AVREF1	I	Reference voltage input pins to comparator
	ACMP0 to ACMP1	I	Analog voltage input pins to comparator
	ACOUT0 to ACOUT1	O	Comparison result output pins of comparator
I/O port	P0_0 to P0_7, P1_0 to P1_7, P3_1, P3_3 to P3_7, P4_5, P5_3, P5_4	I/O	CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program. P1_0 to P1_7 also function as LED drive ports.
Input port	P4_2, P4_6, P4_7	I	Input-only ports

I: Input   O: Output   I/O: Input and output
NOTE:
1. Refer to the oscillator manufacturer for oscillation characteristics.

2.   Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register bank.
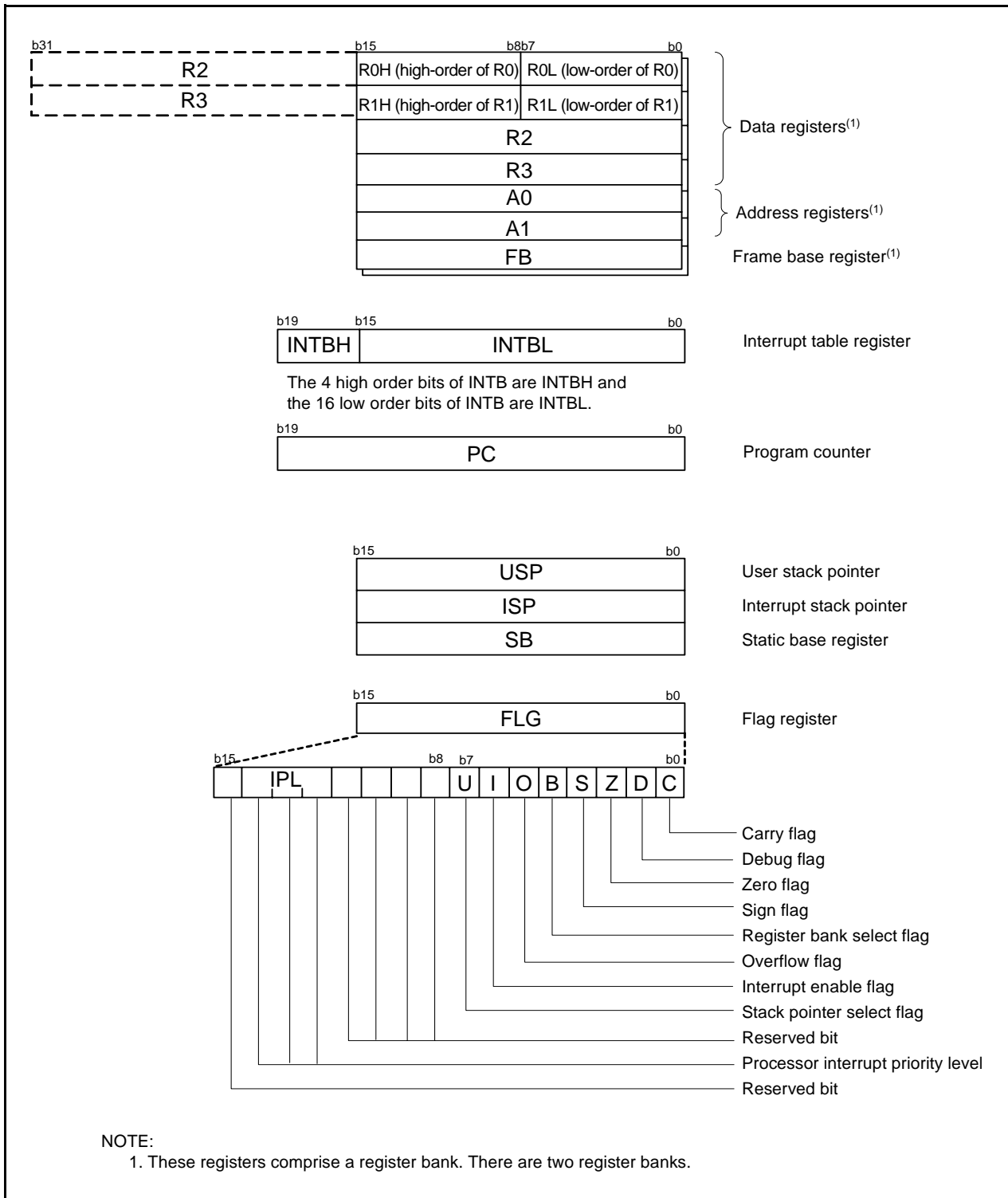
Figure 2.1   CPU Registers

2.8.7   Interrupt Enable Flag (I)

The I flag enables maskable interrupts.
Interrupt are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8   Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.
The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9   Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has higher priority than IPL, the interrupt is enabled.

2.8.10   Reserved Bit

If necessary, set to 0. When read, the content is undefined.

Table 4.3   SFR Information (3)[1]

Address	Register	Symbol	After reset
0080h			
0081h			
0082h			
0083h			
0084h			
0085h			
0086h			
0087h			
0088h			
0089h			
008Ah			
008Bh			
008Ch			
008Dh			
008Eh			
008Fh			
0090h			
0091h			
0092h			
0093h			
0094h			
0095h			
0096h			
0097h			
0098h			
0099h			
009Ah			
009Bh			
009Ch			
009Dh			
009Eh			
009Fh			
00A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h			XXh
00A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00A5h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00A6h	UART0 Receive Buffer Register	U0RB	XXh
00A7h			XXh
00A8h			
00A9h			
00AAh			
00ABh			
00ACh			
00ADh			
00AEh			
00AFh			
00B0h			
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h			
00B9h			
00BAh			
00BBh			
00BCh			
00BDh			
00BEh			
00BFh			

X: Undefined
NOTE:
   1.   The blank regions are reserved. Do not access locations in these regions.

Table 4.4   SFR Information (4)[1]

Address	Register	Symbol	After reset
00C0h	A/D Register	AD	XXh
00C1h			XXh
00C2h			
00C3h			
00C4h			
00C5h			
00C6h			
00C7h			
00C8h			
00C9h			
00CAh			
00CBh			
00CCh			
00CDh			
00CEh			
00CFh			
00D0h			
00D1h			
00D2h			
00D3h			
00D4h	A/D Control Register 2	ADCON2	00h
00D5h			
00D6h	A/D Control Register 0	ADCON0	00h
00D7h	A/D Control Register 1	ADCON1	00h
00D8h	D/A Register 0	DA0	00h
00D9h			
00DAh	D/A Register 1	DA1	00h
00DBh			
00DCh	D/A Control Register	DACON	00h
00DDh			
00DEh			
00DFh			
00E0h	Port P0 Register	P0	00h
00E1h	Port P1 Register	P1	00h
00E2h	Port P0 Direction Register	PD0	00h
00E3h	Port P1 Direction Register	PD1	00h
00E4h			
00E5h	Port P3 Register	P3	00h
00E6h			
00E7h	Port P3 Direction Register	PD3	00h
00E8h	Port P4 Register	P4	00h
00E9h	Port P5 Register	P5	00h
00EAh	Port P4 Direction Register	PD4	00h
00EBh	Port P5 Direction Register	PD5	00h
00ECh			
00EDh			
00EEh			
00EFh			
00F0h			
00F1h			
00F2h			
00F3h			
00F4h			
00F5h			
00F6h	Pin Select Register 2	PINSR2	00h
00F7h	Pin Select Register 3	PINSR3	00h
00F8h	Port Mode Register	PMR	00h
00F9h	External Input Enable Register	INTEN	00h
00FAh	INT Input Filter Select Register	INTF	00h
00FBh	Key Input Enable Register	KIEN	00h
00FCh	Pull-Up Control Register 0	PUR0	00h
00FDh	Pull-Up Control Register 1	PUR1	00h
00FEh	Port P1 Drive Capacity Control Register	P1DRR	00h
00FFh			

X: Undefined
NOTE:
1.   The blank regions are reserved. Do not access locations in these regions.

Table 4.5   SFR Information (5)[1]

Address	Register	Symbol	After reset
0100h	Timer RA Control Register	TRACR	00h
0101h	Timer RA I/O Control Register	TRAIOC	00h
0102h	Timer RA Mode Register	TRAMR	00h
0103h	Timer RA Prescaler Register	TRAPRE	FFh
0104h	Timer RA Register	TRA	FFh
0105h			
0106h	LIN Control Register	LINCR	00h
0107h	LIN Status Register	LINST	00h
0108h	Timer RB Control Register	TRBCR	00h
0109h	Timer RB One-Shot Control Register	TRBOCR	00h
010Ah	Timer RB I/O Control Register	TRBIOC	00h
010Bh	Timer RB Mode Register	TRBMR	00h
010Ch	Timer RB Prescaler Register	TRBPRE	FFh
010Dh	Timer RB Secondary Register	TRBSC	FFh
010Eh	Timer RB Primary Register	TRBPR	FFh
010Fh			
0110h			
0111h			
0112h			
0113h			
0114h			
0115h			
0116h			
0117h			
0118h	Timer RE Counter Data Register	TRESEC	00h
0119h	Timer RE Compare Data Register	TREMIN	00h
011Ah			
011Bh			
011Ch	Timer RE Control Register 1	TRECR1	00h
011Dh	Timer RE Control Register 2	TRECR2	00h
011Eh	Timer RE Clock Source Select Register	TRECSR	00001000b
011Fh			
0120h	Timer RC Mode Register	TRCMR	01001000b
0121h	Timer RC Control Register 1	TRCCR1	00h
0122h	Timer RC Interrupt Enable Register	TRCIER	01110000b
0123h	Timer RC Status Register	TRCSR	01110000b
0124h	Timer RC I/O Control Register 0	TRCIOR0	10001000b
0125h	Timer RC I/O Control Register 1	TRCIOR1	10001000b
0126h	Timer RC Counter	TRC	00h
0127h			00h
0128h	Timer RC General Register A	TRCGRA	FFh
0129h			FFh
012Ah	Timer RC General Register B	TRCGRB	FFh
012Bh			FFh
012Ch	Timer RC General Register C	TRCGRC	FFh
012Dh			FFh
012Eh	Timer RC General Register D	TRCGRD	FFh
012Fh			FFh
0130h	Timer RC Control Register 2	TRCCR2	00011111b
0131h	Timer RC Digital Filter Function Select Register	TRCDF	00h
0132h	Timer RC Output Master Enable Register	TRCOER	01111111b
0133h			
0134h			
0135h			
0136h			
0137h			
0138h			
0139h			
013Ah			
013Bh			
013Ch			
013Dh			
013Eh			
013Fh			

X: Undefined
NOTE:
1.   The blank regions are reserved. Do not access locations in these regions.

Table 5.7   Flash Memory (Data flash Block A, Block B) Electrical Characteristics[4]

| Symbol	Parameter	Conditions	Standard Min.	Standard Typ.	Standard Max.	Unit
–	Program/erase endurance[2]		10,000[3]	–	–	times
–	Byte program time (program/erase endurance ≤ 1,000 times)		–	50	400	μs
–	Byte program time (program/erase endurance > 1,000 times)		–	65	–	μs
–	Block erase time (program/erase endurance ≤ 1,000 times)		–	0.2	9	s
–	Block erase time (program/erase endurance > 1,000 times)		–	0.3	–	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		–	–	97+CPU clock × 6 cycles	μs
–	Interval from erase start/restart until following suspend request		650	–	–	μs
–	Interval from program start/restart until following suspend request		0	–	–	ns
–	Time from suspend until program/erase restart		–	–	3+CPU clock × 4 cycles	μs
–	Program, erase voltage		2.7	–	5.5	V
–	Read voltage		2.7	–	5.5	V
–	Program, erase temperature		−20[8]	–	85	°C
–	Data hold time[9]	Ambient temperature = 55 °C	20	–	–	year

NOTES:
1. V_{CC} = 2.7 to 5.5 V at T_{opr} = −20 to 85°C (N version) / −40 to 85°C (D version), unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 100 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
   However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. Standard of block A and block B when program and erase endurance exceeds 1,000 times. Byte program time to 1,000 times is the same as that in program ROM.
5. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erase count of each block and limit the number of erase operations to a certain number.
6. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
7. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
8. −40°C for D version.
9. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.10 Power-on Reset Circuit, Voltage Monitor 0 Reset Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{por1}	Power-on reset valid voltage[3]		–	–	0.1	V
V_{por2}	Power-on reset valid voltage		0	–	2.6	V
t_{rth}	External power V_{CC} rise gradient[2]		20	–	–	mV/msec

NOTES:
1. The measurement condition is T_{opr} = −20 to 85°C (N version) / −40 to 85°C (D version), unless otherwise specified.
2. This condition (external power V_{CC} rise gradient) does not apply if $V_{CC} \geq 1.0$ V.
3. $t_{w(por1)}$ indicates the duration the external power V_{CC} must be held below the effective voltage (V_{por1}) to enable a power on reset. When turning on the power for the first time, maintain $t_{w(por1)}$ for 30 s or more if −20°C $\leq T_{opr} \leq$ 85°C, maintain $t_{w(por1)}$ for 3,000 s or more if −40°C $\leq T_{opr} <$ −20°C.
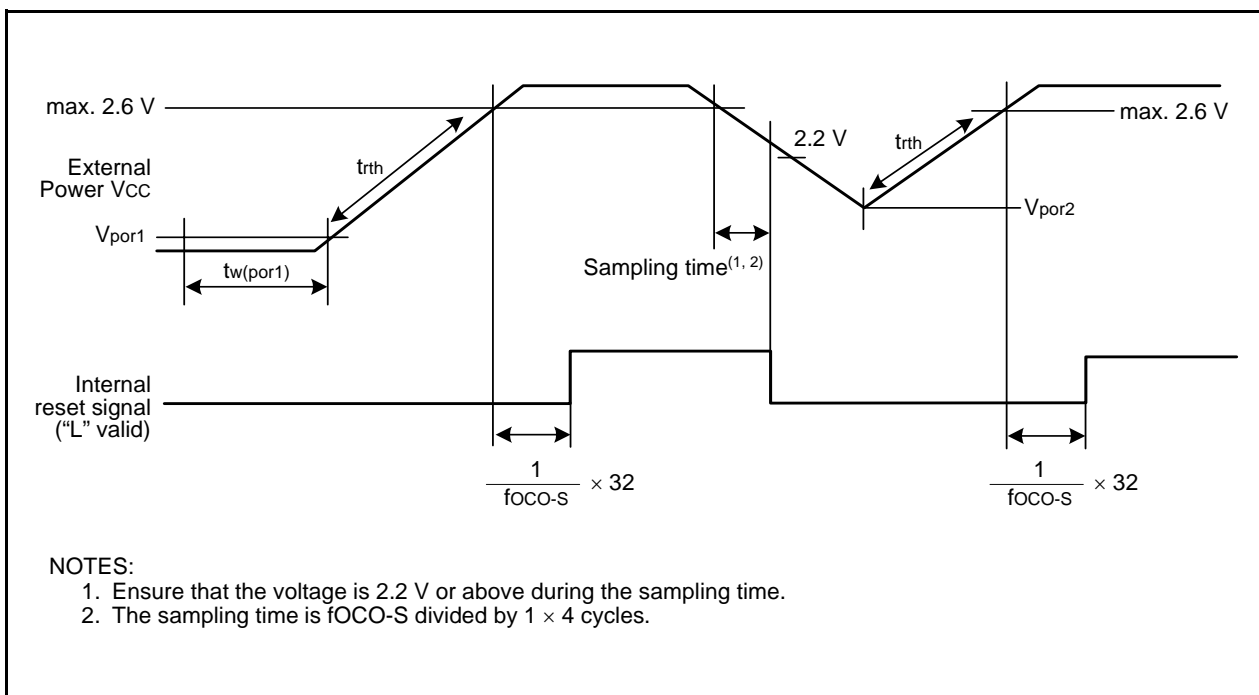
Figure 5.3   Reset Circuit Electrical Characteristics

Timing Requirements
(Unless Otherwise Specified: V_{CC} = 5 V, V_{SS} = 0 V at T_{opr} = 25°C) [V_{CC} = 5 V]

Table 5.16   XIN Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{C(XIN)}$	XIN input cycle time	50	–	ns
$t_{WH(XIN)}$	XIN input "H" width	25	–	ns
$t_{WL(XIN)}$	XIN input "L" width	25	–	ns
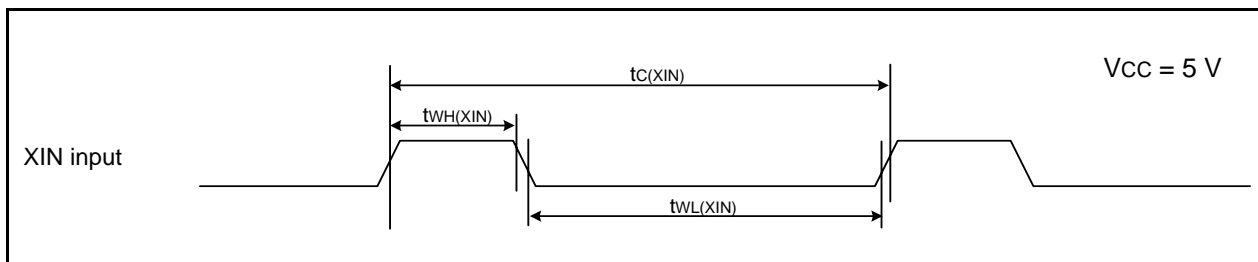
Figure 5.4   XIN Input Timing Diagram when V_{CC} = 5 V

Table 5.17   TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{C(TRAIO)}$	TRAIO input cycle time	100	–	ns
$t_{WH(TRAIO)}$	TRAIO input "H" width	40	–	ns
$t_{WL(TRAIO)}$	TRAIO input "L" width	40	–	ns
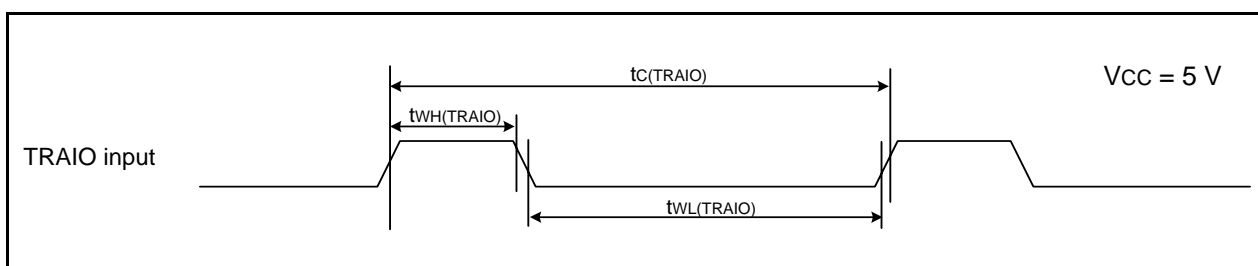
Figure 5.5   TRAIO Input Timing Diagram when V_{CC} = 5 V

Table 5.20   Electrical Characteristics (3) [Vcc = 3 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
Voh	Output "H" voltage	Except P1_0 to P1_7, XOUT	Ioh = −1 mA		Vcc − 0.5	–	Vcc	V
		P1_0 to P1_7	Drive capacity HIGH	Ioh = −2 mA	Vcc − 0.5	–	Vcc	V
			Drive capacity LOW	Ioh = −1 mA	Vcc − 0.5	–	Vcc	V
		XOUT	Drive capacity HIGH	Ioh = −0.1 mA	Vcc − 0.5	–	Vcc	V
			Drive capacity LOW	Ioh = −50 μA	Vcc − 0.5	–	Vcc	V
Vol	Output "L" voltage	Except P1_0 to P1_7, XOUT	Iol = 1 mA		–	–	0.5	V
		P1_0 to P1_7	Drive capacity HIGH	Iol = 2 mA	–	–	0.5	V
			Drive capacity LOW	Iol = 1 mA	–	–	0.5	V
		XOUT	Drive capacity HIGH	Iol = 0.1 mA	–	–	0.5	V
			Drive capacity LOW	Iol = 50 μA	–	–	0.5	V
Vt+-Vt-	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRAIO, RXD0, CLK0			0.1	0.3	–	V
		$\overline{RESET}$			0.1	0.4	–	V
Iih	Input "H" current		VI = 3 V, Vcc = 3 V		–	–	4.0	μA
Iil	Input "L" current		VI = 0 V, Vcc = 3 V		–	–	−4.0	μA
Rpullup	Pull-up resistance		VI = 0 V, Vcc = 3 V		66	160	500	kΩ
RfXIN	Feedback resistance	XIN			–	3.0	–	MΩ
Vram	RAM hold voltage		During stop mode		1.8	–	–	V

NOTE:
1. Vcc =2.7 to 3.3 V at Topr = −20 to 85°C (N version) / −40 to 85°C (D version), f(XIN) = 10 MHz, unless otherwise specified.

Table 5.21   Electrical Characteristics (4) [Vcc = 3 V]
(T$_{opr}$ = −20 to 85°C (N version) / −40 to 85°C (D version), unless otherwise specified.)
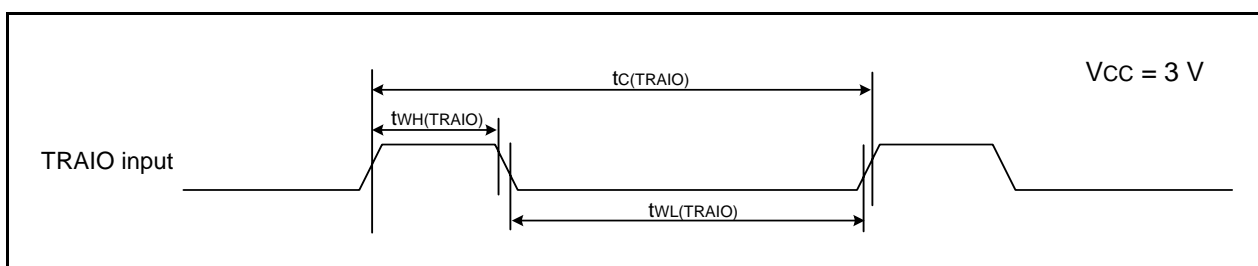
Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 2.7 to 3.3 V) Single-chip mode, output pins are open, other pins are Vss	High-speed clock mode	XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	−	6	−	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	−	2	−	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division	−	5	9	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	−	2	−	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1	−	130	300	µA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = 0 VCA20 = 1	−	25	70	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = 0 VCA20 = 1	−	23	55	µA
		Stop mode	XIN clock off, T$_{opr}$ = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = 0	−	0.7	3.0	µA
			XIN clock off, T$_{opr}$ = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = 0	−	1.1	−	µA

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Timing requirements
(Unless Otherwise Specified: V_{CC} = 3 V, V_{SS} = 0 V at T_{opr} = 25°C) [V_{CC} = 3 V]

Table 5.22   XIN Input

Symbol	Parameter	Standard Min.	Standard Max.	Unit
$t_{c(XIN)}$	XIN input cycle time	100	–	ns
$t_{WH(XIN)}$	XIN input "H" width	40	–	ns
$t_{WL(XIN)}$	XIN input "L" width	40	–	ns
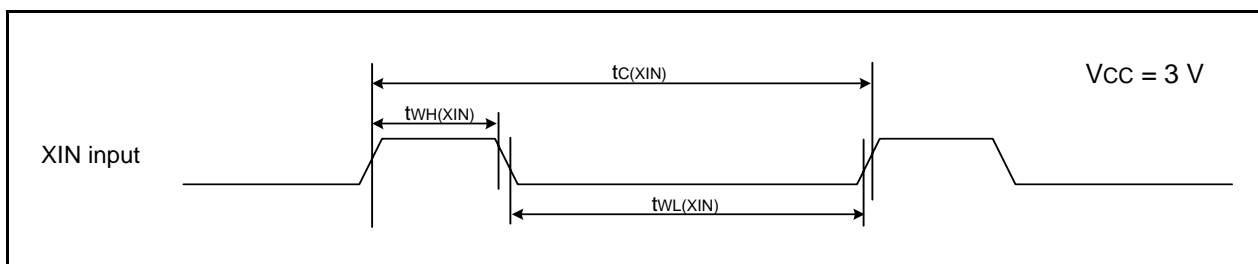
Figure 5.8   XIN Input Timing Diagram when V_{CC} = 3 V

Table 5.23   TRAIO Input

Symbol	Parameter	Standard Min.	Standard Max.	Unit
$t_{c(TRAIO)}$	TRAIO input cycle time	300	–	ns
$t_{WH(TRAIO)}$	TRAIO input "H" width	120	–	ns
$t_{WL(TRAIO)}$	TRAIO input "L" width	120	–	ns

Figure 5.9   TRAIO Input Timing Diagram when V_{CC} = 3 V

Table 5.24   Serial Interface

Symbol	Parameter	Standard Min.	Standard Max.	Unit
$t_{c(CK)}$	CLK0 input cycle time	300	–	ns
$t_{W(CKH)}$	CLK0 input "H" width	150	–	ns
$t_{W(CKL)}$	CLK0 Input "L" width	150	–	ns
$t_{d(C-Q)}$	TXD0 output delay time	–	80	ns
$t_{h(C-Q)}$	TXD0 hold time	0	–	ns
$t_{su(D-C)}$	RXD0 input setup time	70	–	ns
$t_{h(C-D)}$	RXD0 input hold time	90	–	ns
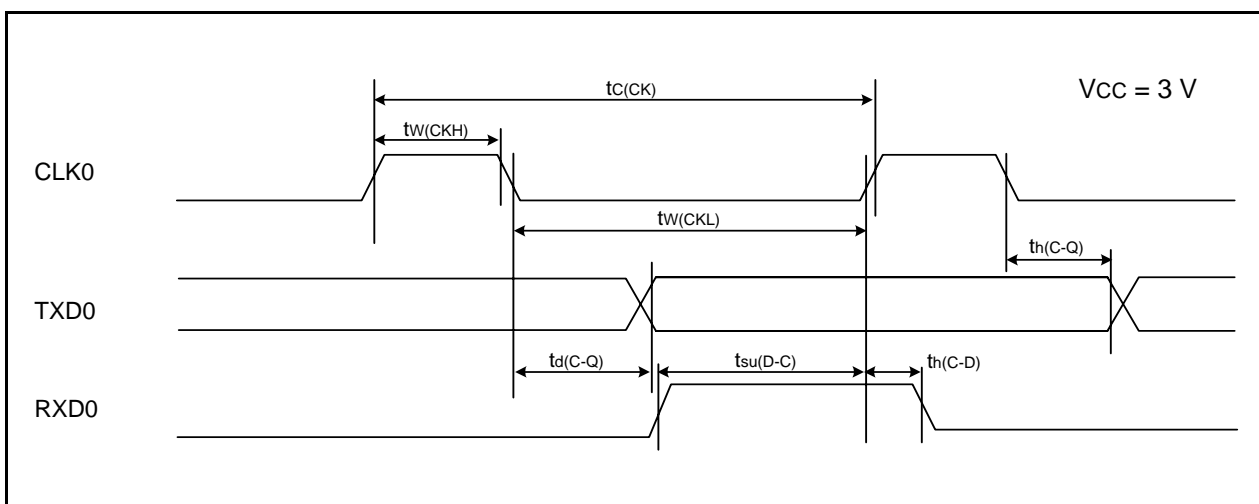

Figure 5.10   Serial Interface Timing Diagram when VCC = 3 V

Table 5.25   External Interrupt INTi (i = 0, 1, 3) Input

Symbol	Parameter	Standard Min.	Standard Max.	Unit
$t_{W(INH)}$	$\overline{INTi}$ input "H" width	380[1]	–	ns
$t_{W(INL)}$	$\overline{INTi}$ input "L" width	380[2]	–	ns

NOTES:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
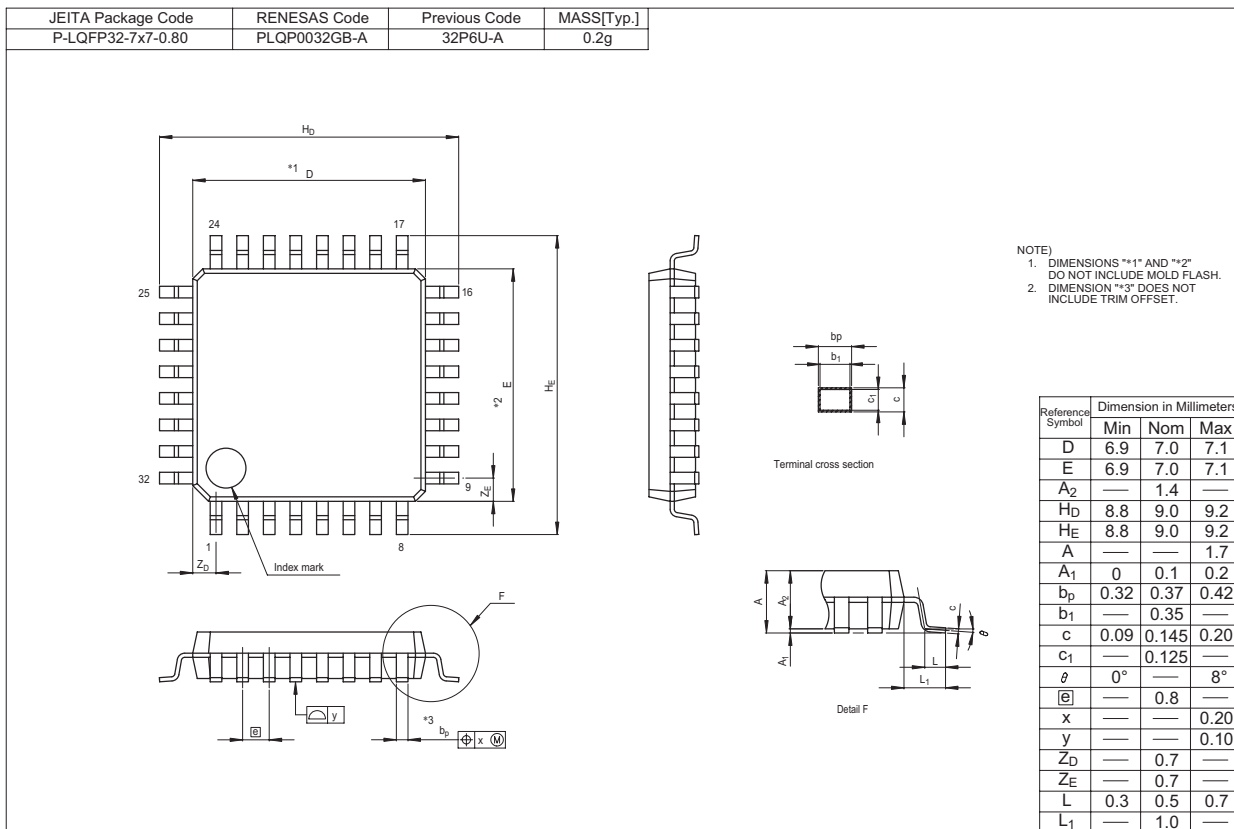2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
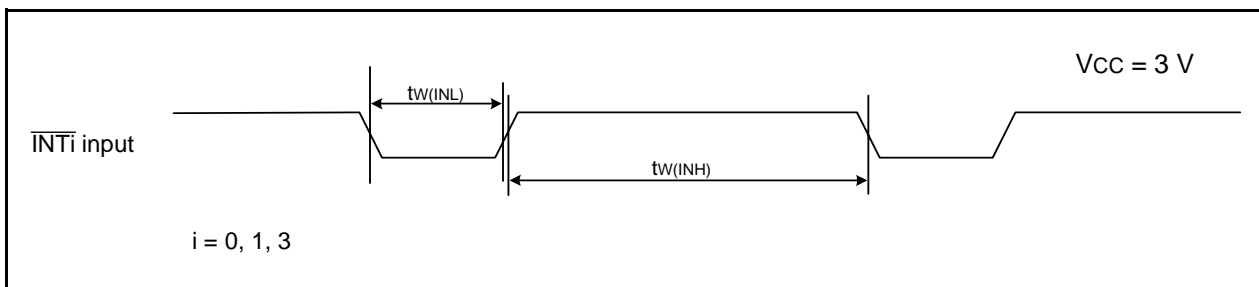
Figure 5.11   External Interrupt INTi Input Timing Diagram when VCC = 3 V

Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the "Packages" section of the Renesas Technology website.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP32-7x7-0.80	PLQP0032GB-A	32P6U-A	0.2g

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Terminal cross section

Detail F

Index mark

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A_2	—	1.4	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.32	0.37	0.42
b_1	—	0.35	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.8	—
x	—	—	0.20
y	—	—	0.10
Z_D	—	0.7	—
Z_E	—	0.7	—
L	0.3	0.5	0.7
L_1	—	1.0	—

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REVISION HISTORY	R8C/2E Group, R8C/2F Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.10	Aug 01, 2007	–	First Edition issued
1.00	Dec 14, 2007	All pages	"Under development" deleted
		2, 4	Table 1.1, Table 1.3: "Interrupts" revised
		6, 7	Table 1.5, Table 1.6: "(D)" deleted
		15, 16	Figure 3.1, Figure 3.2: "Expanded area" deleted
		17	Table 4.1: "002Ch" added
		24	Table 5.2: I_{OH}(sum), NOTE2 revised
		30	Table 5.11: Symbol "fOCO40M"; Parameter added