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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	LINbus, SIO, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	25
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f212f4nfp-u0

1. Overview

1.1 Features

The R8C/2E Group and R8C/2F Group of single-chip MCUs incorporates the R8C/Tiny Series CPU core, employing sophisticated instructions for a high level of efficiency. With 1 Mbyte of address space, and it is capable of executing instructions at high speed. In addition, the CPU core boasts a multiplier for high-speed operation processing.

Power consumption is low, and the supported operating modes allow additional power control. These MCUs also use an anti-noise configuration to reduce emissions of electromagnetic noise and are designed to withstand EMI.

Integration of many peripheral functions, including multifunction timer and serial interface, reduces the number of system components.

Furthermore, the R8C/2F Group has on-chip data flash (1 KB × 2 blocks).

The difference between the R8C/2E Group and R8C/2F Group is only the presence or absence of data flash. Their peripheral functions are the same.

1.1.1 Applications

Electronic household appliances, office equipment, audio equipment, consumer equipment, etc.

Table 1.4   Specifications for R8C/2F Group (2)

Item	Specification
Flash Memory	• Programming and erasure voltage: VCC = 2.7 to 5.5 V • Programming and erasure endurance: 10,000 times (data flash) 1,000 times (program ROM) • Program security: ROM code protect, ID code check • Debug functions: On-chip debug, on-board flash rewrite function
Operating Frequency/Supply Voltage	f(XIN) = 20 MHz (VCC = 3.0 to 5.5 V), f(XIN) = 10 MHz (VCC = 2.7 to 5.5 V)
Current consumption	Typ. 10 mA (VCC = 5.0 V, f(XIN) = 20 MHz) Typ. 6 mA (VCC = 3.0 V, f(XIN) = 10 MHz) Typ. 23 µA (VCC = 3.0 V, wait mode (peripheral clock off)) Typ. 0.7 µA (VCC = 3.0 V, stop mode)
Operating Ambient Temperature	-20 to 85°C (N version) -40 to 85°C (D version)[1]
Package	32-pin LQFP Package code: PLQP0032GB-A (previous code: 32P6U-A)

NOTE:
   1. Specify the D version if D version functions are to be used.

1.2   Product List

Table 1.5 lists Product List for R8C/2E Group, Figure 1.1 shows a Part Number, Memory Size, and Package of
R8C/2E Group, Table 1.6 lists Product List for R8C/2F Group, and Figure 1.2 shows a Part Number, Memory Size,
and Package of R8C/2F Group.

Table 1.5   Product List for R8C/2E Group   **Current of Dec. 2007**

Part No.	ROM Capacity	RAM Capacity	Package Type	Remarks
R5F212E2NFP	8 Kbytes	512 bytes	PLQP0032GB-A	N version
R5F212E4NFP	16 Kbytes	1 Kbyte	PLQP0032GB-A	
R5F212E2DFP	8 Kbytes	512 bytes	PLQP0032GB-A	D version
R5F212E4DFP	16 Kbytes	1 Kbyte	PLQP0032GB-A	
R5F212E2NXXXFP	8 Kbytes	512 bytes	PLQP0032GB-A	N version
R5F212E4NXXXFP	16 Kbytes	1 Kbyte	PLQP0032GB-A	Factory programming product[1]
R5F212E2DXXXFP	8 Kbytes	512 bytes	PLQP0032GB-A	D version
R5F212E4DXXXFP	16 Kbytes	1 Kbyte	PLQP0032GB-A	Factory programming product[1]

NOTE:
1. The user ROM is programmed before shipment.
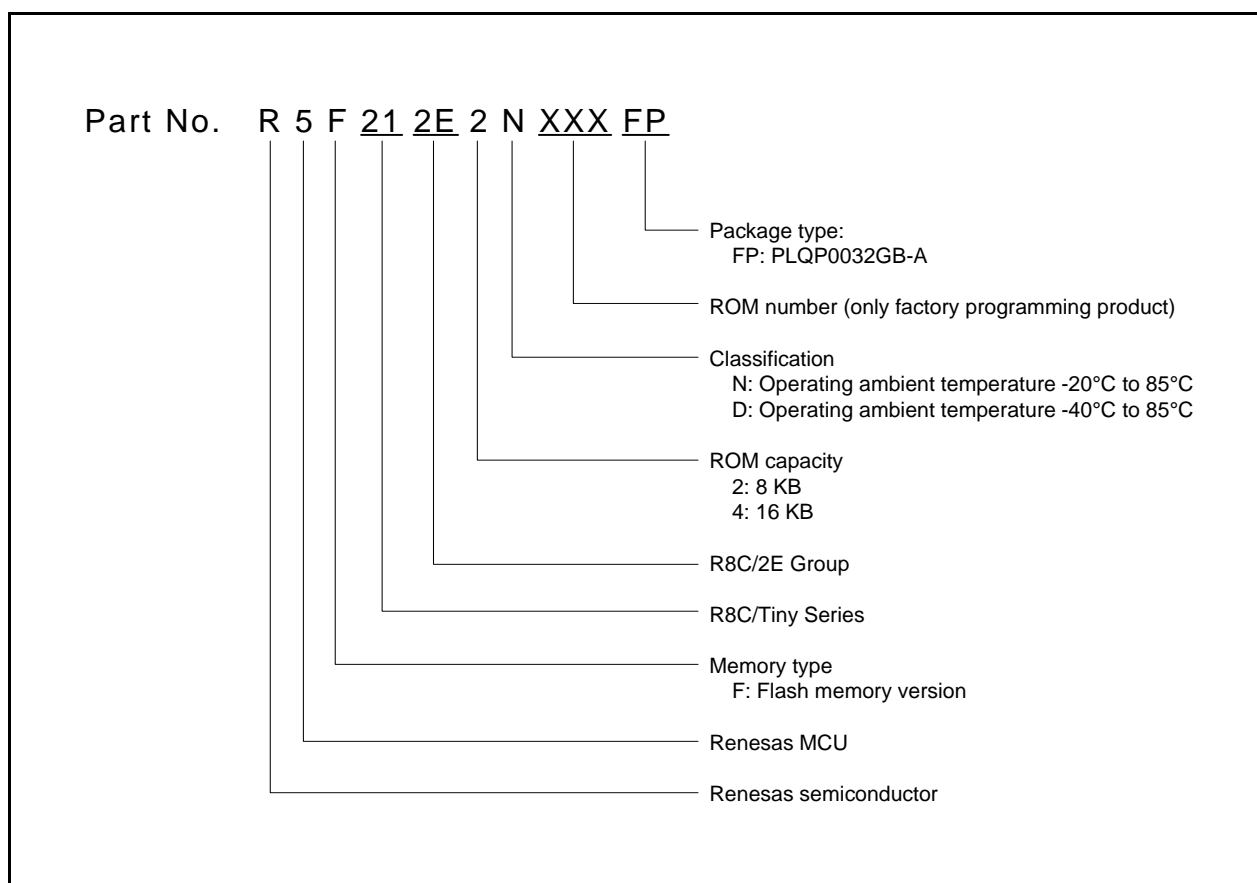
Figure 1.1   Part Number, Memory Size, and Package of R8C/2E Group

Table 1.6   Product List for R8C/2F Group   Current of Dec. 2007

Part No.	ROM Capacity		RAM Capacity	Package Type	Remarks
	Program ROM	Data flash			
R5F212F2NFP	8 Kbytes	1 Kbyte × 2	512 bytes	PLQP0032GB-A	N version
R5F212F4NFP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLQP0032GB-A	
R5F212F2DFP	8 Kbytes	1 Kbyte × 2	512 bytes	PLQP0032GB-A	D version
R5F212F4DFP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLQP0032GB-A	
R5F212F2NXXXFP	8 Kbytes	1 Kbyte × 2	512 bytes	PLQP0032GB-A	N version
R5F212F4NXXXFP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLQP0032GB-A	Factory programming product[1]
R5F212F2DXXXFP	8 Kbytes	1 Kbyte × 2	512 bytes	PLQP0032GB-A	D version
R5F212F4DXXXFP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLQP0032GB-A	Factory programming product[1]

NOTE:
  1. The user ROM is programmed before shipment.
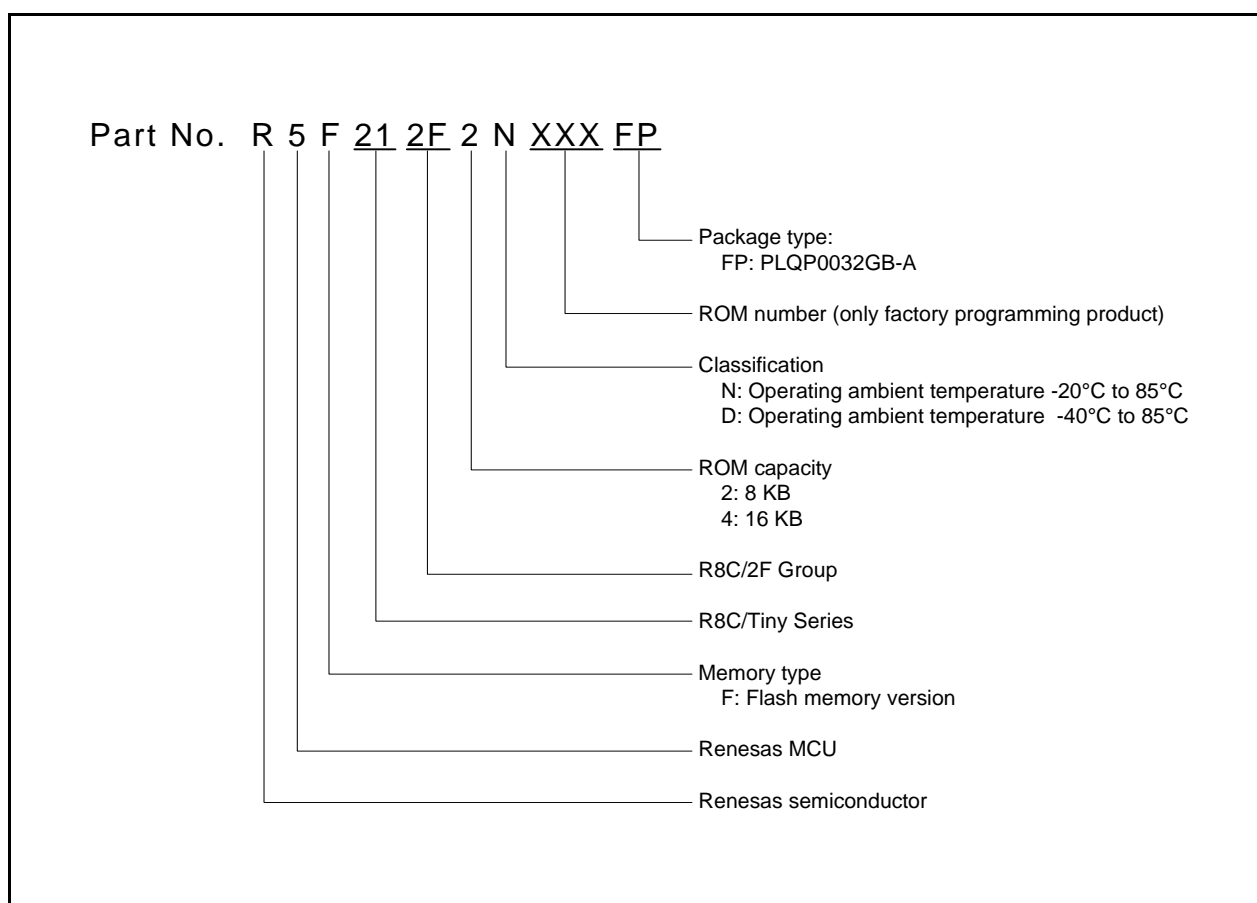
Figure 1.2   Part Number, Memory Size, and Package of R8C/2F Group

Table 1.7   Pin Name Information by Pin Number

Pin Number	Control Pin	Port	I/O Pin Functions for of Peripheral Modules					
			Interrupt	Timer	Serial Interface	A/D Converter	D/A Converter	Comparator
1		P3_5		(TRCIOD)[1]				
2		P3_7		TRAO				
3	$\overline{\text{RESET}}$							
4	XOUT	P4_7						
5	VSS/AVSS							
6	XIN	P4_6						
7	VCC/AVCC							
8	MODE							
9		P4_5	$\overline{\text{INT0}}$					
10		P1_7	$\overline{\text{INT1}}$	TRAIO				
11		P3_6	$(\overline{\text{INT1}})$[1]					
12		P3_1		TRBO				
13		P5_4		TRCIOD				ACOUT1
14		P5_3		TRCIOC				ACOUT0
15		P1_6			CLK0			
16		P1_5	$(\overline{\text{INT1}})$[1]	(TRAIO)[1]	RXD0			
17		P1_4			TXD0			
18		P1_3	$\overline{\text{KI3}}$	(TRBO)[1]		AN11		
19		P1_2	$\overline{\text{KI2}}$	TRCIOB		AN10		
20	VREF	P4_2						
21		P1_1	$\overline{\text{KI1}}$	TRCIOA/ TRCTRG		AN9		
22		P1_0	$\overline{\text{KI0}}$			AN8		
23		P3_3	$\overline{\text{INT3}}$	TRCCLK				
24		P3_4		(TRCIOC)[1]				
25		P0_7				AN0	DA1	
26		P0_6				AN1	DA0	
27		P0_5				AN2		AVREF0
28		P0_4		TREO		AN3		ACMP0
29		P0_3				AN4		AVREF1
30		P0_2				AN5		ACMP1
31		P0_1				AN6		
32		P0_0				AN7		

NOTE:
1. Can be assigned to the pin in parentheses by a program.

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 to be used as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP, and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.
Interrupt are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.
The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has higher priority than IPL, the interrupt is enabled.

2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

Table 4.2   SFR Information (2)[1]

Address	Register	Symbol	After reset
0040h			
0041h			
0042h			
0043h			
0044h			
0045h			
0046h			
0047h	Timer RC Interrupt Control Register	TRCIC	XXXXX000b
0048h			
0049h			
004Ah	Timer RE Interrupt Control Register	TREIC	XXXXX000b
004Bh			
004Ch			
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXXX000b
004Fh			
0050h			
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXXX000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXXX000b
0053h			
0054h			
0055h			
0056h	Timer RA Interrupt Control Register	TRAIC	XXXXX000b
0057h			
0058h	Timer RB Interrupt Control Register	TRBIC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Ah	INT3 Interrupt Control Register	INT3IC	XX00X000b
005Bh	Comparator 0 Interrupt Control Register	CM0IC	XXXXX000b
005Ch	Comparator 1 Interrupt Control Register	CM1IC	XXXXX000b
005Dh	INT0 Interrupt Control Register	INT0IC	XX00X000b
005Eh			
005Fh			
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah			
006Bh			
006Ch			
006Dh			
006Eh			
006Fh			
0070h			
0071h			
0072h			
0073h			
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			

X: Undefined
NOTE:
1.   The blank regions are reserved. Do not access locations in these regions.

Table 4.4 SFR Information (4)[1]

Address	Register	Symbol	After reset
00C0h	A/D Register	AD	XXh
00C1h			XXh
00C2h			
00C3h			
00C4h			
00C5h			
00C6h			
00C7h			
00C8h			
00C9h			
00CAh			
00CBh			
00CCh			
00CDh			
00CEh			
00CFh			
00D0h			
00D1h			
00D2h			
00D3h			
00D4h	A/D Control Register 2	ADCON2	00h
00D5h			
00D6h	A/D Control Register 0	ADCON0	00h
00D7h	A/D Control Register 1	ADCON1	00h
00D8h	D/A Register 0	DA0	00h
00D9h			
00DAh	D/A Register 1	DA1	00h
00DBh			
00DCh	D/A Control Register	DACON	00h
00DDh			
00DEh			
00DFh			
00E0h	Port P0 Register	P0	00h
00E1h	Port P1 Register	P1	00h
00E2h	Port P0 Direction Register	PD0	00h
00E3h	Port P1 Direction Register	PD1	00h
00E4h			
00E5h	Port P3 Register	P3	00h
00E6h			
00E7h	Port P3 Direction Register	PD3	00h
00E8h	Port P4 Register	P4	00h
00E9h	Port P5 Register	P5	00h
00EAh	Port P4 Direction Register	PD4	00h
00EBh	Port P5 Direction Register	PD5	00h
00ECh			
00EDh			
00EEh			
00EFh			
00F0h			
00F1h			
00F2h			
00F3h			
00F4h			
00F5h			
00F6h	Pin Select Register 2	PINSR2	00h
00F7h	Pin Select Register 3	PINSR3	00h
00F8h	Port Mode Register	PMR	00h
00F9h	External Input Enable Register	INTEN	00h
00FAh	INT Input Filter Select Register	INTF	00h
00FBh	Key Input Enable Register	KIEN	00h
00FCh	Pull-Up Control Register 0	PUR0	00h
00FDh	Pull-Up Control Register 1	PUR1	00h
00FEh	Port P1 Drive Capacity Control Register	P1DRR	00h
00FFh			

X: Undefined
NOTE:
1. The blank regions are reserved. Do not access locations in these regions.

Table 4.6   SFR Information (6)[1]

Address	Register	Symbol	After reset
0140h			
0141h			
0142h			
0143h			
0144h			
0145h			
0146h			
0147h			
0148h			
0149h			
014Ah			
014Bh			
014Ch			
014Dh			
014Eh			
014Fh			
0150h			
0151h			
0152h			
0153h			
0154h			
0155h			
0156h			
0157h			
0158h			
0159h			
015Ah			
015Bh			
015Ch			
015Dh			
015Eh			
015Fh			
0160h			
0161h			
0162h			
0163h			
0164h			
0165h			
0166h			
0167h			
0168h			
0169h			
016Ah			
016Bh			
016Ch			
016Dh			
016Eh			
016Fh			
0170h			
0171h			
0172h			
0173h			
0174h	Comparator 0 Control Register	ACCR0	00001000b
0175h	Comparator 1 Control Register	ACCR1	00001000b
0176h			
0177h	Comparator Mode Register	ACMR	00h
0178h			
0179h			
017Ah			
017Bh			
017Ch			
017Dh			
017Eh			
017Fh			

X: Undefined
NOTE:
1. The blank regions are reserved. Do not access locations in these regions.

Table 4.7　　SFR Information (7)[1]

Address	Register	Symbol	After reset
0180h			
0181h			
0182h			
0183h			
0184h			
0185h			
0186h			
0187h			
0188h			
0189h			
018Ah			
018Bh			
018Ch			
018Dh			
018Eh			
018Fh			
0190h			
0191h			
0192h			
0193h			
0194h			
0195h			
0196h			
0197h			
0198h			
0199h			
019Ah			
019Bh			
019Ch			
019Dh			
019Eh			
019Fh			
01A0h			
01A1h			
01A2h			
01A3h			
01A4h			
01A5h			
01A6h			
01A7h			
01A8h			
01A9h			
01AAh			
01ABh			
01ACh			
01ADh			
01AEh			
01AFh			
01B0h			
01B1h			
01B2h			
01B3h	Flash Memory Control Register 4	FMR4	01000000b
01B4h			
01B5h	Flash Memory Control Register1	FMR1	1000000Xb
01B6h			
01B7h	Flash Memory Control Register 0	FMR0	00000001b
01B8h			
01B9h			
01BAh			
01BBh			
01BCh			
01BDh			
01BEh			
01BFh			

FFFFh	Option Function Select Register	OFS	(Note 2)

X: Undefined
NOTES:
　1.　The blank regions are reserved. Do not access locations in these regions.
　2.　The OFS register cannot be changed by a program. Use a flash programmer to write to it.

5. Electrical Characteristics

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated Value	Unit
V_{CC}/AV_{CC}	Supply voltage		−0.3 to 6.5	V
V_I	Input voltage		−0.3 to V_{CC} + 0.3	V
V_O	Output voltage		−0.3 to V_{CC} + 0.3	V
P_d	Power dissipation	T_{opr} = 25°C	500	mW
T_{opr}	Operating ambient temperature		−20 to 85 (N version) / −40 to 85 (D version)	°C
T_{stg}	Storage temperature		−65 to 150	°C

Table 5.2 Recommended Operating Conditions

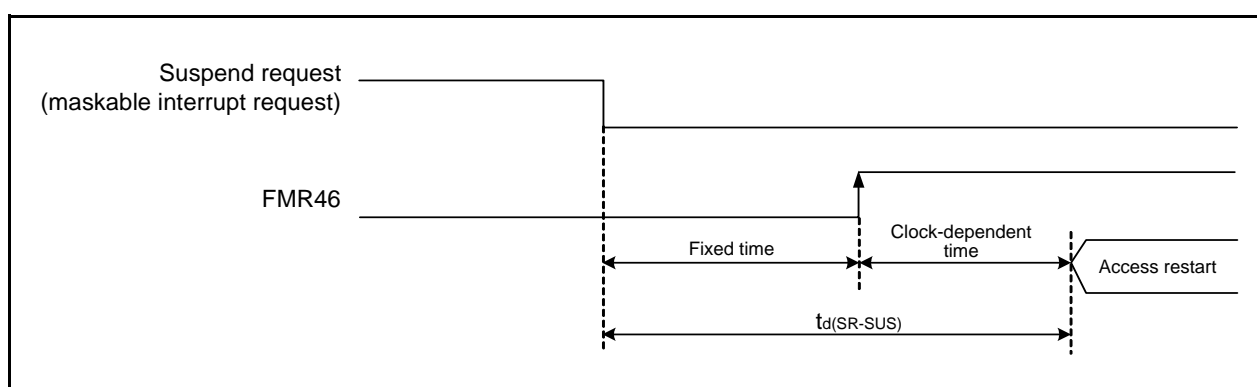| Symbol	Parameter		Conditions	Standard Min.	Standard Typ.	Standard Max.	Unit
V_{CC}/AV_{CC}	Supply voltage			2.7	–	5.5	V
V_{SS}/AV_{SS}	Supply voltage			–	0	–	V
V_{IH}	Input "H" voltage			0.8 V_{CC}	–	V_{CC}	V
V_{IL}	Input "L" voltage			0	–	0.2 V_{CC}	V
$I_{OH(sum)}$	Peak sum output "H" current	Sum of all pins $I_{OH(peak)}$		–	–	−160	mA
$I_{OH(sum)}$	Average sum output "H" current	Sum of all pins $I_{OH(avg)}$		–	–	−80	mA
$I_{OH(peak)}$	Peak output "H" current	Except P1_0 to P1_7		–	–	−10	mA
		P1_0 to P1_7		–	–	−20	mA
$I_{OH(avg)}$	Average output "H" current	Except P1_0 to P1_7		–	–	−5	mA
		P1_0 to P1_7		–	–	−10	mA
$I_{OL(sum)}$	Peak sum output "L" currents	Sum of all pins $I_{OL(peak)}$		–	–	160	mA
$I_{OL(sum)}$	Average sum output "L" currents	Sum of all pins $I_{OL(avg)}$		–	–	80	mA
$I_{OL(peak)}$	Peak output "L" currents	Except P1_0 to P1_7		–	–	10	mA
		P1_0 to P1_7		–	–	20	mA
$I_{OL(avg)}$	Average output "L" current	Except P1_0 to P1_7		–	–	5	mA
		P1_0 to P1_7		–	–	10	mA
$f(XIN)$	XIN clock input oscillation frequency		3.0 V ≤ V_{CC} ≤ 5.5 V	0	–	20	MHz
			2.7 V ≤ V_{CC} < 3.0 V	0	–	10	MHz
–	System clock	OCD2 = 0 XIN clock selected	3.0 V ≤ V_{CC} ≤ 5.5 V	0	–	20	MHz
			2.7 V ≤ V_{CC} < 3.0 V	0	–	10	MHz
		OCD2 = 1 On-chip oscillator clock selected	FRA01 = 0 Low-speed on-chip oscillator clock selected	–	125	–	kHz
			FRA01 = 1 High-speed on-chip oscillator clock selected 3.0 V ≤ V_{CC} ≤ 5.5 V	–	–	20	MHz
			FRA01 = 1 High-speed on-chip oscillator clock selected 2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	10	MHz

NOTES:
1. V_{CC} = 2.7 to 5.5 V at T_{opr} = −20 to 85°C (N version) / −40 to 85°C (D version), unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.

Table 5.7   Flash Memory (Data flash Block A, Block B) Electrical Characteristics[4]

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance[2]		10,000[3]	–	–	times
–	Byte program time (program/erase endurance ≤ 1,000 times)		–	50	400	µs
–	Byte program time (program/erase endurance > 1,000 times)		–	65	–	µs
–	Block erase time (program/erase endurance ≤ 1,000 times)		–	0.2	9	s
–	Block erase time (program/erase endurance > 1,000 times)		–	0.3	–	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		–	–	97+CPU clock × 6 cycles	µs
–	Interval from erase start/restart until following suspend request		650	–	–	µs
–	Interval from program start/restart until following suspend request		0	–	–	ns
–	Time from suspend until program/erase restart		–	–	3+CPU clock × 4 cycles	µs
–	Program, erase voltage		2.7	–	5.5	V
–	Read voltage		2.7	–	5.5	V
–	Program, erase temperature		–20[8]	–	85	°C
–	Data hold time[9]	Ambient temperature = 55 °C	20	–	–	year

NOTES:
1. V_{CC} = 2.7 to 5.5 V at T_{opr} = −20 to 85°C (N version) / −40 to 85°C (D version), unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 100 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
   However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. Standard of block A and block B when program and erase endurance exceeds 1,000 times. Byte program time to 1,000 times is the same as that in program ROM.
5. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erase count of each block and limit the number of erase operations to a certain number.
6. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
7. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
8. −40°C for D version.
9. The data hold time includes time that the power supply is off or the clock is not supplied.

Figure 5.2   Time delay until Suspend

Table 5.8   Voltage Detection 1 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det1}	Voltage detection level[4]		2.7	2.85	3.00	V
–	Voltage monitor 1 interrupt request generation time[2]		–	40	–	μs
–	Voltage detection circuit self power consumption	VCA26 = 1, V_{CC} = 5.0 V	–	0.6	–	μA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts[3]		–	–	100	μs
V_{ccmin}	MCU operating voltage minimum value		2.7	–	–	V

NOTES:
1. The measurement condition is V_{CC} = 2.7 V to 5.5 V and T_{opr} = −20 to 85°C (N version) / −40 to 85°C (D version).
2. Time until the voltage monitor 1 interrupt request is generated after the voltage passes V_{det1}.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.
4. This parameter shows the voltage detection level when the power supply drops.
    The voltage detection level when the power supply rises is higher than the voltage detection level when the power supply drops by approximately 0.1 V.

**Table 5.9   Voltage Detection 2 Circuit Electrical Characteristics**

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det2}	Voltage detection level		3.3	3.6	3.9	V
–	Voltage monitor 2 interrupt request generation time[2]		–	40	–	μs
–	Voltage detection circuit self power consumption	VCA27 = 1, V_{CC} = 5.0 V	–	0.6	–	μA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts[3]		–	–	100	μs

NOTES:
1. The measurement condition is V_{CC} = 2.7 V to 5.5 V and T_{opr} = −20 to 85°C (N version) / −40 to 85°C (D version).
2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes V_{det2}.
3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

Timing Requirements
(Unless Otherwise Specified: V_{CC} = 5 V, V_{SS} = 0 V at T_{opr} = 25°C) [V_{CC} = 5 V]

Table 5.16   XIN Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{C(XIN)}$	XIN input cycle time	50	–	ns
$t_{WH(XIN)}$	XIN input "H" width	25	–	ns
$t_{WL(XIN)}$	XIN input "L" width	25	–	ns
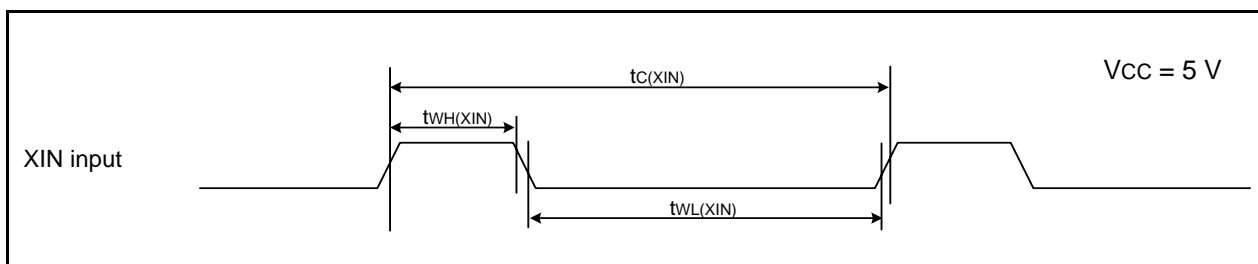
Figure 5.4   XIN Input Timing Diagram when V_{CC} = 5 V

Table 5.17   TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{C(TRAIO)}$	TRAIO input cycle time	100	–	ns
$t_{WH(TRAIO)}$	TRAIO input "H" width	40	–	ns
$t_{WL(TRAIO)}$	TRAIO input "L" width	40	–	ns

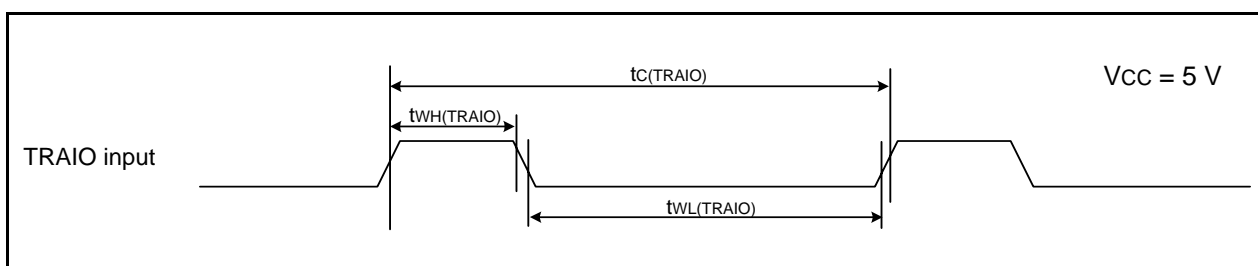

Figure 5.5   TRAIO Input Timing Diagram when V_{CC} = 5 V

Table 5.20 Electrical Characteristics (3) [V$_{CC}$ = 3 V]

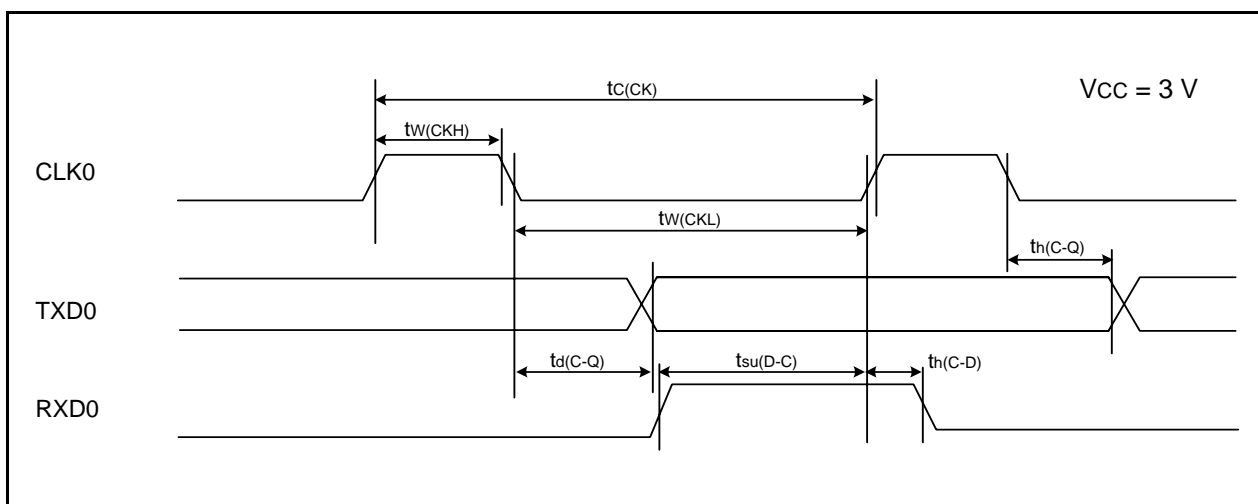| Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V$_{OH}$	Output "H" voltage	Except P1_0 to P1_7, XOUT	I$_{OH}$ = −1 mA		V$_{CC}$ − 0.5	−	V$_{CC}$	V
		P1_0 to P1_7	Drive capacity HIGH	I$_{OH}$ = −2 mA	V$_{CC}$ − 0.5	−	V$_{CC}$	V
			Drive capacity LOW	I$_{OH}$ = −1 mA	V$_{CC}$ − 0.5	−	V$_{CC}$	V
		XOUT	Drive capacity HIGH	I$_{OH}$ = −0.1 mA	V$_{CC}$ − 0.5	−	V$_{CC}$	V
			Drive capacity LOW	I$_{OH}$ = −50 μA	V$_{CC}$ − 0.5	−	V$_{CC}$	V
V$_{OL}$	Output "L" voltage	Except P1_0 to P1_7, XOUT	I$_{OL}$ = 1 mA		−	−	0.5	V
		P1_0 to P1_7	Drive capacity HIGH	I$_{OL}$ = 2 mA	−	−	0.5	V
			Drive capacity LOW	I$_{OL}$ = 1 mA	−	−	0.5	V
		XOUT	Drive capacity HIGH	I$_{OL}$ = 0.1 mA	−	−	0.5	V
			Drive capacity LOW	I$_{OL}$ = 50 μA	−	−	0.5	V
V$_{T+}$-V$_{T-}$	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRAIO, RXD0, CLK0			0.1	0.3	−	V
		$\overline{RESET}$			0.1	0.4	−	V
I$_{IH}$	Input "H" current		VI = 3 V, V$_{CC}$ = 3 V		−	−	4.0	μA
I$_{IL}$	Input "L" current		VI = 0 V, V$_{CC}$ = 3 V		−	−	−4.0	μA
R$_{PULLUP}$	Pull-up resistance		VI = 0 V, V$_{CC}$ = 3 V		66	160	500	kΩ
R$_{fXIN}$	Feedback resistance	XIN			−	3.0	−	MΩ
V$_{RAM}$	RAM hold voltage		During stop mode		1.8	−	−	V

NOTE:
1. V$_{CC}$ =2.7 to 3.3 V at T$_{opr}$ = −20 to 85°C (N version) / −40 to 85°C (D version), f$_{(XIN)}$ = 10 MHz, unless otherwise specified.

Table 5.21   Electrical Characteristics (4) [Vcc = 3 V]
(T$_{opr}$ = −20 to 85°C (N version) / −40 to 85°C (D version), unless otherwise specified.)

| Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 2.7 to 3.3 V) Single-chip mode, output pins are open, other pins are Vss	High-speed clock mode	XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	−	6	−	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	−	2	−	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division	−	5	9	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	−	2	−	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1	−	130	300	µA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = 0 VCA20 = 1	−	25	70	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = 0 VCA20 = 1	−	23	55	µA
		Stop mode	XIN clock off, T$_{opr}$ = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = 0	−	0.7	3.0	µA
			XIN clock off, T$_{opr}$ = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = 0	−	1.1	−	µA

Table 5.24   Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{C(CK)}$	CLK0 input cycle time	300	–	ns
$t_{W(CKH)}$	CLK0 input "H" width	150	–	ns
$t_{W(CKL)}$	CLK0 Input "L" width	150	–	ns
$t_{d(C-Q)}$	TXD0 output delay time	–	80	ns
$t_{h(C-Q)}$	TXD0 hold time	0	–	ns
$t_{su(D-C)}$	RXD0 input setup time	70	–	ns
$t_{h(C-D)}$	RXD0 input hold time	90	–	ns

Figure 5.10   Serial Interface Timing Diagram when Vcc = 3 V

Table 5.25   External Interrupt INTi (i = 0, 1, 3) Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	INTi input "H" width	380[1]	–	ns
$t_{W(INL)}$	INTi input "L" width	380[2]	–	ns

NOTES:
1. When selecting the digital filter by the INTi input filter select bit, use an INTi input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the INTi input filter select bit, use an INTi input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
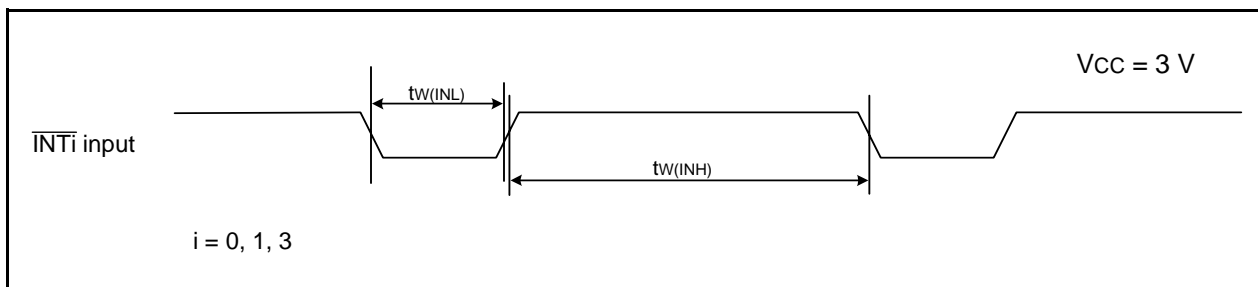
Figure 5.11   External Interrupt INTi Input Timing Diagram when Vcc = 3 V

REVISION HISTORY		R8C/2E Group, R8C/2F Group Datasheet	

Rev.	Date	Description	
		Page	Summary
0.10	Aug 01, 2007	–	First Edition issued
1.00	Dec 14, 2007	All pages	"Under development" deleted
		2, 4	Table 1.1, Table 1.3: "Interrupts" revised
		6, 7	Table 1.5, Table 1.6: "(D)" deleted
		15, 16	Figure 3.1, Figure 3.2: "Expanded area" deleted
		17	Table 4.1: "002Ch" added
		24	Table 5.2: I_{OH}(sum), NOTE2 revised
		30	Table 5.11: Symbol "fOCO40M"; Parameter added