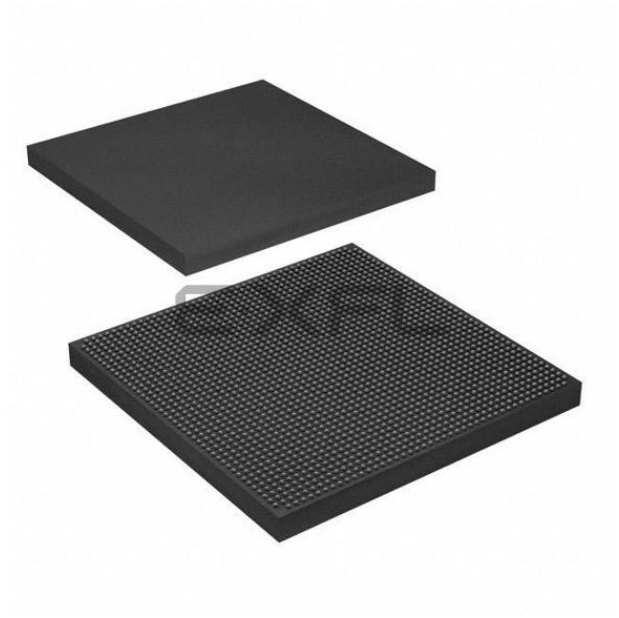

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	359250
Number of Logic Elements/Cells	952000
Total RAM Bits	53248000
Number of I/O	840
Number of Gates	-
Voltage - Supply	0.82V ~ 0.88V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1932-BBGA, FCBGA
Supplier Device Package	1932-FBGA, FC (45x45)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5seebf45c2l

Stratix V E devices offer the highest logic density within the Stratix V family with nearly one million logic elements (LEs) in the largest device. These devices are optimized for applications such as ASIC and system emulation, diagnostic imaging, and instrumentation.

Common to all Stratix V family variants are a rich set of high-performance building blocks, including a redesigned adaptive logic module (ALM), 20 Kbit (M20K) embedded memory blocks, variable precision DSP blocks, and fractional phase-locked loops (PLLs). All of these building blocks are interconnected by Altera's superior multi-track routing architecture and comprehensive fabric clocking network.

Also common to Stratix V devices is the new Embedded HardCopy Block, which is a customizable hard IP block that leverages Altera's unique HardCopy ASIC capabilities. The Embedded HardCopy Block in Stratix V FPGAs is used to harden IP instantiation of PCIe Gen3, Gen2, and Gen1.

Stratix V Features Summary

Table 1: Summary of Features for Stratix V Devices

Feature	Description
Technology	• 28-nm TSMC process technology • 0.85-V or 0.9-V core voltage
Low-power serial transceivers	• 28.05-Gbps transceivers on Stratix V GT devices • Electronic dispersion compensation (EDC) for XFP, SFP+, QSFP, CFP optical module support • Adaptive linear and decision feedback equalization • Transmitter pre-emphasis and de-emphasis • Dynamic reconfiguration of individual channels • On-chip instrumentation (EyeQ non-intrusive data eye monitoring)
Backplane capability	• 600-Megabits per second (Mbps) to 12.5-Gbps data rate capability
General-purpose I/Os (GPIOs)	• 1.6-Gbps LVDS • 1,066-MHz external memory interface • On-chip termination (OCT) • 1.2-V to 3.3-V interfacing for all Stratix V devices
Embedded HardCopy Block	• PCIe Gen3, Gen2, and Gen1 complete protocol stack, x1/x2/x4/x8 end point and root port
Embedded transceiver hard IP	• Interlaken physical coding sublayer (PCS) • Gigabit Ethernet (GbE) and XAUI PCS • 10G Ethernet PCS • Serial RapidIO® (SRIO) PCS • Common Public Radio Interface (CPRI) PCS • Gigabit Passive Optical Networking (GPON) PCS
Power management	• Programmable Power Technology • Quartus II integrated PowerPlay Power Analysis

Feature	Description
High-performance core fabric	• Enhanced ALM with four registers • Improved routing architecture reduces congestion and improves compile times
Embedded memory blocks	• M20K: 20-Kbit with hard error correction code (ECC) • MLAB: 640-bit
Variable precision DSP blocks	• Up to 600 MHz performance • Natively support signal processing with precision ranging from 9x9 up to 54x54 • New native 27x27 multiply mode • 64-bit accumulator and cascade for systolic finite impulse responses (FIRs) • Embedded internal coefficient memory • Pre-adder/subtractor improves efficiency • Increased number of outputs allows more independent multipliers
Fractional PLLs	• Fractional mode with third-order delta-sigma modulation • Integer mode • Precision clock synthesis, clock delay compensation, and zero delay buffer (ZDB)
Clock networks	• 800-MHz fabric clocking • Global, quadrant, and peripheral clock networks • Unused clock networks can be powered down to reduce dynamic power
Device configuration	• Serial and parallel flash interface • Enhanced advanced encryption standard (AES) design security features • Tamper protection • Partial and dynamic reconfiguration • Configuration via Protocol (CvP)
High-performance packaging	• Multiple device densities with identical package footprints enables seamless migration between different FPGA densities • FBGA packaging with on-package decoupling capacitors • Lead and RoHS-compliant lead-free options
HardCopy V migration	—

Stratix V Family Plan

The following tables list the features of the different Stratix V devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Altera Product Selector.

Table 2: Stratix V GT Device Features

Feature	5SGTC5	5SGTC7
Logic Elements (K)	425	622
ALMs	160,400	234,720
Registers (K)	642	939
28.05/12.5-Gbps Transceivers	4/32	4/32
PCIe hard IP Blocks	1	1
Fractional PLLs	28	28
M20K Memory Blocks	2,304	2,560
M20K Memory (MBits)	45	50
Variable Precision Multipliers (18x18)	512	512
Variable Precision Multipliers (27x27)	256	256
DDR3 SDRAM x72 DIMM Interfaces	4	4
User I/Os(1), Full-Duplex LVDS, 28.05/12.5-Gbps Transceivers		
Package (2) (3)	**5SGTC5**	**5SGTC7**
KF40-F1517 (4) (40 mm)	600, 150, 36	600, 150, 36

(1) The number of GPIOs does not include transceiver I/Os. In the Quartus II software, the number of user I/Os includes transceiver I/Os.
(2) Packages are flipchip ball grid array (1.0-mm pitch).
(3) Each package row offers pin migration (common board footprint) for all devices in the row.
(4) Migration between select Stratix V GT devices and Stratix V GX devices is available. For more information, refer to **Table 6** and to *AN 644: Migration Between Stratix V GX and Stratix V GT Devices*.