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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	172600
Number of Logic Elements/Cells	457000
Total RAM Bits	39936000
Number of I/O	552
Number of Gates	-
Voltage - Supply	0.82V ~ 0.88V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5sgsmd5h3f35c2l

Feature	Description
High-performance core fabric	• Enhanced ALM with four registers • Improved routing architecture reduces congestion and improves compile times
Embedded memory blocks	• M20K: 20-Kbit with hard error correction code (ECC) • MLAB: 640-bit
Variable precision DSP blocks	• Up to 600 MHz performance • Natively support signal processing with precision ranging from 9x9 up to 54x54 • New native 27x27 multiply mode • 64-bit accumulator and cascade for systolic finite impulse responses (FIRs) • Embedded internal coefficient memory • Pre-adder/subtractor improves efficiency • Increased number of outputs allows more independent multipliers
Fractional PLLs	• Fractional mode with third-order delta-sigma modulation • Integer mode • Precision clock synthesis, clock delay compensation, and zero delay buffer (ZDB)
Clock networks	• 800-MHz fabric clocking • Global, quadrant, and peripheral clock networks • Unused clock networks can be powered down to reduce dynamic power
Device configuration	• Serial and parallel flash interface • Enhanced advanced encryption standard (AES) design security features • Tamper protection • Partial and dynamic reconfiguration • Configuration via Protocol (CvP)
High-performance packaging	• Multiple device densities with identical package footprints enables seamless migration between different FPGA densities • FBGA packaging with on-package decoupling capacitors • Lead and RoHS-compliant lead-free options
HardCopy V migration	—

Stratix V Family Plan

The following tables list the features of the different Stratix V devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Altera Product Selector.

Table 2: Stratix V GT Device Features

Feature	5SGTC5	5SGTC7
Logic Elements (K)	425	622
ALMs	160,400	234,720
Registers (K)	642	939
28.05/12.5-Gbps Transceivers	4/32	4/32
PCIe hard IP Blocks	1	1
Fractional PLLs	28	28
M20K Memory Blocks	2,304	2,560
M20K Memory (MBits)	45	50
Variable Precision Multipliers (18x18)	512	512
Variable Precision Multipliers (27x27)	256	256
DDR3 SDRAM x72 DIMM Interfaces	4	4
User I/Os[(1)], Full-Duplex LVDS, 28.05/12.5-Gbps Transceivers		
Package [(2)] [(3)]	**5SGTC5**	**5SGTC7**
KF40-F1517 [(4)] (40 mm)	600, 150, 36	600, 150, 36

(1) The number of GPIOs does not include transceiver I/Os. In the Quartus II software, the number of user I/Os includes transceiver I/Os.
(2) Packages are flipchip ball grid array (1.0-mm pitch).
(3) Each package row offers pin migration (common board footprint) for all devices in the row.
(4) Migration between select Stratix V GT devices and Stratix V GX devices is available. For more information, refer to **Table 6** and to *AN 644: Migration Between Stratix V GX and Stratix V GT Devices*.

Table 3: Stratix V GX Device Features

Features	5SGXA 3	5SGXA 4	5SGXA 5	5SGXA 7	5SGXA 9	5SGXA B	5SGXB 5	5SGXB 6	5SGXB 9	5SGXBB
Logic Elements (K)	340	420	490	622	840	952	490	597	840	952
ALMs	128,300	158,500	185,000	234,720	317,000	359,200	185,000	225,400	317,000	359,200
Registers (K)	513	634	740	939	1,268	1,437	740	902	1,268	1,437
14.1-Gbps Transceivers	12, 24, or 36	24 or 36	24, 36, or 48	24, 36, or 48	36 or 48	36 or 48	66	66	66	66
PCIe hard IP Blocks	1 or 2	1 or 2	1, 2, or 4	1, 2, or 4	1, 2, or 4	1, 2, or 4	1 or 4	1 or 4	1 or 4	1 or 4
Fractional PLLs	20 (5)	24	28	28	28	28	24	24	32	32
M20K Memory Blocks	957	1,900	2,304	2,560	2,640	2,640	2,100	2,660	2,640	2,640
M20K Memory (MBits)	19	37	45	50	52	52	41	52	52	52
Variable Precision Multipliers (18x18)	512	512	512	512	704	704	798	798	704	704
Variable Precision Multipliers (27x27)	256	256	256	256	352	352	399	399	352	352

(5) The F1517 package contains 24 PLLs. The other packages with this device contain 20 PLLs.

Features	5SGXA 3	5SGXA 4	5SGXA 5	5SGXA 7	5SGXA 9	5SGXA B	5SGXB 5	5SGXB 6	5SGXB 9	5SGXBB
DDR3 SDRAM x72 DIMM Interfaces (6)	6	6	6	6	6	6	4	4	4	4
User I/Os(1), Full-Duplex LVDS, 14.1-Gbps Transceivers										
Package (2) (3) (7) (8)	5SGXA3	5SGXA4	5SGXA5	5SGXA7	5SGXA9	5SGXA B	5SGXB5	5SGXB6	5SGXB9	5SGXBB
EH29-H780 (33 mm)	360, 90, 12H	—	—	—	—	—	—	—	—	—
HF35-F1152 (9) (35 mm)	432, 108, 24	552, 138, 24	552, 138, 24	552, 138, 24	—	—	—	—	—	—
KF35-F1152 (35 mm)	432, 108, 36	432, 108, 36	432, 108, 36	432, 108, 36	—	—	—	—	—	—
KF40-F1517 (40 mm) KH40-H1517 (9) (45 mm)	696, 174, 36	696, 174, 36	696, 174, 36	696, 174, 36	696, 174, 36H	696, 174, 36H	—	—	—	—

(6) These are the maximum number of x72 interfaces available. The actual number of interfaces depends on the device package.

(7) LVDS counts are full duplex channels. Each full duplex channel is one transmitter (TX) pair plus one receiver (RX) pair.

(8) A superscript H after the number of transceivers indicates that this device is only available in a hybrid package. Hybrid packages are slightly larger than conventional FBGAs. Refer to Altera's packaging documentation for more information.

(9) Migration between select Stratix V GX devices and Stratix V GS devices is available. For more information, refer to **Table 6**.

User I/Os(1), Full-Duplex LVDS, 14.1-Gbps Transceivers										
Package (2) (3) (7) (8)	5SGXA3	5SGXA4	5SGXA5	5SGXA7	5SGXA9	5SGXAB	5SGXB5	5SGXB6	5SGXB9	5SGXBB
NF40-F1517 (4) (40 mm)	—	—	600, 150, 48	600, 150, 48	—	—	—	—	—	—
RF40-F1517 (40 mm)	—	—	—	—	—	—	432, 108, 66	432, 108, 66	—	—
RF43-F1760 (42.5 mm)	—	—	—	—	—	—	600, 150, 66	600, 150, 66	—	—
RH43-H1760 (45 mm)	—	—	—	—	—	—	—	—	600, 150, 66H	600, 150, 66H
NF45-F1932 (9) (45 mm)	—	—	840, 210, 48	840, 210, 48	840, 210, 48	840, 210, 48	—	—	—	—

Table 4: Stratix V GS Device Features

Features	5SGSD3	5SGSD4	5SGSD5	5SGSD6	5SGSD8
Logic Elements (K)	236	360	457	583	695
ALMs	89,000	135,840	172,600	220,000	262,400
Registers (K)	356	543	690	880	1,050
14.1-Gbps transceivers	12 or 24	12, 24, or 36	24 or 36	36 or 48	36 or 48
PCIe hard IP blocks	1	1	1	1, 2, or 4	1, 2, or 4
Fractional PLLs	20	20 (5)	24	28	28
M20K Memory Blocks	688	957	2,014	2,320	2,567

Features	5SGSD3	5SGSD4	5SGSD5	5SGSD6	5SGSD8
M20K Memory (MBits)	13	19	39	45	50
Variable Precision Multipliers (18x18)	1,200	2,088	3,180	3,550	3,926
Variable Precision Multipliers (27x27)	600	1,044	1,590	1,775	1,963
DDR3 SDRAM x72 DIMM Interfaces	2	4	4	6	6
User I/Os(1), Full-Duplex LVDS, 14.1-Gbps Transceivers					
Package (2) (3) (7) (8)	5SGSD3	5SGSD4	5SGSD5	5SGSD6	5SGSD8
EH29-H780 (33 mm)	360, 90, 12H	360, 90, 12H	—	—	—
HF35-F1152 (9) (35 mm)	432, 108, 24	432, 108, 24	552, 138, 24	—	—
KF40-F1517 (9) (40 mm)	—	696, 174, 36	696, 174, 36	696, 174, 36	696, 174, 36
NF45-F1932 (9) (45 mm)	—	—	—	840, 210, 48	840, 210, 48

Table 5: Stratix V E Device Features

Features	5SEE9	5SEEB
Logic Elements (K)	840	952
ALMs	317,000	359,200
Registers (K)	1,268	1,437
Fractional PLLs	28	28
M20K Memory Blocks	2,640	2,640
M20K Memory (MBits)	52	52
Variable Precision Multipliers (18x18)	704	704

Features	5SEE9	5SEEB
Variable Precision Multipliers (27x27)	352	352
DDR3 SDRAM x72 DIMM Interfaces	6	6
User I/Os[1], Full-Duplex LVDS		
Package [2] [3] [7] [8]	**5SEE9**	**5SEEB**
H40-H1517 (45 mm)	696, 174[H]	696, 174[H]
F45-F1932 (45 mm)	840, 210	840, 210

Table 6: Device Migration List Across All Stratix V Device Variants

All devices in a specific column allow migration.

	Package										
	EH29-H780	HF35-F1152 [10]	KF35-F1152	KF40-F1517/KH40-H1517 [11]	NF40/KF40-F1517 [12] [13]	RF40-F1517	H40-H1517	RF43-F1760	NF45-F1932 [11]	F45-F1932	RH43-H1760
Stratix V GX devices											
A3	Yes	Yes	Yes	Yes							
A4		Yes	Yes	Yes							
A5		Yes	Yes	Yes	Yes				Yes		
A7		Yes	Yes	Yes	Yes				Yes		
A9				Yes					Yes		
AB				Yes					Yes		

(10) All devices in this column are in the HF35 package and have twenty-four 14.1-Gbps transceivers.

(11) Different devices within this column have small differences in the overall package height. When multiple Stratix V devices with different package heights are placed on a single board, a single-piece heatsink may not cover the devices evenly. Refer to *AN 670: Thermal Solutions to Address Height Variation in Stratix V Packages*.

(12) The 5SGTC5/7 devices in the KF40 package have four 28.05-Gbps transceivers and thirty-two 12.5-Gbps transceivers. Other devices in this column are in the NF40 package and have forty-eight 14.1-Gbps transceivers.

(13) For more information, refer to *AN 644: Migration Between Stratix V GX and Stratix V GT Devices*.

	Package										
B5						Yes		Yes			
B6						Yes		Yes			
B9											Yes
BB											Yes
Stratix V GT devices											
C5					Yes						
C7					Yes						
Stratix V GS devices											
D3	Yes	Yes									
D4	Yes	Yes		Yes							
D5		Yes		Yes							
D6				Yes					Yes		
D8				Yes					Yes		
Stratix V E devices											
E9							Yes			Yes	
EB							Yes			Yes	

Note: To verify the pin migration compatibility, use the Pin Migration View window in the Quartus II software Pin Planner.

Related Information

- **Altera Product Selector**
  Provides the latest information about Altera products.
- **For more information about verifying the pin migration compatibility, refer to the I/O Management chapter in volume 2 of the Quartus II Handbook.**
- **For full package details, refer to the Package information datasheet for Altera devices.**
- **AN 644: Migration Between Stratix V GX and Stratix V GT Devices**
- **AN 670: Thermal Solutions to Address Height Variation in Stratix V Packages**

Low-Power Serial Transceivers

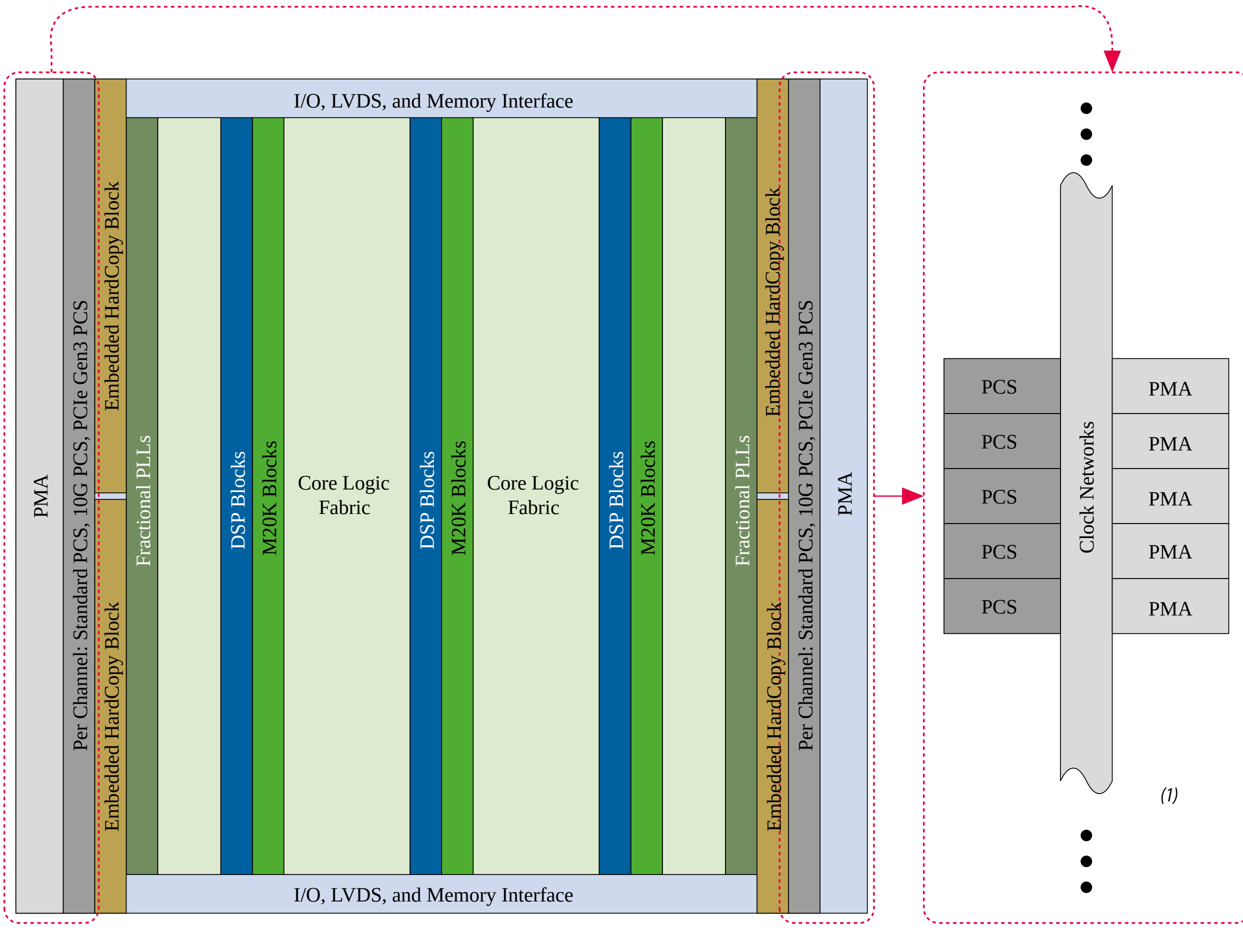
Stratix V FPGAs deliver the industry's most flexible transceivers with the highest bandwidth from 600 Mbps to 28.05 Gbps, low bit error ratio (BER), and low power. Stratix V transceivers have many enhancements to improve flexibility and robustness. These enhancements include robust analog receiver clock and data recovery (CDR), advanced pre-emphasis, and equalization. In addition, each channel provides full featured embedded PCS hard IP to simplify the design, lower the power, and save valuable core resources.

Stratix V transceivers are compliant with a wide range of standard protocols and data rates and are equipped with a variety of signal conditioning features to support backplane, optical module, and chip-to-chip applications.

Stratix V transceivers are located on the left and right sides of the device, as shown in the figure below. The transceivers are isolated from the rest of the chip to prevent core and I/O noise from coupling into the transceivers, thereby ensuring optimal signal integrity. The transceiver channels consist of the physical medium attachment (PMA), PCS, and high-speed clock networks. You can also configure unused transceiver PMA channels as additional transmitter PLLs.

Figure 1: Stratix V GT, GX, and GS Device Chip View

This figure represents one variant of a Stratix V device with transceivers. Other variants may have a different floorplan than the one shown here.



Note:
(1) You can use the unused transceiver channels as additional transceiver transmitter PLLs.

The following table lists the PMA features for the Stratix V transceivers.

Table 7: Transceiver PMA Features

Feature	Capability
Chip-to-chip support	28.05 Gbps and 12.5 Gbps (Stratix V GT devices) and 14.1 Gbps (Stratix V GX and GS devices)

Feature	Capability
Backplane support	12.5 Gbps (Stratix V GX, GS, and GT devices)
Cable driving support	PCIe cable and eSATA applications
Optical module support with EDC	10G Form-factor Pluggable (XFP), Small Form-factor Pluggable (SFP+), Quad Small Form-factor Pluggable (QSFP), CXP, 100G Pluggable (CFP), 100G Form-factor Pluggable
Continuous Time Linear Equalization (CTLE)	Receiver 4-stage linear equalization to support high-attenuation channels
Decision Feedback Equalization (DFE)	Receiver 5-tap digital equalizer to minimize losses and crosstalk
Adaptive equalization (AEQ)	Adaptive engine to automatically adjust equalization to compensate for changes over time
PLL-based clock recovery	Superior jitter tolerance versus phase interpolation techniques
Programmable deserialization and word alignment	Flexible deserialization width and configurable word alignment patterns
Transmitter equalization (pre-emphasis)	Transmitter driver 4-tap pre-emphasis and de-emphasis for protocol compliance under lossy conditions
Ring and LC oscillator transmitter PLLs	Choice of transmitter PLLs per channel, optimized for specific protocols and applications
On-chip instrumentation (EyeQ data-eye monitor)	Allows non-intrusive on-chip monitoring of both width and height of the data eye
Dynamic reconfiguration	Allows reconfiguration of single channels without affecting operation of other channels
Protocol support	Compliance with over 50 industry standard protocols in the range of 600 Mbps to 28.05 Gbps

The Stratix V core logic connects to the PCS through an 8-, 10-, 16-, 20-, 32-, 40-, 64-, or 66-bit interface, depending on the transceiver data rate and protocol. Stratix V devices contain PCS hard IP to support PCIe Gen3, Gen2, Gen1, Interlaken, 10GE, XAUI, GbE, SRIO, CPRI, and GPON protocols. All other standard and proprietary protocols are supported through the transceiver PCS hard IP. The following table lists the transceiver PCS features.

Table 8: Transceiver PCS Features

Protocol	Data Rates (Gbps)	Transmitter Data Path	Receiver Data Path
Custom PHY	0.6 to 8.5	Phase compensation FIFO, byte serializer, 8B/10B encoder, bit-slip, and channel bonding	Word aligner, de-skew FIFO, rate match FIFO, 8B/10B decoder, byte deserializer, and byte ordering
Custom 10G PHY	9.98 to 14.1	TX FIFO, gear box, and bit-slip	RX FIFO and gear box
x1, x4, x8 PCIe Gen1 and Gen2	2.5 and 5.0	Same as custom PHY plus PIPE 2.0 interface to core logic	Same as custom PHY plus PIPE 2.0 interface to core logic
x1, x4, x8 PCIe Gen3	8	Phase compensation FIFO, encoder, scrambler, gear box, and bit-slip	Block synchronization, rate match FIFO, decoder, de-scrambler, and phase compensation FIFO
10G Ethernet	10.3125	TX FIFO, 64/66 encoder, scrambler, and gear box	RX FIFO, 64/66 decoder, de-scrambler, block synchro-nization, and gear box
Interlaken	4.9 to 14.1	TX FIFO, frame generator, CRC-32 generator, scrambler, disparity generator, and gear box	RX FIFO, frame generator, CRC-32 checker, frame decoder, descrambler, disparity checker, block synchronization, and gearbox
OTN 40 and 100	(4 +1) x 11.3	TX FIFO, channel bonding, and byte serializer	RX FIFO, lane deskew, and byte de-serializer
	(10 +1) x 11.3		
GbE	1.25	Same as custom PHY plus GbE state machine	Same as custom PHY plus GbE state machine
XAUI	3.125 to 4.25	Same as custom PHY plus XAUI state machine for bonding four channels	Same as custom PHY plus XAUI state machine for re-aligning four channels
SRIO	1.25 to 6.25	Same as custom PHY plus SRIO V2.1 compliant x2 and x4 channel bonding	Same as custom PHY plus SRIO V2.1compliant x2 and x4 deskew state machine
CPRI	0.6144 to 9.83	Same as custom PHY plus TX deterministic latency	Same as custom PHY plus RX deterministic latency
GPON	1.25, 2.5, and 10	Same as custom PHY	Same as custom PHY

PCIe Gen3, Gen2, and Gen1 Hard IP (Embedded HardCopy Block)

Stratix V devices have PCIe hard IP designed for performance, ease-of-use, and increased functionality. The PCIe hard IP consists of the PCS, data link, and transaction layers. The PCIe hard IP supports Gen3, Gen2, and Gen1 end point and root port up to x8 lane configurations.

The Stratix V PCIe hard IP operates independently from the core logic, which allows the PCIe link to wake up and complete link training in less than 100 ms while the Stratix V device completes loading the programming file for the rest of the FPGA. The PCIe hard IP also provides added functionality, which helps support emerging features such as Single Root I/O Virtualization (SR-IOV) or optional protocol extensions. In addition, the Stratix V device PCIe hard IP has improved end-to-end data path protection using ECC and enables device CvP.

In all Stratix V devices, the primary PCIe hard IP that supports CvP is always in the bottom left corner of the device (IOBANK_B0L) when viewing the die from the top.

External Memory and GPIO

Each Stratix V I/O block has a hard FIFO that improves the resynchronization margin as data is transferred from the external memory to the FPGA.

The hard FIFO also lowers PHY latency, resulting in higher random access performance. GPIOs include on-chip dynamic termination to reduce the number of external components and minimize reflections. On-package decoupling capacitors suppress noise on the power lines, which reduce noise coupling into the I/Os. Memory banks are isolated to prevent core noise from coupling to the output, thus reducing jitter and providing optimal signal integrity.

The external memory interface block uses advanced calibration algorithms to compensate for process, voltage and temperature (PVT) variations in the FPGA and external memory components. The advanced algorithms ensure maximum bandwidth and a robust timing margin across all conditions. Stratix V devices deliver a complete memory solution with the High Performance Memory Controller II (HPMC II) and UniPHY MegaCore® IP that simplifies a design for today's advanced memory modules. The following table lists external memory interface block performance.

Table 9: External Memory Interface Performance

The specifications listed in this table are performance targets. For a current achievable performance, use the *External Memory Interface Spec Estimator*.

Interface	Performance (MHz)
DDR3	933
DDR2	400
QDR II	350
QDR II+	550
RLDRAM II	533
RLDRAM III	800

Related Information

External Memory Interface Spec Estimator

Adaptive Logic Module

Stratix V devices use an improved ALM to implement logic functions more efficiently. The Stratix V ALM has eight inputs with a fracturable look-up table (LUT), two dedicated embedded adders, and four dedicated registers.

The Stratix V ALM has the following enhancements:

- Packs 6% more logic when compared with the ALM found in Stratix IV devices.
- Implements select 7-input LUT-based functions, all 6-input logic functions, and two independent functions consisting of smaller LUT sizes (such as two independent 4-input LUTs) to optimize core usage.
- Adds more registers (four registers per 8-input fracturable LUT). More registers allow Stratix V devices to maximize core performance at a higher core logic usage and provides easier timing closure for register-rich and heavily pipelined designs.

The Quartus II software leverages the Stratix V ALM logic structure to deliver the highest performance, optimal logic usage, and lowest compile times. The Quartus II software simplifies design re-use because it automatically maps legacy Stratix designs into the new Stratix V ALM architecture.

Clocking

The Stratix V device core clock network is designed to support 800-MHz fabric operations and 1,066-MHz and 1,600-Mbps external memory interfaces.

The clock network architecture is based on Altera's proven global, quadrant, and peripheral clock structure, which is supported by dedicated clock input pins and fractional clock synthesis PLLs. The Quartus II software identifies all unused sections of the clock network and powers them down, which reduces power consumption.

Fractional PLL

Stratix V devices contain up to 32 fractional PLLs.

You can use the fractional PLLs to reduce both the number of oscillators required on the board and the clock pins used in the FPGA by synthesizing multiple clock frequencies from a single reference clock source. In addition, you can use the fractional PLLs for clock network delay compensation, zero delay buffering, and transmitter clocking for transceivers. Fractional PLLs can be individually configured for integer mode or fractional mode with third-order delta-sigma modulation.

Embedded Memory

Stratix V devices contain two types of embedded memory blocks: MLAB (640-bit) and M20K (20-Kbit). MLAB blocks are ideal for wide and shallow memories. M20K blocks are useful for supporting larger memory configurations and include ECC.

Both types of memory blocks operate up to 600 MHz and can be configured to be a single- or dual-port RAM, FIFO, ROM, or shift register. These memory blocks are flexible and support a number of memory configurations, as shown in the following table.

Table 10: Embedded Memory Block Configuration

MLAB (640 Bits)	M20K (20,480 Bits)
32x20 64x10	512x40 1Kx20 2Kx10 4Kx5 8Kx2 16Kx1

The Quartus II software simplifies design re-use by automatically mapping memory blocks from legacy Stratix devices into the Stratix V memory architecture.

Variable Precision DSP Block

Stratix V FPGAs feature the industry's first variable precision DSP block that you can configure to natively support signal processing with precision ranging from 9x9 to 36x36.

You can independently configure each DSP block at compile time as either a dual 18x18 multiply accumulate or a single 27x27 multiply accumulate. With a dedicated 64-bit cascade bus, you can cascade multiple variable precision DSP blocks to implement even higher precision DSP functions efficiently. The following table describes how variable precision is accommodated within a DSP block or by using multiple blocks.

Table 11: Variable Precision DSP Block Configurations

Multiplier Size (bits)	DSP Block Resources	Expected Usage
9x9	1/3 of variable precision DSP block	Low precision fixed point
18x18	1/2 of variable precision DSP block	Medium precision fixed point
27x27	1 variable precision DSP block	High precision fixed or single precision floating point
36x36	2 variable precision DSP blocks	Very high precision fixed point

Complex multiplication is common in DSP algorithms. One of the most popular applications of complex multipliers is the fast Fourier transform (FFT) algorithm, which increases precision requirements on only one side of the multiplier. The variable precision DSP block is designed to support the FFT algorithm with a proportional increase in DSP resources with precision growth. The following table lists complex multiplication with variable precision DSP blocks.

Table 12: Complex Multiplication with Variable Precision DSP Blocks

Multiplier Size (bits)	DSP Block Resources	Expected Usage
18x18	2 variable precision DSP blocks	Resource optimized FFTs
18x25	3 variable precision DSP blocks	Accommodate bit growth through FFT stages
18x36	4 variable precision DSP blocks	Highest precision FFT stages
27x27	4 variable precision DSP blocks	Single precision floating point

For FFT applications with high dynamic range requirements, only the Altera® FFT MegaCore offers an option of single precision floating point implementation, with the resource usage and performance similar to high-precision fixed point implementations.

Other new features include:

- 64-bit accumulator, the largest in the industry
- Hard pre-adder, available in both 18- and 27-bit modes
- Cascaded output adders for efficient systolic FIR filters
- Internal coefficient register banks
- Enhanced independent multiplier operation
- Efficient support for single- and double-precision floating point arithmetic
- Ability to infer all the DSP block modes through HDL code using the Altera Complete Design Suite

The variable precision DSP block is ideal for higher bit precision in high-performance DSP applications. At the same time, the variable precision DSP block can efficiently support the many existing 18-bit DSP applications, such as high definition video processing and remote radio heads. Stratix V FPGAs, with the variable precision DSP block architecture, are the only FPGA family that can efficiently support many different precision levels, up to and including floating point implementations. This flexibility results in increased system performance, reduced power consumption, and reduced architecture constraints for system algorithm designers.

Power Management

Stratix V devices leverage FPGA architectural features and process technology advancements to reduce total power consumption by up to 30% when compared with Stratix IV devices at the same performance level.

Stratix V devices continue to provide programmable power technology, introduced in earlier generations of Stratix FPGA families. The Quartus II software PowerPlay feature identifies critical timing paths in a design and biases core logic in that path for high performance. PowerPlay also identifies non-critical timing paths and biases core logic in that path for low power instead of high performance. PowerPlay automatically biases core logic to meet performance and optimize power consumption.

Additionally, Stratix V devices have a number of hard IP blocks that reduce logic resources and deliver substantial power savings when compared with soft implementations. The list includes PCIe Gen1/Gen2/Gen3, Interlaken PCS, hard I/O FIFOs, and transceivers. Hard IP blocks consume up to 50% less power than equivalent soft implementations.

Stratix V transceivers are designed for power efficiency. The transceiver channels consume 50% less power than Stratix IV FPGAs. The transceiver PMA consumes approximately 90 mW at 6.5 Gbps and 170 mW at 12.5 Gbps.

Incremental Compilation

The Quartus II software incremental compilation feature reduces compilation time by up to 70% and preserves performance to ease timing closure.

Incremental compilation supports top-down, bottom-up, and team-based design flows. Incremental compilation facilitates modular hierarchical and team-based design flows where a team of designers work in parallel on a design. Different designers or IP providers can develop and optimize different blocks of the design independently, which you can then import into the top-level project.

Enhanced Configuration and CvP

Stratix V device configuration is enhanced for ease-of-use, speed, and cost.

Stratix V devices support a new 4-bit bus active serial mode (ASx4). ASx4 supports up to a 400Mbps data rate using small low-cost quad interface Flash devices. ASx4 mode is easy to use and offers an ideal balance between cost and speed. Finally, the fast passive parallel (FPP) interface is enhanced to support 8-, 16-, and 32-bit data widths to meet a wide range of performance and cost goals.

You can configure Stratix V FPGAs using CvP with PCIe. CvP with PCIe divides the configuration process into two parts: the PCIe hard IP and periphery and the core logic fabric. CvP uses a much smaller amount of external memory (flash or ROM) because CvP has to store only the configuration file for the PCIe hard IP and periphery. The 100-ms power-up to active time (for PCIe) is much easier to achieve when only the PCIe hard IP and periphery are loaded. After the PCIe hard IP and periphery are loaded and the root port is booted up, application software running on the root port can send the configuration file for the FPGA fabric across the PCIe link where the file is loaded into the FPGA. The FPGA is then fully configured and functional.

The following table lists the configuration modes available for Stratix V devices.

Table 13: Configuration Modes for Stratix V Devices

Mode	Fast or Slow POR	Compression	Encryption	Remote Update	Data Width	Max Clock Rate (MHz)	Max Data Rate (Mbps)
Active Serial (AS)	Yes	Yes	Yes	Yes	1, 4	100	400
Passive Serial (PS)	Yes	Yes	Yes	—	1	125	125
Fast Passive Parallel (FPP)	Yes	Yes	Yes	Yes [14]	8, 16, 32	125 [15]	3,000

(14) Remote update support with the Parallel Flash Loader.
(15) The maximum clock rate is 125 MHz for x8 and x16 FPP, but only 100 MHz for x32 FPP.

Mode	Fast or Slow POR	Compres-sion	Encryption	Remote Update	Data Width	Max Clock Rate (MHz)	Max Data Rate (Mbps)
CvP	—	—	Yes	Yes	1, 2, 4, 8	—	3,000
Partial Reconfigura-tion	—	—	Yes	Yes	16	125	2,000
JTAG	—	—	—	—	1	33	33

Partial Reconfiguration

Partial reconfiguration allows you to reconfigure part of the FPGA while other sections continue to operate.

This capability is required in systems where uptime is critical because partial reconfiguration allows you to make updates or adjust functionality without disrupting services. While lowering power and cost, partial reconfiguration also increases the effective logic density by removing the necessity to place FPGA functions that do not operate simultaneously. Instead, you can store these functions in external memory and load them as required. This capability reduces the size of the FPGA by allowing multiple applications on a single FPGA, saving board space and reducing power.

You no longer need to know all the details of the FPGA architecture to perform partial reconfiguration. Altera simplifies the process by extending the power of incremental compilation used in earlier versions of the Quartus II software.

Partial reconfiguration is supported in the following configurations:

- Partial reconfiguration through the FPP x16 I/O interface
- CvP
- Soft internal core, such as the Nios® II processor.

Automatic Single Event Upset Error Detection and Correction

Stratix V devices offer single event upset (SEU) error detection and correction circuitry that is robust and easy to use.

The correction circuitry includes protection for configuration RAM (CRAM) programming bits and user memories. The CRAM is protected by a continuously running cyclical redundancy check (CRC) error detection circuit with integrated ECC that automatically corrects one or double-adjacent bit errors and detects higher order multi-bit errors. When more than two errors occur, correction is available through a core programming file reload that refreshes a design while the FPGA is operating.

The physical layout of the FPGA is optimized to make the majority of multi-bit upsets appear as independent single- or double-adjacent bit errors, which are automatically corrected by the integrated CRAM ECC circuitry. In addition to the CRAM protection in Stratix V devices, user memories include integrated ECC circuitry and are layout-optimized to enable error detection of 3-bit errors and correction for 2-bit errors.

Document Revision History

Table 14: Document Revision History

Date	Version	Changes Made
October 2015	2015.10.01	Changed heading in the "Ordering Information for Stratix V Devices" figure to "Embedded Hard IP Block Variant".
January 2015	2015.01.15	• Added ALM counts and device package sizes to the four device family features tables. • In the "Stratix V GX Device Features" table, changed the number of DDR3 SDRAM x72 DIMM Interfaces for the 5SGXA3 and 5SGXA4 devices to 6. Also added footnote to this row. • Deleted listings for 40GBASE-R and 100GBASE-R Ethernet from the "Transceiver PCS Features" table in the "Low-Power Serial Transceivers" section. • Added YY code to the Optional Suffix category in the "Ordering Information for Stratix V Devices" figure.
April 2014	2014.04.08	Updated "Variable precision DSP blocks" section of the "Features Summary" table to 600 MHz performance.
April 2014	2014.04.03	• Updated GPIOs section of the "Features Summary" table to 1.6 Gbps LVDS. • Changed clocking speed to 800 MHz in the "Features Summary" and the "Clocking" sections.
January 2014	2014.01.10	• Added link to Altera Product Selector in the "Stratix V Family Plan" section. • Corrected DDR2 performance from 533 MHz to 400 MHz. • Updated "Device Migration List Across All Stratix V Device Variants" table.
May 2013	2013.05.06	• Added link to the known document issues in the Knowledge Base. • Updated backplane support information. • Added a note about the number of I/Os to each table in the "Stratix V Family Plan" section. • Updated the "Ordering Information for Stratix V Devices" figure.
December 2012	3.1	• Updated Table 6 and Table 13. • Updated Figure 2.

Date	Version	Changes Made
June 2012	3.0	• Converted chapter to stand-alone format and removed from the Stratix V handbook. • Changed title of document to Stratix V Device Overview • Updated Figure 1. • Minor text edits.
February 2012	2.3	• Updated Table 1–2, Table 1–3, Table 1–4, and Table 1–5. • Updated Figure 1–2. • Updated "Automatic Single Event Upset Error Detection and Correction" on page 18. • Minor text edits.
December 2011	2.2	Updated Table 1–2 and Table 1–3.
November 2011	2.1	• Changed Stratix V GT transceiver speed from 28 Gbps to 28.05 Gbps. • Updated Figure 1–2.
November 2011	2.0	• Revised Figure 1–2. • Updated Table 1–5. • Minor text edits.
September 2011	1.10	Updated Table 1–2, Table 1–3, and Table 1–4.
September 2011	1.9	• Updated Table 1–1, Table 1–2, Table 1–3, Table 1–4, and Table 1–5. • Updated Figure 1–2. • Minor text edits.
June 2011	1.8	Changed 800 MHz to 1,066 MHz for DDR3 in Table 1–8 and in text.
May 2011	1.7	• For Stratix V GT devices, changed 14.1 Gbps to 12.5 Gbps. • Changed Configuration via PCIe to Configuration via Protocol • Updated Table 1–1, Table 1–2, Table 1–3, Table 1–4, Table 1–5, and Table 1–6. • Chapter moved to Volume 1.
January 2011	1.6	• Added Stratix V GS information. • Updated tables listing device features. • Added device migration information. • Updated 12.5-Gbps transceivers to 14.1-Gbps transceivers
December 2010	1.5	Updated Table 1-1.

Date	Version	Changes Made
December 2010	1.4	• Updated Table 1-1. • Updated Figure 1-2. • Converted to the new template. • Minor text edits.
July 2010	1.3	Updated Table 1–5
July 2010	1.2	• Updated "Features Summary" on page 1–2 • Updated resource counts in Table 1–1 and Table 1–2 • Removed "Interlaken PCS Hard IP" and "10G Ethernet Hard IP" • Added "40G and 100G Ethernet Hard IP (Embedded HardCopy Block)" on page 1–7 • Added information about Configuration via PCIe • Added "Partial Reconfiguration" on page 1–12 • Added "Ordering Information" on page 1–14
May 2010	1.1	Updated part numbers in Table 1–1 and Table 1–2
April 2010	1.0	Initial release