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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	427200
Number of Logic Elements/Cells	1150000
Total RAM Bits	68857856
Number of I/O	600
Number of Gates	-
Voltage - Supply	0.87V ~ 0.93V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	1517-BBGA, FCBGA
Supplier Device Package	1517-FCBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/intel/10at115n2f40e2sges

Feature	Description
Low power serial transceivers	• Continuous operating range of 611 Mbps to 17.4 Gbps for Arria 10 GX devices • Continuous operating range of 611 Mbps to 28.05 Gbps for Arria 10 GT devices • Backplane support up to 16.0 Gbps for Arria 10 GX devices • Backplane support up to 17.4 Gbps for Arria 10 GT devices • Extended range down to 125 Mbps with oversampling • ATX transmit PLLs with user-configurable fractional synthesis capability • Electronic Dispersion Compensation (EDC) for XFP, SFP+, QSFP, and CFP optical module support • Adaptive linear and decision feedback equalization • Transmit pre-emphasis and de-emphasis • Dynamic partial reconfiguration of individual transceiver channels • On-chip instrumentation (EyeQ non-intrusive data eye monitoring)
General purpose I/Os	• 1.6 Gbps LVDS—every pair can be configured as an input or output • 1333 MHz/2666 Mbps DDR4 external memory interface • 1067 MHz/2133 Mbps DDR3 external memory interface • 1.2 V to 3.0 V single-ended LVCMOS/LVTTL interfacing • On-chip termination (OCT)
Embedded hard IP	• PCIe Gen1/Gen2/Gen3 complete protocol stack, x1/x2/x4/x8 end point and root port • DDR4/DDR3/DDR3L/DDR3U/RLDRAM 3/LPDDR3 hard memory controller (RLDRAM2/QDR II+ using soft memory controller) • Multiple hard IP instantiations in each device • Dual-core ARM Cortex-A9 processor (Arria 10 SX devices only)
Transceiver hard IP	• 10GBASE-KR/40GBASE-KR4 Forward Error Correction (FEC) • 10G Ethernet PCS • PCI Express PIPE interface • Interlaken PCS • Gigabit Ethernet PCS • Deterministic latency support for Common Public Radio Interface (CPRI) PCS • Fast lock-time support for Gigabit Passive Optical Networking (GPON) PCS • 8B/10B, 64B/66B, 64B/67B encoders and decoders • Custom mode support for proprietary protocols
Power management	• SmartVoltage ID • V_{CC} PowerManager • Low static power device options • Programmable Power Technology • Quartus® II integrated PowerPlay power analysis
High performance core fabric	• Enhanced adaptive logic module (ALM) with 4 registers • Improved multi-track routing architecture reduces congestion and improves compile times • Hierarchical core clocking architecture • Fine-grained partial reconfiguration

Feature	Description
Internal memory blocks	• M20K—20-Kbit with hard ECC support • MLAB—640-bit distributed LUTRAM
Variable precision DSP blocks	• Natively supports signal processing with precision ranging from 18x19 up to 54x54 • Native 27x27 multiply mode • 64-bit accumulator and cascade for systolic FIRs • Internal coefficient memory banks • Pre-adder/subtractor improves efficiency • Additional pipeline register increases performance and reduces power
Phase locked loops (PLL)	• Fractional synthesis PLLs (fPLL) support both fractional and integer modes • Fractional mode with third-order delta-sigma modulation • Precision frequency synthesis, clock delay compensation, zero delay buffering • Integer PLLs adjacent to general purpose I/Os, support external memory, and LVDS interfaces
Core clock networks	• 800 MHz fabric clocking • 667 MHz external memory interface clocking, supports 2666 Mbps DDR4 interface • 800 MHz LVDS interface clocking, supports 1600 Mbps LVDS interface • Global, regional, and peripheral clock networks • Unused clock trees powered down to reduce dynamic power
Configuration	• Serial and parallel flash interface • Configuration via protocol (CvP) using PCI Express Gen1/Gen2/Gen3 • Fine-grained partial reconfiguration of core fabric • Dynamic reconfiguration of transceivers and PLLs • 256-bit AES bitstream encryption design security with authentication • Tamper protection
Packaging	• Multiple devices with identical package footprints allows seamless migration across different FPGA densities • Devices with compatible package footprints allows migration to next generation high-end Stratix® 10 devices • 1.0 mm ball-pitch FBGA packaging • Lead and lead-free package options
Software and tools	• Quartus II design suite • Transceiver toolkit • Qsys system integration tool • DSP Builder advanced blockset • OpenCL™ support • SoC Embedded Design Suite (EDS)

Feature	Description

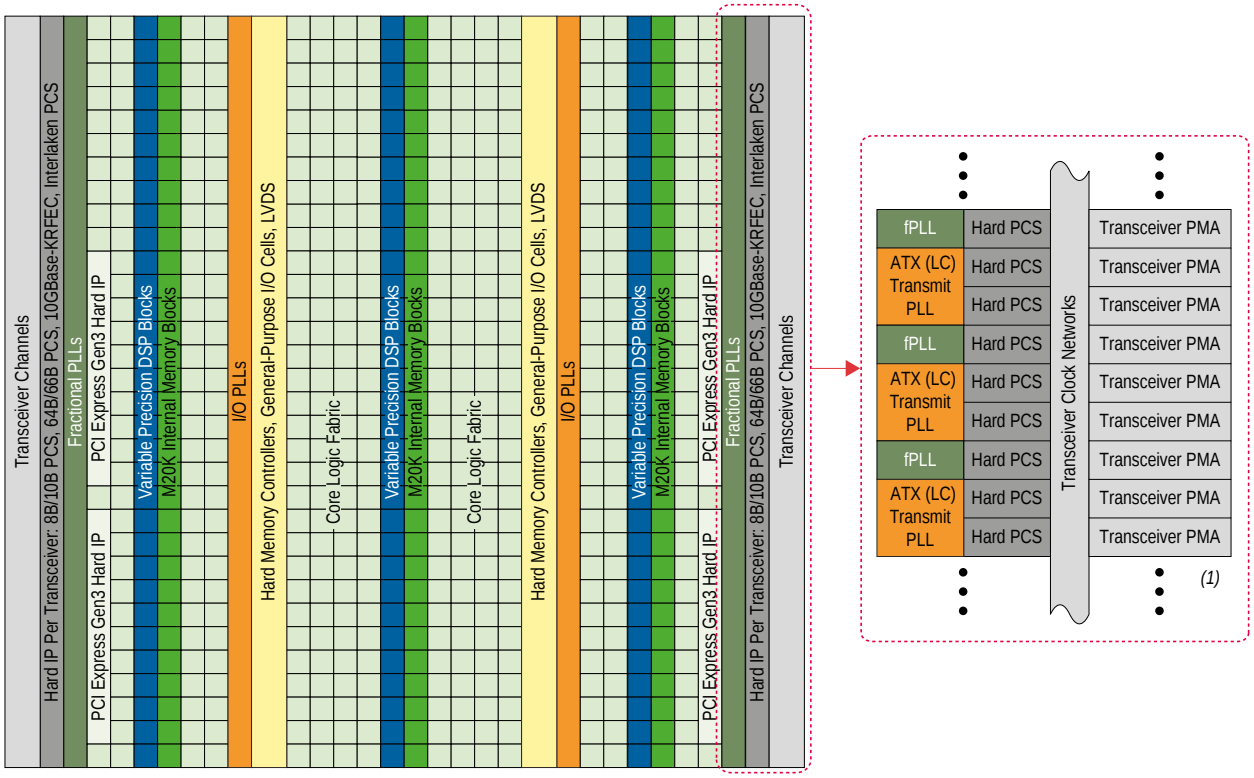
External Memory Interface for HPS	• Hard memory controller with support for DDR4, DDR3, DDR2, LPDDR2
	  • 40-bit (32-bit + 8-bit ECC) with select packages supporting 72-bit (64-bit + 8-bit ECC)
	  • Support for up to 2666 Mbps DDR4 and 2166 Mbps DDR3 frequencies
	  • Error correction code (ECC) support including calculation, error correction, write-back correction, and error counters
	  • Software Configurable Priority Scheduling on individual SDRAM bursts ECC
	  • Fully programmable timing parameter support for all JEDEC specified timing parameters
	  • AXI® Quality of Service (QoS) support for interface to logic core
	  • Multiport front-end (MPFE) scheduler interface to hard memory controller
	• Queued serial peripheral interface (QSPI) flash controller allows port sharing of hard memory controller between CPU and logic core
	  • Single I/O (SIO), Dual I/O (DIO), and Quad I/O (QIO) SPI Flash support
	  • Support for up to 108 MHz for flash frequency
	• NAND flash controller
	  • ONFI 1.0 or later
	  • Integrated descriptor based with DMA
	  • New command DMA to offload CPU for fast power down recovery
	  • Programmable hardware ECC support
	  • Updated to support 8 and 16 bit Flash devices
	  • Support for 50 MHz flash frequency
	• Secure Digital SD/SDIO/MMC controller
	  • eMMC 4.5
	  • Integrated descriptor based DMA
	  • CE-ATA digital commands supported
	  • 50 MHz operating frequency
	• Direct memory access (DMA) controller
	  • 8-channel
	  • Supports up to 32 peripheral handshake interface

Feature	Description

Interconnect to Logic Core	• High-performance ARM AMBA® AXI bus bridges
	  • AMBA AXI-3 compliant
	  • Allows both independent and tightly coupled operation between HPS and logic core
	  • Support simultaneous read and write transactions
	• FPGA-to-HPS Bridge
	  • Allows IP bus masters in the logic core to access to HPS bus slaves
	  • Configurable 32-, 64-, or 128-bit AMBA AXI interface
	  • Up to three masters within the core fabric can share the HPS SDRAM controller with the processor
	• HPS-to-FPGA Bridge
	  • Allows HPS bus masters to access bus slaves in core fabric
	  • Configurable 32-, 6-4, or 128-bit Avalon®/AMBA AXI interface allows high-bandwidth HPS master transactions to logic core
	• Configuration Bridge
	  • Allows configuration manager in HPS to configure the logic core under program control via dedicated 32-bit configuration port
	• Light Weight HPS-to-FPGA Bridge
	  • Light weight 32-bit AXI interface suitable for low-latency register accesses from HPS to soft peripherals in logic core
	• FPGA-to-HPS SDRAM controller Bridge
	  • Up to three masters (command ports), 3x 64-bit read data ports, and 3x 64-bit write data ports

Arria 10 Block Diagrams

Figure 2: Arria 10 FPGA Architecture Block Diagram



Note:
(1) Unused transceiver channels can be used as additional transceiver transmit PLLs

Arria 10 SoC Family Plan

Table 7: Arria 10 SX SoC Family Features

SoC Subsystem	Feature	Available in all Arria 10 SoC Devices
Hard Processor System	Central processing unit (CPU) core	Dual-core ARM Cortex-A9 MPCore processor with ARM CoreSight debug and trace technology
	Co-processors	Vector Floating-point unit (VFPU) single and double precision, ARM NEON media processing engine for each processor Snoop control unit (SCU), Acceleration coherency port (ACP)
	Layer 1 Cache	32 KB L1 instruction cache, 32 KB L1 data cache
	Layer 2 Cache	512 KB Shared L2 Cache
	On-Chip Memory	256 KB On-Chip RAM, 64 KB On-chip ROM
	Direct memory access (DMA) controller	8-Channel DMA
	Ethernet media access controller (EMAC)	Three 10/100/1000 EMAC with integrated DMA
	USB On-The-Go controller (OTG)	2 USB OTG with integrated DMA
	UART controller	2 UART 16550 compatible
	Serial Peripheral Interface (SPI) controller	4 SPI
	I^2C controller	5 I^2C controllers
	QSPI flash controller	1 SIO, DIO, QIO SPI flash supported
	SD/SDIO/MMC controller	1 eMMC 4.5 with DMA and CE-ATA support
	NAND flash controller	1 ONFI 1.0 or later 8 and 16 bit support
	General-purpose I/O (GPIO)	Maximum of 62 software programmable GPIO
	Timers	7 general-purpose timers, 4 watchdog timers
	Security	Secure boot, Advanced Encryption Standard (AES) and authentication (SHA)
External Memory Interface	External Memory Interface	Hard Memory Controller with DDR4 and DDR3

Table 8: Arria 10 SX SoC Family Plan

Device Name [10]	Logic Elements (KLE)	Registers	M20K Blocks	M20K Mbits	MLAB Counts	MLAB Mbits	18x19 Multipliers [11]	Maximum GPIOs	Maximum XCVR (17.4G, 28.05G)	fPLLs	I/O PLLs	PCIe HIPs
SX 160 (10AS016)	160	246,040	440	9	1,680	1	312	288	12, 0	6	6	1
SX 220 (10AS022)	220	326,040	583	11	2,227	1	384	288	12, 0	6	6	1
SX 270 (10AS027)	270	406,480	750	15	3,968	2	1,660	384	24, 0	8	8	2
SX 320 (10AS032)	320	478,640	891	17	4,673	3	1,970	384	24, 0	8	8	2
SX 480 (10AS048)	480	730,880	1,438	28	7,137	4	2,736	492	36, 0	12	12	2
SX 570 (10AS057)	570	868,320	1,800	35	8,241	5	3,046	588	48, 0	16	16	2
SX 660 (10AS066)	660	1,005,800	2,133	42	9,345	6	3,356	588	48, 0	16	16	2

(10) The text in parentheses is the part number reference for this device.
(11) The number of 27x27 multipliers is one-half the number of 18x19 multipliers.

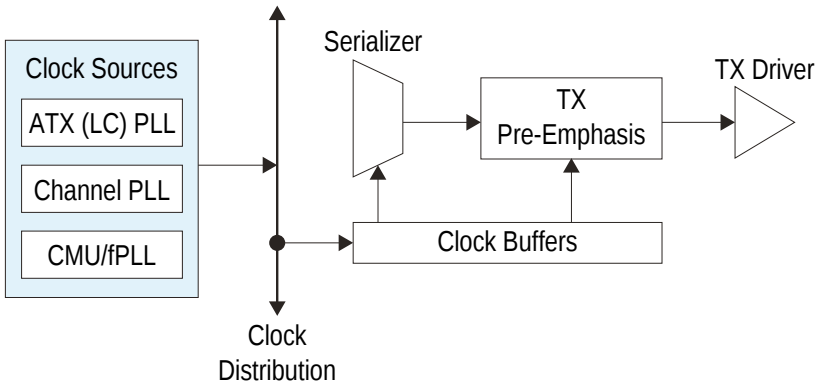
PMA Features

PMA channels are comprised of transmitter (TX), receiver (RX), and high speed clocking resources.

Arria 10 TX features provide exceptional signal integrity at data rates up to 28.05 Gbps. Clocking options include ultra-low jitter ATX (inductor-capacitor) PLLs, channel PLLs, clock multiplier unit (CMU) PLLs, and fractional PLLs (fPLLs):

- ATX PLLs can be configured in integer mode, or optionally, in a new fractional frequency synthesis mode. Each ATX PLL spans the full frequency range of the supported data rate range providing a highly stable and flexible clock source with the lowest jitter.
- CMU PLLs have been enhanced to provide a master clock source within the transceiver bank.
- When not configured as a transceiver channel, select PMA channels can be optionally configured as ring oscillator-based channel PLLs to provide an additional flexible clock source.
- In addition, dedicated on-chip fractional PLLs (fPLLs) are available with precision frequency synthesis capabilities. fPLLs can be used to synthesize multiple clock frequencies from a single reference clock source and replace multiple reference oscillators for multi-protocol and multi-rate applications.

Figure 5: Arria 10 Transmitter Features



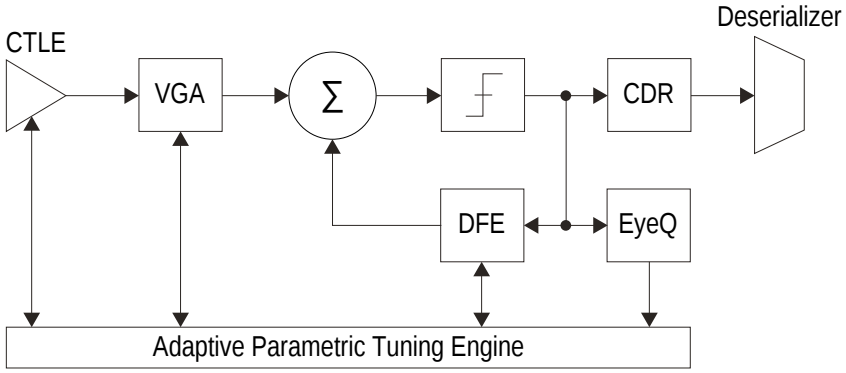
On the receiver side, each PMA channel has a dedicated, independent channel PLL for the CDR to provide the maximum number of clocking resources possible without compromising TX clocking sources. Up to 80 independent data rates can be configured on a single Arria 10 device.

Receiver side features provide unparalleled equalization capabilities to drive a wide range of transmission media with the widest range of protocols and data rates. Each receiver channel includes:

- Continuous Time Linear Equalizers (CTLE)—to compensate for channel losses with low power
- Variable Gain Amplifiers (VGA)—to optimize the receiver's dynamic range
- Decision Feedback Equalizers (DFE)—with 7-fixed taps and 4-floating taps to provide additional equalization capability on backplanes even in the presence of crosstalk and reflections

In addition, On-Die Instrumentation (ODI) provides on-chip eye monitoring capabilities (EyeQ). This capability helps to both optimize link equalization parameters during board bring-up and provide in-system link diagnostics. Combined with on-chip jitter injection capabilities, EyeQ provides powerful functionality to do in-system link equalization margin testing.

Figure 6: Arria 10 Receiver Block Features



All link equalization parameters feature automatic adaptation using the new Altera Digital Adaptive Parametric Tuning (ADAPT) block to dynamically set DFE tap weights, CTLE, VGA Gain, and threshold voltages. Finally, optimal and consistent signal integrity is ensured by using the new hardened Precision Signal Integrity Calibration Engine (PreSICE) to automatically calibrate all transceiver circuit blocks on power-up to give the most link margin and ensure robust, reliable, and error-free operation.

Table 10: Arria 10 Transceiver PMA Features

Feature	Capability
Chip-to-Chip Data Rates	125 Mbps to 17.4 Gbps (Arria 10 GX devices) 125 Mbps to 28.05 Gbps (Arria 10 GT devices)
Backplane Support	Drive backplanes at data rates up to 17.4 Gbps, including 10GBASE-KR compliance
Optical Module Support	SFP+/SFP, XFP, CXP, QSFP/QSFP28, CFP/CFP2/CFP4
Cable Driving Support	SFP+ Direct Attach, PCI Express over cable, eSATA
Transmit Pre-Emphasis	5-tap transmit pre-emphasis and de-emphasis to compensate for system channel loss
Continuous Time Linear Equalizer (CTLE)	Dual mode, high-gain, and high-data rate, linear receive equalization to compensate for system channel loss
Decision Feedback Equalizer (DFE)	7-fixed and 4-floating tap DFE to equalize backplane channel loss in the presence of crosstalk and noisy environments
Altera Digital Adaptive Parametric Tuning (ADAPT)	Fully digital adaptation engine to automatically adjust all link equalization parameters—including CTLE, DFE, and VGA blocks—that provide optimal link margin without intervention from user logic
Precision Signal Integrity Calibration Engine (PreSICE)	Hardened calibration controller to quickly calibrate all transceiver control parameters on power-up, which provides the optimal signal integrity and jitter performance
ATX Transmit PLLs	Low jitter ATX (inductor-capacitor) transmit PLLs with continuous tuning range to cover a wide range of standard and proprietary protocols

Feature	Capability
Fractional PLLs	On-chip fractional frequency synthesizers to replace on-board crystal oscillators and reduce system cost
Digitally Assisted Analog CDR	Superior jitter tolerance with fast lock time
On-Die Instrumentation— EyeQ and Jitter Margin Tool	Simplify board bring-up, debug, and diagnostics with non-intrusive, high-resolution eye monitoring (EyeQ). Also inject jitter from transmitter to test link margin in system.
Dynamic Partial Reconfiguration (DPRIO)	Allows for independent control of each transceiver channel Avalon memory-mapped interface for the most transceiver flexibility
Multiple PCS-PMA and PCS-PLD interface widths	8-, 10-, 16-, 20-, 32-, 40-, or 64-bit interface widths for flexibility of deserialization width, encoding, and reduced latency

PCS Features

Arria 10 PMA channels interface with core logic through configurable PCS interface layers.

Multiple gearbox implementations are available to decouple PCS and PMA interface widths. This feature provides the flexibility to implement a wide range of applications with 8-, 10-, 16-, 20-, 32-, 40-, or 64-bit interface widths. Arria 10 FPGAs contain PCS hard IP to support a wide range of standard and proprietary protocols.

The Standard PCS mode provides support for 8B/10B encoded applications up to 12.5 Gbps. The Enhanced PCS mode supports applications up to 17.4 Gbps. In addition, for highly customized implementations, a PCS Direct mode provides a fixed width interface up to 64 bits wide to core logic to allow for custom encoding including support for standards up to 28.05 Gbps.

The enhanced PCS includes an integrated 10GBASE-KR/40GBASE-KR4 Forward Error Correction (FEC) block.

The following table lists some of the key PCS features of Arria 10 transceivers that can be used in a wide range of standard and proprietary protocols from 125 Mbps to 28.05 Gbps.

Table 11: Arria 10 Transceiver PCS Features

PCS Protocol Support	Data Rate (Gbps)	Transmitter Data Path	Receiver Data Path
Standard PCS	0.125 to 12.5	Phase compensation FIFO, byte serializer, 8B/10B encoder, bit-slipper, channel bonding	Rate match FIFO, word-aligner, 8B/10B decoder, byte deserializer, byte ordering
PCI Express Gen1/Gen2 x1, x4, x8	2.5 and 5.0	Same as Standard PCS plus PIPE 2.0 interface to core	Same as Standard PCS plus PIPE 2.0 interface to core

PCS Protocol Support	Data Rate (Gbps)	Transmitter Data Path	Receiver Data Path
PCI Express Gen3 x1, x4, x8	8.0	Phase compensation FIFO, byte serializer, encoder, scrambler, bit-slipper, gear box, channel bonding, and PIPE 3.0 interface to core, auto speed negotiation	Rate match FIFO (0-600 ppm mode), word-aligner, decoder, descrambler, phase compensation FIFO, block sync, byte deserializer, byte ordering, PIPE 3.0 interface to core, auto speed negotiation
CPRI	0.6144 to 9.8	Same as Standard PCS plus deterministic latency serialization	Same as Standard PCS plus deterministic latency deserialization
Enhanced PCS	2.5 to 17.4	FIFO, channel bonding, bit-slipper, and gear box	FIFO, block sync, bit-slipper, and gear box
10GBASE-R	10.3125	FIFO, 64B/66B encoder, scrambler, FEC, and gear box	FIFO, 64B/66B decoder, descrambler, block sync, FEC, and gear box
Interlaken	4.9 to 17.4	FIFO, channel bonding, frame generator, CRC-32 generator, scrambler, disparity generator, bit-slipper, and gear box	FIFO, CRC-32 checker, frame sync, descrambler, disparity checker, block sync, and gear box
SFI-S/SFI-5.2	11.3	FIFO, channel bonding, bit-slipper, and gear box	FIFO, bit-slipper, and gear box
IEEE 1588	1.25 to 10.3125	FIFO (fixed latency), 64B/66B encoder, scrambler, and gear box	FIFO (fixed latency), 64B/66B decoder, descrambler, block sync, and gear box
SDI	up to 11.9	FIFO and gear box	FIFO, bit-slipper, and gear box
GigE	1.25	Same as Standard PCS plus GigE state machine	Same as Standard PCS plus GigE state machine
PCS Direct	up to 28.05	Custom	Custom

PCI Express Gen1/Gen2/Gen3 Hard IP

Arria 10 devices contain embedded PCI Express hard IP designed for performance, ease-of-use, and increased functionality.

The PCI Express hard IP consists of the PHY, Data Link, and Transaction layers, and supports PCI Express Gen1/Gen2/Gen3 end point and root port, in x1/x2/x4/x8 lane configurations. The PCI Express hard IP is capable of operating independently from the core logic. This feature allows the link to power up and complete link training in less than 100 ms, while the Arria 10 device completes loading the programming file for the rest of the FPGA. The hard IP also provides added functionality, which makes it easier to support emerging features such as Single Root I/O Virtualization (SR-IOV) and optional protocol extensions. The Arria 10 PCI Express hard IP has improved end-to-end data path protection using Error Checking and Correction (ECC). In addition, the hard IP supports configuration of the FPGA via protocol across the PCI Express bus at Gen1/Gen2/Gen3 rates (CvP using PCI Express).

Interface	Controller Type	Performance
DDR3	Hard	2133 Mbps
QDR II+ / II+ Xtreme	Soft	550 MTps
RLDRAM III	Hard	2400 Mbps
RLDRAM II	Soft	533 Mbps

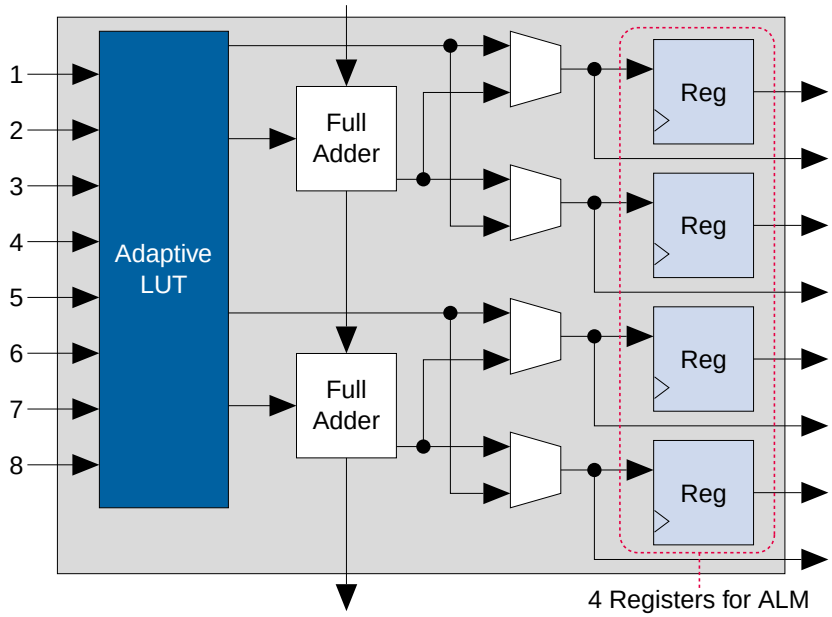
In addition to parallel memory interfaces, Arria 10 devices support serial memory technologies such as the Hybrid Memory Cube (HMC). The HMC is supported by the Arria 10 high-speed serial transceivers, which connect up to four HMC links, with each link running at data rates up to 15 Gbps.

Adaptive Logic Module (ALM)

Arria 10 devices use the same adaptive logic module (ALM) as the previous generation Arria V and Stratix V FPGAs, allowing for efficient implementation of logic functions and easy conversion of IP between the devices.

The ALM block diagram shown in the following figure has eight inputs with a fracturable look-up table (LUT), two dedicated embedded adders, and four dedicated registers.

Figure 7: Arria 10 FPGA and SoC ALM Block Diagram



Key features and capabilities of the Arria 10 ALM include:

- High register count with 4 registers per 8-input fracturable LUT enables Arria 10 devices to maximize core performance at higher core logic utilization
- 6% more logic compared to the traditional 2-register per LUT architecture
- Implements select 7-input logic functions, all 6-input logic functions, and two independent functions consisting of smaller LUT sizes (such as two independent 4-input LUTs) to optimize core logic utilization

Table 15: Complex Multiplication With Variable Precision DSP Block

Complex Multiplier Size	DSP Block Resources	FFT Usage
18x19 bits	2 Variable Precision DSP Blocks	Resource optimized FFTs
27x27 bits	4 Variable Precision DSP Blocks	Highest precision FFT stages and single precision floating point

For FFT applications with high dynamic range requirements, the Altera FFT MegaCore® function offers an option of single precision floating point implementation, with resource usage and performance similar to high precision fixed point implementations.

Other features of the DSP block include:

- Hard 18-bit and 25-bit pre-adders
- 64-bit dual accumulator (for separate I, Q product accumulations)
- Cascaded output adder chains for 18- and 27-bit FIR filters
- Embedded coefficient registers for 18- and 27-bit coefficients
- Fully independent multiplier outputs
- Inferability using HDL templates supplied by the Quartus II software for most modes

The Variable Precision DSP block is ideal to support the growing trend towards higher bit precision in high performance DSP applications. At the same time, it can efficiently support the many existing 18-bit DSP applications, such as high definition video processing and remote radio heads. Arria 10 devices, with the Variable Precision DSP block architecture, can efficiently support many different precision levels, up to and including floating point implementations. This flexibility can result in increased system performance, reduced power consumption, and reduce architecture constraints on system algorithm designers.

Hard Processor System (HPS)

The 20-nm HPS strikes a balance between enabling maximum software compatibility with 28-nm SoCs while still improving upon the 28-nm HPS architecture. These improvements address the requirements of the next generation target markets such as wireless and wireline communications, compute and storage equipment, broadcast and military in terms of performance, memory bandwidth, connectivity via backplane and security.

- Hard memory controller with support for DDR3, DDR4 and optional error correction code (ECC) support
- Multiport Front End (MPFE) Scheduler interface to the hard memory controller
- 8-channel direct memory access (DMA) controller
- QSPI flash controller with SIO, DIO, QIO SPI Flash support
- NAND flash controller (ONFI 1.0 or later) with DMA and ECC support, updated to support 8 and 16-bit Flash devices and new command DMA to offload CPU for fast power down recovery
- Updated SD/SDIO/MMC controller to eMMC 4.5 with DMA with CE-ATA digital command support
- 3 10/100/1000 Ethernet media access control (MAC) with DMA
- 2 USB On-the-Go (OTG) controller with DMA
- 5 I^2C controller (3 can be used by EMAC for MIO to external PHY)
- 2 UART 16550 Compatible
- 4 serial peripheral interface (SPI) (2 Master, 2 Slaves)
- 54 programmable general-purpose I/O (GPIO)
- 48 I/O direct share I/O allows HPS peripherals to connect directly to I/O
- 7 general-purpose timers
- 4 watchdog timers
- Anti-tamper, Secure Boot, Encryption (AES) and Authentication (SHA)

Key Features of 20-nm HPS

The following features are new in the 20-nm Hard Processor System compared to the 28-nm SoCs:

- **Increased Performance and Overdrive Capability**

  While the nominal processor frequency is 1.2 GHz, the 20 nm HPS offers an "overdrive" feature which enables an even higher processor operating frequency. For this a higher supply voltage value is required that is unique to the HPS and may require a separate regulator.

- **Increased Processor Memory Bandwidth and DDR4 Support**

  Up to 64-bit DDR4 memory @ 2666 Mbps is available for the processor. The hard memory controller for the HPS comprises a multi-port front end that manages connections to a single port memory controller. The multi-port front end allows logic core and the HPS share ports and thereby the available bandwidth of the memory controller.

- **Flexible I/O Sharing**

  An advanced I/O pin muxing scheme allows improved sharing of I/O between the HPS and the core logic. The following types of I/O are available for SoC:

  Dedicated I/O (15)—These I/Os are physically located inside the HPS block and are not accessible to logic within the core. The 15 dedicated I/Os are used for HPS clock, resets, and interfacing with boot devices, QSPI, and SD/MMC

  Direct Shared I/O (48)—These shared I/Os are located closest to the HPS block and are ideal for high speed HPS peripherals such as EMAC, USB, and others. There is one bank of 48 I/Os that supports direct sharing where the 48 I/Os can be shared 12 I/Os at a time.

  Standard (Shared) I/O (All other)—All standard I/Os can be shared by the HPS peripherals and any logic within the core. For designs where more than 48 I/Os are required to fully use all the peripherals in the HPS, these I/Os can be connected through the core logic.

- **EMAC Core**

  A third EMAC core is available in the HPS. Three EMAC cores enable an application to support two redundant Ethernet connections; for example, backplane, or two EMAC cores for managing IEEE 1588 time stamp information while allowing a third EMAC core for debug and configuration. All three EMACs can potentially share the same time stamps, simplifying the 1588 time stamping implementation. A new serial time stamp interface allows core logic to access and read the time stamp values. The integrated EMAC controllers can be connected to external Ethernet PHY through the provided MDIO or I^2C interface.

- **On-Chip Memory**

  The on-chip memory is updated to 256 KB support and can support larger data sets and real time algorithms

- **ECC Enhancements**

  Improvements in L2 Cache ECC management allow identification of errors down to the address level. ECC enhancements also enable improved error injection and status reporting via the introduction of new memory mapped access to syndrome and data signals.

- **HPS to FPGA Interconnect Backbone**

  Although the HPS and the Logic Core can operate independently, they are tightly coupled via a high-bandwidth system interconnect built from high-performance ARM AMBA AXI bus bridges. IP bus masters in the FPGA fabric have access to HPS bus slaves via the FPGA-to-HPS interconnect. Similarly, HPS bus masters have access to bus slaves in the core fabric via the HPS-to-FPGA bridge. Both bridges are AMBA AXI-3 compliant and support simultaneous read and write transactions. Up to three masters within the core fabric can share the HPS SDRAM controller with the processor. Additionally, the processor can be used to configure the core fabric under program control via a dedicated 32-bit configuration port.

- **HPS-to-FPGA**—configurable 32-, 64-, or 128-bit Avalon/AMBA AXI interface allows high bandwidth HPS master transactions to Logic Core
- **LW HPS-to-FPGA**—Light Weight 32-bit AXI interface suitable for low latency register accesses from HPS to soft peripherals in logic core
- **FPGA-to-HPS**—configurable 32-, 64-, or 128-bit AMBA AXI interface
- **FPGA-to-HPS SDRAM controller**—up to 3 masters (command ports), 3x 64-bit read data ports and 3x 64-bit write data ports
- **32-bit FPGA configuration manager**
- **Security**

A number of new security features have been introduced for anti-tamper management, secure boot, encryption (AES), and authentication (SHA).

Power Management

Arria 10 devices leverage the advanced 20 nm process technology, a low 0.9 V core power supply, an enhanced core architecture, and several optional power reduction techniques to reduce total power consumption by as much as 40% compared to Arria V devices and as much as 60% compared to Stratix V devices.

The optional power reduction techniques in Arria 10 devices include:

- **SmartVoltage ID**—a code is programmed into each device during manufacturing that allows a smart regulator to operate the device at lower core V_{CC} while maintaining performance
- **Programmable Power Technology**—non-critical timing paths are identified by the Quartus II software and the logic in these paths is biased for low power instead of high performance
- **V_{CC} PowerManager**—allows devices to be run at lower core voltage to trade performance for power savings
- **Low Static Power Options**—devices are available with either standard static power or low static power while maintaining performance

Furthermore, Arria 10 devices feature Altera's industry-leading low power transceivers and include a number of hard IP blocks that not only reduce logic resources but also deliver substantial power savings compared to soft implementations. In general, hard IP blocks consume up to 50% less power than the equivalent soft logic implementations.

Incremental Compilation

The Quartus II software incremental compilation feature reduces compilation time by up to 70% and preserves performance to ease timing closure.

Incremental compilation supports top-down, bottom-up, and team-based design flows. The incremental compilation feature facilitates modular hierarchical and team-based design flows where different designers compile their respective sections of a design in parallel. Furthermore, different designers or IP providers

can develop and optimize different blocks of the design independently. These blocks can then be imported into the top level project. The incremental compilation feature enables the partial reconfiguration flow for Arria 10 devices.

Configuration and Configuration via Protocol Using PCI Express

Arria 10 device configuration is improved for ease-of-use, speed, and cost. The devices can be configured through a variety of techniques such as active and passive serial, fast passive parallel, JTAG, and configuration via protocol using PCI Express including Gen3.

Configuration via protocol (CvP) using PCI Express allows the FPGA to be configured across the PCI Express bus, simplifying the board layout and increasing system integration. Making use of the embedded PCI Express hard IP, this technique allows the PCI Express bus to be powered up and active within the 100 ms time allowed by the PCI Express specification. Arria 10 devices also support partial reconfiguration across the PCI Express bus which reduces system down time by keeping the PCI Express link active while the device is being reconfigured.

Table 16: Arria 10 Device Configuration Modes

Mode	Compression	Encryption	Remote Update	Data Width (bits)	Maximum DCLK Rate (MHz)	Maximum Data Rate (Mbps)
Active Serial	Yes	Yes	Yes	1, 4	100	400
Passive Serial	Yes	Yes	—	1	125	125
Passive Parallel	Yes	Yes	Parallel flash loader	8, 16, 32	125	4000
Configuration via PCI Express	—	Yes	Yes	1, 2, 4, 8	—	4000
JTAG	—	—	—	1	33	33

Partial and Dynamic Reconfiguration

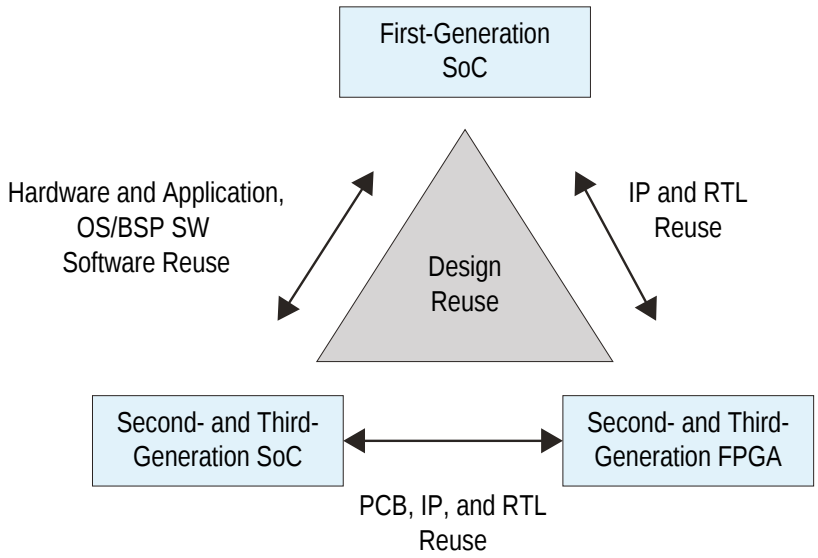
Partial reconfiguration allows you to reconfigure part of the FPGA while other sections continue running. This capability is required in systems where uptime is critical, because it allows you to make updates or adjust functionality without disrupting services.

In addition to lowering power and cost, partial reconfiguration also increases the effective logic density by removing the necessity to place in the FPGA those functions that do not operate simultaneously. Instead, these functions can be stored in external memory and loaded as needed. This reduces the size of the required FPGA by allowing multiple applications on a single FPGA, saving board space and reducing power. The partial reconfiguration process is built on top of the proven incremental compile design flow in the Quartus II design software.

Altera SoC: The Architecture of Choice When Productivity Matters

Productivity is the driving philosophy of Altera's Arria 10 SoC family. By reusing hardware, software, IP, and RTL across FPGAs and SoCs, you can reduce design effort and get products to market faster. The Dual Core ARM Cortex-A9 MPCore-based HPS is common to both 20- and 28-nm SoCs and facilitates extensive software code compatibility as well as tools and OS Board Support Package (BSP) reuse. The extensive tools and OS support available as part of Altera and ARM ecosystem and the fast iteration times inherent in software development (especially as compared to FPGA compile times) results in a highly productive embedded and DSP development flow. In addition, Altera offers high-level automated design flows for hardware development, such as the Altera OpenCL (a C-based hardware design flow) and DSP Builder (a model-based hardware design flow).

Figure 9: Hardware and Software Reuse



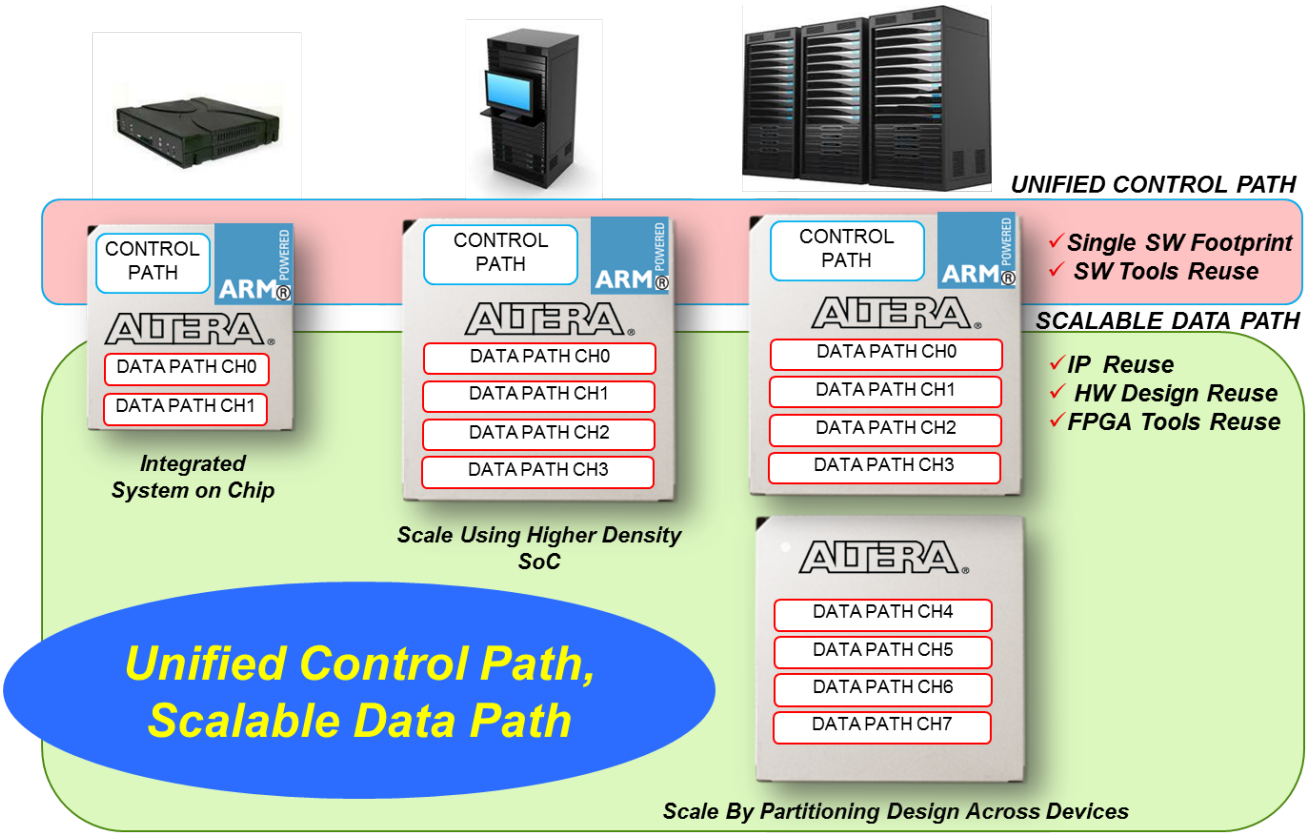
Altera's 20-nm SoCs and FPGAs can be reused in the following ways:

- **Application Code Reuse**: Because 28 nm and 20 nm SoCs share the same Dual Core ARM Cortex-A9 based HPS, any application code, board support packages, and ARM development tools developed for one SoC family can be reused with minimal design effort.
- **IP Reuse**: Arria 10 SoCs share the same core logic, memory, DSP, and I/O as Arria 10 FPGAs. Hardware intellectual property can be shared with minimal design effort. Altera also provides a fully tested and characterized portfolio of over 200 IP cores.
- **PCB Hardware Reuse**: Arria 10 SoCs are also package and footprint compatible with Arria 10 FPGAs, allowing hardware PCBs to be shared between the device categories.
- **Advanced Software Development Tools**:
  - The ecosystem that is available on ARM and the body of software packages, middleware available for operating systems that support ARM as well as the application development and debug tools available for ARM provides a familiar development environment to software developers.
  - Innovations such as Altera's Virtual Target technology allow functional testing of code without the need for hardware. By combining the most advanced multi-core debugger for ARM architectures with FPGA-adaptivity, the ARM DS-5 Altera Edition Toolkit provides embedded software developers an unprecedented level of full-chip visibility and control through the standard DS-5 user interface.
- **Advanced Hardware Development Tools**:
  - Altera's Quartus II software has faster compilation times than ever before. The Quartus II software's support for partial reconfiguration technology allows a single PCB to support multiple protocols by swapping protocols in the field.
  - QSys System Development framework allows rapid system integration of processor and peripherals and automates the process of generating AXI and Avalon based interconnect logic.
  - DSP Builder is a plug-in to MathWorks' Simulink that allows designers to develop DSP based filters, matrix operators and transforms using Model Based design flow and Advanced Blockset tools.
  - Open Computing Language (OpenCL) programming model with Altera's massively parallel FPGA architecture provides a powerful solution for system acceleration. The Altera SDK for OpenCL allows software developers to develop hardware using a C-based high-level design flow.

Single Platform of Devices that Offer Unified Control Path and Scalable Datapath

When you combine the SoC portfolio with the productivity benefits of design reuse in hardware and software, you get a benefit that is unique to Altera's technology. The result is an architecture that offers both unified control path and scalable data path.

Figure 10: Unified Control Path and Scalable Data Path



SoCs and FPGAs can be used across product platforms from low cost customer premise equipment to metro and access service provider equipment all the way to core and transmission equipment. For example, the low-cost Cyclone® V SoC offers a fully integrated system-on-a-chip device for the low end of a product portfolio that is ideal for customer premise, small cell routers, and enterprise routing. On the other end of the spectrum, Arria 10 and Stratix 10 SoCs offer performance and a high level of system integration on the high end of the product portfolio for access, networking, and transmission equipment.

Unified Control: Because all 28-nm and 20-nm SoCs feature a common Dual ARM Cortex-A9 based HPS, there is extensive software tool reuse, operating system board support packages (BSP) reuse and a high degree of software code compatibility across the devices and the end product portfolio.

Scalable Datapath: Altera's SoC offers a portfolio of devices that meet the price, power, performance, logic density, memory bandwidth, and transceiver bandwidth of an entire product portfolio. This scalability both simplifies the system architecture and enhances productivity through design reuse and protocol IP reuse.

Differentiation through Customization

Designers today can choose between many competing technologies: off the shelf processors, ASSPs, ASICs, and SoCs. Altera's SoCs stand out from these competing technologies because they allow maximum customization. Designers can implement their intellectual property in software running on the ARM or in hardware running on the programmable logic. The high speed serial I/O and memory interfaces allow a high degree of customization and flexibility. Designers can choose a standard protocol or memory standard or they can implement a custom protocol or memory controller and still use the embedded PHY circuitry to bypass the controller logic. Altera offers fully characterized turnkey IP cores for a number of communication