Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	427200
Number of Logic Elements/Cells	1150000
Total RAM Bits	68857856
Number of I/O	600
Number of Gates	-
Voltage - Supply	0.87V ~ 0.93V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	1517-BBGA, FCBGA
Supplier Device Package	1517-FCBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/intel/10at115n3f40e3sges

Feature	Arria V FPGAs and SoCs	Arria 10 FPGAs and SoCs
Logic density	504 KLE	1150 KLE
Embedded memory	34 Mbits	53 Mbits
18x19 multipliers	2186	3356
Maximum transceivers	36	96
Maximum transceiver data rate (chip to chip)	10.3125 Gbps	28.05 Gbps
Memory devices supported	DDR3 SDRAM @ 667 MHz/1333 Mbps	DDR4 SDRAM @ 1333 MHz/2666 Mbps DDR3 SDRAM @ 1067 MHz/2133 Mbps Hybrid Memory Cube (HMC)
Hard protocol IP	2 EMACs PCI Express Gen3 x8 (Arria V GZ) PCI Express Gen2 x4/Gen1 x8 (Arria V GX/GT/SX/ST)	3 EMACs PCI Express Gen3 x8 10GBASE-KR/40GBASE-KR4 FEC Interlaken PCS

These features result in the following improvements:

- **Improved Core Logic Performance**: Arria 10 devices offer over 60% improved core performance compared to the previous generation
- **Improved Processor Performance**: Arria 10 SoCs provide 87% improvement in processor performance
- **Improved Processor Power Efficiency**: At 20 nm, the Dual Core ARM Cortex-A9 Processor provides the best power efficiency for any GHz-class processor in the industry
- **Lower Power**: Arria 10 devices deliver up to 40% lower power compared to prior-generation mid-range FPGAs and SoCs, enabled by 20-nm process technology advancements and a variety of innovative power-management options
- **Higher Density**: Arria 10 devices provide a higher level of integration with up to 1150K logic elements (LEs), up to 53 Mbits of embedded memory, and over 3350 18x19 multipliers
- **Improved Transceiver Bandwidth**: Arria 10 devices support chip-to-chip rates up to 28 Gbps and backplane rates up to 17.4 Gbps
- **Improved Memory Bandwidth with DDR4 Support**: Arria 10 devices support DDR4 memory up to 1333 MHz/ 2666 Mbps and feature support for the emerging transceiver-based Hybrid Memory Cube (HMC)
- **Improved DSP Performance**: With over 1.0 TeraFLOPs of single-precision DSP performance, Arria 10 devices deliver a 4 times increase in DSP performance
- **Additional Protocol Support for Hard IP**: Arria 10 devices feature an advanced transceiver architecture with added hard IP support for PCIe Gen3, Interlaken PCS, and 10GBASE-KR/40GBASE-KR4 FEC

Target Markets for Arria 10 FPGAs and SoCs

Arria 10 devices meet the performance, power, and bandwidth requirements of next generation wireless infrastructure, broadcast, compute and storage, networking, and medical and military equipment.

By providing such a highly integrated device, Arria 10 FPGAs and SoCs significantly reduce BOM cost, form factor, and power consumption. Arria 10 devices allow you to differentiate your product through customization by implementing your intellectual property in both hardware and software.

For these applications, Arria 10 devices integrate both logic functions and processor functions in a highly integrated single device. The integrated ARM-based SoCs provide all the functionality of traditional FPGAs, eliminate the need for a local processor, and increase system performance by taking advantage of the tightly coupled high bandwidth interface between the core fabric and the hard processor system.

Figure 1: Arria 10 FPGA and SoC Applications

Wireless Infrastructure	Access, Metro & Core	Transmission	Cloud Servers and Storage	Broadcast
				
Target Applications				
• Remote Radio Head • Mobile Backhaul • Active Antenna • Basestation (BTS) • 4G/LTE Marco eNB • 4G/LTE Micro eNB	• 40G GPON, EPON, FFTH, Switch • 100G / 200G NGPON • 100G Traffic Management	• NX 100G OTU 4 • 2 X OTU 4 • 4 X OTU 4	• Flash Cache • Cloud • Server • Acceleration	• Pro A/V Equipment • Switcher • Server • Transport • Head End • VoD Mux
Logic Functions				
• RF Processing • Digital Pre-Distortion (DPD) • Baseband Interface	• Aggregation • Bridging • Switching • Traffic Management • I/O	• FEC • Aggregation • Muxponding • I/O	• Flash Cache Processing • Acceleration • SATA/SAS • PCIe Gen3	• Video Format Conversion • Muxing • Switching • Bridging
Processor Functions				
• OAM & Link • Digital Pre-Distortion (DPD) • L2 Switch • I/O, Protocol Control	• Host Offload • OAM & Link • L2 Switch • I/O, Protocol Control • Chassis Management	• Host Offload • OAM & Link • I/O Control • Chassis Management	• Flash Cache Control • Host Offload • Co-processing & Acceleration Control	• Audio Processing • Video Compression • Link Management

- For **Wireless infrastructure** particularly remote radio unit, the industry has standardized on ARM-based ASSPs and SoCs for several generations. ARM is widely recognized as the industry leader in low power solutions. At 20 nm, the Dual ARM Cortex MPCore provides the best power efficiency of any GHz class of process. When combined with Altera's industry leading programmable technology, this provides an ideal platform to address the performance, power, and form factor requirements of wireless remote radio unit and small cell base stations.
- For **Wireline communication equipment** such as access, metro, core, and transmission equipment where the FPGA performs critical functions such as protocol bridging, packet framing, aggregation, and I/O expansion, SoCs now offer all this as well as integrated intelligent control and link management, sometimes referred to as Operations, Administration, and Maintenance (OAM). OAM typically is software that executes when a link is established or fails during operation. The integrated ARM processor can also be used for statistics and error monitoring and minimize system downtime when a link is compromised or oversubscribed. Tight coupling of the processor and the data path (implemented in the core logic) saves time and results in significant savings in terms of operating expenses associated with system downtime and loss of quality of service.
- For **Compute and storage equipment**, flash cache storage, the integrated ARM processor can be used to manage Flash sectors and improve overall life and reliability as well as offload the host processor and provide control for search and hardware acceleration functions for cloud storage equipment. The integrated ARM based HPS can configure the hard PCIe interfaces in PCIe root port configuration and also run link layers for SAS and SATA interfaces.
- For **Next generation Broadcast equipment**, where "4K readiness" is the key technology driver, the integrated ARM processor subsystem eliminates the need for a local GHz class processor, which is commonly used for functions such as audio processing, video compression, video link management, and PCIe root port.
- For **Military** applications, new security features such as Secure Boot, Encryption, and Authentication have been introduced for secure wireless and wireline communications, military radar, military intelligence equipment.
- For **Test and Medical** applications, combining ARM HPS with support for high speed memory devices such as DDR4, and Hybrid Memory Cube (HMC) as well as high speed transceivers and embedded controllers such as PCIe Gen3, Arria 10 SoCs are ideal for next generation test and medical equipment.

FPGA and SoC Features Summary

Table 2: Arria 10 FPGA and SoC Common Device Features

Feature	Description
Technology	• 20-nm TSMC SoC process technology • 0.9 V standard V_{CC} core voltage

Table 3: Arria 10 SoC-Specific Device Features

Feature	Description

Dual-core ARM Cortex-A9 MPCore processor unit	• 2.5 MIPS/MHz instruction efficiency
	• CPU frequency 1.2 GHz with 1.5 GHz via overdrive
	  • At 1.5 GHz total performance of 7500 MIPS
	• ARMv7-A architecture
	  • Runs 32-bit ARM instructions
	  • 16-bit and 32-bit Thumb instructions for 30% reduction in memory footprint
	  • Jazelle® RCT execution architecture with 8-bit Java bytecodes
	  • Superscalar, variable length, out-of-order pipeline with dynamic branch prediction
	• ARM NEON™ media processing engine
	• Single- and double-precision floating-point unit
	• CoreSight™ debug and trace technology
	• Snoop Control Unit (SCU) and Acceleration Coherency Port (ACP)

Cache	• L1 Cache
	  • 32 KB of instruction cache
	  • 32 KB of L1 data cache
	  • Parity checking
	• L2 Cache
	  • 512 KB shared
	  • 8-way set associative
	  • SEU Protection with parity on TAG ram and ECC on data RAM
	  • Cache lockdown support

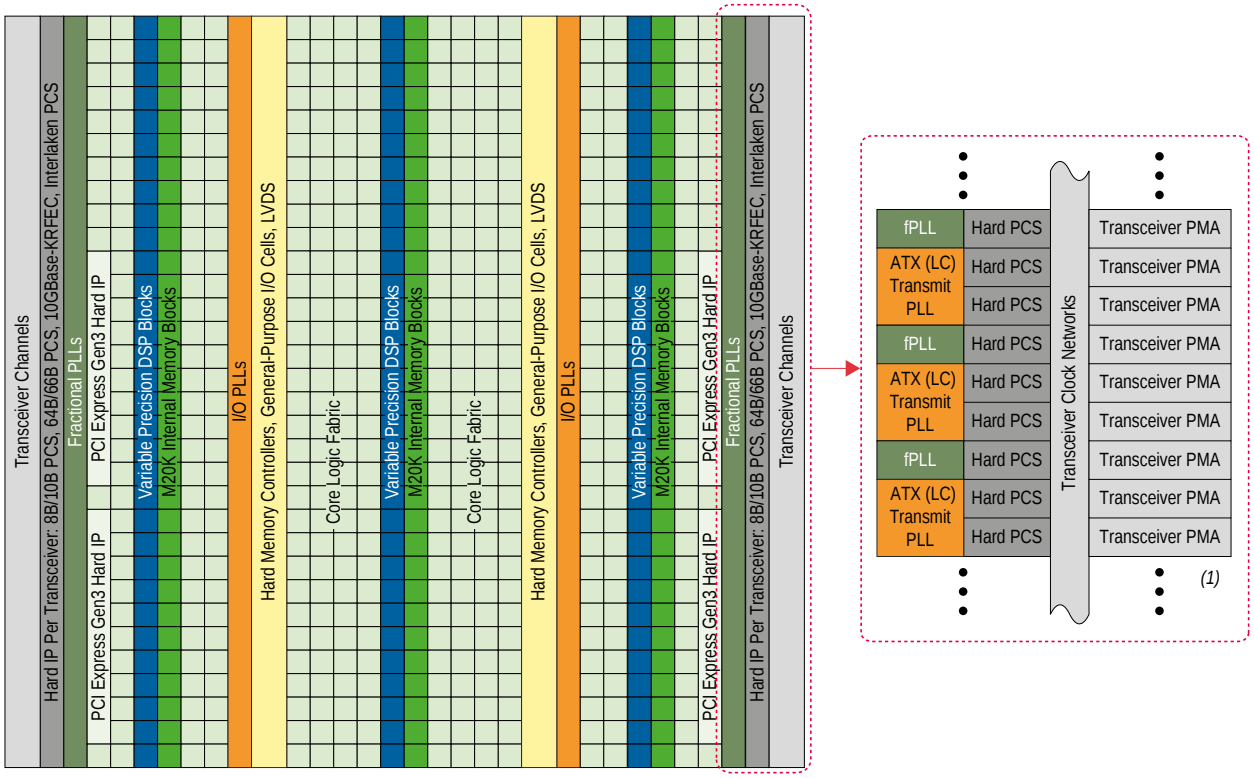
On-Chip Memory	• 256 KB of scratch on-chip RAM • 64 KB on-chip ROM

Feature	Description

Interconnect to Logic Core	• High-performance ARM AMBA® AXI bus bridges
	  • AMBA AXI-3 compliant
	  • Allows both independent and tightly coupled operation between HPS and logic core
	  • Support simultaneous read and write transactions
	• FPGA-to-HPS Bridge
	  • Allows IP bus masters in the logic core to access to HPS bus slaves
	  • Configurable 32-, 64-, or 128-bit AMBA AXI interface
	  • Up to three masters within the core fabric can share the HPS SDRAM controller with the processor
	• HPS-to-FPGA Bridge
	  • Allows HPS bus masters to access bus slaves in core fabric
	  • Configurable 32-, 6-4, or 128-bit Avalon®/AMBA AXI interface allows high-bandwidth HPS master transactions to logic core
	• Configuration Bridge
	  • Allows configuration manager in HPS to configure the logic core under program control via dedicated 32-bit configuration port
	• Light Weight HPS-to-FPGA Bridge
	  • Light weight 32-bit AXI interface suitable for low-latency register accesses from HPS to soft peripherals in logic core
	• FPGA-to-HPS SDRAM controller Bridge
	  • Up to three masters (command ports), 3x 64-bit read data ports, and 3x 64-bit write data ports

Arria 10 Block Diagrams

Figure 2: Arria 10 FPGA Architecture Block Diagram



Note:
(1) Unused transceiver channels can be used as additional transceiver transmit PLLs

Device Name [1]	Logic Elements (KLE)	Registers	M20K Blocks	M20K Mbits	MLAB Counts	MLAB Mbits	18x19 Multipliers [2]	Maximum GPIOs	Maximum XCVR (17.4G, 28.05G)	fPLLs	I/O PLLs	PCIe HIPs
GX 320 (10AX032)	320	478,640	891	17	4,673	3	1,970	384	24, 0	8	8	2
GX 480 (10AX048)	480	730,880	1,438	28	7,137	4	2,736	492	36, 0	12	12	2
GX 570 (10AX057)	570	868,320	1,800	35	8,241	5	3,046	588	48, 0	16	16	2
GX 660 (10AX066)	660	1,005,800	2,133	42	9,345	6	3,356	588	48, 0	16	16	2
GX 900 (10AX090)	900	1,358,480	2,423	47	15,080	9	3,036	768	96, 0	32	16	4
GX 1150 (10AX115)	1,150	1,710,800	2,713	53	20,814	13	3,036	768	96, 0	32	16	4
GT 900 (10AT090)	900	1,358,480	2,423	47	15,080	9	3,036	624	80, 16	32	16	4
GT 1150 (10AT115)	1,150	1,710,800	2,713	53	20,814	13	3,036	624	80, 16	32	16	4

Table 5: Arria 10 GX and Arria 10 GT FPGA Family Package Plan, part 1

Cell legend: General Purpose I/Os, High-Voltage I/Os, LVDS Pairs, Transceivers [3] [4] [5] [6] [7] [8]

Device [1]	U19 (U484) (19x19 mm^2)	F27 (F672) (27x27 mm^2)	F29 (F780) (29x29 mm^2)	F34 (F1152) (35x35 mm^2)	F35 (F1152) (35x35 mm^2) [9]	F36 (F1152) (35x35 mm^2) [9]
GX 160 (10AX016)	192,48,72,6	240,48,96,12	288,48,120,12	—	—	—

[3] All packages are ball grid arrays with 1.0 mm pitch, except for U19 (U484), which is 0.8 mm pitch.
[4] High-Voltage I/O pins are used for 3.3 V and 2.5 V interfacing.
[5] Each LVDS pair can be configured as either a differential input or a differential output.
[6] High-Voltage I/O pins and LVDS pairs are included in the General Purpose I/O count. Transceivers are counted separately.
[7] Each package column offers pin migration (common circuit board footprint) for all devices in the column.
[8] Arria 10 GX devices are pin migratable with Arria 10 GT devices in the same package.
[9] Devices in the F35 (F1152) package are pin migratable with devices in the F36 (F1152) package

Device [1]	U19 (U484) (19x19 mm^2)	F27 (F672) (27x27 mm^2)	F29 (F780) (29x29 mm^2)	F34 (F1152) (35x35 mm^2)	F35 (F1152) (35x35 mm^2) [9]	F36 (F1152) (35x35 mm^2) [9]
GX 220 (10AX022)	192,48,72,6	240,48,96,12	288,48,120,12	—	—	—
GX 270 (10AX027)	—	240,48,96,12	360,48,156,12	384,48,168,24	384,48,168,24	—
GX 320 (10AX032)	—	240,48,96,12	360,48,156,12	384,48,168,24	384,48,168,24	—
GX 480 (10AX048)	—	—	360,48,156,12	492,48,222,24	396,48,174,36	—
GX 570 (10AX057)	—	—	—	492,48,222,24	396,48,174,36	—
GX 660 (10AX066)	—	—	—	492,48,222,24	396,48,174,36	432,48,192,36
GX 900 (10AX090)	—	—	—	528,0,264,24	432,0,216,36	—
GX 1150 (10AX115)	—	—	—	528,0,264,24	432,0,216,36	—
GT 900 (10AT090)	—	—	—	—	—	—
GT 1150 (10AT115)	—	—	—	—	—	—

Table 6: Arria 10 GX and Arria 10 GT FPGA Family Package Plan, part 2

Cell legend: General Purpose I/Os, High-Voltage I/Os, LVDS Pairs, Transceivers [3] [4] [5] [6] [7] [8]

Device [1]	F40 (F1517) (40x40 mm^2)	F40 (F1517) (40x40 mm^2)	F45 (F1932) (45x45 mm^2)	F45 (F1932) (45x45 mm^2)	F45 (F1932) (45x45 mm^2)
GX 160 (10AX016)	—	—	—	—	—
GX 220 (10AX022)	—	—	—	—	—

Device [1]	F40 (F1517) (40x40 mm^2)	F40 (F1517) (40x40 mm^2)	F45 (F1932) (45x45 mm^2)	F45 (F1932) (45x45 mm^2)	F45 (F1932) (45x45 mm^2)
GX 270 (10AX027)	—	—	—	—	—
GX 320 (10AX032)	—	—	—	—	—
GX 480 (10AX048)	—	—	—	—	—
GX 570 (10AX057)	588,48,270,48	—	—	—	—
GX 660 (10AX066)	588,48,270,48	—	—	—	—
GX 900 (10AX090)	624,0,312,48	342,0,154,66	768,0,384,48	624,0,312,72	480,0,240,96
GX 1150 (10AX115)	624,0,312,48	342,0,154,66	768,0,384,48	624,0,312,72	480,0,240,96
GT 900 (10AT090)	624,0,312,48	—	—	624,0,312,72	480,0,240,96
GT 1150 (10AT115)	624,0,312,48	—	—	624,0,312,72	480,0,240,96

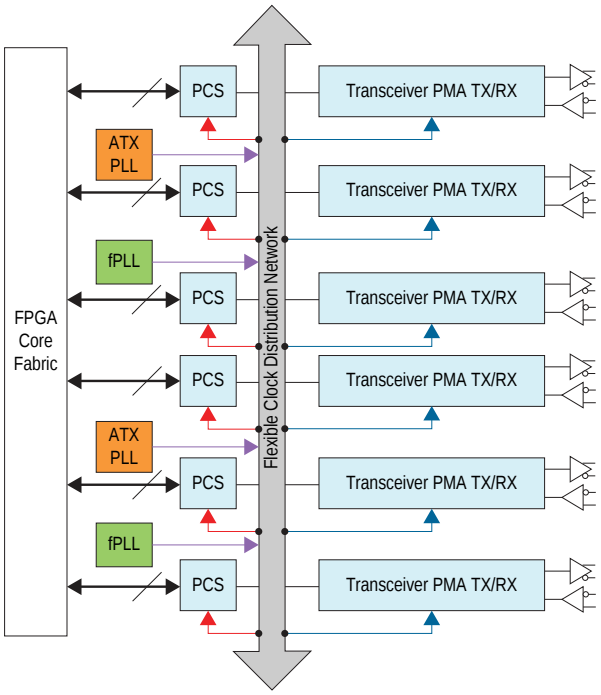
Arria 10 Low Power Serial Transceivers

Arria 10 FPGAs and SoCs provide the lowest power transceivers for applications where power efficiency is paramount, while still delivering high bandwidth, throughput, and low latency.

Arria 10 transceivers feature data rates from 125 Mbps to 28.05 Gbps for chip-to-chip and chip-to-module applications. In addition, for long reach and backplane applications, advanced adaptive equalization is available for driving backplanes at data rates up to 17.4 Gbps. Lower power modes are also available at data rates up to 11.3 Gbps for critical power sensitive designs.

The combination of 20 nm process technology and architectural advances provide a significant reduction of die area and power consumption. Arria 10 transceivers allow for up to a 2X increase in transceiver I/O density compared to previous generation devices while maintaining optimal signal integrity. Arria 10 devices offer up to 96 total transceiver channels. Up to 16 of these channels can be configured to run up to 28.05 Gbps to drive next generation 100G interfaces and CFP2/CFP4 optical modules. All channels feature continuous data rate support up to the maximum rated speed.

Figure 4: Arria 10 Transceiver Block Architecture

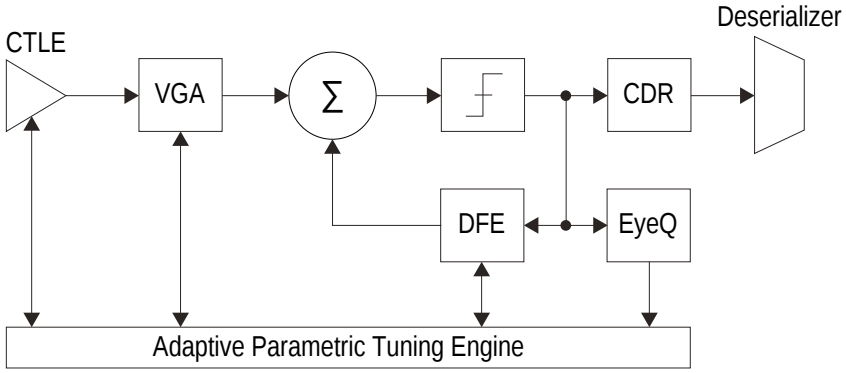


All transceiver channels feature a dedicated Physical Medium Attachment (PMA) and a hardened Physical Coding Sublayer (PCS).

- The PMA provides primary interfacing capabilities to physical channels.
- The PCS typically handles encoding/decoding, word alignment, and other pre-processing functions before transferring data to the FPGA core fabric.

Transceivers are segmented into blocks of six PMA-PCS groups. A wide variety of bonded and non-bonded data rate configurations are possible using a highly configurable clock distribution network. Up to 80 independent transceiver data rates can be configured.

Figure 6: Arria 10 Receiver Block Features



All link equalization parameters feature automatic adaptation using the new Altera Digital Adaptive Parametric Tuning (ADAPT) block to dynamically set DFE tap weights, CTLE, VGA Gain, and threshold voltages. Finally, optimal and consistent signal integrity is ensured by using the new hardened Precision Signal Integrity Calibration Engine (PreSICE) to automatically calibrate all transceiver circuit blocks on power-up to give the most link margin and ensure robust, reliable, and error-free operation.

Table 10: Arria 10 Transceiver PMA Features

Feature	Capability
Chip-to-Chip Data Rates	125 Mbps to 17.4 Gbps (Arria 10 GX devices) 125 Mbps to 28.05 Gbps (Arria 10 GT devices)
Backplane Support	Drive backplanes at data rates up to 17.4 Gbps, including 10GBASE-KR compliance
Optical Module Support	SFP+/SFP, XFP, CXP, QSFP/QSFP28, CFP/CFP2/CFP4
Cable Driving Support	SFP+ Direct Attach, PCI Express over cable, eSATA
Transmit Pre-Emphasis	5-tap transmit pre-emphasis and de-emphasis to compensate for system channel loss
Continuous Time Linear Equalizer (CTLE)	Dual mode, high-gain, and high-data rate, linear receive equalization to compensate for system channel loss
Decision Feedback Equalizer (DFE)	7-fixed and 4-floating tap DFE to equalize backplane channel loss in the presence of crosstalk and noisy environments
Altera Digital Adaptive Parametric Tuning (ADAPT)	Fully digital adaptation engine to automatically adjust all link equalization parameters—including CTLE, DFE, and VGA blocks—that provide optimal link margin without intervention from user logic
Precision Signal Integrity Calibration Engine (PreSICE)	Hardened calibration controller to quickly calibrate all transceiver control parameters on power-up, which provides the optimal signal integrity and jitter performance
ATX Transmit PLLs	Low jitter ATX (inductor-capacitor) transmit PLLs with continuous tuning range to cover a wide range of standard and proprietary protocols

Feature	Capability
Fractional PLLs	On-chip fractional frequency synthesizers to replace on-board crystal oscillators and reduce system cost
Digitally Assisted Analog CDR	Superior jitter tolerance with fast lock time
On-Die Instrumentation— EyeQ and Jitter Margin Tool	Simplify board bring-up, debug, and diagnostics with non-intrusive, high-resolution eye monitoring (EyeQ). Also inject jitter from transmitter to test link margin in system.
Dynamic Partial Reconfiguration (DPRIO)	Allows for independent control of each transceiver channel Avalon memory-mapped interface for the most transceiver flexibility
Multiple PCS-PMA and PCS-PLD interface widths	8-, 10-, 16-, 20-, 32-, 40-, or 64-bit interface widths for flexibility of deserialization width, encoding, and reduced latency

PCS Features

Arria 10 PMA channels interface with core logic through configurable PCS interface layers.

Multiple gearbox implementations are available to decouple PCS and PMA interface widths. This feature provides the flexibility to implement a wide range of applications with 8-, 10-, 16-, 20-, 32-, 40-, or 64-bit interface widths. Arria 10 FPGAs contain PCS hard IP to support a wide range of standard and proprietary protocols.

The Standard PCS mode provides support for 8B/10B encoded applications up to 12.5 Gbps. The Enhanced PCS mode supports applications up to 17.4 Gbps. In addition, for highly customized implementations, a PCS Direct mode provides a fixed width interface up to 64 bits wide to core logic to allow for custom encoding including support for standards up to 28.05 Gbps.

The enhanced PCS includes an integrated 10GBASE-KR/40GBASE-KR4 Forward Error Correction (FEC) block.

The following table lists some of the key PCS features of Arria 10 transceivers that can be used in a wide range of standard and proprietary protocols from 125 Mbps to 28.05 Gbps.

Table 11: Arria 10 Transceiver PCS Features

PCS Protocol Support	Data Rate (Gbps)	Transmitter Data Path	Receiver Data Path
Standard PCS	0.125 to 12.5	Phase compensation FIFO, byte serializer, 8B/10B encoder, bit-slipper, channel bonding	Rate match FIFO, word-aligner, 8B/10B decoder, byte deserializer, byte ordering
PCI Express Gen1/Gen2 x1, x4, x8	2.5 and 5.0	Same as Standard PCS plus PIPE 2.0 interface to core	Same as Standard PCS plus PIPE 2.0 interface to core

Interlaken PCS Hard IP

Arria 10 devices have integrated Interlaken PCS hard IP supporting rates up to 17.4 Gbps per lane.

The Interlaken PCS hard IP is based on the proven functionality of the PCS developed for Altera's previous generation FPGAs, which has demonstrated interoperability with Interlaken ASSP vendors and third-party IP suppliers. The Interlaken PCS hard IP is present in every transceiver channel in Arria 10 devices.

10G Ethernet Hard IP

Arria 10 devices include IEEE 802.3 10-Gbps Ethernet (10GbE) compliant 10GBASE-R PCS and PMA hard IP. The scalable 10GbE hard IP supports multiple independent 10GbE ports while using a single PLL for all the 10GBASE-R PCS instantiations, which saves on core logic resources and clock networks.

The integrated 10G serial transceivers simplify multi-port 10GbE systems compared to XAUI interfaces that require an external XAUI-to-10G PHY. Furthermore, the integrated 10G transceivers incorporate Electronic Dispersion Compensation (EDC), which enables direct connection to standard 10G XFP and SFP+ pluggable optical modules. The 10G transceivers also support backplane Ethernet applications and include a hard 10GBASE-KR Forward Error Correction (FEC) circuit that can be used for both 10G and 40G applications. The integrated 10G Ethernet hard IP and 10G transceivers save external PHY cost, board space, and system power. The 10G Ethernet PCS hard IP and 10GBASE-KR FEC are present in every transceiver channel.

External Memory and General Purpose I/O

Arria 10 devices offer massive external memory bandwidth, with up to seven 32-bit DDR4 memory interfaces running at up to 2666 Mbps.

This bandwidth provides additional ease of design, lower power, and resource efficiencies of hardened high-performance memory controllers. Memory interfaces can be configured up to a maximum width of 144 bits when using either hard or soft memory controllers. Arria 10 devices also feature general purpose I/O capable of supporting a wide range of single-ended and differential I/O interfaces. LVDS rates up to 1.6 Gbps are supported, with each pair of pins having both a differential driver and a differential input buffer allowing for configurable LVDS direction on each pair.

The memory interface within Arria 10 FPGAs and SoCs delivers the highest performance and ease of use. Each I/O bank contains 48 general purpose I/Os and a high-efficiency hard memory controller capable of supporting many different memory types, each with different performance capabilities. The hard memory controller is also capable of being bypassed and replaced by a soft controller implemented in the user logic. The I/Os each have a hardened DDR read/write path (PHY) capable of performing key memory interface functionality such as read/write leveling, FIFO buffering to lower latency and improve margin, timing calibration, and on-chip termination. The timing calibration is aided by the inclusion of hard microcontrollers based on Altera's Nios® II technology, specifically tailored to control the calibration of multiple memory interfaces. This calibration allows the Arria 10 device to compensate for any changes in process, voltage, or temperature either within the Arria 10 device itself, or within the external memory device. The advanced calibration algorithms ensure maximum bandwidth and robust timing margin across all operating conditions.

Table 12: Arria 10 External Memory Interface Performance

The listed speeds are for the 1-rank case.

Interface	Controller Type	Performance
DDR4	Hard	2666 Mbps

Interface	Controller Type	Performance
DDR3	Hard	2133 Mbps
QDR II+ / II+ Xtreme	Soft	550 MTps
RLDRAM III	Hard	2400 Mbps
RLDRAM II	Soft	533 Mbps

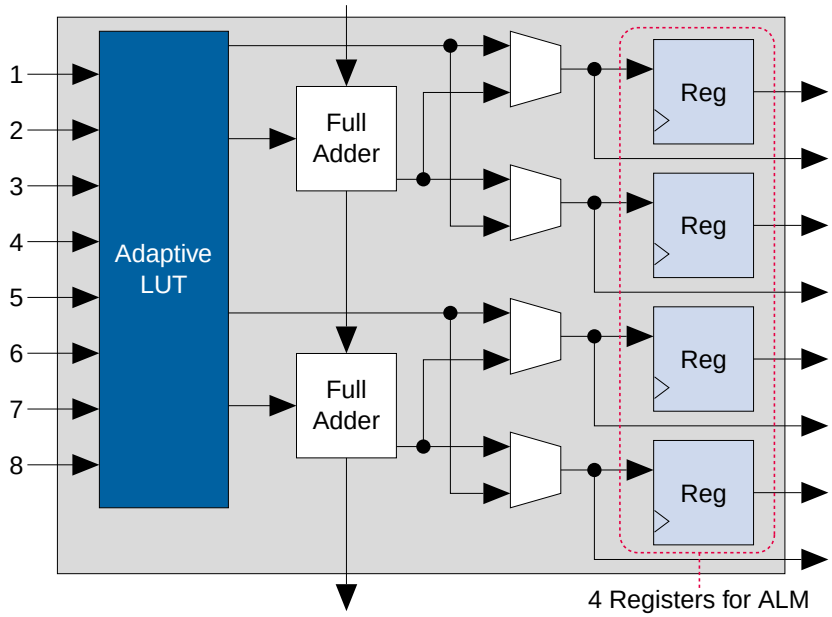
In addition to parallel memory interfaces, Arria 10 devices support serial memory technologies such as the Hybrid Memory Cube (HMC). The HMC is supported by the Arria 10 high-speed serial transceivers, which connect up to four HMC links, with each link running at data rates up to 15 Gbps.

Adaptive Logic Module (ALM)

Arria 10 devices use the same adaptive logic module (ALM) as the previous generation Arria V and Stratix V FPGAs, allowing for efficient implementation of logic functions and easy conversion of IP between the devices.

The ALM block diagram shown in the following figure has eight inputs with a fracturable look-up table (LUT), two dedicated embedded adders, and four dedicated registers.

Figure 7: Arria 10 FPGA and SoC ALM Block Diagram



Key features and capabilities of the Arria 10 ALM include:

- High register count with 4 registers per 8-input fracturable LUT enables Arria 10 devices to maximize core performance at higher core logic utilization
- 6% more logic compared to the traditional 2-register per LUT architecture
- Implements select 7-input logic functions, all 6-input logic functions, and two independent functions consisting of smaller LUT sizes (such as two independent 4-input LUTs) to optimize core logic utilization

- Hard memory controller with support for DDR3, DDR4 and optional error correction code (ECC) support
- Multiport Front End (MPFE) Scheduler interface to the hard memory controller
- 8-channel direct memory access (DMA) controller
- QSPI flash controller with SIO, DIO, QIO SPI Flash support
- NAND flash controller (ONFI 1.0 or later) with DMA and ECC support, updated to support 8 and 16-bit Flash devices and new command DMA to offload CPU for fast power down recovery
- Updated SD/SDIO/MMC controller to eMMC 4.5 with DMA with CE-ATA digital command support
- 3 10/100/1000 Ethernet media access control (MAC) with DMA
- 2 USB On-the-Go (OTG) controller with DMA
- 5 I^2C controller (3 can be used by EMAC for MIO to external PHY)
- 2 UART 16550 Compatible
- 4 serial peripheral interface (SPI) (2 Master, 2 Slaves)
- 54 programmable general-purpose I/O (GPIO)
- 48 I/O direct share I/O allows HPS peripherals to connect directly to I/O
- 7 general-purpose timers
- 4 watchdog timers
- Anti-tamper, Secure Boot, Encryption (AES) and Authentication (SHA)

- **HPS to FPGA Interconnect Backbone**

  Although the HPS and the Logic Core can operate independently, they are tightly coupled via a high-bandwidth system interconnect built from high-performance ARM AMBA AXI bus bridges. IP bus masters in the FPGA fabric have access to HPS bus slaves via the FPGA-to-HPS interconnect. Similarly, HPS bus masters have access to bus slaves in the core fabric via the HPS-to-FPGA bridge. Both bridges are AMBA AXI-3 compliant and support simultaneous read and write transactions. Up to three masters within the core fabric can share the HPS SDRAM controller with the processor. Additionally, the processor can be used to configure the core fabric under program control via a dedicated 32-bit configuration port.

- **HPS-to-FPGA**—configurable 32-, 64-, or 128-bit Avalon/AMBA AXI interface allows high bandwidth HPS master transactions to Logic Core
- **LW HPS-to-FPGA**—Light Weight 32-bit AXI interface suitable for low latency register accesses from HPS to soft peripherals in logic core
- **FPGA-to-HPS**—configurable 32-, 64-, or 128-bit AMBA AXI interface
- **FPGA-to-HPS SDRAM controller**—up to 3 masters (command ports), 3x 64-bit read data ports and 3x 64-bit write data ports
- **32-bit FPGA configuration manager**
- **Security**

A number of new security features have been introduced for anti-tamper management, secure boot, encryption (AES), and authentication (SHA).

Power Management

Arria 10 devices leverage the advanced 20 nm process technology, a low 0.9 V core power supply, an enhanced core architecture, and several optional power reduction techniques to reduce total power consumption by as much as 40% compared to Arria V devices and as much as 60% compared to Stratix V devices.

The optional power reduction techniques in Arria 10 devices include:

- **SmartVoltage ID**—a code is programmed into each device during manufacturing that allows a smart regulator to operate the device at lower core V_{CC} while maintaining performance
- **Programmable Power Technology**—non-critical timing paths are identified by the Quartus II software and the logic in these paths is biased for low power instead of high performance
- **V_{CC} PowerManager**—allows devices to be run at lower core voltage to trade performance for power savings
- **Low Static Power Options**—devices are available with either standard static power or low static power while maintaining performance

Furthermore, Arria 10 devices feature Altera's industry-leading low power transceivers and include a number of hard IP blocks that not only reduce logic resources but also deliver substantial power savings compared to soft implementations. In general, hard IP blocks consume up to 50% less power than the equivalent soft logic implementations.

Incremental Compilation

The Quartus II software incremental compilation feature reduces compilation time by up to 70% and preserves performance to ease timing closure.

Incremental compilation supports top-down, bottom-up, and team-based design flows. The incremental compilation feature facilitates modular hierarchical and team-based design flows where different designers compile their respective sections of a design in parallel. Furthermore, different designers or IP providers

can develop and optimize different blocks of the design independently. These blocks can then be imported into the top level project. The incremental compilation feature enables the partial reconfiguration flow for Arria 10 devices.

Configuration and Configuration via Protocol Using PCI Express

Arria 10 device configuration is improved for ease-of-use, speed, and cost. The devices can be configured through a variety of techniques such as active and passive serial, fast passive parallel, JTAG, and configuration via protocol using PCI Express including Gen3.

Configuration via protocol (CvP) using PCI Express allows the FPGA to be configured across the PCI Express bus, simplifying the board layout and increasing system integration. Making use of the embedded PCI Express hard IP, this technique allows the PCI Express bus to be powered up and active within the 100 ms time allowed by the PCI Express specification. Arria 10 devices also support partial reconfiguration across the PCI Express bus which reduces system down time by keeping the PCI Express link active while the device is being reconfigured.

Table 16: Arria 10 Device Configuration Modes

Mode	Compression	Encryption	Remote Update	Data Width (bits)	Maximum DCLK Rate (MHz)	Maximum Data Rate (Mbps)
Active Serial	Yes	Yes	Yes	1, 4	100	400
Passive Serial	Yes	Yes	—	1	125	125
Passive Parallel	Yes	Yes	Parallel flash loader	8, 16, 32	125	4000
Configuration via PCI Express	—	Yes	Yes	1, 2, 4, 8	—	4000
JTAG	—	—	—	1	33	33

Partial and Dynamic Reconfiguration

Partial reconfiguration allows you to reconfigure part of the FPGA while other sections continue running. This capability is required in systems where uptime is critical, because it allows you to make updates or adjust functionality without disrupting services.

In addition to lowering power and cost, partial reconfiguration also increases the effective logic density by removing the necessity to place in the FPGA those functions that do not operate simultaneously. Instead, these functions can be stored in external memory and loaded as needed. This reduces the size of the required FPGA by allowing multiple applications on a single FPGA, saving board space and reducing power. The partial reconfiguration process is built on top of the proven incremental compile design flow in the Quartus II design software.

Partial reconfiguration in Arria 10 devices is supported through the following configuration options:

- Partial reconfiguration through the FPP x16 I/O interface
- Partial reconfiguration using PCI Express

Dynamic reconfiguration in Arria 10 devices allows transceiver data rates, protocols and analog settings to be changed dynamically on a channel-by-channel basis while maintaining data transfer on adjacent transceiver channels. Dynamic reconfiguration is ideal for applications that require on-the-fly multi-protocol or multi-rate support, and both the PMA and PCS blocks within the transceiver can be reconfigured using this technique. Dynamic reconfiguration of the transceivers can be used in conjunction with partial reconfiguration of the FPGA to enable partial reconfiguration of both core and transceivers simultaneously.

Single Event Upset (SEU) Error Detection and Correction

Arria 10 devices offer robust and easy-to-use SEU error detection and correction circuitry.

The detection and correction circuitry includes protection for Configuration RAM (CRAM) programming bits and user memories. The CRAM is protected by a continuously running CRC error detection circuit with integrated ECC that automatically corrects one or two errors and detects higher order multi-bit errors. When more than two errors occur, correction is available through reloading of the core programming file, providing a complete design refresh while the FPGA continues to operate.

The physical layout of the Arria 10 CRAM array is optimized to make the majority of multi-bit upsets appear as independent single-bit or double-bit errors which are automatically corrected by the integrated CRAM ECC circuitry. In addition to the CRAM protection, the user memories also include integrated ECC circuitry and are layout optimized for error detection and correction.

Appendix: Arria 10 SoC Developers Corner

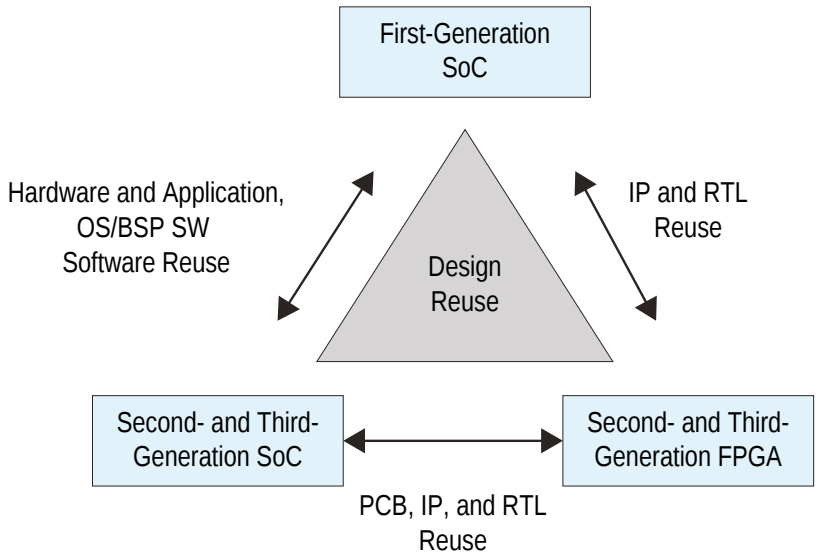
Altera's Arria 10 SoCs provide the combined benefits of programmable logic for high-speed data paths with ARM processor for intelligent control functions:

- High performance programmable core logic, hard memory controllers and high speed transceivers can be used to implement data path centric functions for 40G/100G systems including functions such as framing, bridging, aggregation, switching, traffic management, FEC, multirate aggregation, and data transmission.
- The integrated ARM based HPS implements intelligent control function and eliminates the need for a local processor, thereby reducing system power, form factor, and BOM cost. By adding intelligence to the data path, software on the ARM HPS manages and reduces system downtime and reduces the associated operating expenses. The Dual Core ARM Cortex-A9 based HPS comes with a rich set of embedded peripherals and associated device drivers for wide range of operating systems including Linux and VxWorks. The resulting board support packages can be used as the basis of a number of software applications such as:
  - Operations, Administration and Maintenance (OAM)
  - PCIe Root Port management
  - Remote Debug and System Update
  - Host offload and Algorithm acceleration
  - Chassis management
  - Routing and Look up management
  - Error handling and system downtime management
  - Rule management for deep packet inspection, packet parsing
  - Audio and Video Processing

Altera SoC: The Architecture of Choice When Productivity Matters

Productivity is the driving philosophy of Altera's Arria 10 SoC family. By reusing hardware, software, IP, and RTL across FPGAs and SoCs, you can reduce design effort and get products to market faster. The Dual Core ARM Cortex-A9 MPCore-based HPS is common to both 20- and 28-nm SoCs and facilitates extensive software code compatibility as well as tools and OS Board Support Package (BSP) reuse. The extensive tools and OS support available as part of Altera and ARM ecosystem and the fast iteration times inherent in software development (especially as compared to FPGA compile times) results in a highly productive embedded and DSP development flow. In addition, Altera offers high-level automated design flows for hardware development, such as the Altera OpenCL (a C-based hardware design flow) and DSP Builder (a model-based hardware design flow).

Figure 9: Hardware and Software Reuse



Altera's 20-nm SoCs and FPGAs can be reused in the following ways:

- **Application Code Reuse**: Because 28 nm and 20 nm SoCs share the same Dual Core ARM Cortex-A9 based HPS, any application code, board support packages, and ARM development tools developed for one SoC family can be reused with minimal design effort.
- **IP Reuse**: Arria 10 SoCs share the same core logic, memory, DSP, and I/O as Arria 10 FPGAs. Hardware intellectual property can be shared with minimal design effort. Altera also provides a fully tested and characterized portfolio of over 200 IP cores.
- **PCB Hardware Reuse**: Arria 10 SoCs are also package and footprint compatible with Arria 10 FPGAs, allowing hardware PCBs to be shared between the device categories.
- **Advanced Software Development Tools**:
  - The ecosystem that is available on ARM and the body of software packages, middleware available for operating systems that support ARM as well as the application development and debug tools available for ARM provides a familiar development environment to software developers.
  - Innovations such as Altera's Virtual Target technology allow functional testing of code without the need for hardware. By combining the most advanced multi-core debugger for ARM architectures with FPGA-adaptivity, the ARM DS-5 Altera Edition Toolkit provides embedded software developers an unprecedented level of full-chip visibility and control through the standard DS-5 user interface.
- **Advanced Hardware Development Tools**:
  - Altera's Quartus II software has faster compilation times than ever before. The Quartus II software's support for partial reconfiguration technology allows a single PCB to support multiple protocols by swapping protocols in the field.
  - QSys System Development framework allows rapid system integration of processor and peripherals and automates the process of generating AXI and Avalon based interconnect logic.
  - DSP Builder is a plug-in to MathWorks' Simulink that allows designers to develop DSP based filters, matrix operators and transforms using Model Based design flow and Advanced Blockset tools.
  - Open Computing Language (OpenCL) programming model with Altera's massively parallel FPGA architecture provides a powerful solution for system acceleration. The Altera SDK for OpenCL allows software developers to develop hardware using a C-based high-level design flow.

Single Platform of Devices that Offer Unified Control Path and Scalable Datapath

When you combine the SoC portfolio with the productivity benefits of design reuse in hardware and software, you get a benefit that is unique to Altera's technology. The result is an architecture that offers both unified control path and scalable data path.