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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	427200
Number of Logic Elements/Cells	1150000
Total RAM Bits	68857856
Number of I/O	600
Number of Gates	-
Voltage - Supply	0.87V ~ 0.93V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	1517-BBGA, FCBGA
Supplier Device Package	1517-FCBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/intel/10at115n4f40e4sges

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Arria 10 Family Variants

Arria 10 devices are available in GX, GT, and SX variants.

- **Arria 10 GX** devices deliver over 500 MHz core fabric performance and 2666 Mbps DDR4 external memory interface performance across the industrial temperature range, while providing over 1.1 million logic elements and 96 general purpose transceivers. Every transceiver is capable of 17.4 Gbps for short reach applications and 16.0 Gbps across the backplane. These devices are optimized for a broad range of applications such as wireless remote radio heads, broadcast studio equipment, 40G/100G communication systems, server acceleration, and medical imaging.
- **Arria 10 GT** devices have the same core performance and feature set as Arria 10 GX devices, with the added capability of sixteen 28.05-Gbps short reach transceivers for chip-to-chip and chip-to-module applications. The 28.05-Gbps transceivers are ideal for interfacing with the emerging CFP2 and CFP4 optical modules that typically require four lanes at data rates in the range of 25 to 28 Gbps. Backplane driving capability is also increased to 17.4 Gbps in Arria 10 GT devices.
- **Arria 10 SX** devices have a feature set that is similar to Arria 10 GX devices plus an ARM Cortex-A9 hard processor system.

Common to all Arria 10 family variants is the enhanced logic array utilizing Altera's adaptive logic module (ALM) and a rich set of high performance building blocks that includes 20Kbit (M20K) internal memory blocks, variable precision DSP blocks, fractional synthesis and integer PLLs, hard memory PHY and controllers for external memory interfaces, and general purpose I/O cells. These building blocks are interconnected by an updated version of Altera's superior multi-track routing architecture and comprehensive fabric clocking network. All devices support in-system, fine-grained partial reconfiguration of the logic array, allowing logic to be added and removed from the system during operation.

All family variants also contain high speed serial transceivers, containing both the physical medium attachment (PMA) and the physical coding sublayer (PCS), which can be used to implement a variety of industry standard and proprietary protocols. In addition to the hard PCS, Arria 10 devices contain multiple instantiations of PCI Express hard IP that supports Gen1/Gen2/Gen3 rates in x1/x2/x4/x8 lane configurations. The hard PCS and hard PCI Express IP free up valuable core logic resources, save power, and increase productivity for the user.

Improvements in Arria 10 FPGAs and SoCs

Altera has combined in-house innovations with TSMC's advanced 20-nm process technology to deliver major improvements over Arria V FPGAs and SoCs in nearly every category.

Table 1: Key Features of Arria 10 Devices Compared to Arria V Devices

Feature	Arria V FPGAs and SoCs	Arria 10 FPGAs and SoCs
Process technology	28-nm TSMC	20-nm TSMC
Processor core	Dual ARM Cortex-A9 MPCore™	Dual ARM Cortex-A9 MPCore
Processor performance	800 MHz	1.5 GHz
Logic core performance	300 MHz	500 MHz
Power dissipation	1x	0.6x

Feature	Arria V FPGAs and SoCs	Arria 10 FPGAs and SoCs
Logic density	504 KLE	1150 KLE
Embedded memory	34 Mbits	53 Mbits
18x19 multipliers	2186	3356
Maximum transceivers	36	96
Maximum transceiver data rate (chip to chip)	10.3125 Gbps	28.05 Gbps
Memory devices supported	DDR3 SDRAM @ 667 MHz/1333 Mbps	DDR4 SDRAM @ 1333 MHz/2666 Mbps DDR3 SDRAM @ 1067 MHz/2133 Mbps Hybrid Memory Cube (HMC)
Hard protocol IP	2 EMACs PCI Express Gen3 x8 (Arria V GZ) PCI Express Gen2 x4/Gen1 x8 (Arria V GX/GT/SX/ST)	3 EMACs PCI Express Gen3 x8 10GBASE-KR/40GBASE-KR4 FEC Interlaken PCS

These features result in the following improvements:

- **Improved Core Logic Performance**: Arria 10 devices offer over 60% improved core performance compared to the previous generation
- **Improved Processor Performance**: Arria 10 SoCs provide 87% improvement in processor performance
- **Improved Processor Power Efficiency**: At 20 nm, the Dual Core ARM Cortex-A9 Processor provides the best power efficiency for any GHz-class processor in the industry
- **Lower Power**: Arria 10 devices deliver up to 40% lower power compared to prior-generation mid-range FPGAs and SoCs, enabled by 20-nm process technology advancements and a variety of innovative power-management options
- **Higher Density**: Arria 10 devices provide a higher level of integration with up to 1150K logic elements (LEs), up to 53 Mbits of embedded memory, and over 3350 18x19 multipliers
- **Improved Transceiver Bandwidth**: Arria 10 devices support chip-to-chip rates up to 28 Gbps and backplane rates up to 17.4 Gbps
- **Improved Memory Bandwidth with DDR4 Support**: Arria 10 devices support DDR4 memory up to 1333 MHz/ 2666 Mbps and feature support for the emerging transceiver-based Hybrid Memory Cube (HMC)
- **Improved DSP Performance**: With over 1.0 TeraFLOPs of single-precision DSP performance, Arria 10 devices deliver a 4 times increase in DSP performance
- **Additional Protocol Support for Hard IP**: Arria 10 devices feature an advanced transceiver architecture with added hard IP support for PCIe Gen3, Interlaken PCS, and 10GBASE-KR/40GBASE-KR4 FEC

Target Markets for Arria 10 FPGAs and SoCs

Arria 10 devices meet the performance, power, and bandwidth requirements of next generation wireless infrastructure, broadcast, compute and storage, networking, and medical and military equipment.

- For **Wireless infrastructure** particularly remote radio unit, the industry has standardized on ARM-based ASSPs and SoCs for several generations. ARM is widely recognized as the industry leader in low power solutions. At 20 nm, the Dual ARM Cortex MPCore provides the best power efficiency of any GHz class of process. When combined with Altera's industry leading programmable technology, this provides an ideal platform to address the performance, power, and form factor requirements of wireless remote radio unit and small cell base stations.
- For **Wireline communication equipment** such as access, metro, core, and transmission equipment where the FPGA performs critical functions such as protocol bridging, packet framing, aggregation, and I/O expansion, SoCs now offer all this as well as integrated intelligent control and link management, sometimes referred to as Operations, Administration, and Maintenance (OAM). OAM typically is software that executes when a link is established or fails during operation. The integrated ARM processor can also be used for statistics and error monitoring and minimize system downtime when a link is compromised or oversubscribed. Tight coupling of the processor and the data path (implemented in the core logic) saves time and results in significant savings in terms of operating expenses associated with system downtime and loss of quality of service.
- For **Compute and storage equipment**, flash cache storage, the integrated ARM processor can be used to manage Flash sectors and improve overall life and reliability as well as offload the host processor and provide control for search and hardware acceleration functions for cloud storage equipment. The integrated ARM based HPS can configure the hard PCIe interfaces in PCIe root port configuration and also run link layers for SAS and SATA interfaces.
- For **Next generation Broadcast equipment**, where "4K readiness" is the key technology driver, the integrated ARM processor subsystem eliminates the need for a local GHz class processor, which is commonly used for functions such as audio processing, video compression, video link management, and PCIe root port.
- For **Military** applications, new security features such as Secure Boot, Encryption, and Authentication have been introduced for secure wireless and wireline communications, military radar, military intelligence equipment.
- For **Test and Medical** applications, combining ARM HPS with support for high speed memory devices such as DDR4, and Hybrid Memory Cube (HMC) as well as high speed transceivers and embedded controllers such as PCIe Gen3, Arria 10 SoCs are ideal for next generation test and medical equipment.

FPGA and SoC Features Summary

Table 2: Arria 10 FPGA and SoC Common Device Features

Feature	Description
Technology	• 20-nm TSMC SoC process technology • 0.9 V standard V_{CC} core voltage

Feature	Description
Low power serial transceivers	• Continuous operating range of 611 Mbps to 17.4 Gbps for Arria 10 GX devices • Continuous operating range of 611 Mbps to 28.05 Gbps for Arria 10 GT devices • Backplane support up to 16.0 Gbps for Arria 10 GX devices • Backplane support up to 17.4 Gbps for Arria 10 GT devices • Extended range down to 125 Mbps with oversampling • ATX transmit PLLs with user-configurable fractional synthesis capability • Electronic Dispersion Compensation (EDC) for XFP, SFP+, QSFP, and CFP optical module support • Adaptive linear and decision feedback equalization • Transmit pre-emphasis and de-emphasis • Dynamic partial reconfiguration of individual transceiver channels • On-chip instrumentation (EyeQ non-intrusive data eye monitoring)
General purpose I/Os	• 1.6 Gbps LVDS—every pair can be configured as an input or output • 1333 MHz/2666 Mbps DDR4 external memory interface • 1067 MHz/2133 Mbps DDR3 external memory interface • 1.2 V to 3.0 V single-ended LVCMOS/LVTTL interfacing • On-chip termination (OCT)
Embedded hard IP	• PCIe Gen1/Gen2/Gen3 complete protocol stack, x1/x2/x4/x8 end point and root port • DDR4/DDR3/DDR3L/DDR3U/RLDRAM 3/LPDDR3 hard memory controller (RLDRAM2/QDR II+ using soft memory controller) • Multiple hard IP instantiations in each device • Dual-core ARM Cortex-A9 processor (Arria 10 SX devices only)
Transceiver hard IP	• 10GBASE-KR/40GBASE-KR4 Forward Error Correction (FEC) • 10G Ethernet PCS • PCI Express PIPE interface • Interlaken PCS • Gigabit Ethernet PCS • Deterministic latency support for Common Public Radio Interface (CPRI) PCS • Fast lock-time support for Gigabit Passive Optical Networking (GPON) PCS • 8B/10B, 64B/66B, 64B/67B encoders and decoders • Custom mode support for proprietary protocols
Power management	• SmartVoltage ID • V_{CC} PowerManager • Low static power device options • Programmable Power Technology • Quartus® II integrated PowerPlay power analysis
High performance core fabric	• Enhanced adaptive logic module (ALM) with 4 registers • Improved multi-track routing architecture reduces congestion and improves compile times • Hierarchical core clocking architecture • Fine-grained partial reconfiguration

Feature	Description

External Memory Interface for HPS	• Hard memory controller with support for DDR4, DDR3, DDR2, LPDDR2
	  ◦ 40-bit (32-bit + 8-bit ECC) with select packages supporting 72-bit (64-bit + 8-bit ECC)
	  ◦ Support for up to 2666 Mbps DDR4 and 2166 Mbps DDR3 frequencies
	  ◦ Error correction code (ECC) support including calculation, error correction, write-back correction, and error counters
	  ◦ Software Configurable Priority Scheduling on individual SDRAM bursts ECC
	  ◦ Fully programmable timing parameter support for all JEDEC specified timing parameters
	  ◦ AXI® Quality of Service (QoS) support for interface to logic core
	  ◦ Multiport front-end (MPFE) scheduler interface to hard memory controller
	• Queued serial peripheral interface (QSPI) flash controller allows port sharing of hard memory controller between CPU and logic core
	  ◦ Single I/O (SIO), Dual I/O (DIO), and Quad I/O (QIO) SPI Flash support
	  ◦ Support for up to 108 MHz for flash frequency
	• NAND flash controller
	  ◦ ONFI 1.0 or later
	  ◦ Integrated descriptor based with DMA
	  ◦ New command DMA to offload CPU for fast power down recovery
	  ◦ Programmable hardware ECC support
	  ◦ Updated to support 8 and 16 bit Flash devices
	  ◦ Support for 50 MHz flash frequency
	• Secure Digital SD/SDIO/MMC controller
	  ◦ eMMC 4.5
	  ◦ Integrated descriptor based DMA
	  ◦ CE-ATA digital commands supported
	  ◦ 50 MHz operating frequency
	• Direct memory access (DMA) controller
	  ◦ 8-channel
	  ◦ Supports up to 32 peripheral handshake interface

Feature	Description

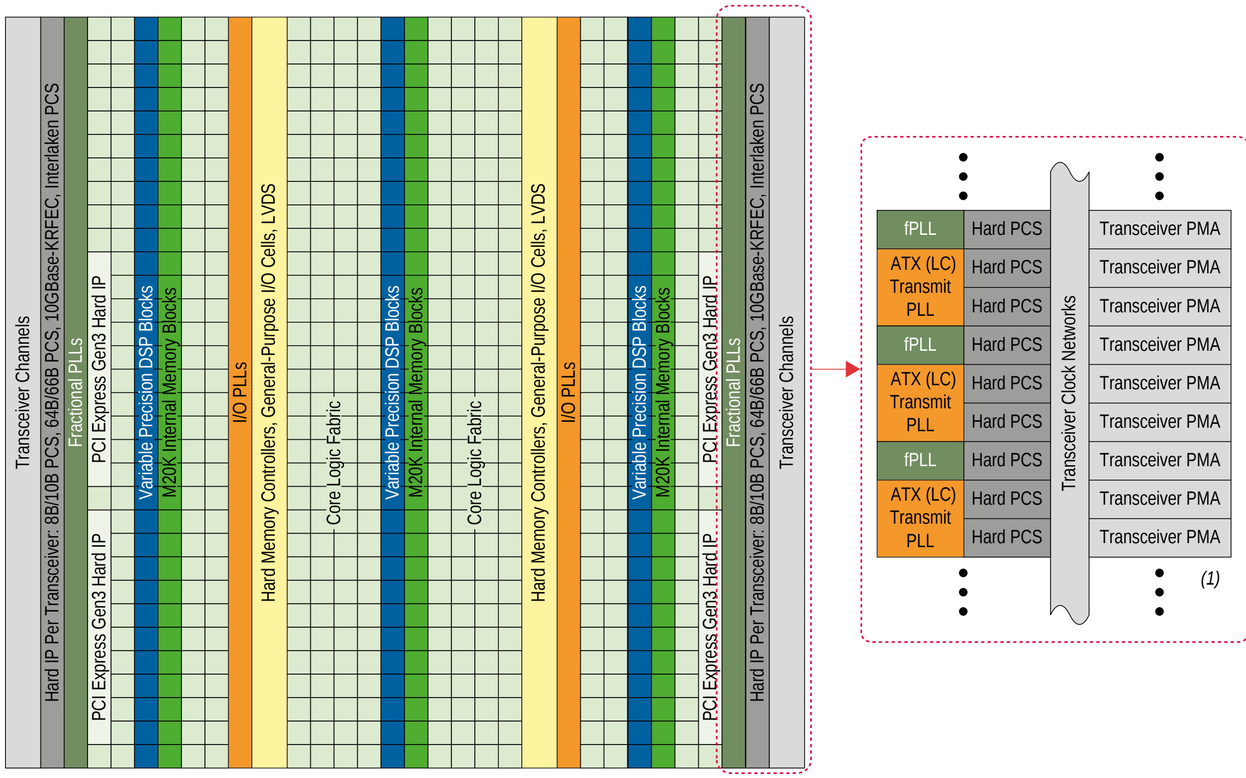
Communication Interface Controllers	• Three 10/100/1000 Ethernet media access controls (MAC) with integrated DMA
	  • Supports RGMII and RMII external PHY Interfaces
	  • Option to support other PHY interfaces through FPGA logic
	    • GMII and SGMII
	  • Supports IEEE 1588-2002 and IEEE 1588-2008 standards for precision networked clock synchronization
	  • Supports IEEE 802.1Q VLAN tag detection for reception frames
	  • Supports Ethernet AVB standard
	• 2 USB On-the-Go (OTG) controllers with DMA
	  • Dual-Role Device (device and host functions)
	    • High-speed (480 Mbps)
	    • Full-speed (12 Mbps)
	    • Low-speed (1.5 Mbps)
	    • Supports USB 1.1 (full-speed and low-speed)
	  • Integrated descriptor-based scatter-gather DMA
	  • Support for external ULPI PHY
	  • Up to 16 bidirectional endpoints, including control endpoint
	  • Up to 16 host channels
	  • Supports generic root hub
	  • Configurable to OTG 1.3 and OTG 2.0 modes
	• 5 I^2C controllers (3 can be used by EMAC for MIO to external PHY)
	  • Support both 100Kbps and 400Kbps modes
	  • Support both 7-bit and 10-bit addressing modes
	  • Support Master and Slave operating mode
	• 2 UART 16550 compatible
	  • Support IrDA 1.0 SIR mode
	  • Programmable baud rate up to 115.2Kbaud
	• 4 serial peripheral interfaces (SPI) (2 Master, 2 Slaves)
	  • Full and Half duplex

Timers and I/O	• Timers
	  • 7 general-purpose timers
	  • 4 watchdog timers
	• 62 programmable general-purpose I/O (GPIO)
	  • 3 modules 24, 24, and 14
	• 48 I/O direct share I/O allows HPS peripherals to connect directly to I/O

Security	• Anti-tamper, secure boot, Advanced Encryption Standard (AES) and authentication (SHA)

Arria 10 Block Diagrams

Figure 2: Arria 10 FPGA Architecture Block Diagram



Note:
(1) Unused transceiver channels can be used as additional transceiver transmit PLLs

Device Name [1]	Logic Elements (KLE)	Registers	M20K Blocks	M20K Mbits	MLAB Counts	MLAB Mbits	18x19 Multipliers [2]	Maximum GPIOs	Maximum XCVR (17.4G, 28.05G)	fPLLs	I/O PLLs	PCIe HIPs
GX 320 (10AX032)	320	478,640	891	17	4,673	3	1,970	384	24, 0	8	8	2
GX 480 (10AX048)	480	730,880	1,438	28	7,137	4	2,736	492	36, 0	12	12	2
GX 570 (10AX057)	570	868,320	1,800	35	8,241	5	3,046	588	48, 0	16	16	2
GX 660 (10AX066)	660	1,005,800	2,133	42	9,345	6	3,356	588	48, 0	16	16	2
GX 900 (10AX090)	900	1,358,480	2,423	47	15,080	9	3,036	768	96, 0	32	16	4
GX 1150 (10AX115)	1,150	1,710,800	2,713	53	20,814	13	3,036	768	96, 0	32	16	4
GT 900 (10AT090)	900	1,358,480	2,423	47	15,080	9	3,036	624	80, 16	32	16	4
GT 1150 (10AT115)	1,150	1,710,800	2,713	53	20,814	13	3,036	624	80, 16	32	16	4

Table 5: Arria 10 GX and Arria 10 GT FPGA Family Package Plan, part 1

Cell legend: General Purpose I/Os, High-Voltage I/Os, LVDS Pairs, Transceivers [3] [4] [5] [6] [7] [8]

Device [1]	U19 (U484) (19x19 mm^2)	F27 (F672) (27x27 mm^2)	F29 (F780) (29x29 mm^2)	F34 (F1152) (35x35 mm^2)	F35 (F1152) (35x35 mm^2) [9]	F36 (F1152) (35x35 mm^2) [9]
GX 160 (10AX016)	192,48,72,6	240,48,96,12	288,48,120,12	—	—	—

(3) All packages are ball grid arrays with 1.0 mm pitch, except for U19 (U484), which is 0.8 mm pitch.
(4) High-Voltage I/O pins are used for 3.3 V and 2.5 V interfacing.
(5) Each LVDS pair can be configured as either a differential input or a differential output.
(6) High-Voltage I/O pins and LVDS pairs are included in the General Purpose I/O count. Transceivers are counted separately.
(7) Each package column offers pin migration (common circuit board footprint) for all devices in the column.
(8) Arria 10 GX devices are pin migratable with Arria 10 GT devices in the same package.
(9) Devices in the F35 (F1152) package are pin migratable with devices in the F36 (F1152) package

Device [1]	F40 (F1517) (40x40 mm^2)	F40 (F1517) (40x40 mm^2)	F45 (F1932) (45x45 mm^2)	F45 (F1932) (45x45 mm^2)	F45 (F1932) (45x45 mm^2)
GX 270 (10AX027)	—	—	—	—	—
GX 320 (10AX032)	—	—	—	—	—
GX 480 (10AX048)	—	—	—	—	—
GX 570 (10AX057)	588,48,270,48	—	—	—	—
GX 660 (10AX066)	588,48,270,48	—	—	—	—
GX 900 (10AX090)	624,0,312,48	342,0,154,66	768,0,384,48	624,0,312,72	480,0,240,96
GX 1150 (10AX115)	624,0,312,48	342,0,154,66	768,0,384,48	624,0,312,72	480,0,240,96
GT 900 (10AT090)	624,0,312,48	—	—	624,0,312,72	480,0,240,96
GT 1150 (10AT115)	624,0,312,48	—	—	624,0,312,72	480,0,240,96

Table 9: Arria 10 SX SoC Family Package Plan

Cell legend: General Purpose I/Os, High-Voltage I/Os, LVDS Pairs, Transceivers (12) (13) (14) (15) (16)

Device (10)	U19 (U484) (19x19 mm^2)	F27 (F672) (27x27 mm^2)	F29 (F780) (29x29 mm^2)	F34 (F1152) (35x35 mm^2)	F35 (F1152) (35x35 mm^2) (17)	F36 (F1152) (35x35 mm^2) (17) 72-bit HPS DDR	F40 (F1517) (40x40 mm^2)
SX 160 (10AS016)	192,48,72,6	240,48,96,12	288,48,120,12	—	—	—	—
SX 220 (10AS022)	192,48,72,6	240,48,96,12	288,48,120,12	—	—	—	—
SX 270 (10AS027)	—	240,48,96,12	360,48,156,12	384,48,168,24	384,48,168,24	—	—
SX 320 (10AS032)	—	240,48,96,12	360,48,156,12	384,48,168,24	384,48,168,24	—	—
SX 480 (10AS048)	—	—	360,48,156,12	492,48,222,24	396,48,174,36	—	—
SX 570 (10AS057)	—	—	—	492,48,222,24	396,48,174,36	—	588,48,270,48
SX 660 (10AS066)	—	—	—	492,48,222,24	396,48,174,36	432,48,192,36	588,48,270,48

Migration Between Arria 10 Devices and Stratix 10 Devices

You can start developing with Arria 10 devices and then move to Stratix 10 devices, because there is footprint compatibility between the Arria 10 and Stratix 10 packages. Contact Altera for more details about the migration possibilities between the two device families.

(12) All packages are ball grid arrays with 1.0 mm pitch, except for U19 (U484), which is 0.8 mm pitch.
(13) High-Voltage I/O pins are used for 3.3 V and 2.5 V interfacing.
(14) Each LVDS pair can be configured as either a differential input or a differential output.
(15) High-Voltage I/O pins and LVDS pairs are included in the General Purpose I/O count. Transceivers are counted separately.
(16) Each package column offers pin migration (common circuit board footprint) for all devices in the column.
(17) Devices in the F35 (F1152) package are pin migratable with devices in the F36 (F1152) package

Feature	Capability
Fractional PLLs	On-chip fractional frequency synthesizers to replace on-board crystal oscillators and reduce system cost
Digitally Assisted Analog CDR	Superior jitter tolerance with fast lock time
On-Die Instrumenta-tion— EyeQ and Jitter Margin Tool	Simplify board bring-up, debug, and diagnostics with non-intrusive, high-resolution eye monitoring (EyeQ). Also inject jitter from transmitter to test link margin in system.
Dynamic Partial Reconfiguration (DPRIO)	Allows for independent control of each transceiver channel Avalon memory-mapped interface for the most transceiver flexibility
Multiple PCS-PMA and PCS-PLD interface widths	8-, 10-, 16-, 20-, 32-, 40-, or 64-bit interface widths for flexibility of deserialization width, encoding, and reduced latency

PCS Features

Arria 10 PMA channels interface with core logic through configurable PCS interface layers.

Multiple gearbox implementations are available to decouple PCS and PMA interface widths. This feature provides the flexibility to implement a wide range of applications with 8-, 10-, 16-, 20-, 32-, 40-, or 64-bit interface widths. Arria 10 FPGAs contain PCS hard IP to support a wide range of standard and proprietary protocols.

The Standard PCS mode provides support for 8B/10B encoded applications up to 12.5 Gbps. The Enhanced PCS mode supports applications up to 17.4 Gbps. In addition, for highly customized implementations, a PCS Direct mode provides a fixed width interface up to 64 bits wide to core logic to allow for custom encoding including support for standards up to 28.05 Gbps.

The enhanced PCS includes an integrated 10GBASE-KR/40GBASE-KR4 Forward Error Correction (FEC) block.

The following table lists some of the key PCS features of Arria 10 transceivers that can be used in a wide range of standard and proprietary protocols from 125 Mbps to 28.05 Gbps.

Table 11: Arria 10 Transceiver PCS Features

PCS Protocol Support	Data Rate (Gbps)	Transmitter Data Path	Receiver Data Path
Standard PCS	0.125 to 12.5	Phase compensation FIFO, byte serializer, 8B/10B encoder, bit-slipper, channel bonding	Rate match FIFO, word-aligner, 8B/10B decoder, byte deserializer, byte ordering
PCI Express Gen1/Gen2 x1, x4, x8	2.5 and 5.0	Same as Standard PCS plus PIPE 2.0 interface to core	Same as Standard PCS plus PIPE 2.0 interface to core

PCS Protocol Support	Data Rate (Gbps)	Transmitter Data Path	Receiver Data Path
PCI Express Gen3 x1, x4, x8	8.0	Phase compensation FIFO, byte serializer, encoder, scrambler, bit-slipper, gear box, channel bonding, and PIPE 3.0 interface to core, auto speed negotiation	Rate match FIFO (0-600 ppm mode), word-aligner, decoder, descrambler, phase compensation FIFO, block sync, byte deserializer, byte ordering, PIPE 3.0 interface to core, auto speed negotiation
CPRI	0.6144 to 9.8	Same as Standard PCS plus deterministic latency serialization	Same as Standard PCS plus deterministic latency deserialization
Enhanced PCS	2.5 to 17.4	FIFO, channel bonding, bit-slipper, and gear box	FIFO, block sync, bit-slipper, and gear box
10GBASE-R	10.3125	FIFO, 64B/66B encoder, scrambler, FEC, and gear box	FIFO, 64B/66B decoder, descrambler, block sync, FEC, and gear box
Interlaken	4.9 to 17.4	FIFO, channel bonding, frame generator, CRC-32 generator, scrambler, disparity generator, bit-slipper, and gear box	FIFO, CRC-32 checker, frame sync, descrambler, disparity checker, block sync, and gear box
SFI-S/SFI-5.2	11.3	FIFO, channel bonding, bit-slipper, and gear box	FIFO, bit-slipper, and gear box
IEEE 1588	1.25 to 10.3125	FIFO (fixed latency), 64B/66B encoder, scrambler, and gear box	FIFO (fixed latency), 64B/66B decoder, descrambler, block sync, and gear box
SDI	up to 11.9	FIFO and gear box	FIFO, bit-slipper, and gear box
GigE	1.25	Same as Standard PCS plus GigE state machine	Same as Standard PCS plus GigE state machine
PCS Direct	up to 28.05	Custom	Custom

PCI Express Gen1/Gen2/Gen3 Hard IP

Arria 10 devices contain embedded PCI Express hard IP designed for performance, ease-of-use, and increased functionality.

The PCI Express hard IP consists of the PHY, Data Link, and Transaction layers, and supports PCI Express Gen1/Gen2/Gen3 end point and root port, in x1/x2/x4/x8 lane configurations. The PCI Express hard IP is capable of operating independently from the core logic. This feature allows the link to power up and complete link training in less than 100 ms, while the Arria 10 device completes loading the programming file for the rest of the FPGA. The hard IP also provides added functionality, which makes it easier to support emerging features such as Single Root I/O Virtualization (SR-IOV) and optional protocol extensions. The Arria 10 PCI Express hard IP has improved end-to-end data path protection using Error Checking and Correction (ECC). In addition, the hard IP supports configuration of the FPGA via protocol across the PCI Express bus at Gen1/Gen2/Gen3 rates (CvP using PCI Express).

Interlaken PCS Hard IP

Arria 10 devices have integrated Interlaken PCS hard IP supporting rates up to 17.4 Gbps per lane.

The Interlaken PCS hard IP is based on the proven functionality of the PCS developed for Altera's previous generation FPGAs, which has demonstrated interoperability with Interlaken ASSP vendors and third-party IP suppliers. The Interlaken PCS hard IP is present in every transceiver channel in Arria 10 devices.

10G Ethernet Hard IP

Arria 10 devices include IEEE 802.3 10-Gbps Ethernet (10GbE) compliant 10GBASE-R PCS and PMA hard IP. The scalable 10GbE hard IP supports multiple independent 10GbE ports while using a single PLL for all the 10GBASE-R PCS instantiations, which saves on core logic resources and clock networks.

The integrated 10G serial transceivers simplify multi-port 10GbE systems compared to XAUI interfaces that require an external XAUI-to-10G PHY. Furthermore, the integrated 10G transceivers incorporate Electronic Dispersion Compensation (EDC), which enables direct connection to standard 10G XFP and SFP+ pluggable optical modules. The 10G transceivers also support backplane Ethernet applications and include a hard 10GBASE-KR Forward Error Correction (FEC) circuit that can be used for both 10G and 40G applications. The integrated 10G Ethernet hard IP and 10G transceivers save external PHY cost, board space, and system power. The 10G Ethernet PCS hard IP and 10GBASE-KR FEC are present in every transceiver channel.

External Memory and General Purpose I/O

Arria 10 devices offer massive external memory bandwidth, with up to seven 32-bit DDR4 memory interfaces running at up to 2666 Mbps.

This bandwidth provides additional ease of design, lower power, and resource efficiencies of hardened high-performance memory controllers. Memory interfaces can be configured up to a maximum width of 144 bits when using either hard or soft memory controllers. Arria 10 devices also feature general purpose I/O capable of supporting a wide range of single-ended and differential I/O interfaces. LVDS rates up to 1.6 Gbps are supported, with each pair of pins having both a differential driver and a differential input buffer allowing for configurable LVDS direction on each pair.

The memory interface within Arria 10 FPGAs and SoCs delivers the highest performance and ease of use. Each I/O bank contains 48 general purpose I/Os and a high-efficiency hard memory controller capable of supporting many different memory types, each with different performance capabilities. The hard memory controller is also capable of being bypassed and replaced by a soft controller implemented in the user logic. The I/Os each have a hardened DDR read/write path (PHY) capable of performing key memory interface functionality such as read/write leveling, FIFO buffering to lower latency and improve margin, timing calibration, and on-chip termination. The timing calibration is aided by the inclusion of hard microcontrollers based on Altera's Nios® II technology, specifically tailored to control the calibration of multiple memory interfaces. This calibration allows the Arria 10 device to compensate for any changes in process, voltage, or temperature either within the Arria 10 device itself, or within the external memory device. The advanced calibration algorithms ensure maximum bandwidth and robust timing margin across all operating conditions.

Table 12: Arria 10 External Memory Interface Performance

The listed speeds are for the 1-rank case.

Interface	Controller Type	Performance
DDR4	Hard	2666 Mbps

Table 13: Arria 10 Internal Embedded Memory Block Configurations

MLAB (640 bits)	M20K (20 Kbits)
64 x 10 (supported through emulation)	16K x 1
32 x 20	8K x 2
	4K x 5
	2K x 10
	1K x 20
	512 x 40

The Quartus II software simplifies design reuse by automatically mapping memory blocks from previous generations of devices into the Arria 10 MLAB and M20K blocks.

Variable Precision DSP Block

The Arria 10 DSP blocks are based upon the Variable Precision DSP Architecture used in Altera's previous generation Arria V FPGAs. The blocks can be configured to natively support signal processing with precision ranging from 18x19 up to 54x54. A pipeline register has been added to increase the maximum operating frequency of the DSP block and reduce power consumption.

Each DSP block can be independently configured at compile time as either dual 18x19 or a single 27x27 multiply accumulate. With a dedicated 64-bit cascade bus, multiple variable precision DSP blocks can be cascaded to implement even higher precision DSP functions efficiently. The following table shows how different precisions are accommodated within a DSP block, or by utilizing multiple blocks.

Table 14: Variable Precision DSP Block Configurations

Multiplier Size	DSP Block Resources	Expected Usage
18x19 bits	1/2 of Variable Precision DSP Block	Medium precision fixed point
27x27 bits	1 Variable Precision DSP Block	High precision fixed or Single Precision floating point
19x36 bits	1 Variable Precision DSP Block with external adder	Fixed point FFTs
36x36 bits	2 Variable Precision DSP Blocks with external adder	Very high precision fixed point
54x54 bits	4 Variable Precision DSP Blocks with external adder	Double Precision floating point

Complex multiplication is very common in DSP algorithms. One of the most popular applications of complex multipliers is the FFT algorithm. This algorithm has the characteristic of increasing precision requirements on only one side of the multiplier. The Variable Precision DSP block supports the FFT algorithm with proportional increase in DSP resources as the precision grows.

Table 15: Complex Multiplication With Variable Precision DSP Block

Complex Multiplier Size	DSP Block Resources	FFT Usage
18x19 bits	2 Variable Precision DSP Blocks	Resource optimized FFTs
27x27 bits	4 Variable Precision DSP Blocks	Highest precision FFT stages and single precision floating point

For FFT applications with high dynamic range requirements, the Altera FFT MegaCore® function offers an option of single precision floating point implementation, with resource usage and performance similar to high precision fixed point implementations.

Other features of the DSP block include:

- Hard 18-bit and 25-bit pre-adders
- 64-bit dual accumulator (for separate I, Q product accumulations)
- Cascaded output adder chains for 18- and 27-bit FIR filters
- Embedded coefficient registers for 18- and 27-bit coefficients
- Fully independent multiplier outputs
- Inferability using HDL templates supplied by the Quartus II software for most modes

The Variable Precision DSP block is ideal to support the growing trend towards higher bit precision in high performance DSP applications. At the same time, it can efficiently support the many existing 18-bit DSP applications, such as high definition video processing and remote radio heads. Arria 10 devices, with the Variable Precision DSP block architecture, can efficiently support many different precision levels, up to and including floating point implementations. This flexibility can result in increased system performance, reduced power consumption, and reduce architecture constraints on system algorithm designers.

Hard Processor System (HPS)

The 20-nm HPS strikes a balance between enabling maximum software compatibility with 28-nm SoCs while still improving upon the 28-nm HPS architecture. These improvements address the requirements of the next generation target markets such as wireless and wireline communications, compute and storage equipment, broadcast and military in terms of performance, memory bandwidth, connectivity via backplane and security.

- Hard memory controller with support for DDR3, DDR4 and optional error correction code (ECC) support
- Multiport Front End (MPFE) Scheduler interface to the hard memory controller
- 8-channel direct memory access (DMA) controller
- QSPI flash controller with SIO, DIO, QIO SPI Flash support
- NAND flash controller (ONFI 1.0 or later) with DMA and ECC support, updated to support 8 and 16-bit Flash devices and new command DMA to offload CPU for fast power down recovery
- Updated SD/SDIO/MMC controller to eMMC 4.5 with DMA with CE-ATA digital command support
- 3 10/100/1000 Ethernet media access control (MAC) with DMA
- 2 USB On-the-Go (OTG) controller with DMA
- 5 I^2C controller (3 can be used by EMAC for MIO to external PHY)
- 2 UART 16550 Compatible
- 4 serial peripheral interface (SPI) (2 Master, 2 Slaves)
- 54 programmable general-purpose I/O (GPIO)
- 48 I/O direct share I/O allows HPS peripherals to connect directly to I/O
- 7 general-purpose timers
- 4 watchdog timers
- Anti-tamper, Secure Boot, Encryption (AES) and Authentication (SHA)

- **HPS to FPGA Interconnect Backbone**

  Although the HPS and the Logic Core can operate independently, they are tightly coupled via a high-bandwidth system interconnect built from high-performance ARM AMBA AXI bus bridges. IP bus masters in the FPGA fabric have access to HPS bus slaves via the FPGA-to-HPS interconnect. Similarly, HPS bus masters have access to bus slaves in the core fabric via the HPS-to-FPGA bridge. Both bridges are AMBA AXI-3 compliant and support simultaneous read and write transactions. Up to three masters within the core fabric can share the HPS SDRAM controller with the processor. Additionally, the processor can be used to configure the core fabric under program control via a dedicated 32-bit configuration port.

- **HPS-to-FPGA**—configurable 32-, 64-, or 128-bit Avalon/AMBA AXI interface allows high bandwidth HPS master transactions to Logic Core
- **LW HPS-to-FPGA**—Light Weight 32-bit AXI interface suitable for low latency register accesses from HPS to soft peripherals in logic core
- **FPGA-to-HPS**—configurable 32-, 64-, or 128-bit AMBA AXI interface
- **FPGA-to-HPS SDRAM controller**—up to 3 masters (command ports), 3x 64-bit read data ports and 3x 64-bit write data ports
- **32-bit FPGA configuration manager**
- **Security**

A number of new security features have been introduced for anti-tamper management, secure boot, encryption (AES), and authentication (SHA).

Power Management

Arria 10 devices leverage the advanced 20 nm process technology, a low 0.9 V core power supply, an enhanced core architecture, and several optional power reduction techniques to reduce total power consumption by as much as 40% compared to Arria V devices and as much as 60% compared to Stratix V devices.

The optional power reduction techniques in Arria 10 devices include:

- **SmartVoltage ID**—a code is programmed into each device during manufacturing that allows a smart regulator to operate the device at lower core V_{CC} while maintaining performance
- **Programmable Power Technology**—non-critical timing paths are identified by the Quartus II software and the logic in these paths is biased for low power instead of high performance
- **V_{CC} PowerManager**—allows devices to be run at lower core voltage to trade performance for power savings
- **Low Static Power Options**—devices are available with either standard static power or low static power while maintaining performance

Furthermore, Arria 10 devices feature Altera's industry-leading low power transceivers and include a number of hard IP blocks that not only reduce logic resources but also deliver substantial power savings compared to soft implementations. In general, hard IP blocks consume up to 50% less power than the equivalent soft logic implementations.

Incremental Compilation

The Quartus II software incremental compilation feature reduces compilation time by up to 70% and preserves performance to ease timing closure.

Incremental compilation supports top-down, bottom-up, and team-based design flows. The incremental compilation feature facilitates modular hierarchical and team-based design flows where different designers compile their respective sections of a design in parallel. Furthermore, different designers or IP providers can develop and optimize different blocks of the design independently. These blocks can then be imported into the top level project. The incremental compilation feature enables the partial reconfiguration flow for Arria 10 devices.

Configuration and Configuration via Protocol Using PCI Express

Arria 10 device configuration is improved for ease-of-use, speed, and cost. The devices can be configured through a variety of techniques such as active and passive serial, fast passive parallel, JTAG, and configuration via protocol using PCI Express including Gen3.

Configuration via protocol (CvP) using PCI Express allows the FPGA to be configured across the PCI Express bus, simplifying the board layout and increasing system integration. Making use of the embedded PCI Express hard IP, this technique allows the PCI Express bus to be powered up and active within the 100 ms time allowed by the PCI Express specification. Arria 10 devices also support partial reconfiguration across the PCI Express bus which reduces system down time by keeping the PCI Express link active while the device is being reconfigured.

Table 16: Arria 10 Device Configuration Modes

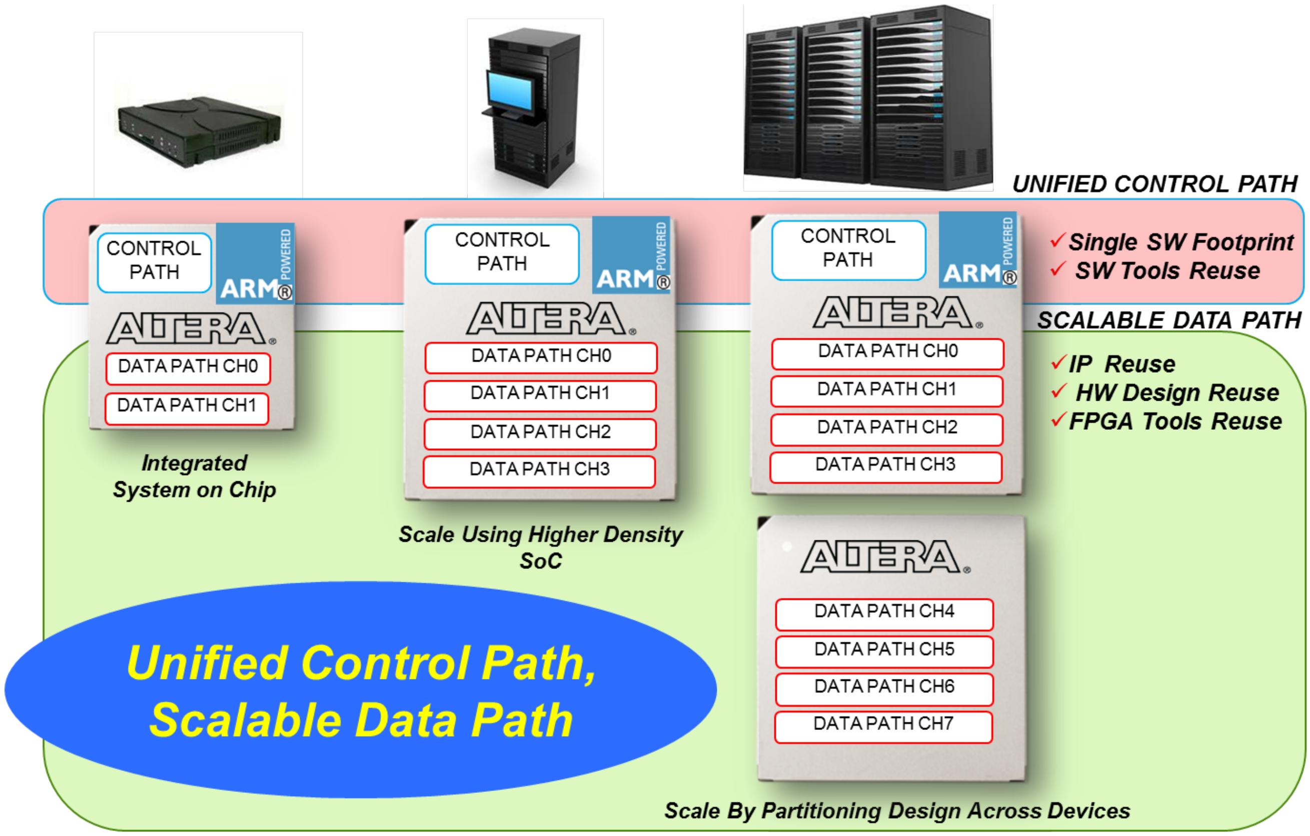
Mode	Compression	Encryption	Remote Update	Data Width (bits)	Maximum DCLK Rate (MHz)	Maximum Data Rate (Mbps)
Active Serial	Yes	Yes	Yes	1, 4	100	400
Passive Serial	Yes	Yes	—	1	125	125
Passive Parallel	Yes	Yes	Parallel flash loader	8, 16, 32	125	4000
Configuration via PCI Express	—	Yes	Yes	1, 2, 4, 8	—	4000
JTAG	—	—	—	1	33	33

Partial and Dynamic Reconfiguration

Partial reconfiguration allows you to reconfigure part of the FPGA while other sections continue running. This capability is required in systems where uptime is critical, because it allows you to make updates or adjust functionality without disrupting services.

In addition to lowering power and cost, partial reconfiguration also increases the effective logic density by removing the necessity to place in the FPGA those functions that do not operate simultaneously. Instead, these functions can be stored in external memory and loaded as needed. This reduces the size of the required FPGA by allowing multiple applications on a single FPGA, saving board space and reducing power. The partial reconfiguration process is built on top of the proven incremental compile design flow in the Quartus II design software.

Figure 10: Unified Control Path and Scalable Data Path



SoCs and FPGAs can be used across product platforms from low cost customer premise equipment to metro and access service provider equipment all the way to core and transmission equipment. For example, the low-cost Cyclone® V SoC offers a fully integrated system-on-a-chip device for the low end of a product portfolio that is ideal for customer premise, small cell routers, and enterprise routing. On the other end of the spectrum, Arria 10 and Stratix 10 SoCs offer performance and a high level of system integration on the high end of the product portfolio for access, networking, and transmission equipment.

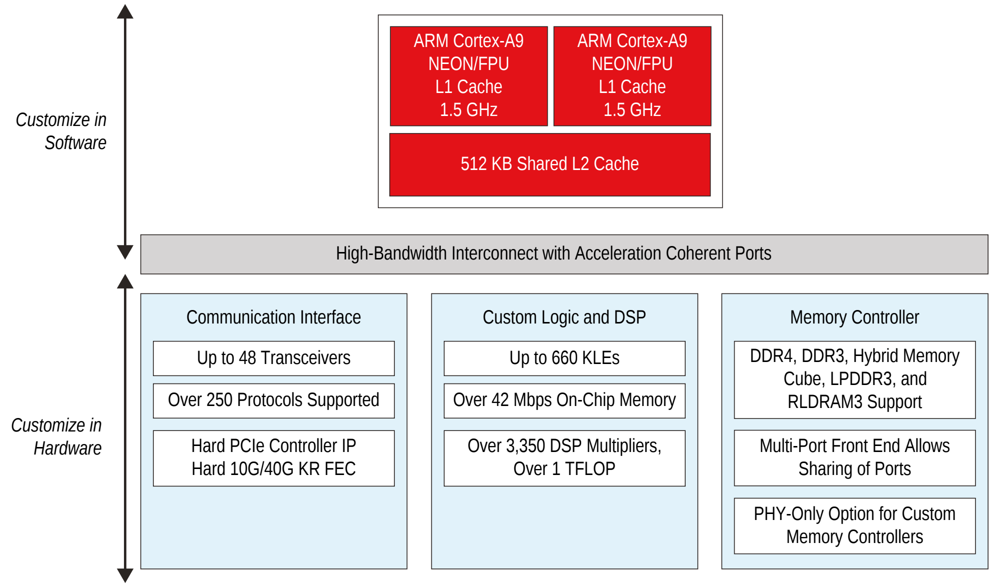
Unified Control: Because all 28-nm and 20-nm SoCs feature a common Dual ARM Cortex-A9 based HPS, there is extensive software tool reuse, operating system board support packages (BSP) reuse and a high degree of software code compatibility across the devices and the end product portfolio.

Scalable Datapath: Altera's SoC offers a portfolio of devices that meet the price, power, performance, logic density, memory bandwidth, and transceiver bandwidth of an entire product portfolio. This scalability both simplifies the system architecture and enhances productivity through design reuse and protocol IP reuse.

Differentiation through Customization

Designers today can choose between many competing technologies: off the shelf processors, ASSPs, ASICs, and SoCs. Altera's SoCs stand out from these competing technologies because they allow maximum customization. Designers can implement their intellectual property in software running on the ARM or in hardware running on the programmable logic. The high speed serial I/O and memory interfaces allow a high degree of customization and flexibility. Designers can choose a standard protocol or memory standard or they can implement a custom protocol or memory controller and still use the embedded PHY circuitry to bypass the controller logic. Altera offers fully characterized turnkey IP cores for a number of communication interfaces, memories, and DSP functions, allowing Altera devices to offer the largest variety of interface and feature support than any off the shelf processor or ASSP. The design cycles for Altera's SoCs are a fraction of ASIC design cycles and offer a much lower risk path compared to an ASIC.

Figure 11: Differentiation through Customization



A New, More Productive DSP Design Flow

With Altera's SoCs, a more productive design flow for DSP design is now available. For the first time, DSP and embedded developers who may be unfamiliar to FPGA and HDL design can develop hardware and take advantage of the remarkable DSP performance available with Altera's SoCs.

In this design flow, DSP and embedded developers begin by running DSP algorithms directly on the ARM HPS. This a natural place to begin as, in many cases, C/C++ are the very languages in which these algorithms have been conceived in the first place. The Dual Core ARM Cortex-A9 MPCore features a double precision FPU and a NEON co-processor for 128-bit SIMD co-processor and is ideal for closed loop control, audio, video, and multimedia processing. The inherent productivity of software design cycles and iterations as compared to FPGA compilation times reduces system compile times drastically. When more performance is required, these software algorithms can be then profiled to identify bottlenecks and subsequently become candidates for hardware acceleration. Hardware accelerators can share data and computed results directly with ARM processor's L2 Cache via the Acceleration Coherency Port (ACP) that manages data coherency without having to incur the penalty of a full L2 Cache flush.