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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	427200
Number of Logic Elements/Cells	1150000
Total RAM Bits	68857856
Number of I/O	624
Number of Gates	-
Voltage - Supply	0.87V ~ 0.93V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	1932-BBGA, FCBGA
Supplier Device Package	1932-FBGA, FC (45x45)
Purchase URL	https://www.e-xfl.com/product-detail/intel/10at115u2f45e2sges

Arria 10 Family Variants

Arria 10 devices are available in GX, GT, and SX variants.

- **Arria 10 GX** devices deliver over 500 MHz core fabric performance and 2666 Mbps DDR4 external memory interface performance across the industrial temperature range, while providing over 1.1 million logic elements and 96 general purpose transceivers. Every transceiver is capable of 17.4 Gbps for short reach applications and 16.0 Gbps across the backplane. These devices are optimized for a broad range of applications such as wireless remote radio heads, broadcast studio equipment, 40G/100G communication systems, server acceleration, and medical imaging.
- **Arria 10 GT** devices have the same core performance and feature set as Arria 10 GX devices, with the added capability of sixteen 28.05-Gbps short reach transceivers for chip-to-chip and chip-to-module applications. The 28.05-Gbps transceivers are ideal for interfacing with the emerging CFP2 and CFP4 optical modules that typically require four lanes at data rates in the range of 25 to 28 Gbps. Backplane driving capability is also increased to 17.4 Gbps in Arria 10 GT devices.
- **Arria 10 SX** devices have a feature set that is similar to Arria 10 GX devices plus an ARM Cortex-A9 hard processor system.

Common to all Arria 10 family variants is the enhanced logic array utilizing Altera's adaptive logic module (ALM) and a rich set of high performance building blocks that includes 20Kbit (M20K) internal memory blocks, variable precision DSP blocks, fractional synthesis and integer PLLs, hard memory PHY and controllers for external memory interfaces, and general purpose I/O cells. These building blocks are interconnected by an updated version of Altera's superior multi-track routing architecture and comprehensive fabric clocking network. All devices support in-system, fine-grained partial reconfiguration of the logic array, allowing logic to be added and removed from the system during operation.

All family variants also contain high speed serial transceivers, containing both the physical medium attachment (PMA) and the physical coding sublayer (PCS), which can be used to implement a variety of industry standard and proprietary protocols. In addition to the hard PCS, Arria 10 devices contain multiple instantiations of PCI Express hard IP that supports Gen1/Gen2/Gen3 rates in x1/x2/x4/x8 lane configurations. The hard PCS and hard PCI Express IP free up valuable core logic resources, save power, and increase productivity for the user.

Improvements in Arria 10 FPGAs and SoCs

Altera has combined in-house innovations with TSMC's advanced 20-nm process technology to deliver major improvements over Arria V FPGAs and SoCs in nearly every category.

Table 1: Key Features of Arria 10 Devices Compared to Arria V Devices

Feature	Arria V FPGAs and SoCs	Arria 10 FPGAs and SoCs
Process technology	28-nm TSMC	20-nm TSMC
Processor core	Dual ARM Cortex-A9 MPCore™	Dual ARM Cortex-A9 MPCore
Processor performance	800 MHz	1.5 GHz
Logic core performance	300 MHz	500 MHz
Power dissipation	1x	0.6x

Feature	Arria V FPGAs and SoCs	Arria 10 FPGAs and SoCs
Logic density	504 KLE	1150 KLE
Embedded memory	34 Mbits	53 Mbits
18x19 multipliers	2186	3356
Maximum transceivers	36	96
Maximum transceiver data rate (chip to chip)	10.3125 Gbps	28.05 Gbps
Memory devices supported	DDR3 SDRAM @ 667 MHz/1333 Mbps	DDR4 SDRAM @ 1333 MHz/2666 Mbps DDR3 SDRAM @ 1067 MHz/2133 Mbps Hybrid Memory Cube (HMC)
Hard protocol IP	2 EMACs PCI Express Gen3 x8 (Arria V GZ) PCI Express Gen2 x4/Gen1 x8 (Arria V GX/GT/SX/ST)	3 EMACs PCI Express Gen3 x8 10GBASE-KR/40GBASE-KR4 FEC Interlaken PCS

These features result in the following improvements:

- **Improved Core Logic Performance**: Arria 10 devices offer over 60% improved core performance compared to the previous generation
- **Improved Processor Performance**: Arria 10 SoCs provide 87% improvement in processor performance
- **Improved Processor Power Efficiency**: At 20 nm, the Dual Core ARM Cortex-A9 Processor provides the best power efficiency for any GHz-class processor in the industry
- **Lower Power**: Arria 10 devices deliver up to 40% lower power compared to prior-generation mid-range FPGAs and SoCs, enabled by 20-nm process technology advancements and a variety of innovative power-management options
- **Higher Density**: Arria 10 devices provide a higher level of integration with up to 1150K logic elements (LEs), up to 53 Mbits of embedded memory, and over 3350 18x19 multipliers
- **Improved Transceiver Bandwidth**: Arria 10 devices support chip-to-chip rates up to 28 Gbps and backplane rates up to 17.4 Gbps
- **Improved Memory Bandwidth with DDR4 Support**: Arria 10 devices support DDR4 memory up to 1333 MHz/ 2666 Mbps and feature support for the emerging transceiver-based Hybrid Memory Cube (HMC)
- **Improved DSP Performance**: With over 1.0 TeraFLOPs of single-precision DSP performance, Arria 10 devices deliver a 4 times increase in DSP performance
- **Additional Protocol Support for Hard IP**: Arria 10 devices feature an advanced transceiver architecture with added hard IP support for PCIe Gen3, Interlaken PCS, and 10GBASE-KR/40GBASE-KR4 FEC

Target Markets for Arria 10 FPGAs and SoCs

Arria 10 devices meet the performance, power, and bandwidth requirements of next generation wireless infrastructure, broadcast, compute and storage, networking, and medical and military equipment.

Feature	Description
Low power serial transceivers	• Continuous operating range of 611 Mbps to 17.4 Gbps for Arria 10 GX devices • Continuous operating range of 611 Mbps to 28.05 Gbps for Arria 10 GT devices • Backplane support up to 16.0 Gbps for Arria 10 GX devices • Backplane support up to 17.4 Gbps for Arria 10 GT devices • Extended range down to 125 Mbps with oversampling • ATX transmit PLLs with user-configurable fractional synthesis capability • Electronic Dispersion Compensation (EDC) for XFP, SFP+, QSFP, and CFP optical module support • Adaptive linear and decision feedback equalization • Transmit pre-emphasis and de-emphasis • Dynamic partial reconfiguration of individual transceiver channels • On-chip instrumentation (EyeQ non-intrusive data eye monitoring)
General purpose I/Os	• 1.6 Gbps LVDS—every pair can be configured as an input or output • 1333 MHz/2666 Mbps DDR4 external memory interface • 1067 MHz/2133 Mbps DDR3 external memory interface • 1.2 V to 3.0 V single-ended LVCMOS/LVTTL interfacing • On-chip termination (OCT)
Embedded hard IP	• PCIe Gen1/Gen2/Gen3 complete protocol stack, x1/x2/x4/x8 end point and root port • DDR4/DDR3/DDR3L/DDR3U/RLDRAM 3/LPDDR3 hard memory controller (RLDRAM2/QDR II+ using soft memory controller) • Multiple hard IP instantiations in each device • Dual-core ARM Cortex-A9 processor (Arria 10 SX devices only)
Transceiver hard IP	• 10GBASE-KR/40GBASE-KR4 Forward Error Correction (FEC) • 10G Ethernet PCS • PCI Express PIPE interface • Interlaken PCS • Gigabit Ethernet PCS • Deterministic latency support for Common Public Radio Interface (CPRI) PCS • Fast lock-time support for Gigabit Passive Optical Networking (GPON) PCS • 8B/10B, 64B/66B, 64B/67B encoders and decoders • Custom mode support for proprietary protocols
Power management	• SmartVoltage ID • V_{CC} PowerManager • Low static power device options • Programmable Power Technology • Quartus® II integrated PowerPlay power analysis
High performance core fabric	• Enhanced adaptive logic module (ALM) with 4 registers • Improved multi-track routing architecture reduces congestion and improves compile times • Hierarchical core clocking architecture • Fine-grained partial reconfiguration

Table 3: Arria 10 SoC-Specific Device Features

Feature	Description

Dual-core ARM Cortex-A9 MPCore processor unit	• 2.5 MIPS/MHz instruction efficiency
	• CPU frequency 1.2 GHz with 1.5 GHz via overdrive
	  ◦ At 1.5 GHz total performance of 7500 MIPS
	• ARMv7-A architecture
	  ◦ Runs 32-bit ARM instructions
	  ◦ 16-bit and 32-bit Thumb instructions for 30% reduction in memory footprint
	  ◦ Jazelle® RCT execution architecture with 8-bit Java bytecodes
	  ◦ Superscalar, variable length, out-of-order pipeline with dynamic branch prediction
	• ARM NEON™ media processing engine
	• Single- and double-precision floating-point unit
	• CoreSight™ debug and trace technology
	• Snoop Control Unit (SCU) and Acceleration Coherency Port (ACP)

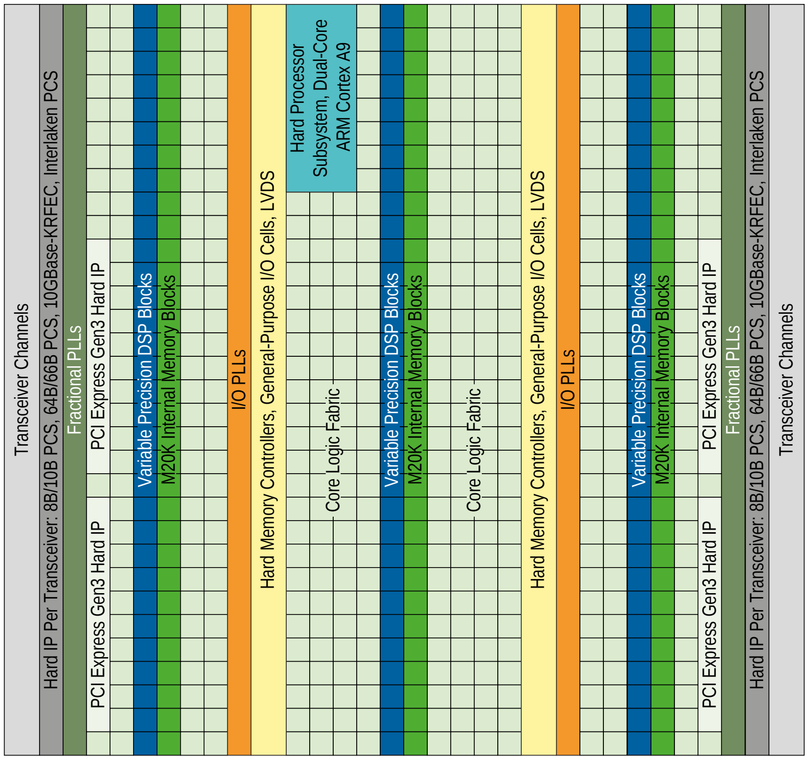
Cache	• L1 Cache
	  ◦ 32 KB of instruction cache
	  ◦ 32 KB of L1 data cache
	  ◦ Parity checking
	• L2 Cache
	  ◦ 512 KB shared
	  ◦ 8-way set associative
	  ◦ SEU Protection with parity on TAG ram and ECC on data RAM
	  ◦ Cache lockdown support

On-Chip Memory	• 256 KB of scratch on-chip RAM • 64 KB on-chip ROM

Feature	Description

Interconnect to Logic Core	• High-performance ARM AMBA® AXI bus bridges
	  • AMBA AXI-3 compliant
	  • Allows both independent and tightly coupled operation between HPS and logic core
	  • Support simultaneous read and write transactions
	• FPGA-to-HPS Bridge
	  • Allows IP bus masters in the logic core to access to HPS bus slaves
	  • Configurable 32-, 64-, or 128-bit AMBA AXI interface
	  • Up to three masters within the core fabric can share the HPS SDRAM controller with the processor
	• HPS-to-FPGA Bridge
	  • Allows HPS bus masters to access bus slaves in core fabric
	  • Configurable 32-, 6-4, or 128-bit Avalon®/AMBA AXI interface allows high-bandwidth HPS master transactions to logic core
	• Configuration Bridge
	  • Allows configuration manager in HPS to configure the logic core under program control via dedicated 32-bit configuration port
	• Light Weight HPS-to-FPGA Bridge
	  • Light weight 32-bit AXI interface suitable for low-latency register accesses from HPS to soft peripherals in logic core
	• FPGA-to-HPS SDRAM controller Bridge
	  • Up to three masters (command ports), 3x 64-bit read data ports, and 3x 64-bit write data ports

Figure 3: Arria 10 SoC Architecture Block Diagram



Arria 10 FPGA Family Plan

Table 4: Arria 10 GX and Arria 10 GT FPGA Family Plan

Device Name [1]	Logic Elements (KLE)	Registers	M20K Blocks	M20K Mbits	MLAB Counts	MLAB Mbits	18x19 Multipliers [2]	Maximum GPIOs	Maximum XCVR (17.4G, 28.05G)	fPLLs	I/O PLLs	PCIe HIPs
GX 160 (10AX016)	160	246,040	440	9	1,680	1	312	288	12, 0	6	6	1
GX 220 (10AX022)	220	326,040	583	11	2,227	1	384	288	12, 0	6	6	1
GX 270 (10AX027)	270	406,480	750	15	3,968	2	1,660	384	24, 0	8	8	2

(1) The text in parentheses is the part number reference for this device.
(2) The number of 27x27 multipliers is one-half the number of 18x19 multipliers.

Table 8: Arria 10 SX SoC Family Plan

Device Name [10]	Logic Elements (KLE)	Registers	M20K Blocks	M20K Mbits	MLAB Counts	MLAB Mbits	18x19 Multipliers [11]	Maximum GPIOs	Maximum XCVR (17.4G, 28.05G)	fPLLs	I/O PLLs	PCIe HIPs
SX 160 (10AS016)	160	246,040	440	9	1,680	1	312	288	12, 0	6	6	1
SX 220 (10AS022)	220	326,040	583	11	2,227	1	384	288	12, 0	6	6	1
SX 270 (10AS027)	270	406,480	750	15	3,968	2	1,660	384	24, 0	8	8	2
SX 320 (10AS032)	320	478,640	891	17	4,673	3	1,970	384	24, 0	8	8	2
SX 480 (10AS048)	480	730,880	1,438	28	7,137	4	2,736	492	36, 0	12	12	2
SX 570 (10AS057)	570	868,320	1,800	35	8,241	5	3,046	588	48, 0	16	16	2
SX 660 (10AS066)	660	1,005,800	2,133	42	9,345	6	3,356	588	48, 0	16	16	2

(10) The text in parentheses is the part number reference for this device.
(11) The number of 27x27 multipliers is one-half the number of 18x19 multipliers.

Table 9: Arria 10 SX SoC Family Package Plan

Cell legend: General Purpose I/Os, High-Voltage I/Os, LVDS Pairs, Transceivers [12] [13] [14] [15] [16]

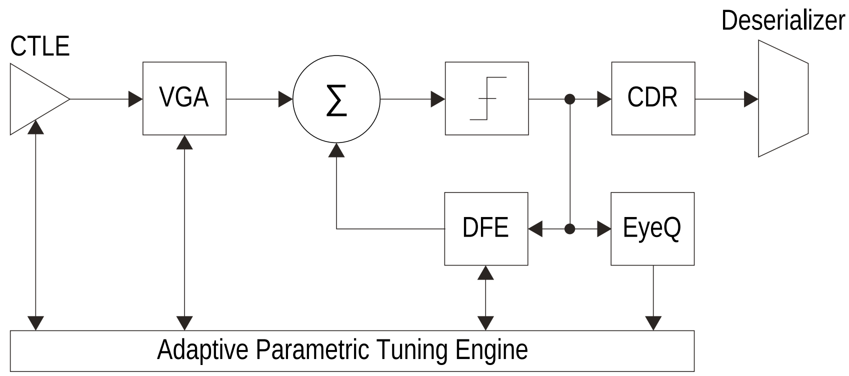
Device [10]	U19 (U484) (19x19 mm^2)	F27 (F672) (27x27 mm^2)	F29 (F780) (29x29 mm^2)	F34 (F1152) (35x35 mm^2)	F35 (F1152) (35x35 mm^2) [17]	F36 (F1152) (35x35 mm^2) [17] 72-bit HPS DDR	F40 (F1517) (40x40 mm^2)
SX 160 (10AS016)	192,48,72,6	240,48,96,12	288,48,120,12	—	—	—	—
SX 220 (10AS022)	192,48,72,6	240,48,96,12	288,48,120,12	—	—	—	—
SX 270 (10AS027)	—	240,48,96,12	360,48,156,12	384,48,168,24	384,48,168,24	—	—
SX 320 (10AS032)	—	240,48,96,12	360,48,156,12	384,48,168,24	384,48,168,24	—	—
SX 480 (10AS048)	—	—	360,48,156,12	492,48,222,24	396,48,174,36	—	—
SX 570 (10AS057)	—	—	—	492,48,222,24	396,48,174,36	—	588,48,270,48
SX 660 (10AS066)	—	—	—	492,48,222,24	396,48,174,36	432,48,192,36	588,48,270,48

Migration Between Arria 10 Devices and Stratix 10 Devices

You can start developing with Arria 10 devices and then move to Stratix 10 devices, because there is footprint compatibility between the Arria 10 and Stratix 10 packages. Contact Altera for more details about the migration possibilities between the two device families.

(12) All packages are ball grid arrays with 1.0 mm pitch, except for U19 (U484), which is 0.8 mm pitch.
(13) High-Voltage I/O pins are used for 3.3 V and 2.5 V interfacing.
(14) Each LVDS pair can be configured as either a differential input or a differential output.
(15) High-Voltage I/O pins and LVDS pairs are included in the General Purpose I/O count. Transceivers are counted separately.
(16) Each package column offers pin migration (common circuit board footprint) for all devices in the column.
(17) Devices in the F35 (F1152) package are pin migratable with devices in the F36 (F1152) package

Figure 6: Arria 10 Receiver Block Features



All link equalization parameters feature automatic adaptation using the new Altera Digital Adaptive Parametric Tuning (ADAPT) block to dynamically set DFE tap weights, CTLE, VGA Gain, and threshold voltages. Finally, optimal and consistent signal integrity is ensured by using the new hardened Precision Signal Integrity Calibration Engine (PreSICE) to automatically calibrate all transceiver circuit blocks on power-up to give the most link margin and ensure robust, reliable, and error-free operation.

Table 10: Arria 10 Transceiver PMA Features

Feature	Capability
Chip-to-Chip Data Rates	125 Mbps to 17.4 Gbps (Arria 10 GX devices) 125 Mbps to 28.05 Gbps (Arria 10 GT devices)
Backplane Support	Drive backplanes at data rates up to 17.4 Gbps, including 10GBASE-KR compliance
Optical Module Support	SFP+/SFP, XFP, CXP, QSFP/QSFP28, CFP/CFP2/CFP4
Cable Driving Support	SFP+ Direct Attach, PCI Express over cable, eSATA
Transmit Pre-Emphasis	5-tap transmit pre-emphasis and de-emphasis to compensate for system channel loss
Continuous Time Linear Equalizer (CTLE)	Dual mode, high-gain, and high-data rate, linear receive equalization to compensate for system channel loss
Decision Feedback Equalizer (DFE)	7-fixed and 4-floating tap DFE to equalize backplane channel loss in the presence of crosstalk and noisy environments
Altera Digital Adaptive Parametric Tuning (ADAPT)	Fully digital adaptation engine to automatically adjust all link equalization parameters—including CTLE, DFE, and VGA blocks—that provide optimal link margin without intervention from user logic
Precision Signal Integrity Calibration Engine (PreSICE)	Hardened calibration controller to quickly calibrate all transceiver control parameters on power-up, which provides the optimal signal integrity and jitter performance
ATX Transmit PLLs	Low jitter ATX (inductor-capacitor) transmit PLLs with continuous tuning range to cover a wide range of standard and proprietary protocols

Feature	Capability
Fractional PLLs	On-chip fractional frequency synthesizers to replace on-board crystal oscillators and reduce system cost
Digitally Assisted Analog CDR	Superior jitter tolerance with fast lock time
On-Die Instrumentation— EyeQ and Jitter Margin Tool	Simplify board bring-up, debug, and diagnostics with non-intrusive, high-resolution eye monitoring (EyeQ). Also inject jitter from transmitter to test link margin in system.
Dynamic Partial Reconfiguration (DPRIO)	Allows for independent control of each transceiver channel Avalon memory-mapped interface for the most transceiver flexibility
Multiple PCS-PMA and PCS-PLD interface widths	8-, 10-, 16-, 20-, 32-, 40-, or 64-bit interface widths for flexibility of deserialization width, encoding, and reduced latency

PCS Features

Arria 10 PMA channels interface with core logic through configurable PCS interface layers.

Multiple gearbox implementations are available to decouple PCS and PMA interface widths. This feature provides the flexibility to implement a wide range of applications with 8-, 10-, 16-, 20-, 32-, 40-, or 64-bit interface widths. Arria 10 FPGAs contain PCS hard IP to support a wide range of standard and proprietary protocols.

The Standard PCS mode provides support for 8B/10B encoded applications up to 12.5 Gbps. The Enhanced PCS mode supports applications up to 17.4 Gbps. In addition, for highly customized implementations, a PCS Direct mode provides a fixed width interface up to 64 bits wide to core logic to allow for custom encoding including support for standards up to 28.05 Gbps.

The enhanced PCS includes an integrated 10GBASE-KR/40GBASE-KR4 Forward Error Correction (FEC) block.

The following table lists some of the key PCS features of Arria 10 transceivers that can be used in a wide range of standard and proprietary protocols from 125 Mbps to 28.05 Gbps.

Table 11: Arria 10 Transceiver PCS Features

PCS Protocol Support	Data Rate (Gbps)	Transmitter Data Path	Receiver Data Path
Standard PCS	0.125 to 12.5	Phase compensation FIFO, byte serializer, 8B/10B encoder, bit-slipper, channel bonding	Rate match FIFO, word-aligner, 8B/10B decoder, byte deserializer, byte ordering
PCI Express Gen1/Gen2 x1, x4, x8	2.5 and 5.0	Same as Standard PCS plus PIPE 2.0 interface to core	Same as Standard PCS plus PIPE 2.0 interface to core

Table 13: Arria 10 Internal Embedded Memory Block Configurations

MLAB (640 bits)	M20K (20 Kbits)
64 x 10 (supported through emulation)	16K x 1
32 x 20	8K x 2
	4K x 5
	2K x 10
	1K x 20
	512 x 40

The Quartus II software simplifies design reuse by automatically mapping memory blocks from previous generations of devices into the Arria 10 MLAB and M20K blocks.

Variable Precision DSP Block

The Arria 10 DSP blocks are based upon the Variable Precision DSP Architecture used in Altera's previous generation Arria V FPGAs. The blocks can be configured to natively support signal processing with precision ranging from 18x19 up to 54x54. A pipeline register has been added to increase the maximum operating frequency of the DSP block and reduce power consumption.

Each DSP block can be independently configured at compile time as either dual 18x19 or a single 27x27 multiply accumulate. With a dedicated 64-bit cascade bus, multiple variable precision DSP blocks can be cascaded to implement even higher precision DSP functions efficiently. The following table shows how different precisions are accommodated within a DSP block, or by utilizing multiple blocks.

Table 14: Variable Precision DSP Block Configurations

Multiplier Size	DSP Block Resources	Expected Usage
18x19 bits	1/2 of Variable Precision DSP Block	Medium precision fixed point
27x27 bits	1 Variable Precision DSP Block	High precision fixed or Single Precision floating point
19x36 bits	1 Variable Precision DSP Block with external adder	Fixed point FFTs
36x36 bits	2 Variable Precision DSP Blocks with external adder	Very high precision fixed point
54x54 bits	4 Variable Precision DSP Blocks with external adder	Double Precision floating point

Complex multiplication is very common in DSP algorithms. One of the most popular applications of complex multipliers is the FFT algorithm. This algorithm has the characteristic of increasing precision requirements on only one side of the multiplier. The Variable Precision DSP block supports the FFT algorithm with proportional increase in DSP resources as the precision grows.

Table 15: Complex Multiplication With Variable Precision DSP Block

Complex Multiplier Size	DSP Block Resources	FFT Usage
18x19 bits	2 Variable Precision DSP Blocks	Resource optimized FFTs
27x27 bits	4 Variable Precision DSP Blocks	Highest precision FFT stages and single precision floating point

For FFT applications with high dynamic range requirements, the Altera FFT MegaCore® function offers an option of single precision floating point implementation, with resource usage and performance similar to high precision fixed point implementations.

Other features of the DSP block include:

- Hard 18-bit and 25-bit pre-adders
- 64-bit dual accumulator (for separate I, Q product accumulations)
- Cascaded output adder chains for 18- and 27-bit FIR filters
- Embedded coefficient registers for 18- and 27-bit coefficients
- Fully independent multiplier outputs
- Inferability using HDL templates supplied by the Quartus II software for most modes

The Variable Precision DSP block is ideal to support the growing trend towards higher bit precision in high performance DSP applications. At the same time, it can efficiently support the many existing 18-bit DSP applications, such as high definition video processing and remote radio heads. Arria 10 devices, with the Variable Precision DSP block architecture, can efficiently support many different precision levels, up to and including floating point implementations. This flexibility can result in increased system performance, reduced power consumption, and reduce architecture constraints on system algorithm designers.

Hard Processor System (HPS)

The 20-nm HPS strikes a balance between enabling maximum software compatibility with 28-nm SoCs while still improving upon the 28-nm HPS architecture. These improvements address the requirements of the next generation target markets such as wireless and wireline communications, compute and storage equipment, broadcast and military in terms of performance, memory bandwidth, connectivity via backplane and security.

Key Features of 20-nm HPS

The following features are new in the 20-nm Hard Processor System compared to the 28-nm SoCs:

- **Increased Performance and Overdrive Capability**

  While the nominal processor frequency is 1.2 GHz, the 20 nm HPS offers an “overdrive” feature which enables an even higher processor operating frequency. For this a higher supply voltage value is required that is unique to the HPS and may require a separate regulator.

- **Increased Processor Memory Bandwidth and DDR4 Support**

  Up to 64-bit DDR4 memory @ 2666 Mbps is available for the processor. The hard memory controller for the HPS comprises a multi-port front end that manages connections to a single port memory controller. The multi-port front end allows logic core and the HPS share ports and thereby the available bandwidth of the memory controller.

- **Flexible I/O Sharing**

  An advanced I/O pin muxing scheme allows improved sharing of I/O between the HPS and the core logic. The following types of I/O are available for SoC:

  Dedicated I/O (15)—These I/Os are physically located inside the HPS block and are not accessible to logic within the core. The 15 dedicated I/Os are used for HPS clock, resets, and interfacing with boot devices, QSPI, and SD/MMC

  Direct Shared I/O (48)—These shared I/Os are located closest to the HPS block and are ideal for high speed HPS peripherals such as EMAC, USB, and others. There is one bank of 48 I/Os that supports direct sharing where the 48 I/Os can be shared 12 I/Os at a time.

  Standard (Shared) I/O (All other)—All standard I/Os can be shared by the HPS peripherals and any logic within the core. For designs where more than 48 I/Os are required to fully use all the peripherals in the HPS, these I/Os can be connected through the core logic.

- **EMAC Core**

  A third EMAC core is available in the HPS. Three EMAC cores enable an application to support two redundant Ethernet connections; for example, backplane, or two EMAC cores for managing IEEE 1588 time stamp information while allowing a third EMAC core for debug and configuration. All three EMACs can potentially share the same time stamps, simplifying the 1588 time stamping implementation. A new serial time stamp interface allows core logic to access and read the time stamp values. The integrated EMAC controllers can be connected to external Ethernet PHY through the provided MDIO or I^2C interface.

- **On-Chip Memory**

  The on-chip memory is updated to 256 KB support and can support larger data sets and real time algorithms

- **ECC Enhancements**

  Improvements in L2 Cache ECC management allow identification of errors down to the address level. ECC enhancements also enable improved error injection and status reporting via the introduction of new memory mapped access to syndrome and data signals.

- **HPS to FPGA Interconnect Backbone**

  Although the HPS and the Logic Core can operate independently, they are tightly coupled via a high-bandwidth system interconnect built from high-performance ARM AMBA AXI bus bridges. IP bus masters in the FPGA fabric have access to HPS bus slaves via the FPGA-to-HPS interconnect. Similarly, HPS bus masters have access to bus slaves in the core fabric via the HPS-to-FPGA bridge. Both bridges are AMBA AXI-3 compliant and support simultaneous read and write transactions. Up to three masters within the core fabric can share the HPS SDRAM controller with the processor. Additionally, the processor can be used to configure the core fabric under program control via a dedicated 32-bit configuration port.

- **HPS-to-FPGA**—configurable 32-, 64-, or 128-bit Avalon/AMBA AXI interface allows high bandwidth HPS master transactions to Logic Core
- **LW HPS-to-FPGA**—Light Weight 32-bit AXI interface suitable for low latency register accesses from HPS to soft peripherals in logic core
- **FPGA-to-HPS**—configurable 32-, 64-, or 128-bit AMBA AXI interface
- **FPGA-to-HPS SDRAM controller**—up to 3 masters (command ports), 3x 64-bit read data ports and 3x 64-bit write data ports
- **32-bit FPGA configuration manager**
- **Security**

A number of new security features have been introduced for anti-tamper management, secure boot, encryption (AES), and authentication (SHA).

Power Management

Arria 10 devices leverage the advanced 20 nm process technology, a low 0.9 V core power supply, an enhanced core architecture, and several optional power reduction techniques to reduce total power consumption by as much as 40% compared to Arria V devices and as much as 60% compared to Stratix V devices.

The optional power reduction techniques in Arria 10 devices include:

- **SmartVoltage ID**—a code is programmed into each device during manufacturing that allows a smart regulator to operate the device at lower core V_{CC} while maintaining performance
- **Programmable Power Technology**—non-critical timing paths are identified by the Quartus II software and the logic in these paths is biased for low power instead of high performance
- **V_{CC} PowerManager**—allows devices to be run at lower core voltage to trade performance for power savings
- **Low Static Power Options**—devices are available with either standard static power or low static power while maintaining performance

Furthermore, Arria 10 devices feature Altera's industry-leading low power transceivers and include a number of hard IP blocks that not only reduce logic resources but also deliver substantial power savings compared to soft implementations. In general, hard IP blocks consume up to 50% less power than the equivalent soft logic implementations.

Incremental Compilation

The Quartus II software incremental compilation feature reduces compilation time by up to 70% and preserves performance to ease timing closure.

Incremental compilation supports top-down, bottom-up, and team-based design flows. The incremental compilation feature facilitates modular hierarchical and team-based design flows where different designers compile their respective sections of a design in parallel. Furthermore, different designers or IP providers can develop and optimize different blocks of the design independently. These blocks can then be imported into the top level project. The incremental compilation feature enables the partial reconfiguration flow for Arria 10 devices.

Configuration and Configuration via Protocol Using PCI Express

Arria 10 device configuration is improved for ease-of-use, speed, and cost. The devices can be configured through a variety of techniques such as active and passive serial, fast passive parallel, JTAG, and configuration via protocol using PCI Express including Gen3.

Configuration via protocol (CvP) using PCI Express allows the FPGA to be configured across the PCI Express bus, simplifying the board layout and increasing system integration. Making use of the embedded PCI Express hard IP, this technique allows the PCI Express bus to be powered up and active within the 100 ms time allowed by the PCI Express specification. Arria 10 devices also support partial reconfiguration across the PCI Express bus which reduces system down time by keeping the PCI Express link active while the device is being reconfigured.

Table 16: Arria 10 Device Configuration Modes

Mode	Compression	Encryption	Remote Update	Data Width (bits)	Maximum DCLK Rate (MHz)	Maximum Data Rate (Mbps)
Active Serial	Yes	Yes	Yes	1, 4	100	400
Passive Serial	Yes	Yes	—	1	125	125
Passive Parallel	Yes	Yes	Parallel flash loader	8, 16, 32	125	4000
Configuration via PCI Express	—	Yes	Yes	1, 2, 4, 8	—	4000
JTAG	—	—	—	1	33	33

Partial and Dynamic Reconfiguration

Partial reconfiguration allows you to reconfigure part of the FPGA while other sections continue running. This capability is required in systems where uptime is critical, because it allows you to make updates or adjust functionality without disrupting services.

In addition to lowering power and cost, partial reconfiguration also increases the effective logic density by removing the necessity to place in the FPGA those functions that do not operate simultaneously. Instead, these functions can be stored in external memory and loaded as needed. This reduces the size of the required FPGA by allowing multiple applications on a single FPGA, saving board space and reducing power. The partial reconfiguration process is built on top of the proven incremental compile design flow in the Quartus II design software.

Partial reconfiguration in Arria 10 devices is supported through the following configuration options:

- Partial reconfiguration through the FPP x16 I/O interface
- Partial reconfiguration using PCI Express

Dynamic reconfiguration in Arria 10 devices allows transceiver data rates, protocols and analog settings to be changed dynamically on a channel-by-channel basis while maintaining data transfer on adjacent transceiver channels. Dynamic reconfiguration is ideal for applications that require on-the-fly multi-protocol or multi-rate support, and both the PMA and PCS blocks within the transceiver can be reconfigured using this technique. Dynamic reconfiguration of the transceivers can be used in conjunction with partial reconfiguration of the FPGA to enable partial reconfiguration of both core and transceivers simultaneously.

Single Event Upset (SEU) Error Detection and Correction

Arria 10 devices offer robust and easy-to-use SEU error detection and correction circuitry.

The detection and correction circuitry includes protection for Configuration RAM (CRAM) programming bits and user memories. The CRAM is protected by a continuously running CRC error detection circuit with integrated ECC that automatically corrects one or two errors and detects higher order multi-bit errors. When more than two errors occur, correction is available through reloading of the core programming file, providing a complete design refresh while the FPGA continues to operate.

The physical layout of the Arria 10 CRAM array is optimized to make the majority of multi-bit upsets appear as independent single-bit or double-bit errors which are automatically corrected by the integrated CRAM ECC circuitry. In addition to the CRAM protection, the user memories also include integrated ECC circuitry and are layout optimized for error detection and correction.

Appendix: Arria 10 SoC Developers Corner

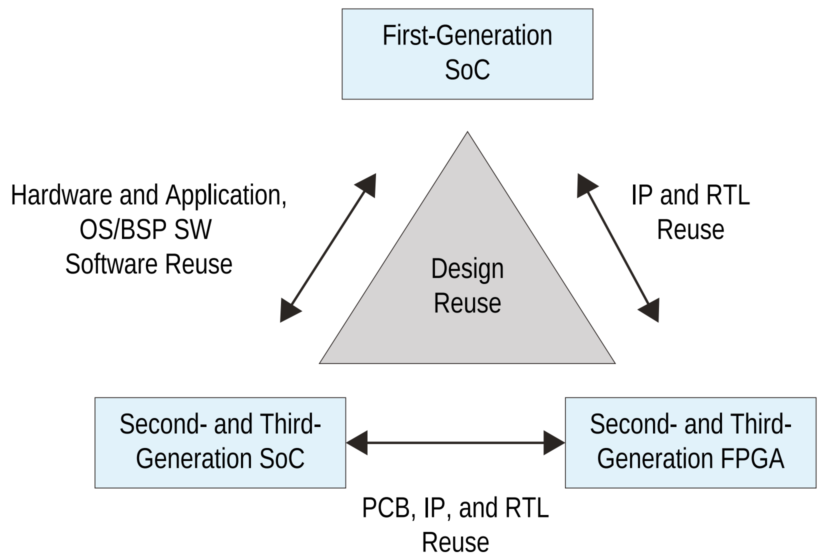
Altera's Arria 10 SoCs provide the combined benefits of programmable logic for high-speed data paths with ARM processor for intelligent control functions:

- High performance programmable core logic, hard memory controllers and high speed transceivers can be used to implement data path centric functions for 40G/100G systems including functions such as framing, bridging, aggregation, switching, traffic management, FEC, multirate aggregation, and data transmission.
- The integrated ARM based HPS implements intelligent control function and eliminates the need for a local processor, thereby reducing system power, form factor, and BOM cost. By adding intelligence to the data path, software on the ARM HPS manages and reduces system downtime and reduces the associated operating expenses. The Dual Core ARM Cortex-A9 based HPS comes with a rich set of embedded peripherals and associated device drivers for wide range of operating systems including Linux and VxWorks. The resulting board support packages can be used as the basis of a number of software applications such as:
    - Operations, Administration and Maintenance (OAM)
    - PCIe Root Port management
    - Remote Debug and System Update
    - Host offload and Algorithm acceleration
    - Chassis management
    - Routing and Look up management
    - Error handling and system downtime management
    - Rule management for deep packet inspection, packet parsing
    - Audio and Video Processing

Altera SoC: The Architecture of Choice When Productivity Matters

Productivity is the driving philosophy of Altera's Arria 10 SoC family. By reusing hardware, software, IP, and RTL across FPGAs and SoCs, you can reduce design effort and get products to market faster. The Dual Core ARM Cortex-A9 MPCore-based HPS is common to both 20- and 28-nm SoCs and facilitates extensive software code compatibility as well as tools and OS Board Support Package (BSP) reuse. The extensive tools and OS support available as part of Altera and ARM ecosystem and the fast iteration times inherent in software development (especially as compared to FPGA compile times) results in a highly productive embedded and DSP development flow. In addition, Altera offers high-level automated design flows for hardware development, such as the Altera OpenCL (a C-based hardware design flow) and DSP Builder (a model-based hardware design flow).

Figure 9: Hardware and Software Reuse



Altera's 20-nm SoCs and FPGAs can be reused in the following ways:

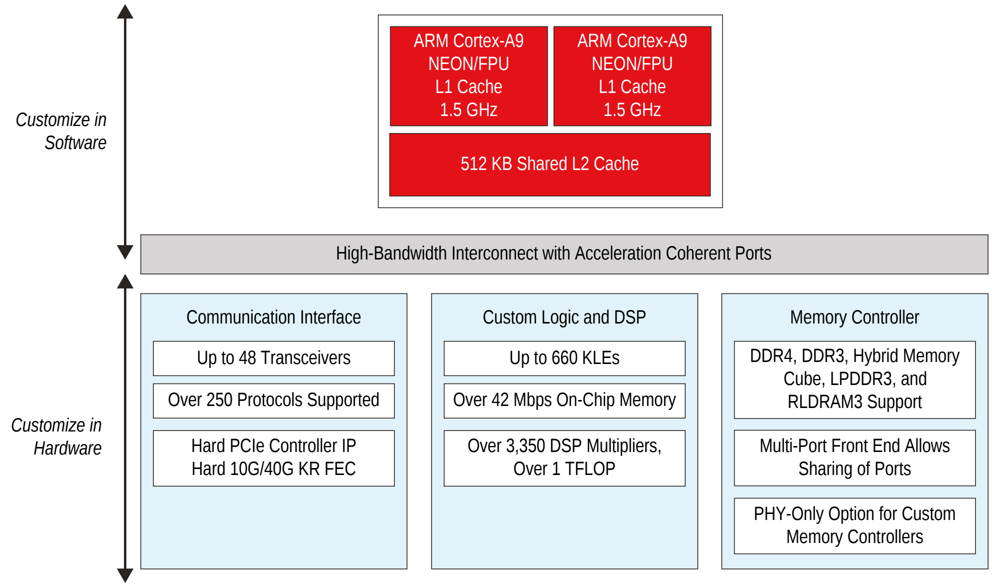
- **Application Code Reuse**: Because 28 nm and 20 nm SoCs share the same Dual Core ARM Cortex-A9 based HPS, any application code, board support packages, and ARM development tools developed for one SoC family can be reused with minimal design effort.
- **IP Reuse**: Arria 10 SoCs share the same core logic, memory, DSP, and I/O as Arria 10 FPGAs. Hardware intellectual property can be shared with minimal design effort. Altera also provides a fully tested and characterized portfolio of over 200 IP cores.
- **PCB Hardware Reuse**: Arria 10 SoCs are also package and footprint compatible with Arria 10 FPGAs, allowing hardware PCBs to be shared between the device categories.
- **Advanced Software Development Tools**:
    - The ecosystem that is available on ARM and the body of software packages, middleware available for operating systems that support ARM as well as the application development and debug tools available for ARM provides a familiar development environment to software developers.
    - Innovations such as Altera's Virtual Target technology allow functional testing of code without the need for hardware. By combining the most advanced multi-core debugger for ARM architectures with FPGA-adaptivity, the ARM DS-5 Altera Edition Toolkit provides embedded software developers an unprecedented level of full-chip visibility and control through the standard DS-5 user interface.
- **Advanced Hardware Development Tools**:
    - Altera's Quartus II software has faster compilation times than ever before. The Quartus II software's support for partial reconfiguration technology allows a single PCB to support multiple protocols by swapping protocols in the field.
    - QSys System Development framework allows rapid system integration of processor and peripherals and automates the process of generating AXI and Avalon based interconnect logic.
    - DSP Builder is a plug-in to MathWorks' Simulink that allows designers to develop DSP based filters, matrix operators and transforms using Model Based design flow and Advanced Blockset tools.
    - Open Computing Language (OpenCL) programming model with Altera's massively parallel FPGA architecture provides a powerful solution for system acceleration. The Altera SDK for OpenCL allows software developers to develop hardware using a C-based high-level design flow.

Single Platform of Devices that Offer Unified Control Path and Scalable Datapath

When you combine the SoC portfolio with the productivity benefits of design reuse in hardware and software, you get a benefit that is unique to Altera's technology. The result is an architecture that offers both unified control path and scalable data path.

interfaces, memories, and DSP functions, allowing Altera devices to offer the largest variety of interface and feature support than any off the shelf processor or ASSP. The design cycles for Altera's SoCs are a fraction of ASIC design cycles and offer a much lower risk path compared to an ASIC.

Figure 11: Differentiation through Customization



A New, More Productive DSP Design Flow

With Altera's SoCs, a more productive design flow for DSP design is now available. For the first time, DSP and embedded developers who may be unfamiliar to FPGA and HDL design can develop hardware and take advantage of the remarkable DSP performance available with Altera's SoCs.

In this design flow, DSP and embedded developers begin by running DSP algorithms directly on the ARM HPS. This a natural place to begin as, in many cases, C/C++ are the very languages in which these algorithms have been conceived in the first place. The Dual Core ARM Cortex-A9 MPCore features a double precision FPU and a NEON co-processor for 128-bit SIMD co-processor and is ideal for closed loop control, audio, video, and multimedia processing. The inherent productivity of software design cycles and iterations as compared to FPGA compilation times reduces system compile times drastically. When more performance is required, these software algorithms can be then profiled to identify bottlenecks and subsequently become candidates for hardware acceleration. Hardware accelerators can share data and computed results directly with ARM processor's L2 Cache via the Acceleration Coherency Port (ACP) that manages data coherency without having to incur the penalty of a full L2 Cache flush.

To develop these hardware accelerators, Altera offers two high-level automated design tools:

- With Altera's **OpenCL design flow**, hardware accelerators are created by coding the algorithm in a C-based high-level language. Using an automatic compiler, instruction streams are then developed and implemented as hardware running on the SoC. In this case, the OpenCL host code is run directly on the Dual ARM processor whereas the OpenCL kernels are implemented as hardware accelerators running in the logic core. By having an integrated processor on chip, the need for an external host processor to implement OpenCL host code is eliminated. For more information about OpenCL and the design flow, refer to the *OpenCL for Altera FPGAs: Accelerating Performance and Design Productivity* page.
- With Altera's **DSP Builder technology**, system definition and simulation is performed using the industry-standard MathWorks Simulink tools. The DSP Builder Signal Compiler block reads Simulink Model Files (**.mdl**) that are built using DSP Builder and MegaCore blocks and generates VHDL files and Tcl scripts for synthesis, hardware implementation, and simulation. This technology allows the automatic generation timing-optimized register transfer level (RTL) code based on high-level Simulink design descriptions. This is a significant productivity savings compared to the hours or days required to hand-optimize HDL code. In addition, advanced blockset DSP Builder libraries are available for commonly used DSP operations and transforms. For more information, refer to the *DSP Builder* page.

Related Information

- **OpenCL for Altera FPGAs: Accelerating Performance and Design Productivity**
- **DSP Builder**

Document Revision History

Table 17: Document Revision History

Date	Version	Changes
July 2013	2013.07.09	Added product names to tables in "Arria 10 FPGA Family Plan" and "Arria 10 SoC Family Plan" sections.
June 2013	2013.06.10	Initial release.