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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

| | |
|--------------------------------|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 427200 |
| Number of Logic Elements/Cells | 1150000 |
| Total RAM Bits | 68857856 |
| Number of I/O | 624 |
| Number of Gates | - |
| Voltage - Supply | 0.87V ~ 0.93V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 100°C (TJ) |
| Package / Case | 1932-BBGA, FCBGA |
| Supplier Device Package | 1932-FCBGA (45x45) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/10at115u3f45e3sges |

Arria 10 Family Variants

Arria 10 devices are available in GX, GT, and SX variants.

- **Arria 10 GX** devices deliver over 500 MHz core fabric performance and 2666 Mbps DDR4 external memory interface performance across the industrial temperature range, while providing over 1.1 million logic elements and 96 general purpose transceivers. Every transceiver is capable of 17.4 Gbps for short reach applications and 16.0 Gbps across the backplane. These devices are optimized for a broad range of applications such as wireless remote radio heads, broadcast studio equipment, 40G/100G communication systems, server acceleration, and medical imaging.
- **Arria 10 GT** devices have the same core performance and feature set as Arria 10 GX devices, with the added capability of sixteen 28.05-Gbps short reach transceivers for chip-to-chip and chip-to-module applications. The 28.05-Gbps transceivers are ideal for interfacing with the emerging CFP2 and CFP4 optical modules that typically require four lanes at data rates in the range of 25 to 28 Gbps. Backplane driving capability is also increased to 17.4 Gbps in Arria 10 GT devices.
- **Arria 10 SX** devices have a feature set that is similar to Arria 10 GX devices plus an ARM Cortex-A9 hard processor system.

Common to all Arria 10 family variants is the enhanced logic array utilizing Altera's adaptive logic module (ALM) and a rich set of high performance building blocks that includes 20Kbit (M20K) internal memory blocks, variable precision DSP blocks, fractional synthesis and integer PLLs, hard memory PHY and controllers for external memory interfaces, and general purpose I/O cells. These building blocks are interconnected by an updated version of Altera's superior multi-track routing architecture and comprehensive fabric clocking network. All devices support in-system, fine-grained partial reconfiguration of the logic array, allowing logic to be added and removed from the system during operation.

All family variants also contain high speed serial transceivers, containing both the physical medium attachment (PMA) and the physical coding sublayer (PCS), which can be used to implement a variety of industry standard and proprietary protocols. In addition to the hard PCS, Arria 10 devices contain multiple instantiations of PCI Express hard IP that supports Gen1/Gen2/Gen3 rates in x1/x2/x4/x8 lane configurations. The hard PCS and hard PCI Express IP free up valuable core logic resources, save power, and increase productivity for the user.

Improvements in Arria 10 FPGAs and SoCs

Altera has combined in-house innovations with TSMC's advanced 20-nm process technology to deliver major improvements over Arria V FPGAs and SoCs in nearly every category.

Table 1: Key Features of Arria 10 Devices Compared to Arria V Devices

| Feature | Arria V FPGAs and SoCs | Arria 10 FPGAs and SoCs |
|-------------------------------|----------------------------|---------------------------|
| Process technology | 28-nm TSMC | 20-nm TSMC |
| Processor core | Dual ARM Cortex-A9 MPCore™ | Dual ARM Cortex-A9 MPCore |
| Processor performance | 800 MHz | 1.5 GHz |
| Logic core performance | 300 MHz | 500 MHz |
| Power dissipation | 1x | 0.6x |

| Feature | Arria V FPGAs and SoCs | Arria 10 FPGAs and SoCs |
|---|--|--|
| Logic density | 504 KLE | 1150 KLE |
| Embedded memory | 34 Mbits | 53 Mbits |
| 18x19 multipliers | 2186 | 3356 |
| Maximum transceivers | 36 | 96 |
| Maximum transceiver data rate (chip to chip) | 10.3125 Gbps | 28.05 Gbps |
| Memory devices supported | DDR3 SDRAM @ 667 MHz/1333 Mbps | DDR4 SDRAM @ 1333 MHz/2666 Mbps DDR3 SDRAM @ 1067 MHz/2133 Mbps Hybrid Memory Cube (HMC) |
| Hard protocol IP | 2 EMACs PCI Express Gen3 x8 (Arria V GZ) PCI Express Gen2 x4/Gen1 x8 (Arria V GX/GT/SX/ST) | 3 EMACs PCI Express Gen3 x8 10GBASE-KR/40GBASE-KR4 FEC Interlaken PCS |

These features result in the following improvements:

- **Improved Core Logic Performance:** Arria 10 devices offer over 60% improved core performance compared to the previous generation
- **Improved Processor Performance:** Arria 10 SoCs provide 87% improvement in processor performance
- **Improved Processor Power Efficiency:** At 20 nm, the Dual Core ARM Cortex-A9 Processor provides the best power efficiency for any GHz-class processor in the industry
- **Lower Power:** Arria 10 devices deliver up to 40% lower power compared to prior-generation mid-range FPGAs and SoCs, enabled by 20-nm process technology advancements and a variety of innovative power-management options
- **Higher Density:** Arria 10 devices provide a higher level of integration with up to 1150K logic elements (LEs), up to 53 Mbits of embedded memory, and over 3350 18x19 multipliers
- **Improved Transceiver Bandwidth:** Arria 10 devices support chip-to-chip rates up to 28 Gbps and backplane rates up to 17.4 Gbps
- **Improved Memory Bandwidth with DDR4 Support:** Arria 10 devices support DDR4 memory up to 1333 MHz/ 2666 Mbps and feature support for the emerging transceiver-based Hybrid Memory Cube (HMC)
- **Improved DSP Performance:** With over 1.0 TeraFLOPs of single-precision DSP performance, Arria 10 devices deliver a 4 times increase in DSP performance
- **Additional Protocol Support for Hard IP:** Arria 10 devices feature an advanced transceiver architecture with added hard IP support for PCIe Gen3, Interlaken PCS, and 10GBASE-KR/40GBASE-KR4 FEC

Target Markets for Arria 10 FPGAs and SoCs

Arria 10 devices meet the performance, power, and bandwidth requirements of next generation wireless infrastructure, broadcast, compute and storage, networking, and medical and military equipment.

| Feature | Description |
|-------------------------------|---|
| Low power serial transceivers | <ul style="list-style-type: none"> • Continuous operating range of 611 Mbps to 17.4 Gbps for Arria 10 GX devices • Continuous operating range of 611 Mbps to 28.05 Gbps for Arria 10 GT devices • Backplane support up to 16.0 Gbps for Arria 10 GX devices • Backplane support up to 17.4 Gbps for Arria 10 GT devices • Extended range down to 125 Mbps with oversampling • ATX transmit PLLs with user-configurable fractional synthesis capability • Electronic Dispersion Compensation (EDC) for XFP, SFP+, QSFP, and CFP optical module support • Adaptive linear and decision feedback equalization • Transmit pre-emphasis and de-emphasis • Dynamic partial reconfiguration of individual transceiver channels • On-chip instrumentation (EyeQ non-intrusive data eye monitoring) |
| General purpose I/Os | <ul style="list-style-type: none"> • 1.6 Gbps LVDS—every pair can be configured as an input or output • 1333 MHz/2666 Mbps DDR4 external memory interface • 1067 MHz/2133 Mbps DDR3 external memory interface • 1.2 V to 3.0 V single-ended LVCMOS/LVTTL interfacing • On-chip termination (OCT) |
| Embedded hard IP | <ul style="list-style-type: none"> • PCIe Gen1/Gen2/Gen3 complete protocol stack, x1/x2/x4/x8 end point and root port • DDR4/DDR3/DDR3L/DDR3U/RLDRAM 3/LPDDR3 hard memory controller (RLDRAM2/QDR II+ using soft memory controller) • Multiple hard IP instantiations in each device • Dual-core ARM Cortex-A9 processor (Arria 10 SX devices only) |
| Transceiver hard IP | <ul style="list-style-type: none"> • 10GBASE-KR/40GBASE-KR4 Forward Error Correction (FEC) • 10G Ethernet PCS • PCI Express PIPE interface • Interlaken PCS • Gigabit Ethernet PCS • Deterministic latency support for Common Public Radio Interface (CPRI) PCS • Fast lock-time support for Gigabit Passive Optical Networking (GPON) PCS • 8B/10B, 64B/66B, 64B/67B encoders and decoders • Custom mode support for proprietary protocols |
| Power management | <ul style="list-style-type: none"> • SmartVoltage ID • V_{CC} PowerManager • Low static power device options • Programmable Power Technology • Quartus® II integrated PowerPlay power analysis |
| High performance core fabric | <ul style="list-style-type: none"> • Enhanced adaptive logic module (ALM) with 4 registers • Improved multi-track routing architecture reduces congestion and improves compile times • Hierarchical core clocking architecture • Fine-grained partial reconfiguration |

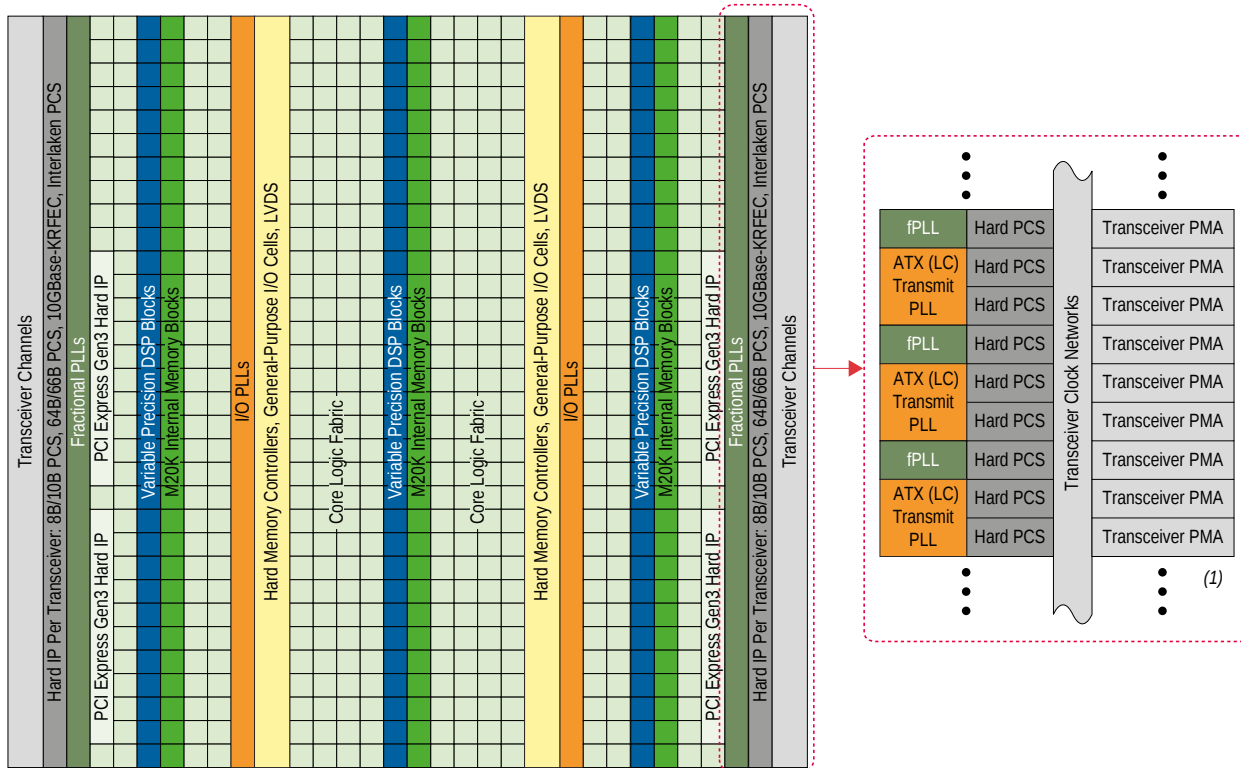
| Feature | Description |
|-------------------------------|---|
| Internal memory blocks | <ul style="list-style-type: none">• M20K—20-Kbit with hard ECC support• MLAB—640-bit distributed LUTRAM |
| Variable precision DSP blocks | <ul style="list-style-type: none">• Natively supports signal processing with precision ranging from 18x19 up to 54x54• Native 27x27 multiply mode• 64-bit accumulator and cascade for systolic FIRs• Internal coefficient memory banks• Pre-adder/subtractor improves efficiency• Additional pipeline register increases performance and reduces power |
| Phase locked loops (PLL) | <ul style="list-style-type: none">• Fractional synthesis PLLs (fPLL) support both fractional and integer modes• Fractional mode with third-order delta-sigma modulation• Precision frequency synthesis, clock delay compensation, zero delay buffering• Integer PLLs adjacent to general purpose I/Os, support external memory, and LVDS interfaces |
| Core clock networks | <ul style="list-style-type: none">• 800 MHz fabric clocking• 667 MHz external memory interface clocking, supports 2666 Mbps DDR4 interface• 800 MHz LVDS interface clocking, supports 1600 Mbps LVDS interface• Global, regional, and peripheral clock networks• Unused clock trees powered down to reduce dynamic power |
| Configuration | <ul style="list-style-type: none">• Serial and parallel flash interface• Configuration via protocol (CvP) using PCI Express Gen1/Gen2/Gen3• Fine-grained partial reconfiguration of core fabric• Dynamic reconfiguration of transceivers and PLLs• 256-bit AES bitstream encryption design security with authentication• Tamper protection |
| Packaging | <ul style="list-style-type: none">• Multiple devices with identical package footprints allows seamless migration across different FPGA densities• Devices with compatible package footprints allows migration to next generation high-end Stratix® 10 devices• 1.0 mm ball-pitch FBGA packaging• Lead and lead-free package options |
| Software and tools | <ul style="list-style-type: none">• Quartus II design suite• Transceiver toolkit• Qsys system integration tool• DSP Builder advanced blockset• OpenCL™ support• SoC Embedded Design Suite (EDS) |

Table 3: Arria 10 SoC-Specific Device Features

| Feature | Description |
|---|--|
| Dual-core ARM Cortex-A9 MPCore processor unit | <ul style="list-style-type: none"> • 2.5 MIPS/MHz instruction efficiency • CPU frequency 1.2 GHz with 1.5 GHz via overdrive <ul style="list-style-type: none"> • At 1.5 GHz total performance of 7500 MIPS • ARMv7-A architecture <ul style="list-style-type: none"> • Runs 32-bit ARM instructions • 16-bit and 32-bit Thumb instructions for 30% reduction in memory footprint • Jazelle[®] RCT execution architecture with 8-bit Java bytecodes • Superscalar, variable length, out-of-order pipeline with dynamic branch prediction • ARM NEON[™] media processing engine • Single- and double-precision floating-point unit • CoreSight[™] debug and trace technology • Snoop Control Unit (SCU) and Acceleration Coherency Port (ACP) |
| Cache | <ul style="list-style-type: none"> • L1 Cache <ul style="list-style-type: none"> • 32 KB of instruction cache • 32 KB of L1 data cache • Parity checking • L2 Cache <ul style="list-style-type: none"> • 512 KB shared • 8-way set associative • SEU Protection with parity on TAG ram and ECC on data RAM • Cache lockdown support |
| On-Chip Memory | <ul style="list-style-type: none"> • 256 KB of scratch on-chip RAM • 64 KB on-chip ROM |

Arria 10 Block Diagrams

Figure 2: Arria 10 FPGA Architecture Block Diagram



Note:

(1) Unused transceiver channels can be used as additional transceiver transmit PLLs

| Device Name ⁽¹⁾ | Logic Elements (KLE) | Registers | M20K Blocks | M20K Mbits | MLAB Counts | MLAB Mbits | 18x19 Multipliers ⁽²⁾ | Maximum GPIOs | Maximum XCVR (17.4G, 28.05G) | fPLLs | I/O PLLs | PCIe HIPs |
|----------------------------|----------------------|-----------|-------------|------------|-------------|------------|----------------------------------|---------------|------------------------------|-------|----------|-----------|
| GX 320 (10AX032) | 320 | 478,640 | 891 | 17 | 4,673 | 3 | 1,970 | 384 | 24, 0 | 8 | 8 | 2 |
| GX 480 (10AX048) | 480 | 730,880 | 1,438 | 28 | 7,137 | 4 | 2,736 | 492 | 36, 0 | 12 | 12 | 2 |
| GX 570 (10AX057) | 570 | 868,320 | 1,800 | 35 | 8,241 | 5 | 3,046 | 588 | 48, 0 | 16 | 16 | 2 |
| GX 660 (10AX066) | 660 | 1,005,800 | 2,133 | 42 | 9,345 | 6 | 3,356 | 588 | 48, 0 | 16 | 16 | 2 |
| GX 900 (10AX090) | 900 | 1,358,480 | 2,423 | 47 | 15,080 | 9 | 3,036 | 768 | 96, 0 | 32 | 16 | 4 |
| GX 1150 (10AX115) | 1,150 | 1,710,800 | 2,713 | 53 | 20,814 | 13 | 3,036 | 768 | 96, 0 | 32 | 16 | 4 |
| GT 900 (10AT090) | 900 | 1,358,480 | 2,423 | 47 | 15,080 | 9 | 3,036 | 624 | 80, 16 | 32 | 16 | 4 |
| GT 1150 (10AT115) | 1,150 | 1,710,800 | 2,713 | 53 | 20,814 | 13 | 3,036 | 624 | 80, 16 | 32 | 16 | 4 |

Table 5: Arria 10 GX and Arria 10 GT FPGA Family Package Plan, part 1

Cell legend: General Purpose I/Os, High-Voltage I/Os, LVDS Pairs, Transceivers ⁽³⁾ ⁽⁴⁾ ⁽⁵⁾ ⁽⁶⁾ ⁽⁷⁾ ⁽⁸⁾

| Device ⁽¹⁾ | U19 (U484) (19x19 mm ²) | F27 (F672) (27x27 mm ²) | F29 (F780) (29x29 mm ²) | F34 (F1152) (35x35 mm ²) | F35 (F1152) (35x35 mm ²) ⁽⁹⁾ | F36 (F1152) (35x35 mm ²) ⁽⁹⁾ |
|-----------------------|--|--|--|---|--|--|
| GX 160 (10AX016) | 192,48,72,6 | 240,48,96,12 | 288,48,120,12 | — | — | — |

⁽³⁾ All packages are ball grid arrays with 1.0 mm pitch, except for U19 (U484), which is 0.8 mm pitch.⁽⁴⁾ High-Voltage I/O pins are used for 3.3 V and 2.5 V interfacing.⁽⁵⁾ Each LVDS pair can be configured as either a differential input or a differential output.⁽⁶⁾ High-Voltage I/O pins and LVDS pairs are included in the General Purpose I/O count. Transceivers are counted separately.⁽⁷⁾ Each package column offers pin migration (common circuit board footprint) for all devices in the column.⁽⁸⁾ Arria 10 GX devices are pin migratable with Arria 10 GT devices in the same package.⁽⁹⁾ Devices in the F35 (F1152) package are pin migratable with devices in the F36 (F1152) package

| Device ⁽¹⁾ | F40 (F1517) (40x40 mm ²) | F40 (F1517) (40x40 mm ²) | F45 (F1932) (45x45 mm ²) | F45 (F1932) (45x45 mm ²) | F45 (F1932) (45x45 mm ²) |
|-----------------------|---|---|---|---|---|
| GX 270 (10AX027) | — | — | — | — | — |
| GX 320 (10AX032) | — | — | — | — | — |
| GX 480 (10AX048) | — | — | — | — | — |
| GX 570 (10AX057) | 588,48,270,48 | — | — | — | — |
| GX 660 (10AX066) | 588,48,270,48 | — | — | — | — |
| GX 900 (10AX090) | 624,0,312,48 | 342,0,154,66 | 768,0,384,48 | 624,0,312,72 | 480,0,240,96 |
| GX 1150 (10AX115) | 624,0,312,48 | 342,0,154,66 | 768,0,384,48 | 624,0,312,72 | 480,0,240,96 |
| GT 900 (10AT090) | 624,0,312,48 | — | — | 624,0,312,72 | 480,0,240,96 |
| GT 1150 (10AT115) | 624,0,312,48 | — | — | 624,0,312,72 | 480,0,240,96 |

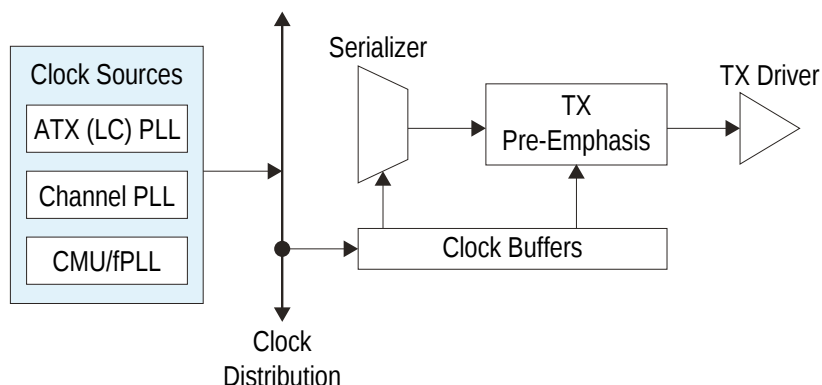
PMA Features

PMA channels are comprised of transmitter (TX), receiver (RX), and high speed clocking resources.

Arria 10 TX features provide exceptional signal integrity at data rates up to 28.05 Gbps. Clocking options include ultra-low jitter ATX (inductor-capacitor) PLLs, channel PLLs, clock multiplier unit (CMU) PLLs, and fractional PLLs (fPLLs):

- ATX PLLs can be configured in integer mode, or optionally, in a new fractional frequency synthesis mode. Each ATX PLL spans the full frequency range of the supported data rate range providing a highly stable and flexible clock source with the lowest jitter.
- CMU PLLs have been enhanced to provide a master clock source within the transceiver bank.
- When not configured as a transceiver channel, select PMA channels can be optionally configured as ring oscillator-based channel PLLs to provide an additional flexible clock source.
- In addition, dedicated on-chip fractional PLLs (fPLLs) are available with precision frequency synthesis capabilities. fPLLs can be used to synthesize multiple clock frequencies from a single reference clock source and replace multiple reference oscillators for multi-protocol and multi-rate applications.

Figure 5: Arria 10 Transmitter Features



On the receiver side, each PMA channel has a dedicated, independent channel PLL for the CDR to provide the maximum number of clocking resources possible without compromising TX clocking sources. Up to 80 independent data rates can be configured on a single Arria 10 device.

Receiver side features provide unparalleled equalization capabilities to drive a wide range of transmission media with the widest range of protocols and data rates. Each receiver channel includes:

- Continuous Time Linear Equalizers (CTLE)—to compensate for channel losses with low power
- Variable Gain Amplifiers (VGA)—to optimize the receiver's dynamic range
- Decision Feedback Equalizers (DFE)—with 7-fixed taps and 4-floating taps to provide additional equalization capability on backplanes even in the presence of crosstalk and reflections

In addition, On-Die Instrumentation (ODI) provides on-chip eye monitoring capabilities (EyeQ). This capability helps to both optimize link equalization parameters during board bring-up and provide in-system link diagnostics. Combined with on-chip jitter injection capabilities, EyeQ provides powerful functionality to do in-system link equalization margin testing.

| Feature | Capability |
|---|---|
| Fractional PLLs | On-chip fractional frequency synthesizers to replace on-board crystal oscillators and reduce system cost |
| Digitally Assisted Analog CDR | Superior jitter tolerance with fast lock time |
| On-Die Instrumentation— EyeQ and Jitter Margin Tool | Simplify board bring-up, debug, and diagnostics with non-intrusive, high-resolution eye monitoring (EyeQ). Also inject jitter from transmitter to test link margin in system. |
| Dynamic Partial Reconfiguration (DPRIO) | Allows for independent control of each transceiver channel Avalon memory-mapped interface for the most transceiver flexibility |
| Multiple PCS-PMA and PCS-PLD interface widths | 8-, 10-, 16-, 20-, 32-, 40-, or 64-bit interface widths for flexibility of deserialization width, encoding, and reduced latency |

PCS Features

Arria 10 PMA channels interface with core logic through configurable PCS interface layers.

Multiple gearbox implementations are available to decouple PCS and PMA interface widths. This feature provides the flexibility to implement a wide range of applications with 8-, 10-, 16-, 20-, 32-, 40-, or 64-bit interface widths. Arria 10 FPGAs contain PCS hard IP to support a wide range of standard and proprietary protocols.

The Standard PCS mode provides support for 8B/10B encoded applications up to 12.5 Gbps. The Enhanced PCS mode supports applications up to 17.4 Gbps. In addition, for highly customized implementations, a PCS Direct mode provides a fixed width interface up to 64 bits wide to core logic to allow for custom encoding including support for standards up to 28.05 Gbps.

The enhanced PCS includes an integrated 10GBASE-KR/40GBASE-KR4 Forward Error Correction (FEC) block.

The following table lists some of the key PCS features of Arria 10 transceivers that can be used in a wide range of standard and proprietary protocols from 125 Mbps to 28.05 Gbps.

Table 11: Arria 10 Transceiver PCS Features

| PCS Protocol Support | Data Rate (Gbps) | Transmitter Data Path | Receiver Data Path |
|----------------------------------|------------------|--|---|
| Standard PCS | 0.125 to 12.5 | Phase compensation FIFO, byte serializer, 8B/10B encoder, bit-slipper, channel bonding | Rate match FIFO, word-aligner, 8B/10B decoder, byte deserializer, byte ordering |
| PCI Express Gen1/Gen2 x1, x4, x8 | 2.5 and 5.0 | Same as Standard PCS plus PIPE 2.0 interface to core | Same as Standard PCS plus PIPE 2.0 interface to core |

Interlaken PCS Hard IP

Arria 10 devices have integrated Interlaken PCS hard IP supporting rates up to 17.4 Gbps per lane.

The Interlaken PCS hard IP is based on the proven functionality of the PCS developed for Altera's previous generation FPGAs, which has demonstrated interoperability with Interlaken ASSP vendors and third-party IP suppliers. The Interlaken PCS hard IP is present in every transceiver channel in Arria 10 devices.

10G Ethernet Hard IP

Arria 10 devices include IEEE 802.3 10-Gbps Ethernet (10GbE) compliant 10GBASE-R PCS and PMA hard IP. The scalable 10GbE hard IP supports multiple independent 10GbE ports while using a single PLL for all the 10GBASE-R PCS instantiations, which saves on core logic resources and clock networks.

The integrated 10G serial transceivers simplify multi-port 10GbE systems compared to XAUI interfaces that require an external XAUI-to-10G PHY. Furthermore, the integrated 10G transceivers incorporate Electronic Dispersion Compensation (EDC), which enables direct connection to standard 10G XFP and SFP+ pluggable optical modules. The 10G transceivers also support backplane Ethernet applications and include a hard 10GBASE-KR Forward Error Correction (FEC) circuit that can be used for both 10G and 40G applications. The integrated 10G Ethernet hard IP and 10G transceivers save external PHY cost, board space, and system power. The 10G Ethernet PCS hard IP and 10GBASE-KR FEC are present in every transceiver channel.

External Memory and General Purpose I/O

Arria 10 devices offer massive external memory bandwidth, with up to seven 32-bit DDR4 memory interfaces running at up to 2666 Mbps.

This bandwidth provides additional ease of design, lower power, and resource efficiencies of hardened high-performance memory controllers. Memory interfaces can be configured up to a maximum width of 144 bits when using either hard or soft memory controllers. Arria 10 devices also feature general purpose I/O capable of supporting a wide range of single-ended and differential I/O interfaces. LVDS rates up to 1.6 Gbps are supported, with each pair of pins having both a differential driver and a differential input buffer allowing for configurable LVDS direction on each pair.

The memory interface within Arria 10 FPGAs and SoCs delivers the highest performance and ease of use. Each I/O bank contains 48 general purpose I/Os and a high-efficiency hard memory controller capable of supporting many different memory types, each with different performance capabilities. The hard memory controller is also capable of being bypassed and replaced by a soft controller implemented in the user logic. The I/Os each have a hardened DDR read/write path (PHY) capable of performing key memory interface functionality such as read/write leveling, FIFO buffering to lower latency and improve margin, timing calibration, and on-chip termination. The timing calibration is aided by the inclusion of hard microcontrollers based on Altera's Nios[®] II technology, specifically tailored to control the calibration of multiple memory interfaces. This calibration allows the Arria 10 device to compensate for any changes in process, voltage, or temperature either within the Arria 10 device itself, or within the external memory device. The advanced calibration algorithms ensure maximum bandwidth and robust timing margin across all operating conditions.

Table 12: Arria 10 External Memory Interface Performance

The listed speeds are for the 1-rank case.

| Interface | Controller Type | Performance |
|-----------|-----------------|-------------|
| DDR4 | Hard | 2666 Mbps |

| Interface | Controller Type | Performance |
|----------------------|-----------------|-------------|
| DDR3 | Hard | 2133 Mbps |
| QDR II+ / II+ Xtreme | Soft | 550 MTps |
| RLDRAM III | Hard | 2400 Mbps |
| RLDRAM II | Soft | 533 Mbps |

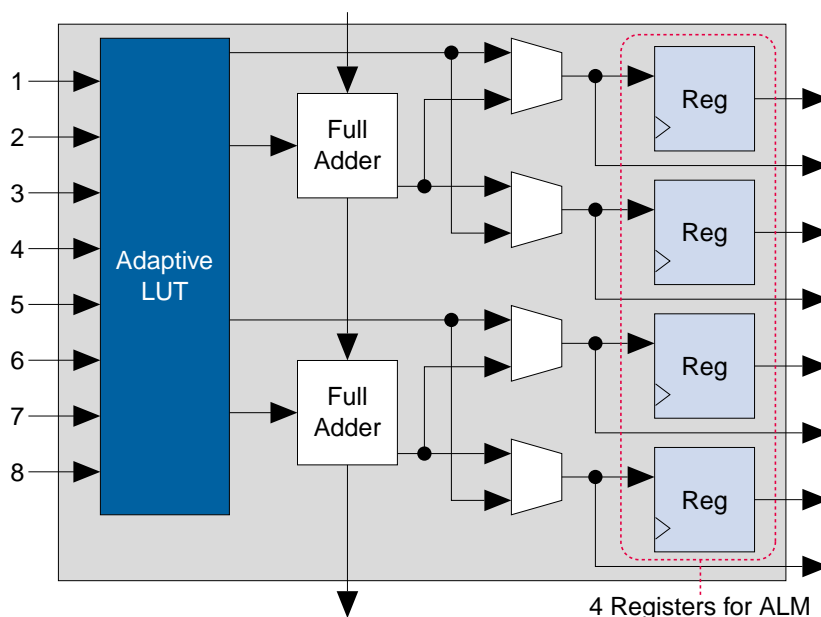
In addition to parallel memory interfaces, Arria 10 devices support serial memory technologies such as the Hybrid Memory Cube (HMC). The HMC is supported by the Arria 10 high-speed serial transceivers, which connect up to four HMC links, with each link running at data rates up to 15 Gbps.

Adaptive Logic Module (ALM)

Arria 10 devices use the same adaptive logic module (ALM) as the previous generation Arria V and Stratix V FPGAs, allowing for efficient implementation of logic functions and easy conversion of IP between the devices.

The ALM block diagram shown in the following figure has eight inputs with a fracturable look-up table (LUT), two dedicated embedded adders, and four dedicated registers.

Figure 7: Arria 10 FPGA and SoC ALM Block Diagram



Key features and capabilities of the Arria 10 ALM include:

- High register count with 4 registers per 8-input fracturable LUT enables Arria 10 devices to maximize core performance at higher core logic utilization
- 6% more logic compared to the traditional 2-register per LUT architecture
- Implements select 7-input logic functions, all 6-input logic functions, and two independent functions consisting of smaller LUT sizes (such as two independent 4-input LUTs) to optimize core logic utilization

The Quartus II software leverages the Arria 10 ALM logic structure to deliver the highest performance, optimal logic utilization, and lowest compile times. The Quartus II software simplifies design reuse as it automatically maps legacy designs into the Arria 10 ALM architecture.

Core Clocking

The Arria 10 device core clock network supports over 500 MHz fabric operation across the full industrial temperature range, and supports the hard memory controllers up to 2666 Mbps with a quarter rate transfer.

The clock network architecture is based on Altera's proven global, regional, and periphery clock structure, which is supported by dedicated clock input pins, fractional clock synthesis PLLs, and integer I/O PLLs. All unused sections of the clock network are identified by the Quartus II software and are powered down to reduce dynamic power consumption.

Fractional Synthesis PLLs and I/O PLLs

Arria 10 devices have up to 32 fractional synthesis PLLs (fPLL) and up to 16 I/O PLLs (IOPLL) that are available for both specific and general purpose use in the core.

The fPLLs are located in columns adjacent to the transceiver blocks. They can be used to reduce both the number of oscillators required on the board and the number of clock pins required, by synthesizing multiple clock frequencies from a single reference clock source. In addition to synthesizing reference clock frequencies for the transceiver CMU and ATX (LC) transmit PLLs, the fPLLs can be used for clock network delay compensation, zero-delay buffering, and direct transmit clocking for transceivers. Each fPLL may be independently configured for conventional integer mode, which is equivalent to a general purpose PLL (GPLL), or enhanced fractional mode with third-order delta-sigma modulation.

The integer mode IOPLLs are located in each bank of 48 I/Os. They can be used to simplify the design of external memory interfaces and high-speed LVDS interfaces. The IOPLLs are adjacent to the hard memory controllers and LVDS SERDES in each I/O bank, making it easier to close timing because these PLLs are tightly coupled with the I/Os that need to use them. Like the fPLLs, the IOPLLs can be used for general purpose applications in the core such as clock network delay compensation and zero-delay buffering.

Internal Embedded Memory

Arria 10 devices contain two types of embedded memory blocks: MLAB (640-bit) and M20K (20-Kbit).

The MLAB blocks are ideal for wide and shallow memories. The M20K blocks are double the size of the M10K blocks used in the previous generation Arria V devices, and are useful for supporting larger memory configurations and include hard ECC. Both types of embedded memory block can be configured as a single-port or dual-port RAM, FIFO, ROM or shift register. These memory blocks are highly flexible and support a number of memory configuration as shown in the following table.

Table 13: Arria 10 Internal Embedded Memory Block Configurations

| MLAB (640 bits) | M20K (20 Kbits) |
|---------------------------------------|-----------------|
| 64 x 10 (supported through emulation) | 16K x 1 |
| 32 x 20 | 8K x 2 |
| | 4K x 5 |
| | 2K x 10 |
| | 1K x 20 |
| | 512 x 40 |

The Quartus II software simplifies design reuse by automatically mapping memory blocks from previous generations of devices into the Arria 10 MLAB and M20K blocks.

Variable Precision DSP Block

The Arria 10 DSP blocks are based upon the Variable Precision DSP Architecture used in Altera's previous generation Arria V FPGAs. The blocks can be configured to natively support signal processing with precision ranging from 18x19 up to 54x54. A pipeline register has been added to increase the maximum operating frequency of the DSP block and reduce power consumption.

Each DSP block can be independently configured at compile time as either dual 18x19 or a single 27x27 multiply accumulate. With a dedicated 64-bit cascade bus, multiple variable precision DSP blocks can be cascaded to implement even higher precision DSP functions efficiently. The following table shows how different precisions are accommodated within a DSP block, or by utilizing multiple blocks.

Table 14: Variable Precision DSP Block Configurations

| Multiplier Size | DSP Block Resources | Expected Usage |
|-----------------|---|---|
| 18x19 bits | 1/2 of Variable Precision DSP Block | Medium precision fixed point |
| 27x27 bits | 1 Variable Precision DSP Block | High precision fixed or Single Precision floating point |
| 19x36 bits | 1 Variable Precision DSP Block with external adder | Fixed point FFTs |
| 36x36 bits | 2 Variable Precision DSP Blocks with external adder | Very high precision fixed point |
| 54x54 bits | 4 Variable Precision DSP Blocks with external adder | Double Precision floating point |

Complex multiplication is very common in DSP algorithms. One of the most popular applications of complex multipliers is the FFT algorithm. This algorithm has the characteristic of increasing precision requirements on only one side of the multiplier. The Variable Precision DSP block supports the FFT algorithm with proportional increase in DSP resources as the precision grows.

- Hard memory controller with support for DDR3, DDR4 and optional error correction code (ECC) support
- Multiport Front End (MPFE) Scheduler interface to the hard memory controller
- 8-channel direct memory access (DMA) controller
- QSPI flash controller with SIO, DIO, QIO SPI Flash support
- NAND flash controller (ONFI 1.0 or later) with DMA and ECC support, updated to support 8 and 16-bit Flash devices and new command DMA to offload CPU for fast power down recovery
- Updated SD/SDIO/MMC controller to eMMC 4.5 with DMA with CE-ATA digital command support
- 3 10/100/1000 Ethernet media access control (MAC) with DMA
- 2 USB On-the-Go (OTG) controller with DMA
- 5 I²C controller (3 can be used by EMAC for MIO to external PHY)
- 2 UART 16550 Compatible
- 4 serial peripheral interface (SPI) (2 Master, 2 Slaves)
- 54 programmable general-purpose I/O (GPIO)
- 48 I/O direct share I/O allows HPS peripherals to connect directly to I/O
- 7 general-purpose timers
- 4 watchdog timers
- Anti-tamper, Secure Boot, Encryption (AES) and Authentication (SHA)

Key Features of 20-nm HPS

The following features are new in the 20-nm Hard Processor System compared to the 28-nm SoCs:

- **Increased Performance and Overdrive Capability**

While the nominal processor frequency is 1.2 GHz, the 20 nm HPS offers an “overdrive” feature which enables an even higher processor operating frequency. For this a higher supply voltage value is required that is unique to the HPS and may require a separate regulator.

- **Increased Processor Memory Bandwidth and DDR4 Support**

Up to 64-bit DDR4 memory @ 2666 Mbps is available for the processor. The hard memory controller for the HPS comprises a multi-port front end that manages connections to a single port memory controller. The multi-port front end allows logic core and the HPS share ports and thereby the available bandwidth of the memory controller.

- **Flexible I/O Sharing**

An advanced I/O pin muxing scheme allows improved sharing of I/O between the HPS and the core logic. The following types of I/O are available for SoC:

Dedicated I/O (15)—These I/Os are physically located inside the HPS block and are not accessible to logic within the core. The 15 dedicated I/Os are used for HPS clock, resets, and interfacing with boot devices, QSPI, and SD/MMC

Direct Shared I/O (48)—These shared I/Os are located closest to the HPS block and are ideal for high speed HPS peripherals such as EMAC, USB, and others. There is one bank of 48 I/Os that supports direct sharing where the 48 I/Os can be shared 12 I/Os at a time.

Standard (Shared) I/O (All other)—All standard I/Os can be shared by the HPS peripherals and any logic within the core. For designs where more than 48 I/Os are required to fully use all the peripherals in the HPS, these I/Os can be connected through the core logic.

- **EMAC Core**

A third EMAC core is available in the HPS. Three EMAC cores enable an application to support two redundant Ethernet connections; for example, backplane, or two EMAC cores for managing IEEE 1588 time stamp information while allowing a third EMAC core for debug and configuration. All three EMACs can potentially share the same time stamps, simplifying the 1588 time stamping implementation. A new serial time stamp interface allows core logic to access and read the time stamp values. The integrated EMAC controllers can be connected to external Ethernet PHY through the provided MDIO or I²C interface.

- **On-Chip Memory**

The on-chip memory is updated to 256 KB support and can support larger data sets and real time algorithms

- **ECC Enhancements**

Improvements in L2 Cache ECC management allow identification of errors down to the address level. ECC enhancements also enable improved error injection and status reporting via the introduction of new memory mapped access to syndrome and data signals.

- **HPS to FPGA Interconnect Backbone**

Although the HPS and the Logic Core can operate independently, they are tightly coupled via a high-bandwidth system interconnect built from high-performance ARM AMBA AXI bus bridges. IP bus masters in the FPGA fabric have access to HPS bus slaves via the FPGA-to-HPS interconnect. Similarly, HPS bus masters have access to bus slaves in the core fabric via the HPS-to-FPGA bridge. Both bridges are AMBA AXI-3 compliant and support simultaneous read and write transactions. Up to three masters within the core fabric can share the HPS SDRAM controller with the processor. Additionally, the processor can be used to configure the core fabric under program control via a dedicated 32-bit configuration port.

- **HPS-to-FPGA**—configurable 32-, 64-, or 128-bit Avalon/AMBA AXI interface allows high bandwidth HPS master transactions to Logic Core
- **LW HPS-to-FPGA**—Light Weight 32-bit AXI interface suitable for low latency register accesses from HPS to soft peripherals in logic core
- **FPGA-to-HPS**—configurable 32-, 64-, or 128-bit AMBA AXI interface
- **FPGA-to-HPS SDRAM controller**—up to 3 masters (command ports), 3x 64-bit read data ports and 3x 64-bit write data ports
- **32-bit FPGA configuration manager**
- **Security**

A number of new security features have been introduced for anti-tamper management, secure boot, encryption (AES), and authentication (SHA).

Power Management

Arria 10 devices leverage the advanced 20 nm process technology, a low 0.9 V core power supply, an enhanced core architecture, and several optional power reduction techniques to reduce total power consumption by as much as 40% compared to Arria V devices and as much as 60% compared to Stratix V devices.

The optional power reduction techniques in Arria 10 devices include:

- **SmartVoltage ID**—a code is programmed into each device during manufacturing that allows a smart regulator to operate the device at lower core V_{CC} while maintaining performance
- **Programmable Power Technology**—non-critical timing paths are identified by the Quartus II software and the logic in these paths is biased for low power instead of high performance
- **V_{CC} PowerManager**—allows devices to be run at lower core voltage to trade performance for power savings
- **Low Static Power Options**—devices are available with either standard static power or low static power while maintaining performance

Furthermore, Arria 10 devices feature Altera's industry-leading low power transceivers and include a number of hard IP blocks that not only reduce logic resources but also deliver substantial power savings compared to soft implementations. In general, hard IP blocks consume up to 50% less power than the equivalent soft logic implementations.

Incremental Compilation

The Quartus II software incremental compilation feature reduces compilation time by up to 70% and preserves performance to ease timing closure.

Incremental compilation supports top-down, bottom-up, and team-based design flows. The incremental compilation feature facilitates modular hierarchical and team-based design flows where different designers compile their respective sections of a design in parallel. Furthermore, different designers or IP providers

can develop and optimize different blocks of the design independently. These blocks can then be imported into the top level project. The incremental compilation feature enables the partial reconfiguration flow for Arria 10 devices.

Configuration and Configuration via Protocol Using PCI Express

Arria 10 device configuration is improved for ease-of-use, speed, and cost. The devices can be configured through a variety of techniques such as active and passive serial, fast passive parallel, JTAG, and configuration via protocol using PCI Express including Gen3.

Configuration via protocol (CvP) using PCI Express allows the FPGA to be configured across the PCI Express bus, simplifying the board layout and increasing system integration. Making use of the embedded PCI Express hard IP, this technique allows the PCI Express bus to be powered up and active within the 100 ms time allowed by the PCI Express specification. Arria 10 devices also support partial reconfiguration across the PCI Express bus which reduces system down time by keeping the PCI Express link active while the device is being reconfigured.

Table 16: Arria 10 Device Configuration Modes

| Mode | Compression | Encryption | Remote Update | Data Width (bits) | Maximum DCLK Rate (MHz) | Maximum Data Rate (Mbps) |
|-------------------------------|-------------|------------|-----------------------|-------------------|-------------------------|--------------------------|
| Active Serial | Yes | Yes | Yes | 1, 4 | 100 | 400 |
| Passive Serial | Yes | Yes | — | 1 | 125 | 125 |
| Passive Parallel | Yes | Yes | Parallel flash loader | 8, 16, 32 | 125 | 4000 |
| Configuration via PCI Express | — | Yes | Yes | 1, 2, 4, 8 | — | 4000 |
| JTAG | — | — | — | 1 | 33 | 33 |

Partial and Dynamic Reconfiguration

Partial reconfiguration allows you to reconfigure part of the FPGA while other sections continue running. This capability is required in systems where uptime is critical, because it allows you to make updates or adjust functionality without disrupting services.

In addition to lowering power and cost, partial reconfiguration also increases the effective logic density by removing the necessity to place in the FPGA those functions that do not operate simultaneously. Instead, these functions can be stored in external memory and loaded as needed. This reduces the size of the required FPGA by allowing multiple applications on a single FPGA, saving board space and reducing power. The partial reconfiguration process is built on top of the proven incremental compile design flow in the Quartus II design software.

Altera SoC: The Architecture of Choice When Productivity Matters

Productivity is the driving philosophy of Altera's Arria 10 SoC family. By reusing hardware, software, IP, and RTL across FPGAs and SoCs, you can reduce design effort and get products to market faster. The Dual Core ARM Cortex-A9 MPCore-based HPS is common to both 20- and 28-nm SoCs and facilitates extensive software code compatibility as well as tools and OS Board Support Package (BSP) reuse. The extensive tools and OS support available as part of Altera and ARM ecosystem and the fast iteration times inherent in software development (especially as compared to FPGA compile times) results in a highly productive embedded and DSP development flow. In addition, Altera offers high-level automated design flows for hardware development, such as the Altera OpenCL (a C-based hardware design flow) and DSP Builder (a model-based hardware design flow).

Figure 9: Hardware and Software Reuse

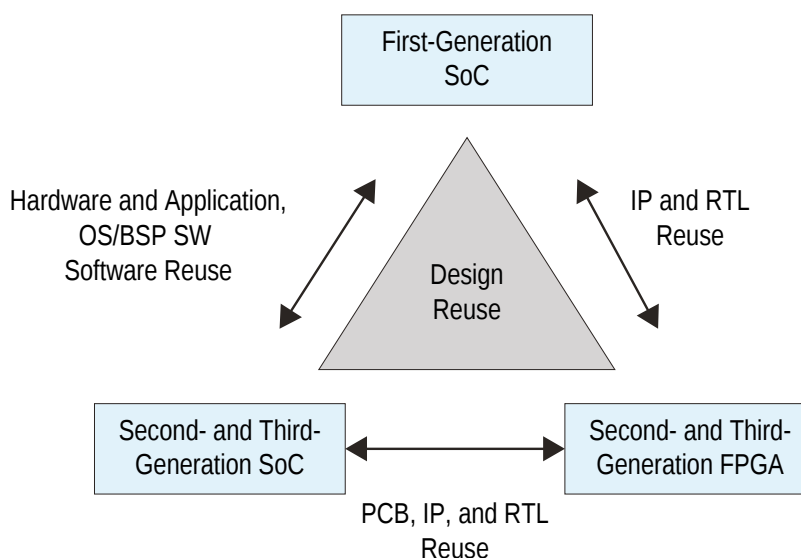
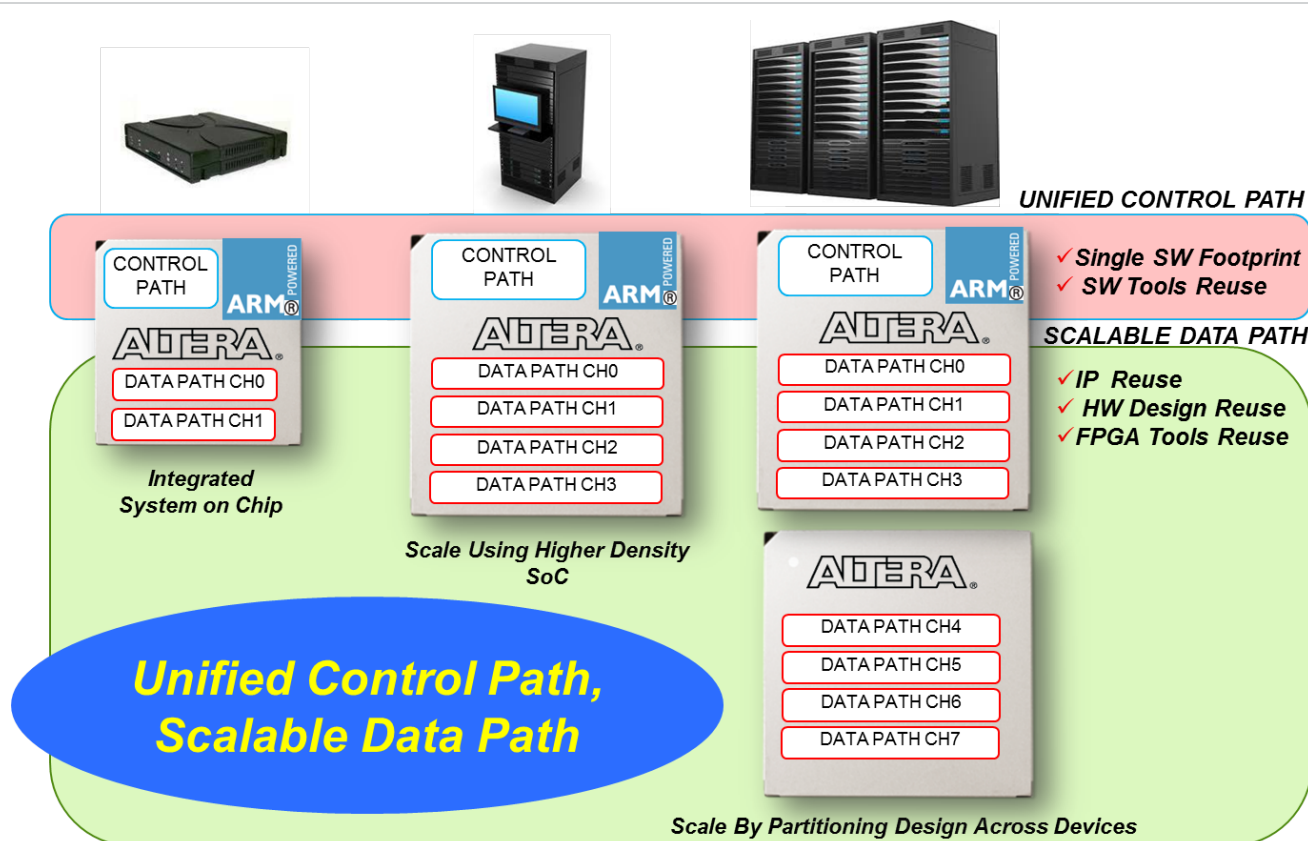


Figure 10: Unified Control Path and Scalable Data Path



SoCs and FPGAs can be used across product platforms from low cost customer premise equipment to metro and access service provider equipment all the way to core and transmission equipment. For example, the low-cost Cyclone® V SoC offers a fully integrated system-on-a-chip device for the low end of a product portfolio that is ideal for customer premise, small cell routers, and enterprise routing. On the other end of the spectrum, Arria 10 and Stratix 10 SoCs offer performance and a high level of system integration on the high end of the product portfolio for access, networking, and transmission equipment.

Unified Control: Because all 28-nm and 20-nm SoCs feature a common Dual ARM Cortex-A9 based HPS, there is extensive software tool reuse, operating system board support packages (BSP) reuse and a high degree of software code compatibility across the devices and the end product portfolio.

Scalable Datapath: Altera's SoC offers a portfolio of devices that meet the price, power, performance, logic density, memory bandwidth, and transceiver bandwidth of an entire product portfolio. This scalability both simplifies the system architecture and enhances productivity through design reuse and protocol IP reuse.

Differentiation through Customization

Designers today can choose between many competing technologies: off the shelf processors, ASSPs, ASICs, and SoCs. Altera's SoCs stand out from these competing technologies because they allow maximum customization. Designers can implement their intellectual property in software running on the ARM or in hardware running on the programmable logic. The high speed serial I/O and memory interfaces allow a high degree of customization and flexibility. Designers can choose a standard protocol or memory standard or they can implement a custom protocol or memory controller and still use the embedded PHY circuitry to bypass the controller logic. Altera offers fully characterized turnkey IP cores for a number of communication