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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	427200
Number of Logic Elements/Cells	1150000
Total RAM Bits	68857856
Number of I/O	624
Number of Gates	-
Voltage - Supply	0.87V ~ 0.93V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	1932-BBGA, FCBGA
Supplier Device Package	1932-FBGA, FC (45x45)
Purchase URL	https://www.e-xfl.com/product-detail/intel/10at115u4f45e4sges

Arria 10 Family Variants

Arria 10 devices are available in GX, GT, and SX variants.

- **Arria 10 GX** devices deliver over 500 MHz core fabric performance and 2666 Mbps DDR4 external memory interface performance across the industrial temperature range, while providing over 1.1 million logic elements and 96 general purpose transceivers. Every transceiver is capable of 17.4 Gbps for short reach applications and 16.0 Gbps across the backplane. These devices are optimized for a broad range of applications such as wireless remote radio heads, broadcast studio equipment, 40G/100G communication systems, server acceleration, and medical imaging.
- **Arria 10 GT** devices have the same core performance and feature set as Arria 10 GX devices, with the added capability of sixteen 28.05-Gbps short reach transceivers for chip-to-chip and chip-to-module applications. The 28.05-Gbps transceivers are ideal for interfacing with the emerging CFP2 and CFP4 optical modules that typically require four lanes at data rates in the range of 25 to 28 Gbps. Backplane driving capability is also increased to 17.4 Gbps in Arria 10 GT devices.
- **Arria 10 SX** devices have a feature set that is similar to Arria 10 GX devices plus an ARM Cortex-A9 hard processor system.

Common to all Arria 10 family variants is the enhanced logic array utilizing Altera's adaptive logic module (ALM) and a rich set of high performance building blocks that includes 20Kbit (M20K) internal memory blocks, variable precision DSP blocks, fractional synthesis and integer PLLs, hard memory PHY and controllers for external memory interfaces, and general purpose I/O cells. These building blocks are interconnected by an updated version of Altera's superior multi-track routing architecture and comprehensive fabric clocking network. All devices support in-system, fine-grained partial reconfiguration of the logic array, allowing logic to be added and removed from the system during operation.

All family variants also contain high speed serial transceivers, containing both the physical medium attachment (PMA) and the physical coding sublayer (PCS), which can be used to implement a variety of industry standard and proprietary protocols. In addition to the hard PCS, Arria 10 devices contain multiple instantiations of PCI Express hard IP that supports Gen1/Gen2/Gen3 rates in x1/x2/x4/x8 lane configurations. The hard PCS and hard PCI Express IP free up valuable core logic resources, save power, and increase productivity for the user.

Improvements in Arria 10 FPGAs and SoCs

Altera has combined in-house innovations with TSMC's advanced 20-nm process technology to deliver major improvements over Arria V FPGAs and SoCs in nearly every category.

Table 1: Key Features of Arria 10 Devices Compared to Arria V Devices

Feature	Arria V FPGAs and SoCs	Arria 10 FPGAs and SoCs
Process technology	28-nm TSMC	20-nm TSMC
Processor core	Dual ARM Cortex-A9 MPCore™	Dual ARM Cortex-A9 MPCore
Processor performance	800 MHz	1.5 GHz
Logic core performance	300 MHz	500 MHz
Power dissipation	1x	0.6x

By providing such a highly integrated device, Arria 10 FPGAs and SoCs significantly reduce BOM cost, form factor, and power consumption. Arria 10 devices allow you to differentiate your product through customization by implementing your intellectual property in both hardware and software.

For these applications, Arria 10 devices integrate both logic functions and processor functions in a highly integrated single device. The integrated ARM-based SoCs provide all the functionality of traditional FPGAs, eliminate the need for a local processor, and increase system performance by taking advantage of the tightly coupled high bandwidth interface between the core fabric and the hard processor system.

Figure 1: Arria 10 FPGA and SoC Applications

Wireless Infrastructure	Access, Metro & Core	Transmission	Cloud Servers and Storage	Broadcast
				
Target Applications				
• Remote Radio Head • Mobile Backhaul • Active Antenna • Basestation (BTS) • 4G/LTE Marco eNB • 4G/LTE Micro eNB	• 40G GPON, EPON, FFTH, Switch • 100G / 200G NGPON • 100G Traffic Management	• NX 100G OTU 4 • 2 X OTU 4 • 4 X OTU 4	• Flash Cache • Cloud • Server • Acceleration	• Pro A/V Equipment • Switcher • Server • Transport • Head End • VoD Mux
Logic Functions				
• RF Processing • Digital Pre-Distortion (DPD) • Baseband Interface	• Aggregation • Bridging • Switching • Traffic Management • I/O	• FEC • Aggregation • Muxponding • I/O	• Flash Cache Processing • Acceleration • SATA/SAS • PCIe Gen3	• Video Format Conversion • Muxing • Switching • Bridging
Processor Functions				
• OAM & Link • Digital Pre-Distortion (DPD) • L2 Switch • I/O, Protocol Control	• Host Offload • OAM & Link • L2 Switch • I/O, Protocol Control • Chassis Management	• Host Offload • OAM & Link • I/O Control • Chassis Management	• Flash Cache Control • Host Offload • Co-processing & Acceleration Control	• Audio Processing • Video Compression • Link Management

Feature	Description
Internal memory blocks	• M20K—20-Kbit with hard ECC support • MLAB—640-bit distributed LUTRAM
Variable precision DSP blocks	• Natively supports signal processing with precision ranging from 18x19 up to 54x54 • Native 27x27 multiply mode • 64-bit accumulator and cascade for systolic FIRs • Internal coefficient memory banks • Pre-adder/subtractor improves efficiency • Additional pipeline register increases performance and reduces power
Phase locked loops (PLL)	• Fractional synthesis PLLs (fPLL) support both fractional and integer modes • Fractional mode with third-order delta-sigma modulation • Precision frequency synthesis, clock delay compensation, zero delay buffering • Integer PLLs adjacent to general purpose I/Os, support external memory, and LVDS interfaces
Core clock networks	• 800 MHz fabric clocking • 667 MHz external memory interface clocking, supports 2666 Mbps DDR4 interface • 800 MHz LVDS interface clocking, supports 1600 Mbps LVDS interface • Global, regional, and peripheral clock networks • Unused clock trees powered down to reduce dynamic power
Configuration	• Serial and parallel flash interface • Configuration via protocol (CvP) using PCI Express Gen1/Gen2/Gen3 • Fine-grained partial reconfiguration of core fabric • Dynamic reconfiguration of transceivers and PLLs • 256-bit AES bitstream encryption design security with authentication • Tamper protection
Packaging	• Multiple devices with identical package footprints allows seamless migration across different FPGA densities • Devices with compatible package footprints allows migration to next generation high-end Stratix® 10 devices • 1.0 mm ball-pitch FBGA packaging • Lead and lead-free package options
Software and tools	• Quartus II design suite • Transceiver toolkit • Qsys system integration tool • DSP Builder advanced blockset • OpenCL™ support • SoC Embedded Design Suite (EDS)

Feature	Description

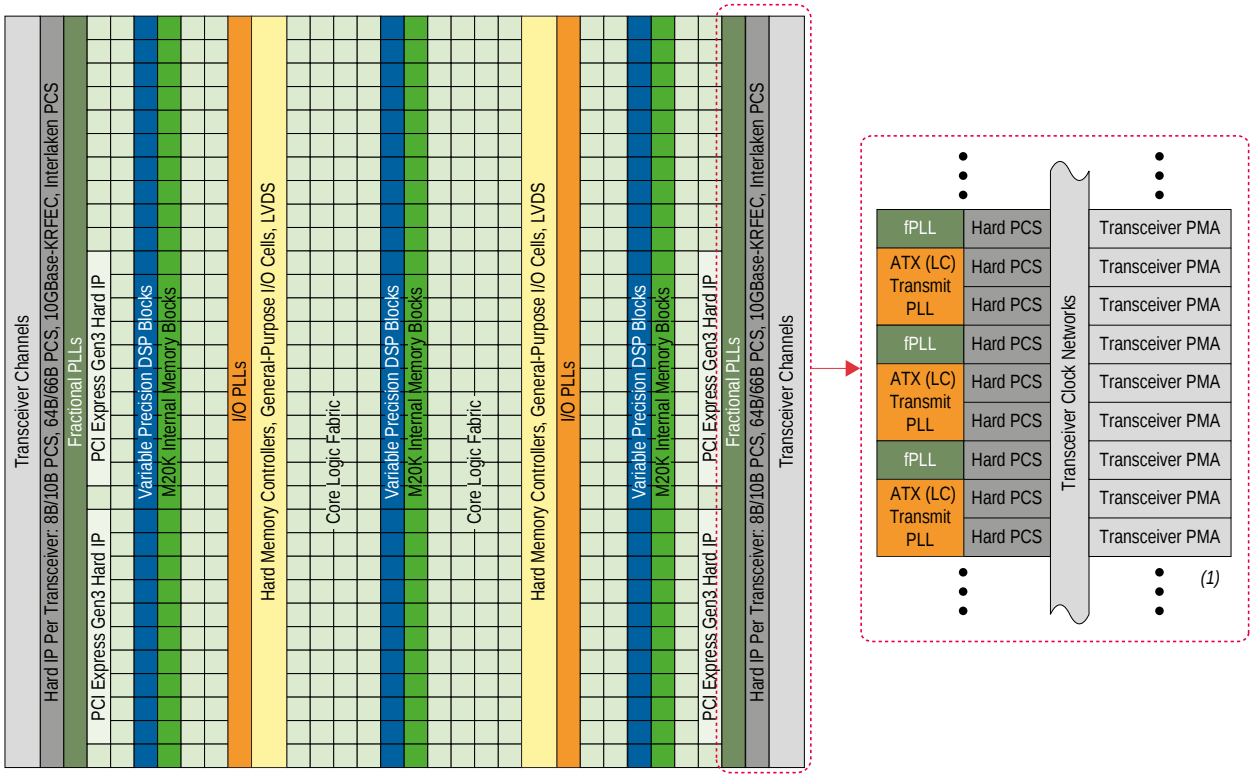
External Memory Interface for HPS	• Hard memory controller with support for DDR4, DDR3, DDR2, LPDDR2
	  • 40-bit (32-bit + 8-bit ECC) with select packages supporting 72-bit (64-bit + 8-bit ECC)
	  • Support for up to 2666 Mbps DDR4 and 2166 Mbps DDR3 frequencies
	  • Error correction code (ECC) support including calculation, error correction, write-back correction, and error counters
	  • Software Configurable Priority Scheduling on individual SDRAM bursts ECC
	  • Fully programmable timing parameter support for all JEDEC specified timing parameters
	  • AXI® Quality of Service (QoS) support for interface to logic core
	  • Multiport front-end (MPFE) scheduler interface to hard memory controller
	• Queued serial peripheral interface (QSPI) flash controller allows port sharing of hard memory controller between CPU and logic core
	  • Single I/O (SIO), Dual I/O (DIO), and Quad I/O (QIO) SPI Flash support
	  • Support for up to 108 MHz for flash frequency
	• NAND flash controller
	  • ONFI 1.0 or later
	  • Integrated descriptor based with DMA
	  • New command DMA to offload CPU for fast power down recovery
	  • Programmable hardware ECC support
	  • Updated to support 8 and 16 bit Flash devices
	  • Support for 50 MHz flash frequency
	• Secure Digital SD/SDIO/MMC controller
	  • eMMC 4.5
	  • Integrated descriptor based DMA
	  • CE-ATA digital commands supported
	  • 50 MHz operating frequency
	• Direct memory access (DMA) controller
	  • 8-channel
	  • Supports up to 32 peripheral handshake interface

Feature	Description

Interconnect to Logic Core	• High-performance ARM AMBA® AXI bus bridges
	  • AMBA AXI-3 compliant
	  • Allows both independent and tightly coupled operation between HPS and logic core
	  • Support simultaneous read and write transactions
	• FPGA-to-HPS Bridge
	  • Allows IP bus masters in the logic core to access to HPS bus slaves
	  • Configurable 32-, 64-, or 128-bit AMBA AXI interface
	  • Up to three masters within the core fabric can share the HPS SDRAM controller with the processor
	• HPS-to-FPGA Bridge
	  • Allows HPS bus masters to access bus slaves in core fabric
	  • Configurable 32-, 6-4, or 128-bit Avalon®/AMBA AXI interface allows high-bandwidth HPS master transactions to logic core
	• Configuration Bridge
	  • Allows configuration manager in HPS to configure the logic core under program control via dedicated 32-bit configuration port
	• Light Weight HPS-to-FPGA Bridge
	  • Light weight 32-bit AXI interface suitable for low-latency register accesses from HPS to soft peripherals in logic core
	• FPGA-to-HPS SDRAM controller Bridge
	  • Up to three masters (command ports), 3x 64-bit read data ports, and 3x 64-bit write data ports

Arria 10 Block Diagrams

Figure 2: Arria 10 FPGA Architecture Block Diagram



Note:
(1) Unused transceiver channels can be used as additional transceiver transmit PLLs

Device [1]	U19 (U484) (19x19 mm^2)	F27 (F672) (27x27 mm^2)	F29 (F780) (29x29 mm^2)	F34 (F1152) (35x35 mm^2)	F35 (F1152) (35x35 mm^2) [9]	F36 (F1152) (35x35 mm^2) [9]
GX 220 (10AX022)	192,48,72,6	240,48,96,12	288,48,120,12	—	—	—
GX 270 (10AX027)	—	240,48,96,12	360,48,156,12	384,48,168,24	384,48,168,24	—
GX 320 (10AX032)	—	240,48,96,12	360,48,156,12	384,48,168,24	384,48,168,24	—
GX 480 (10AX048)	—	—	360,48,156,12	492,48,222,24	396,48,174,36	—
GX 570 (10AX057)	—	—	—	492,48,222,24	396,48,174,36	—
GX 660 (10AX066)	—	—	—	492,48,222,24	396,48,174,36	432,48,192,36
GX 900 (10AX090)	—	—	—	528,0,264,24	432,0,216,36	—
GX 1150 (10AX115)	—	—	—	528,0,264,24	432,0,216,36	—
GT 900 (10AT090)	—	—	—	—	—	—
GT 1150 (10AT115)	—	—	—	—	—	—

Table 6: Arria 10 GX and Arria 10 GT FPGA Family Package Plan, part 2

Cell legend: General Purpose I/Os, High-Voltage I/Os, LVDS Pairs, Transceivers [3] [4] [5] [6] [7] [8]

Device [1]	F40 (F1517) (40x40 mm^2)	F40 (F1517) (40x40 mm^2)	F45 (F1932) (45x45 mm^2)	F45 (F1932) (45x45 mm^2)	F45 (F1932) (45x45 mm^2)
GX 160 (10AX016)	—	—	—	—	—
GX 220 (10AX022)	—	—	—	—	—

Device [1]	F40 (F1517) (40x40 mm^2)	F40 (F1517) (40x40 mm^2)	F45 (F1932) (45x45 mm^2)	F45 (F1932) (45x45 mm^2)	F45 (F1932) (45x45 mm^2)
GX 270 (10AX027)	—	—	—	—	—
GX 320 (10AX032)	—	—	—	—	—
GX 480 (10AX048)	—	—	—	—	—
GX 570 (10AX057)	588,48,270,48	—	—	—	—
GX 660 (10AX066)	588,48,270,48	—	—	—	—
GX 900 (10AX090)	624,0,312,48	342,0,154,66	768,0,384,48	624,0,312,72	480,0,240,96
GX 1150 (10AX115)	624,0,312,48	342,0,154,66	768,0,384,48	624,0,312,72	480,0,240,96
GT 900 (10AT090)	624,0,312,48	—	—	624,0,312,72	480,0,240,96
GT 1150 (10AT115)	624,0,312,48	—	—	624,0,312,72	480,0,240,96

Table 8: Arria 10 SX SoC Family Plan

Device Name [10]	Logic Elements (KLE)	Registers	M20K Blocks	M20K Mbits	MLAB Counts	MLAB Mbits	18x19 Multipliers [11]	Maximum GPIOs	Maximum XCVR (17.4G, 28.05G)	fPLLs	I/O PLLs	PCIe HIPs
SX 160 (10AS016)	160	246,040	440	9	1,680	1	312	288	12, 0	6	6	1
SX 220 (10AS022)	220	326,040	583	11	2,227	1	384	288	12, 0	6	6	1
SX 270 (10AS027)	270	406,480	750	15	3,968	2	1,660	384	24, 0	8	8	2
SX 320 (10AS032)	320	478,640	891	17	4,673	3	1,970	384	24, 0	8	8	2
SX 480 (10AS048)	480	730,880	1,438	28	7,137	4	2,736	492	36, 0	12	12	2
SX 570 (10AS057)	570	868,320	1,800	35	8,241	5	3,046	588	48, 0	16	16	2
SX 660 (10AS066)	660	1,005,800	2,133	42	9,345	6	3,356	588	48, 0	16	16	2

(10) The text in parentheses is the part number reference for this device.
(11) The number of 27x27 multipliers is one-half the number of 18x19 multipliers.

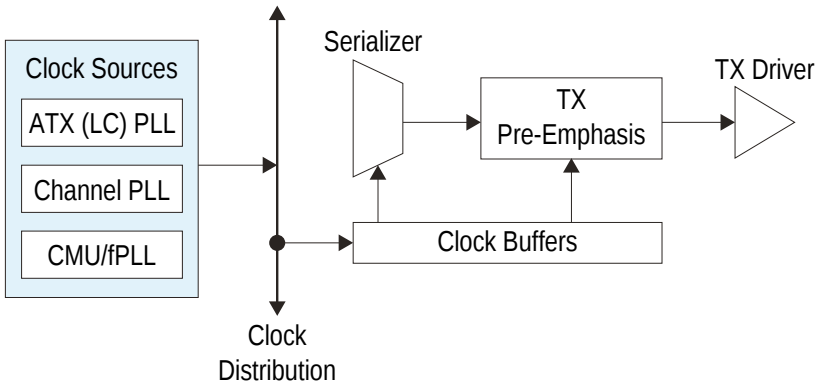
PMA Features

PMA channels are comprised of transmitter (TX), receiver (RX), and high speed clocking resources.

Arria 10 TX features provide exceptional signal integrity at data rates up to 28.05 Gbps. Clocking options include ultra-low jitter ATX (inductor-capacitor) PLLs, channel PLLs, clock multiplier unit (CMU) PLLs, and fractional PLLs (fPLLs):

- ATX PLLs can be configured in integer mode, or optionally, in a new fractional frequency synthesis mode. Each ATX PLL spans the full frequency range of the supported data rate range providing a highly stable and flexible clock source with the lowest jitter.
- CMU PLLs have been enhanced to provide a master clock source within the transceiver bank.
- When not configured as a transceiver channel, select PMA channels can be optionally configured as ring oscillator-based channel PLLs to provide an additional flexible clock source.
- In addition, dedicated on-chip fractional PLLs (fPLLs) are available with precision frequency synthesis capabilities. fPLLs can be used to synthesize multiple clock frequencies from a single reference clock source and replace multiple reference oscillators for multi-protocol and multi-rate applications.

Figure 5: Arria 10 Transmitter Features



On the receiver side, each PMA channel has a dedicated, independent channel PLL for the CDR to provide the maximum number of clocking resources possible without compromising TX clocking sources. Up to 80 independent data rates can be configured on a single Arria 10 device.

Receiver side features provide unparalleled equalization capabilities to drive a wide range of transmission media with the widest range of protocols and data rates. Each receiver channel includes:

- Continuous Time Linear Equalizers (CTLE)—to compensate for channel losses with low power
- Variable Gain Amplifiers (VGA)—to optimize the receiver's dynamic range
- Decision Feedback Equalizers (DFE)—with 7-fixed taps and 4-floating taps to provide additional equalization capability on backplanes even in the presence of crosstalk and reflections

In addition, On-Die Instrumentation (ODI) provides on-chip eye monitoring capabilities (EyeQ). This capability helps to both optimize link equalization parameters during board bring-up and provide in-system link diagnostics. Combined with on-chip jitter injection capabilities, EyeQ provides powerful functionality to do in-system link equalization margin testing.

Feature	Capability
Fractional PLLs	On-chip fractional frequency synthesizers to replace on-board crystal oscillators and reduce system cost
Digitally Assisted Analog CDR	Superior jitter tolerance with fast lock time
On-Die Instrumentation— EyeQ and Jitter Margin Tool	Simplify board bring-up, debug, and diagnostics with non-intrusive, high-resolution eye monitoring (EyeQ). Also inject jitter from transmitter to test link margin in system.
Dynamic Partial Reconfiguration (DPRIO)	Allows for independent control of each transceiver channel Avalon memory-mapped interface for the most transceiver flexibility
Multiple PCS-PMA and PCS-PLD interface widths	8-, 10-, 16-, 20-, 32-, 40-, or 64-bit interface widths for flexibility of deserialization width, encoding, and reduced latency

PCS Features

Arria 10 PMA channels interface with core logic through configurable PCS interface layers.

Multiple gearbox implementations are available to decouple PCS and PMA interface widths. This feature provides the flexibility to implement a wide range of applications with 8-, 10-, 16-, 20-, 32-, 40-, or 64-bit interface widths. Arria 10 FPGAs contain PCS hard IP to support a wide range of standard and proprietary protocols.

The Standard PCS mode provides support for 8B/10B encoded applications up to 12.5 Gbps. The Enhanced PCS mode supports applications up to 17.4 Gbps. In addition, for highly customized implementations, a PCS Direct mode provides a fixed width interface up to 64 bits wide to core logic to allow for custom encoding including support for standards up to 28.05 Gbps.

The enhanced PCS includes an integrated 10GBASE-KR/40GBASE-KR4 Forward Error Correction (FEC) block.

The following table lists some of the key PCS features of Arria 10 transceivers that can be used in a wide range of standard and proprietary protocols from 125 Mbps to 28.05 Gbps.

Table 11: Arria 10 Transceiver PCS Features

PCS Protocol Support	Data Rate (Gbps)	Transmitter Data Path	Receiver Data Path
Standard PCS	0.125 to 12.5	Phase compensation FIFO, byte serializer, 8B/10B encoder, bit-slipper, channel bonding	Rate match FIFO, word-aligner, 8B/10B decoder, byte deserializer, byte ordering
PCI Express Gen1/Gen2 x1, x4, x8	2.5 and 5.0	Same as Standard PCS plus PIPE 2.0 interface to core	Same as Standard PCS plus PIPE 2.0 interface to core

PCS Protocol Support	Data Rate (Gbps)	Transmitter Data Path	Receiver Data Path
PCI Express Gen3 x1, x4, x8	8.0	Phase compensation FIFO, byte serializer, encoder, scrambler, bit-slipper, gear box, channel bonding, and PIPE 3.0 interface to core, auto speed negotiation	Rate match FIFO (0-600 ppm mode), word-aligner, decoder, descrambler, phase compensation FIFO, block sync, byte deserializer, byte ordering, PIPE 3.0 interface to core, auto speed negotiation
CPRI	0.6144 to 9.8	Same as Standard PCS plus deterministic latency serialization	Same as Standard PCS plus deterministic latency deserialization
Enhanced PCS	2.5 to 17.4	FIFO, channel bonding, bit-slipper, and gear box	FIFO, block sync, bit-slipper, and gear box
10GBASE-R	10.3125	FIFO, 64B/66B encoder, scrambler, FEC, and gear box	FIFO, 64B/66B decoder, descrambler, block sync, FEC, and gear box
Interlaken	4.9 to 17.4	FIFO, channel bonding, frame generator, CRC-32 generator, scrambler, disparity generator, bit-slipper, and gear box	FIFO, CRC-32 checker, frame sync, descrambler, disparity checker, block sync, and gear box
SFI-S/SFI-5.2	11.3	FIFO, channel bonding, bit-slipper, and gear box	FIFO, bit-slipper, and gear box
IEEE 1588	1.25 to 10.3125	FIFO (fixed latency), 64B/66B encoder, scrambler, and gear box	FIFO (fixed latency), 64B/66B decoder, descrambler, block sync, and gear box
SDI	up to 11.9	FIFO and gear box	FIFO, bit-slipper, and gear box
GigE	1.25	Same as Standard PCS plus GigE state machine	Same as Standard PCS plus GigE state machine
PCS Direct	up to 28.05	Custom	Custom

PCI Express Gen1/Gen2/Gen3 Hard IP

Arria 10 devices contain embedded PCI Express hard IP designed for performance, ease-of-use, and increased functionality.

The PCI Express hard IP consists of the PHY, Data Link, and Transaction layers, and supports PCI Express Gen1/Gen2/Gen3 end point and root port, in x1/x2/x4/x8 lane configurations. The PCI Express hard IP is capable of operating independently from the core logic. This feature allows the link to power up and complete link training in less than 100 ms, while the Arria 10 device completes loading the programming file for the rest of the FPGA. The hard IP also provides added functionality, which makes it easier to support emerging features such as Single Root I/O Virtualization (SR-IOV) and optional protocol extensions. The Arria 10 PCI Express hard IP has improved end-to-end data path protection using Error Checking and Correction (ECC). In addition, the hard IP supports configuration of the FPGA via protocol across the PCI Express bus at Gen1/Gen2/Gen3 rates (CvP using PCI Express).

Interface	Controller Type	Performance
DDR3	Hard	2133 Mbps
QDR II+ / II+ Xtreme	Soft	550 MTps
RLDRAM III	Hard	2400 Mbps
RLDRAM II	Soft	533 Mbps

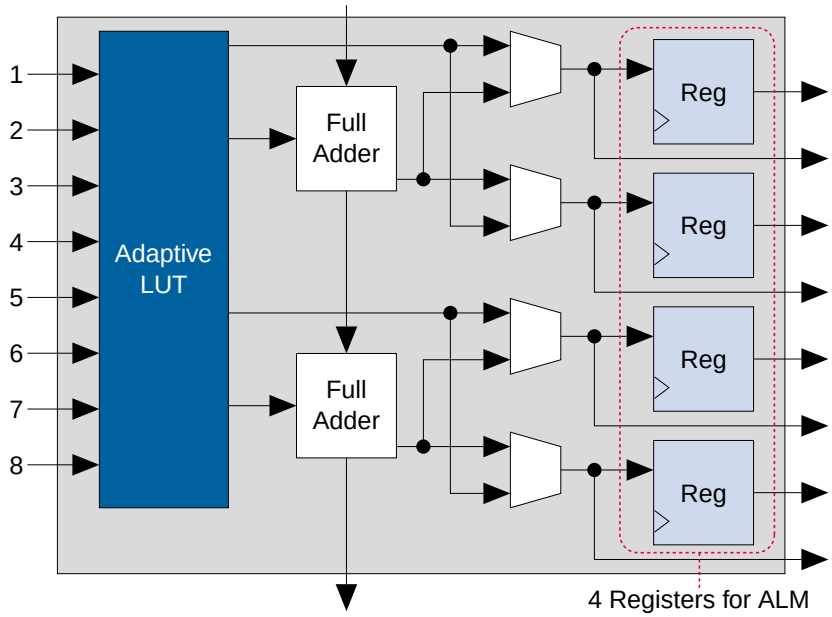
In addition to parallel memory interfaces, Arria 10 devices support serial memory technologies such as the Hybrid Memory Cube (HMC). The HMC is supported by the Arria 10 high-speed serial transceivers, which connect up to four HMC links, with each link running at data rates up to 15 Gbps.

Adaptive Logic Module (ALM)

Arria 10 devices use the same adaptive logic module (ALM) as the previous generation Arria V and Stratix V FPGAs, allowing for efficient implementation of logic functions and easy conversion of IP between the devices.

The ALM block diagram shown in the following figure has eight inputs with a fracturable look-up table (LUT), two dedicated embedded adders, and four dedicated registers.

Figure 7: Arria 10 FPGA and SoC ALM Block Diagram



Key features and capabilities of the Arria 10 ALM include:

- High register count with 4 registers per 8-input fracturable LUT enables Arria 10 devices to maximize core performance at higher core logic utilization
- 6% more logic compared to the traditional 2-register per LUT architecture
- Implements select 7-input logic functions, all 6-input logic functions, and two independent functions consisting of smaller LUT sizes (such as two independent 4-input LUTs) to optimize core logic utilization

The Quartus II software leverages the Arria 10 ALM logic structure to deliver the highest performance, optimal logic utilization, and lowest compile times. The Quartus II software simplifies design reuse as it automatically maps legacy designs into the Arria 10 ALM architecture.

Core Clocking

The Arria 10 device core clock network supports over 500 MHz fabric operation across the full industrial temperature range, and supports the hard memory controllers up to 2666 Mbps with a quarter rate transfer.

The clock network architecture is based on Altera's proven global, regional, and periphery clock structure, which is supported by dedicated clock input pins, fractional clock synthesis PLLs, and integer I/O PLLs. All unused sections of the clock network are identified by the Quartus II software and are powered down to reduce dynamic power consumption.

Fractional Synthesis PLLs and I/O PLLs

Arria 10 devices have up to 32 fractional synthesis PLLs (fPLL) and up to 16 I/O PLLs (IOPLL) that are available for both specific and general purpose use in the core.

The fPLLs are located in columns adjacent to the transceiver blocks. They can be used to reduce both the number of oscillators required on the board and the number of clock pins required, by synthesizing multiple clock frequencies from a single reference clock source. In addition to synthesizing reference clock frequencies for the transceiver CMU and ATX (LC) transmit PLLs, the fPLLs can be used for clock network delay compensation, zero-delay buffering, and direct transmit clocking for transceivers. Each fPLL may be independently configured for conventional integer mode, which is equivalent to a general purpose PLL (GPLL), or enhanced fractional mode with third-order delta-sigma modulation.

The integer mode IOPLLs are located in each bank of 48 I/Os. They can be used to simplify the design of external memory interfaces and high-speed LVDS interfaces. The IOPLLs are adjacent to the hard memory controllers and LVDS SERDES in each I/O bank, making it easier to close timing because these PLLs are tightly coupled with the I/Os that need to use them. Like the fPLLs, the IOPLLs can be used for general purpose applications in the core such as clock network delay compensation and zero-delay buffering.

Internal Embedded Memory

Arria 10 devices contain two types of embedded memory blocks: MLAB (640-bit) and M20K (20-Kbit).

The MLAB blocks are ideal for wide and shallow memories. The M20K blocks are double the size of the M10K blocks used in the previous generation Arria V devices, and are useful for supporting larger memory configurations and include hard ECC. Both types of embedded memory block can be configured as a single-port or dual-port RAM, FIFO, ROM or shift register. These memory blocks are highly flexible and support a number of memory configuration as shown in the following table.

Table 13: Arria 10 Internal Embedded Memory Block Configurations

MLAB (640 bits)	M20K (20 Kbits)
64 x 10 (supported through emulation) 32 x 20	16K x 1 8K x 2 4K x 5 2K x 10 1K x 20 512 x 40

The Quartus II software simplifies design reuse by automatically mapping memory blocks from previous generations of devices into the Arria 10 MLAB and M20K blocks.

Variable Precision DSP Block

The Arria 10 DSP blocks are based upon the Variable Precision DSP Architecture used in Altera's previous generation Arria V FPGAs. The blocks can be configured to natively support signal processing with precision ranging from 18x19 up to 54x54. A pipeline register has been added to increase the maximum operating frequency of the DSP block and reduce power consumption.

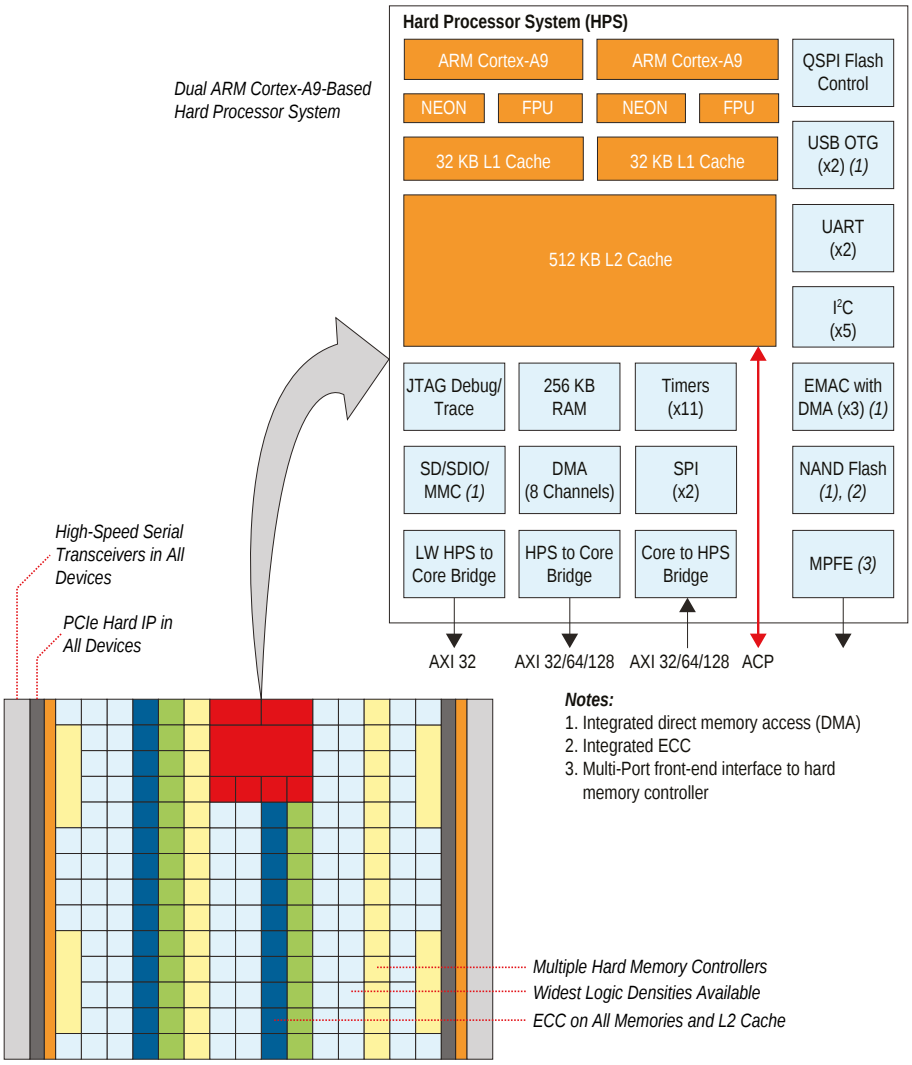
Each DSP block can be independently configured at compile time as either dual 18x19 or a single 27x27 multiply accumulate. With a dedicated 64-bit cascade bus, multiple variable precision DSP blocks can be cascaded to implement even higher precision DSP functions efficiently. The following table shows how different precisions are accommodated within a DSP block, or by utilizing multiple blocks.

Table 14: Variable Precision DSP Block Configurations

Multiplier Size	DSP Block Resources	Expected Usage
18x19 bits	1/2 of Variable Precision DSP Block	Medium precision fixed point
27x27 bits	1 Variable Precision DSP Block	High precision fixed or Single Precision floating point
19x36 bits	1 Variable Precision DSP Block with external adder	Fixed point FFTs
36x36 bits	2 Variable Precision DSP Blocks with external adder	Very high precision fixed point
54x54 bits	4 Variable Precision DSP Blocks with external adder	Double Precision floating point

Complex multiplication is very common in DSP algorithms. One of the most popular applications of complex multipliers is the FFT algorithm. This algorithm has the characteristic of increasing precision requirements on only one side of the multiplier. The Variable Precision DSP block supports the FFT algorithm with proportional increase in DSP resources as the precision grows.

Figure 8: HPS Block Diagram



The HPS has the following features:

- 1.2-GHz, dual-core ARM Cortex-A9 MPCore processor with up to 1.5-GHz via overdrive
  - ARMv7-A architecture and runs 32-bit ARM instructions, 16-bit and 32-bit Thumb instructions, and 8-bit Java byte codes in Jazelle style
  - Superscalar, variable length, out-of-order pipeline with dynamic branch prediction
  - Instruction Efficiency 2.5 MIPS/MHz, at 1.5 GHz total performance of 7500 MIPS
- Each processor core includes:
  - 32 KB of L1 instruction cache, 32 KB of L1 data cache
  - Single- and double-precision floating-point unit and NEON media engine
  - CoreSight debug and trace technology
  - Snoop Control Unit (SCU) and Acceleration Coherency Port (ACP)
- 512 KB of shared L2 cache
- 256 KB of scratch RAM

Key Features of 20-nm HPS

The following features are new in the 20-nm Hard Processor System compared to the 28-nm SoCs:

- **Increased Performance and Overdrive Capability**

  While the nominal processor frequency is 1.2 GHz, the 20 nm HPS offers an "overdrive" feature which enables an even higher processor operating frequency. For this a higher supply voltage value is required that is unique to the HPS and may require a separate regulator.

- **Increased Processor Memory Bandwidth and DDR4 Support**

  Up to 64-bit DDR4 memory @ 2666 Mbps is available for the processor. The hard memory controller for the HPS comprises a multi-port front end that manages connections to a single port memory controller. The multi-port front end allows logic core and the HPS share ports and thereby the available bandwidth of the memory controller.

- **Flexible I/O Sharing**

  An advanced I/O pin muxing scheme allows improved sharing of I/O between the HPS and the core logic. The following types of I/O are available for SoC:

  Dedicated I/O (15)—These I/Os are physically located inside the HPS block and are not accessible to logic within the core. The 15 dedicated I/Os are used for HPS clock, resets, and interfacing with boot devices, QSPI, and SD/MMC

  Direct Shared I/O (48)—These shared I/Os are located closest to the HPS block and are ideal for high speed HPS peripherals such as EMAC, USB, and others. There is one bank of 48 I/Os that supports direct sharing where the 48 I/Os can be shared 12 I/Os at a time.

  Standard (Shared) I/O (All other)—All standard I/Os can be shared by the HPS peripherals and any logic within the core. For designs where more than 48 I/Os are required to fully use all the peripherals in the HPS, these I/Os can be connected through the core logic.

- **EMAC Core**

  A third EMAC core is available in the HPS. Three EMAC cores enable an application to support two redundant Ethernet connections; for example, backplane, or two EMAC cores for managing IEEE 1588 time stamp information while allowing a third EMAC core for debug and configuration. All three EMACs can potentially share the same time stamps, simplifying the 1588 time stamping implementation. A new serial time stamp interface allows core logic to access and read the time stamp values. The integrated EMAC controllers can be connected to external Ethernet PHY through the provided MDIO or I^2C interface.

- **On-Chip Memory**

  The on-chip memory is updated to 256 KB support and can support larger data sets and real time algorithms

- **ECC Enhancements**

  Improvements in L2 Cache ECC management allow identification of errors down to the address level. ECC enhancements also enable improved error injection and status reporting via the introduction of new memory mapped access to syndrome and data signals.

Partial reconfiguration in Arria 10 devices is supported through the following configuration options:

- Partial reconfiguration through the FPP x16 I/O interface
- Partial reconfiguration using PCI Express

Dynamic reconfiguration in Arria 10 devices allows transceiver data rates, protocols and analog settings to be changed dynamically on a channel-by-channel basis while maintaining data transfer on adjacent transceiver channels. Dynamic reconfiguration is ideal for applications that require on-the-fly multi-protocol or multi-rate support, and both the PMA and PCS blocks within the transceiver can be reconfigured using this technique. Dynamic reconfiguration of the transceivers can be used in conjunction with partial reconfiguration of the FPGA to enable partial reconfiguration of both core and transceivers simultaneously.

Single Event Upset (SEU) Error Detection and Correction

Arria 10 devices offer robust and easy-to-use SEU error detection and correction circuitry.

The detection and correction circuitry includes protection for Configuration RAM (CRAM) programming bits and user memories. The CRAM is protected by a continuously running CRC error detection circuit with integrated ECC that automatically corrects one or two errors and detects higher order multi-bit errors. When more than two errors occur, correction is available through reloading of the core programming file, providing a complete design refresh while the FPGA continues to operate.

The physical layout of the Arria 10 CRAM array is optimized to make the majority of multi-bit upsets appear as independent single-bit or double-bit errors which are automatically corrected by the integrated CRAM ECC circuitry. In addition to the CRAM protection, the user memories also include integrated ECC circuitry and are layout optimized for error detection and correction.

Appendix: Arria 10 SoC Developers Corner

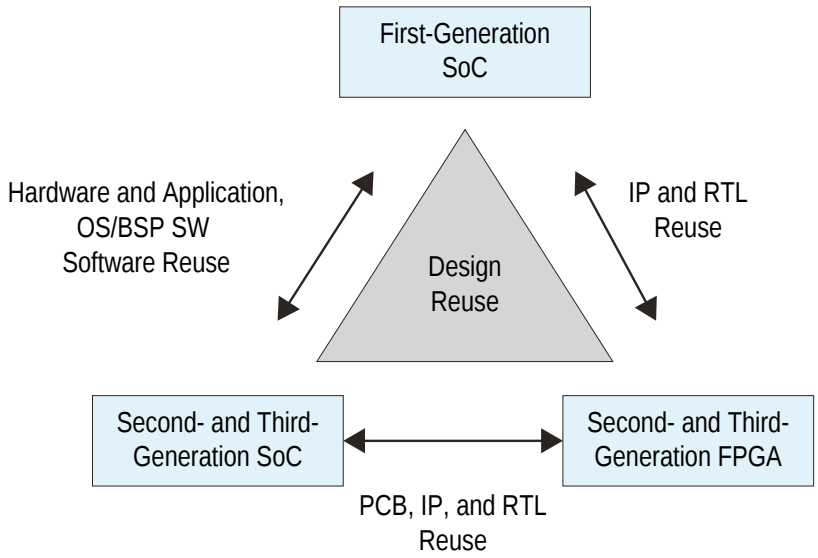
Altera's Arria 10 SoCs provide the combined benefits of programmable logic for high-speed data paths with ARM processor for intelligent control functions:

- High performance programmable core logic, hard memory controllers and high speed transceivers can be used to implement data path centric functions for 40G/100G systems including functions such as framing, bridging, aggregation, switching, traffic management, FEC, multirate aggregation, and data transmission.
- The integrated ARM based HPS implements intelligent control function and eliminates the need for a local processor, thereby reducing system power, form factor, and BOM cost. By adding intelligence to the data path, software on the ARM HPS manages and reduces system downtime and reduces the associated operating expenses. The Dual Core ARM Cortex-A9 based HPS comes with a rich set of embedded peripherals and associated device drivers for wide range of operating systems including Linux and VxWorks. The resulting board support packages can be used as the basis of a number of software applications such as:
  - Operations, Administration and Maintenance (OAM)
  - PCIe Root Port management
  - Remote Debug and System Update
  - Host offload and Algorithm acceleration
  - Chassis management
  - Routing and Look up management
  - Error handling and system downtime management
  - Rule management for deep packet inspection, packet parsing
  - Audio and Video Processing

Altera SoC: The Architecture of Choice When Productivity Matters

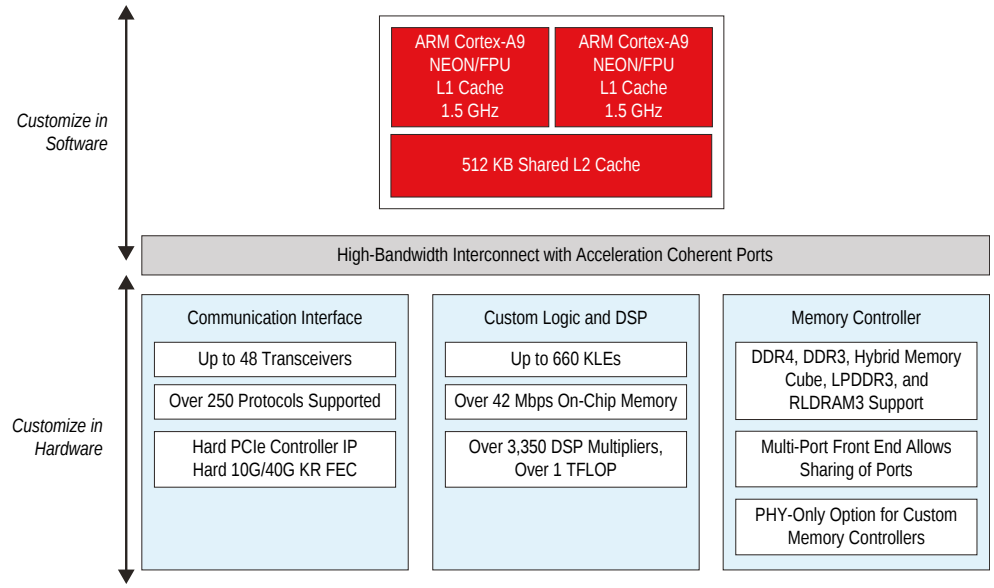
Productivity is the driving philosophy of Altera's Arria 10 SoC family. By reusing hardware, software, IP, and RTL across FPGAs and SoCs, you can reduce design effort and get products to market faster. The Dual Core ARM Cortex-A9 MPCore-based HPS is common to both 20- and 28-nm SoCs and facilitates extensive software code compatibility as well as tools and OS Board Support Package (BSP) reuse. The extensive tools and OS support available as part of Altera and ARM ecosystem and the fast iteration times inherent in software development (especially as compared to FPGA compile times) results in a highly productive embedded and DSP development flow. In addition, Altera offers high-level automated design flows for hardware development, such as the Altera OpenCL (a C-based hardware design flow) and DSP Builder (a model-based hardware design flow).

Figure 9: Hardware and Software Reuse



interfaces, memories, and DSP functions, allowing Altera devices to offer the largest variety of interface and feature support than any off the shelf processor or ASSP. The design cycles for Altera's SoCs are a fraction of ASIC design cycles and offer a much lower risk path compared to an ASIC.

Figure 11: Differentiation through Customization



A New, More Productive DSP Design Flow

With Altera's SoCs, a more productive design flow for DSP design is now available. For the first time, DSP and embedded developers who may be unfamiliar to FPGA and HDL design can develop hardware and take advantage of the remarkable DSP performance available with Altera's SoCs.

In this design flow, DSP and embedded developers begin by running DSP algorithms directly on the ARM HPS. This a natural place to begin as, in many cases, C/C++ are the very languages in which these algorithms have been conceived in the first place. The Dual Core ARM Cortex-A9 MPCore features a double precision FPU and a NEON co-processor for 128-bit SIMD co-processor and is ideal for closed loop control, audio, video, and multimedia processing. The inherent productivity of software design cycles and iterations as compared to FPGA compilation times reduces system compile times drastically. When more performance is required, these software algorithms can be then profiled to identify bottlenecks and subsequently become candidates for hardware acceleration. Hardware accelerators can share data and computed results directly with ARM processor's L2 Cache via the Acceleration Coherency Port (ACP) that manages data coherency without having to incur the penalty of a full L2 Cache flush.