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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

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Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, IrDA, LINbus, Microwire, SmartCard, SPI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, Cap Sense, LCD, LVD, POR, PWM, SmartSense, WDT
Number of I/O	55
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	68-VFQFN Exposed Pad
Supplier Device Package	68-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4245lti-dm405t

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



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Functional Definition

CPU and Memory Subsystem

CPU

The Cortex-M0 CPU in the PSoC 4200-M is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. Most instructions are 16 bits in length and execute a subset of the Thumb-2 instruction set. The Cypress implementation includes a hardware multiplier that provides a 32-bit result in one cycle. It includes a nested vectored interrupt controller (NVIC) block with 32 interrupt inputs and also includes a Wakeup Interrupt Controller (WIC), which can wake the processor up from the Deep Sleep mode allowing power to be switched off to the main processor when the chip is in the Deep Sleep mode. The Cortex-M0 CPU provides a Non-Maskable Interrupt (NMI) input, which is made available to the user when it is not in use for system functions requested by the user.

The CPU also includes a debug interface, the serial wire debug (SWD) interface, which is a 2-wire form of JTAG; the debug configuration used for PSoC 4200-M has four break-point (address) comparators and two watchpoint (data) comparators.

Flash

The PSoC 4200-M has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The flash accelerator delivers 85% of single-cycle SRAM access performance on average. Part of the flash module can be used to emulate EEPROM operation if required.

SRAM

SRAM memory is retained during Hibernate.

SROM

A supervisory ROM that contains boot and configuration routines is provided.

DMA

A DMA engine, with eight channels, is provided that can do 32-bit transfers and has chainable ping-pong descriptors.

System Resources

Power System

The power system is described in detail in the section Power on page 14. It provides assurance that voltage levels are as required for each respective mode and either delay mode entry (on power-on reset (POR), for example) until voltage levels are as required for proper function or generate resets (brown-out detect (BOD)) or interrupts (low voltage detect (LVD)). The PSoC 4200M operates with a single external supply over the range of 1.71 to 5.5 V and has five different power modes, transitions between which are managed by the power system. The PSoC 4200M provides Sleep, Deep Sleep, Hibernate, and Stop low-power modes.

Clock System

The PSoC 4200-M clock system is responsible for providing clocks to all subsystems that require clocks and for switching between different clock sources without glitching. In addition, the clock system ensures that no meta-stable conditions occur.

The clock system for the PSoC 4200-M consists of a Watch Crystal Oscillator (WCO) running at 32 kHz, the IMO (3 to 48 MHz) and the ILO (32-kHz nominal) internal oscillators, and provision for an external clock.

Figure 2. PSoC 4200M MCU Clocking Architecture



The clk_hf signal can be divided down to generate synchronous clocks for the UDBs, and the analog and digital peripherals. There are a total of 16 clock dividers for the PSoC 4200-M, each with 16-bit divide capability; this allows 12 to be used for the fixed-function blocks and four for the UDBs. The analog clock leads the digital clocks to allow analog events to occur before digital clock-related noise is generated. The 16-bit capability allows a lot of flexibility in generating fine-grained frequency values and is fully supported in PSoC Creator.

IMO Clock Source

The IMO is the primary source of internal clocking in the PSoC 4200M. It is trimmed during testing to achieve the specified accuracy. Trim values are stored in nonvolatile memory. Trimming can also be done on the fly to allow in-field calibration. The IMO default frequency is 24 MHz and it can be adjusted between 3 to 48 MHz in steps of 1 MHz. IMO tolerance with Cypress-provided calibration settings is ±2%.

ILO Clock Source

The ILO is a very low power oscillator, nominally 32 kHz, which is primarily used to generate clocks for peripheral operation in Deep Sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy. Cypress provides a software component, which does the calibration.

Crystal Oscillator

The PSoC 4200M clock subsystem also includes a low-frequency crystal oscillator (32-kHz WCO) that is available during the Deep Sleep mode and can be used for Real-Time Clock (RTC) and Watchdog Timer applications.



Watchdog Timer

A watchdog timer is implemented in the clock block running from the low-frequency clock; this allows watchdog operation during Deep Sleep and generates a watchdog reset or an interrupt if not serviced before the timeout occurs. The watchdog reset is recorded in the Reset Cause register.

Reset

The PSoC 4200M can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through reset and allows software to determine the cause of the reset. An XRES pin is reserved for external reset to avoid complications with configuration and multiple pin functions during power-on or reconfiguration.

Voltage Reference

The PSoC 4200M reference system generates all internally required references. A 1% voltage reference spec is provided for the 12-bit ADC. To allow better signal-to-noise ratios (SNR) and better absolute accuracy, it is possible to add an external bypass capacitor to the internal reference using a GPIO pin or to use an external reference for the SAR.

Analog Blocks

12-bit SAR ADC

The 12-bit 1 MSample/second SAR ADC can operate at a maximum clock rate of 18 MHz and requires a minimum of 18 clocks at that frequency to do a 12-bit conversion.

The block functionality is augmented for the user by adding a reference buffer to it (trimmable to \pm 1%) and by providing the choice of three internal voltage references: V_{DD}, V_{DD}/2, and

V_{REF} (nominally 1.024 V) as well as an external reference through a GPIO pin. The Sample-and-Hold (S/H) aperture is programmable allowing the gain bandwidth requirements of the amplifier driving the SAR inputs, which determine its settling time, to be relaxed if required. The system performance will be 65 dB for true 12-bit precision if appropriate references are used and system noise levels permit. To improve performance in noisy conditions, it is possible to provide an external bypass (through a fixed pin location) for the internal reference amplifier.

The SAR is connected to a fixed set of pins through an 8-input sequencer (expandable to 16 inputs). The sequencer cycles through selected channels autonomously (sequencer scan) and does so with zero switching overhead (that is, the aggregate sampling bandwidth is equal to 1 Msps, whether it is for a single channel or distributed over several channels). The sequencer switching is effected through a state machine or through firmware-driven switching. A feature provided by the sequencer is buffering of each channel to reduce CPU interrupt service requirements. To accommodate signals with varying source impedance and frequency, it is possible to have different sample times programmable for each channel. In addition, the signal range specification through a pair of range registers (low and high range values) is implemented with a corresponding out-of-range interrupt if the digitized value exceeds the programmed range; this allows fast detection of out-of-range values without the necessity of having to wait for a sequencer scan to be completed and the CPU to read the values and check for out-of-range values in software.

The SAR is able to digitize the output of the on-board temperature sensor for calibration and other temperature-dependent functions. The SAR is not available in Deep Sleep and Hibernate modes as it requires a high-speed clock (up to 18 MHz). The SAR operating range is 1.71 to 5.5 V.

Figure 3. SAR ADC System Diagram





UDBs can be clocked from a clock divider block, from a port interface (required for peripherals such as SPI), and from the DSI network directly or after synchronization.

A port interface is defined, which acts as a register that can be clocked with the same source as the PLDs inside the UDB array. This allows faster operation because the inputs and outputs can be registered at the port interface close to the I/O pins and at the edge of the array. The port interface registers can be clocked by one of the I/Os from the same port. This allows interfaces such as SPI to operate at higher clock speeds by eliminating the delay for the port input to be routed over DSI and used to register other inputs. The port interface is shown in Figure 6.

The UDBs can generate interrupts (one UDB at a time) to the interrupt controller. The UDBs can connect to any pin on Ports 0, 1, 2, and 3 (each port interconnect requires one UDB) through the DSI.

Figure 6. Port Interface



Fixed Function Digital

Timer/Counter/PWM (TCPWM) Block

The TCPWM block uses a16-bit counter with user-programmable period length. There is a Capture register to record the count value at the time of an event (which may be an I/O event), a period register which is used to either stop or auto-reload the counter when its count is equal to the period register, and compare registers to generate compare value signals, which are used as PWM duty cycle outputs. The block also provides true and complementary outputs with programmable offset between them to allow use as deadband programmable complementary PWM outputs. It also has a Kill input to force outputs to a predetermined state; for example, this is used in motor drive systems when an overcurrent state is indicated and the PWMs driving the FETs need to be shut off immediately with no time for software intervention. The PSoC 4200M has eight TCPWM blocks.

Serial Communication Blocks (SCB)

The PSoC 4200M has four SCBs, which can each implement an I^2 C, UART, or SPI interface.

I²C Mode: The hardware I²C block implements a full multi-master and slave interface (it is capable of multimaster arbitration). This block is capable of operating at speeds of up to 1 Mbps (Fast Mode Plus) and has flexible buffering options to reduce interrupt overhead and latency for the CPU. It also supports EzI²C that creates a mailbox address range in the memory of the PSoC 4200M and effectively reduces I²C communication to reading from and writing to an array in memory. In

addition, the block supports an 8-deep FIFO for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduces the need for clock stretching caused by the CPU not having read data on time. The FIFO mode is available in all channels and is very useful in the absence of DMA.

The I²C peripheral is compatible with the I²C Standard-mode, Fast-mode, and Fast-mode Plus devices as defined in the NXP I²C-bus specification and user manual (UM10204). The I²C bus I/O is implemented with GPIO in open-drain modes.

UART Mode: This is a full-feature UART operating at up to 1 Mbps. It supports automotive single-wire interface (LIN), infrared interface (IrDA), and SmartCard (ISO7816) protocols, all of which are minor variants of the basic UART protocol. In addition, it supports the 9-bit multiprocessor mode that allows addressing of peripherals connected over common RX and TX lines. Common UART functions such as parity error, break detect, and frame error are supported. An 8-deep FIFO allows much greater CPU service latencies to be tolerated.

SPI Mode: The SPI mode supports full Motorola SPI, TI SSP (essentially adds a start pulse used to synchronize SPI Codecs), and National Microwire (half-duplex form of SPI). The SPI block can use the FIFO and also supports an EzSPI mode in which data interchange is reduced to reading and writing an array in memory.

CAN Blocks

There are two independent CAN 2.0B blocks, which are certified CAN conformant.



Each of the pins shown in the previous table can have multiple programmable functions as shown in the following table. Column headings refer to Analog and Alternate pin functions.:

Port/Pin	Analog	Alt. Function 1	Alt. Function 2	Alt. Function 3	Alt. Function 4	Alt. Function 5
P0.0	lpcomp.in_p[0]			can[1].can_rx:0		scb[0].spi_select1:0
P0.1	lpcomp.in_n[0]			can[1].can_tx:0		scb[0].spi_select2:0
P0.2	lpcomp.in_p[1]					scb[0].spi_select3:0
P0.3	lpcomp.in_n[1]					
P0.4	wco_in		scb[1].uart_rx:0		scb[1].i2c_scl:0	scb[1].spi_mosi:1
P0.5	wco_out		scb[1].uart_tx:0		scb[1].i2c_sda:0	scb[1].spi_miso:1
P0.6		ext_clk:0	scb[1].uart_cts:0			scb[1].spi_clk:1
P0.7			scb[1].uart_rts:0	can[1].can_tx_enb_n:0	wakeup	scb[1].spi_select0:1
P5.0	ctb1.oa0.inp	tcpwm.line[4]:2	scb[2].uart_rx:0		scb[2].i2c_scl:0	scb[2].spi_mosi:0
P5.1	ctb1.oa0.inm	tcpwm.line_compl[4]:2	scb[2].uart_tx:0		scb[2].i2c_sda:0	scb[2].spi_miso:0
P5.2	ctb1.oa0.out	tcpwm.line[5]:2	scb[2].uart_cts:0		lpcomp.comp[0]:1	scb[2].spi_clk:0
P5.3	ctb1.oa1.out	tcpwm.line_compl[5]:2	scb[2].uart_rts:0		lpcomp.comp[1]:1	scb[2].spi_select0:0
P5.4	ctb1.oa1.inm	tcpwm.line[6]:2				scb[2].spi_select1:0
P5.5	ctb1.oa1.inp	tcpwm.line_compl[6]:2				scb[2].spi_select2:0
P5.6	ctb1.oa0.inp_alt	tcpwm.line[7]:0				scb[2].spi_select3:0
P5.7	ctb1.oa1.inp_alt	tcpwm.line_compl[7]:0				
P1.0	ctb0.oa0.inp	tcpwm.line[2]:1	scb[0].uart_rx:1		scb[0].i2c_scl:0	scb[0].spi_mosi:1
P1.1	ctb0.oa0.inm	tcpwm.line_compl[2]:1	scb[0].uart_tx:1		scb[0].i2c_sda:0	scb[0].spi_miso:1
P1.2	ctb0.oa0.out	tcpwm.line[3]:1	scb[0].uart_cts:1			scb[0].spi_clk:1
P1.3	ctb0.oa1.out	tcpwm.line_compl[3]:1	scb[0].uart_rts:1			scb[0].spi_select0:1
P1.4	ctb0.oa1.inm	tcpwm.line[6]:1				scb[0].spi_select1:1
P1.5	ctb0.oa1.inp	tcpwm.line_compl[6]:1				scb[0].spi_select2:1
P1.6	ctb0.oa0.inp_alt	tcpwm.line[7]:1				scb[0].spi_select3:1
P1.7	ctb0.oa1.inp_alt	tcpwm.line_compl[7]:1				
P2.0	sarmux.0	tcpwm.line[4]:1			scb[1].i2c_scl:1	scb[1].spi_mosi:2
P2.1	sarmux.1	tcpwm.line_compl[4]:1			scb[1].i2c_sda:1	scb[1].spi_miso:2
P2.2	sarmux.2	tcpwm.line[5]:1				scb[1].spi_clk:2
P2.3	sarmux.3	tcpwm.line_compl[5]:1				scb[1].spi_select0:2
P2.4	sarmux.4	tcpwm.line[0]:1				scb[1].spi_select1:1
P2.5	sarmux.5	tcpwm.line_compl[0]:1				scb[1].spi_select2:1
P2.6	sarmux.6	tcpwm.line[1]:1				scb[1].spi_select3:1



Power

The supply voltage range is 1.71 to 5.5 V with all functions and circuits operating over that range.

The PSoC 4200M family allows two distinct modes of power supply operation: Unregulated External Supply and Regulated External Supply modes.

Unregulated External Supply

In this mode, the PSoC 4200M is powered by an External Power Supply that can be anywhere in the range of 1.8 to 5.5 V. This range is also designed for battery-powered operation, for instance, the chip can be powered from a battery system that starts at 3.5V and works down to 1.8 V. In this mode, the internal regulator of the PSoC 4200M supplies the internal logic and the VCCD output of the PSoC 4200M must be bypassed to ground via an external Capacitor (in the range of 1 to 1.6 μ F; X5R ceramic or better).

The grounds, VSSA and VSS, must be shorted together. Bypass capacitors must be used from VDDD and VDDA to ground, typical practice for systems in this frequency range is to use a capacitor in the 1 μ F range in parallel with a smaller capacitor (0.1 μ F, for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the Bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

Power Supply	Bypass Capacitors
VDDD–VSS and VDDIO-VSS	0.1 μ F ceramic at each pin plus bulk capacitor 1 to 10 μ F.
VDDA-VSSA	0.1 μ F ceramic at pin. Additional 1 μ F to 10 μ F bulk capacitor
VCCD-VSS	1 μ F ceramic capacitor at the VCCD pin
VREF–VSSA (optional)	The internal bandgap may be bypassed with a 1 μ F to 10 μ F capacitor for better ADC performance.

Regulated External Supply

In this mode, the PSoC 4200M is powered by an external power supply that must be within the range of 1.71 to 1.89 V (1.8 \pm 5%); note that this range needs to include power supply ripple. VCCD and VDDD pins are shorted together and bypassed. The internal regulator is disabled in firmware.



Table 3. AC Specifications

Spec ID#	Parameter	Description	Min	Тур	Мах	Units	Details/ Conditions
SID48	F _{CPU}	CPU frequency	DC	-	48	MHz	$1.71 \leq V_{DD} \leq 5.5$
SID49	T _{SLEEP}	Wakeup from sleep mode	-	0	_	μs	Guaranteed by characterization
SID50	T _{DEEPSLEEP}	Wakeup from Deep Sleep mode	-	_	25	μs	24 MHz IMO. Guaranteed by characterization
SID51	T _{HIBERNATE}	Wakeup from Hibernate mode	-	-	0.7	ms	Guaranteed by characterization
SID51A	T _{STOP}	Wakeup from Stop mode	-	-	2	ms	Guaranteed by characterization
SID52	T _{RESETWIDTH}	External reset pulse width	1	_	_	μs	Guaranteed by characterization

GPIO

Table 4. GPIO DC Specifications

Spec ID#	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID57	V _{IH} ^[2]	Input voltage high threshold	0.7 × V _{DDD}	-	-	V	CMOS Input
SID57A	IIHS	Input current when Pad > V _{DDIO} for OVT inputs	-	_	10	μA	Per I ² C Spec
SID58	V _{IL}	Input voltage low threshold	-	-	0.3 × V _{DDD}	V	CMOS Input
SID241	V _{IH} ^[2]	LVTTL input, V _{DDD} < 2.7 V	0.7× V _{DDD}	-	_	V	
SID242	V _{IL}	LVTTL input, V _{DDD} < 2.7 V	_	_	0.3 × V _{DDD}	V	
SID243	V _{IH} ^[2]	LVTTL input, $V_{DDD} \ge 2.7 \text{ V}$	2.0	-	-	V	
SID244	V _{IL}	LVTTL input, $V_{DDD} \ge 2.7 \text{ V}$	-	-	0.8	V	
SID59	V _{OH}	Output voltage high level	V _{DDD} -0.6	-	-	V	I _{OH} = 4 mA at 3-V V _{DDD}
SID60	V _{OH}	Output voltage high level	V _{DDD} -0.5	_	-	V	I _{OH} = 1 mA at 1.8-V V _{DDD}
SID61	V _{OL}	Output voltage low level	-	-	0.6	V	I _{OL} = 4 mA at 1.8-V V _{DDD}
SID62	V _{OL}	Output voltage low level	_	-	0.6	V	I _{OL} = 8 mA at 3-V V _{DDD}
SID62A	V _{OL}	Output voltage low level	-	_	0.4	V	I _{OL} = 3 mA at 3-V V _{DDD}
SID63	R _{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	
SID64	R _{PULLDOWN}	Pull-down resistor	3.5	5.6	8.5	kΩ	
SID65	IIL	Input leakage current (absolute value)	-	-	2	nA	25 °C, V _{DDD} = 3.0 V. Guaranteed by Characterization
SID65A	I _{IL_CTBM}	Input leakage current (absolute value) for CTBM pins	-	-	4	nA	Guaranteed by Characterization
SID66	C _{IN}	Input capacitance	-	-	7	pF	
SID67	V _{HYSTTL}	Input hysteresis LVTTL	25	40	_	mV	$V_{DDD} \ge 2.7 V$

Note 2. V_{IH} must not exceed V_{DDD} + 0.2 V.



Table 4. GPIO DC Specifications (continued)

Spec ID#	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID68	V _{HYSCMOS}	Input hysteresis CMOS	0.05 × V _{DDD}	-	-	mV	
SID69	IDIODE	Current through protection diode to V_{DD}/Vss	-	-	100	μA	Guaranteed by characterization
SID69A	I _{TOT_GPIO}	Maximum Total Source or Sink Chip Current	-	-	200	mA	Guaranteed by characterization

Table 5. GPIO AC Specifications

(Guaranteed by Characterization)^[3]

Spec ID#	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID70	T _{RISEF}	Rise time in fast strong mode	2	-	12	ns	3.3 V V _{DDD} , Cload = 25 pF
SID71	T _{FALLF}	Fall time in fast strong mode	2	-	12	ns	3.3 V V _{DDD} , Cload = 25 pF
SID72	T _{RISES}	Rise time in slow strong mode	10	-	60	ns	3.3 V V _{DDD} , Cload = 25 pF
SID73	T _{FALLS}	Fall time in slow strong mode	10	-	60	ns	3.3 V V _{DDD} , Cload = 25 pF
SID74	F _{GPIOUT1}	GPIO Fout;3.3 V \leq V _{DDD} \leq 5.5 V. Fast strong mode.	_	-	33	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID75	F _{GPIOUT2}	GPIO Fout;1.7 V \leq V _{DDD} \leq 3.3 V. Fast strong mode.	_	-	16.7	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID76	F _{GPIOUT3}	GPIO Fout;3.3 V \leq V _{DDD} \leq 5.5 V. Slow strong mode.	_	-	7	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID245	F _{GPIOUT4}	GPIO Fout;1.7 V \leq V _{DDD} \leq 3.3 V. Slow strong mode.	_	-	3.5	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID246	F _{GPIOIN}	GPIO input operating frequency; 1.71 V \leq V _{DDD} \leq 5.5 V	_	-	48	MHz	90/10% V _{IO}

XRES

Table 6. XRES DC Specifications

Spec ID#	Parameter	Description	Min	Тур	Max	Units	Details/ Conditions
SID77	V _{IH}	Input voltage high threshold	0.7 × V _{DDD}	-	-	V	CMOS Input
SID78	V _{IL}	Input voltage low threshold	-	-	0.3 × V _{DDD}	V	CMOS Input
SID79	R _{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	
SID80	C _{IN}	Input capacitance	-	3	-	pF	
SID81	V _{HYSXRES}	Input voltage hysteresis	-	100	-	mV	Guaranteed by characterization
SID82	IDIODE	Current through protection diode to V_{DDD}/V_{SS}	_	-	100	μA	Guaranteed by characterization

Table 7. XRES AC Specifications

Spec ID#	Parameter	Description	Min	Тур	Max	Units	Details/ Conditions
SID83	T _{RESETWIDTH}	Reset pulse width	1	_	_	μs	Guaranteed by characterization

Note

 Simultaneous switching transitions on many fully-loaded GPIO pins may cause ground perturbations depending on several factors including PCB and decoupling capacitor design. For applications that are very sensitive to ground perturbations, the slower GPIO slew rate setting may be used.



Analog Peripherals

Opamp

Table 8. Opamp Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Тур	Max	Units	Details/ Conditions
	I _{DD}	Opamp block current. No load.	_	_	-	_	
SID269	I _{DD_HI}	Power = high	-	1100	1850	μA	
SID270	I _{DD_MED}	Power = medium	-	550	950	μA	
SID271	I _{DD_LOW}	Power = low	-	150	350	μA	
	GBW	Load = 20 pF, 0.1 mA. V _{DDA} = 2.7 V	-	_	-	_	
SID272	GBW_HI	Power = high	6	-	-	MHz	
SID273	GBW_MED	Power = medium	4	_	-	MHz	
SID274	GBW_LO	Power = low	-	1	-	MHz	
	I _{OUT_MAX}	$V_{DDA} \ge 2.7 \text{ V}, 500 \text{ mV}$ from rail	-	-	-	-	
SID275	I _{OUT_MAX_HI}	Power = high	10	_	-	mA	
SID276	IOUT_MAX_MID	Power = medium	10	-	-	mA	
SID277	IOUT_MAX_LO	Power = low	-	5	-	mA	
	I _{OUT}	V _{DDA} = 1.71 V, 500 mV from rail	-	-	-	_	
SID278	I _{OUT_MAX_HI}	Power = high	4	-	-	mA	
SID279	IOUT_MAX_MID	Power = medium	4	-	-	mA	
SID280	IOUT_MAX_LO	Power = low	-	2	-	mA	
SID281	V _{IN}	Input voltage range	-0.05	-	VDDA - 0.2	V	Charge-pump on, $V_{DDA} \ge 2.7 V$
SID282	V _{CM}	Input common mode voltage	-0.05	-	VDDA - 0.2	V	Charge-pump on, $V_{DDA} \ge 2.7 V$
	V _{OUT}	$V_{DDA} \ge 2.7 V$	-	-	-		
SID283	V _{OUT_1}	Power = high, Iload=10 mA	0.5	-	VDDA - 0.5	V	
SID284	V _{OUT_2}	Power = high, lload=1 mA	0.2	-	VDDA - 0.2	V	
SID285	V _{OUT_3}	Power = medium, Iload=1 mA	0.2	_	VDDA - 0.2	V	
SID286	V _{OUT_4}	Power = low, lload=0.1mA	0.2	_	VDDA - 0.2	V	
SID288	V _{OS TR}	Offset voltage, trimmed	1	±0.5	1	mV	High mode
SID288A	V _{OS TR}	Offset voltage, trimmed	-	±1	-	mV	Medium mode
SID288B	V _{OS TR}	Offset voltage, trimmed	-	±2	-	mV	Low mode
SID290	V _{OS_DR_TR}	Offset voltage drift, trimmed	-10	±3	10	µV/°C	High mode. T _A ≤ 85 °C.
SID290Q	V _{OS_DR_TR}	Offset voltage drift, trimmed	15	±3	15	µV/°C	High mode. T _A ≤ 105 °C
SID290A	V _{OS_DR_TR}	Offset voltage drift, trimmed	-	±10	-	μV/°C	Medium mode
SID290B	V _{OS_DR_TR}	Offset voltage drift, trimmed	-	±10	-	μV/°C	Low mode
SID291	CMRR	DC Common mode rejection ratio. High-power mode. Common Model voltage range from 0.5 V to V _{DDA} - 0.5 V.	60	70	-	dB	V _{DDD} = 3.6 V



Table 9. Comparator DC Specifications (continued)

Spec ID#	Parameter	Description	Min	Тур	Мах	Units	Details/ Conditions
SID248	I _{CMP2}	Block current, low power mode	-	-	100	μA	Guaranteed by characterization
SID259	I _{CMP3}	Block current, ultra low power mode ($V_{DDD} \ge 2.2 \text{ V}$ for Temp < 0 °C, $V_{DDD} \ge$ 1.8 V for Temp > 0 °C)	-	6	28	μA	Guaranteed by characterization
SID90	Z _{CMP}	DC input impedance of comparator	35	-	-	MΩ	Guaranteed by characterization

Table 10. Comparator AC Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID91	T _{RESP1}	Response time, normal mode	-	-	110	ns	50-mV overdrive
SID258	T _{RESP2}	Response time, low power mode	-	-	200	ns	50-mV overdrive
SID92	T _{RESP3}	Response time, ultra low power mode ($V_{DDD} \ge 2.2 \text{ V}$ for Temp < 0 °C, $V_{DDD} \ge$ 1.8 V for Temp > 0 °C)	-	-	15	μs	200-mV overdrive

Temperature Sensor

Table 11. Temperature Sensor Specifications

Spec ID#	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID93	T _{SENSACC}	Temperature sensor accuracy	-5	±1	+5	°C	–40 to +85 °C

SAR ADC

Table 12. SAR ADC DC Specifications

Spec ID#	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID94	A_RES	Resolution	-	-	12	bits	
SID95	A_CHNIS_S	Number of channels - single ended	-	-	16		8 full speed
SID96	A-CHNKS_D	Number of channels - differential	_	-	8		Diff inputs use neighboring I/O
SID97	A-MONO	Monotonicity	-	-	-		Yes. Based on characterization
SID98	A_GAINERR	Gain error	-	-	±0.1	%	With external reference.
SID99	A_OFFSET	Input offset voltage	-	-	2	mV	Measured with 1-V V _{REF.}
SID100	A_ISAR	Current consumption	-	-	1	mA	
SID101	A_VINS	Input voltage range - single ended	V _{SS}	-	V _{DDA}	V	Based on device characterization
SID102	A_VIND	Input voltage range - differential	V _{SS}	-	V _{DDA}	V	Based on device characterization
SID103	A_INRES	Input resistance	_	-	2.2	KΩ	Based on device characterization
SID104	A_INCAP	Input capacitance	_	-	10	pF	Based on device characterization



Digital Peripherals

The following specifications apply to the Timer/Counter/PWM peripheral in timer mode.

Timer/Counter/PWM

Table 15. TCPWM Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID.TCPWM.1	ITCPWM1	Block current consumption at 3 MHz	_	_	45	μA	All modes (Timer/Counter/PWM)
SID.TCPWM.2	ITCPWM2	Block current consumption at 12 MHz	_	-	155	μA	All modes (Timer/Counter/PWM)
SID.TCPWM.2A	ITCPWM3	Block current consumption at 48 MHz	_	_	650	μA	All modes (Timer/Counter/PWM)
SID.TCPWM.3	TCPWMFREQ	Operating frequency	_	-	Fc	MHz	Fc max = Fcpu. Maximum = 24 MHz
SID.TCPWM.4	TPWMENEXT	Input Trigger Pulse Width for all Trigger Events	2/Fc	-	_	ns	Trigger Events can be Stop, Start, Reload, Count, Capture, or Kill depending on which mode of operation is selected.
SID.TCPWM.5	TPWMEXT	Output Trigger Pulse widths	2/Fc	_	_	ns	Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) trigger outputs
SID.TCPWM.5A	TCRES	Resolution of Counter	1/Fc	_	_	ns	Minimum time between successive counts
SID.TCPWM.5B	PWMRES	PWM Resolution	1/Fc	-	-	ns	Minimum pulse width of PWM Output
SID.TCPWM.5C	QRES	Quadrature inputs resolution	1/Fc	_	_	ns	Minimum pulse width between Quadrature phase inputs.

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Table 16. Fixed I²C DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID149	I _{I2C1}	Block current consumption at 100 kHz	-	-	50	μA	
SID150	I _{I2C2}	Block current consumption at 400 kHz	-	-	135	μA	
SID151	I _{I2C3}	Block current consumption at 1 Mbps	-	-	310	μA	
SID152	I _{I2C4}	I ² C enabled in Deep Sleep mode	-	-	1.4	μA	

Table 17. Fixed I²C AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID153	F _{I2C1}	Bit rate	-	-	1	Mbps	



LCD Direct Drive

Table 18. LCD Direct Drive DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID154	ILCDLOW	Operating current in low power mode	-	5	-	μA	16 × 4 small segment disp. at 50 Hz
SID155	C _{LCDCAP}	LCD capacitance per segment/common driver	_	500	5000	pF	Guaranteed by Design
SID156	LCD _{OFFSET}	Long-term segment offset	_	20	-	mV	
SID157	I _{LCDOP1}	PWM Mode current. 5-V bias. 24-MHz IMO	-	0.6	-	mA	32 × 4 segments. 50 Hz, 25 °C
SID158	I _{LCDOP2}	PWM Mode current. 3.3-V bias. 24-MHz IMO.	-	0.5	-	mA	32 × 4 segments. 50 Hz, 25 °C

Table 19. LCD Direct Drive AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID159	F _{LCD}	LCD frame rate	10	50	150	Hz	

Table 20. Fixed UART DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID160	I _{UART1}	Block current consumption at 100 Kbps	-	-	55	μA	
SID161	I _{UART2}	Block current consumption at 1000 Kbps	_	_	312	μA	

Table 21. Fixed UART AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID162	F _{UART}	Bit rate	_	Ι	1	Mbps	

SPI Specifications

Table 22. Fixed SPI DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID163	I _{SPI1}	Block current consumption at 1 Mbps	-	-	360	μΑ	
SID164	I _{SPI2}	Block current consumption at 4 Mbps	-	-	560	μA	
SID165	I _{SPI3}	Block current consumption at 8 Mbps	-	-	600	μA	

Table 23. Fixed SPI AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID166	F _{SPI}	SPI operating frequency (master; 6X oversampling)	Ι	Ι	8	MHz	



Table 24. Fixed SPI Master mode AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID167	Т _{DMO}	MOSI valid after Sclock driving edge	-	-	15	ns	
SID168	T _{DSI}	MISO valid before Sclock capturing edge. Full clock, late MISO Sampling used	20	-	-	ns	
SID169	Т _{НМО}	Previous MOSI data hold time with respect to capturing edge at Slave	0	_	-	ns	

Table 25. Fixed SPI Slave mode AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID170	Т _{DMI}	MOSI valid before Sclock capturing edge	40	-	-	ns	
SID171	T _{DSO}	MISO valid after Sclock driving edge	-	-	42 + 3 × (1/FCPU)	ns	
SID171A	T _{DSO_ext}	MISO valid after Sclock driving edge in Ext. Clock mode	-	-	48	ns	
SID172	T _{HSO}	Previous MISO data hold time	0	-	-	ns	
SID172A	T _{SSELSCK}	SSEL Valid to first SCK Valid edge	100	-	_	ns	

Memory

Table 26. Flash DC Specifications

Spec ID	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID173	V _{PE}	Erase and program voltage	1.71	-	5.5	V	

Table 27. Flash AC Specifications

Spec ID	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID174	T _{ROWWRITE}	Row (block) write time (erase and program)	-	_	20	ms	Row (block) = 128 bytes
SID175	T _{ROWERASE}	Row erase time	-	-	13	ms	
SID176	T _{ROWPROGRAM}	Row program time after erase	-	-	7	ms	
SID178	T _{BULKERASE}	Bulk erase time (128 KB)	-	_	35	ms	
SID179	T _{SECTORERASE}	Sector erase time (8 KB)	-	-	15	ms	
SID180	T _{DEVPROG}	Total device program time	_	_	15	seconds	Guaranteed by charac- terization
SID181	F _{END}	Flash endurance	100 K	_	_	cycles	Guaranteed by charac- terization
SID182	F _{RET}	Flash retention. $T_A \le 55 \degree$ C, 100 K P/E cycles	20	_	_	years	Guaranteed by charac- terization
SID182A		Flash retention. $T_A \le 85$ °C, 10 K P/E cycles	10	_	_	years	Guaranteed by charac- terization
SID182B	F _{RETQ}	Flash retention. $T_A \le 105$ °C, 10K P/E cycles, \le three years at $T_A \ge$ 85 °C	10	20	-	years	Guaranteed by charac- terization.



System Resources

Power-on-Reset (POR) with Brown Out

Table 28. Imprecise Power On Reset (PRES)

Spec ID	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID185	V _{RISEIPOR}	Rising trip voltage	0.80	-	1.45	V	Guaranteed by charac- terization
SID186	V _{FALLIPOR}	Falling trip voltage	0.75	-	1.4	V	Guaranteed by charac- terization
SID187	V _{IPORHYST}	Hysteresis	15	-	200	mV	Guaranteed by charac- terization

Table 29. Precise Power On Reset (POR)

Spec ID	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID190	V _{FALLPPOR}	BOD trip voltage in active and sleep modes	1.64	_	_	V	Guaranteed by charac- terization
SID192	V _{FALLDPSLP}	BOD trip voltage in Deep Sleep	1.4	-	-	V	Guaranteed by charac- terization

Voltage Monitors

Table 30. Voltage Monitors DC Specifications

Spec ID	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID195	V _{LVI1}	LVI_A/D_SEL[3:0] = 0000b	1.71	1.75	1.79	V	
SID196	V _{LVI2}	LVI_A/D_SEL[3:0] = 0001b	1.76	1.80	1.85	V	
SID197	V _{LVI3}	LVI_A/D_SEL[3:0] = 0010b	1.85	1.90	1.95	V	
SID198	V _{LVI4}	LVI_A/D_SEL[3:0] = 0011b	1.95	2.00	2.05	V	
SID199	V _{LVI5}	LVI_A/D_SEL[3:0] = 0100b	2.05	2.10	2.15	V	
SID200	V _{LVI6}	LVI_A/D_SEL[3:0] = 0101b	2.15	2.20	2.26	V	
SID201	V _{LVI7}	LVI_A/D_SEL[3:0] = 0110b	2.24	2.30	2.36	V	
SID202	V _{LVI8}	LVI_A/D_SEL[3:0] = 0111b	2.34	2.40	2.46	V	
SID203	V _{LVI9}	LVI_A/D_SEL[3:0] = 1000b	2.44	2.50	2.56	V	
SID204	V _{LVI10}	LVI_A/D_SEL[3:0] = 1001b	2.54	2.60	2.67	V	
SID205	V _{LVI11}	LVI_A/D_SEL[3:0] = 1010b	2.63	2.70	2.77	V	
SID206	V _{LVI12}	LVI_A/D_SEL[3:0] = 1011b	2.73	2.80	2.87	V	
SID207	V _{LVI13}	LVI_A/D_SEL[3:0] = 1100b	2.83	2.90	2.97	V	
SID208	V _{LVI14}	LVI_A/D_SEL[3:0] = 1101b	2.93	3.00	3.08	V	
SID209	V _{LVI15}	LVI_A/D_SEL[3:0] = 1110b	3.12	3.20	3.28	V	
SID210	V _{LVI16}	LVI_A/D_SEL[3:0] = 1111b	4.39	4.50	4.61	V	
SID211	LVI_IDD	Block current	_	_	100	μA	Guaranteed by charac- terization

Table 31. Voltage Monitors AC Specifications

Spec ID	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID212	T _{MONTRIP}	Voltage monitor trip time	1	-	1	μs	Guaranteed by charac- terization







51-85051 *D









Acronyms

Table 46. Acronyms Used in this Document

Acronym	Description
abus	analog local bus
ADC	analog-to-digital converter
AG	analog global
АНВ	AMBA (advanced microcontroller bus archi- tecture) high-performance bus, an ARM data transfer bus
ALU	arithmetic logic unit
AMUXBUS	analog multiplexer bus
API	application programming interface
APSR	application program status register
ARM®	advanced RISC machine, a CPU architecture
ATM	automatic thump mode
BW	bandwidth
CAN	Controller Area Network, a communications protocol
CMRR	common-mode rejection ratio
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
DAC	digital-to-analog converter, see also IDAC, VDAC
DFB	digital filter block
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DMIPS	Dhrystone million instructions per second
DMA	direct memory access, see also TD
DNL	differential nonlinearity, see also INL
DNU	do not use
DR	port write data registers
DSI	digital system interconnect
DWT	data watchpoint and trace
ECC	error correcting code
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
EMIF	external memory interface
EOC	end of conversion
EOF	end of frame
EPSR	execution program status register
ESD	electrostatic discharge

Table 46. Acronyms Used in this Document (continu	ied)
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Acronym	Description
ETM	embedded trace macrocell
FIR	finite impulse response, see also IIR
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output, applies to a PSoC pin
HVI	high-voltage interrupt, see also LVI, LVD
IC	integrated circuit
IDAC	current DAC, see also DAC, VDAC
IDE	integrated development environment
I ² C, or IIC	Inter-Integrated Circuit, a communications protocol
lir	infinite impulse response, see also FIR
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
INL	integral nonlinearity, see also DNL
I/O	input/output, see also GPIO, DIO, SIO, USBIO
IPOR	initial power-on reset
IPSR	interrupt program status register
IRQ	interrupt request
ITM	instrumentation trace macrocell
LCD	liquid crystal display
LIN	Local Interconnect Network, a communications protocol.
LR	link register
LUT	lookup table
LVD	low-voltage detect, see also LVI
LVI	low-voltage interrupt, see also HVI
LVTTL	low-voltage transistor-transistor logic
MAC	multiply-accumulate
MCU	microcontroller unit
MISO	master-in slave-out
NC	no connect
NMI	nonmaskable interrupt
NRZ	non-return-to-zero
NVIC	nested vectored interrupt controller
NVL	nonvolatile latch, see also WOL
opamp	operational amplifier
PAL	programmable array logic, see also PLD
PC	program counter
PCB	printed circuit board



Table 46. Acronyms Used in this Document (continued)

Acronym	Description	
PGA	programmable gain amplifier	
PHUB	peripheral hub	
PHY	physical layer	
PICU	port interrupt control unit	
PLA	programmable logic array	
PLD	programmable logic device, see also PAL	
PLL	phase-locked loop	
PMDD	package material declaration data sheet	
POR	power-on reset	
PRES	precise power-on reset	
PRS	pseudo random sequence	
PS	port read data register	
PSoC [®]	Programmable System-on-Chip™	
PSRR	power supply rejection ratio	
PWM	pulse-width modulator	
RAM	random-access memory	
RISC	reduced-instruction-set computing	
RMS	root-mean-square	
RTC	real-time clock	
RTL	register transfer language	
RTR	remote transmission request	
RX	receive	
SAR	successive approximation register	
SC/CT	switched capacitor/continuous time	
SCL	I ² C serial clock	
SDA	I ² C serial data	
S/H	sample and hold	
SINAD	signal to noise and distortion ratio	
SIO	special input/output, GPIO with advanced features. See GPIO.	
SOC	start of conversion	
SOF	start of frame	
SPI	Serial Peripheral Interface, a communications protocol	
SR	slew rate	
SRAM	static random access memory	
SRES	software reset	
SWD	serial wire debug, a test protocol	
SWV	single-wire viewer	
TD	transaction descriptor, see also DMA	

Table 46. Acronyms Used in this Document (continued)

Acronym	Description	
THD	total harmonic distortion	
TIA	transimpedance amplifier	
TRM	technical reference manual	
TTL	transistor-transistor logic	
ТΧ	transmit	
UART	Universal Asynchronous Transmitter Receiver, a communications protocol	
UDB	universal digital block	
USB	Universal Serial Bus	
USBIO	USB input/output, PSoC pins used to connect to a USB port	
VDAC	voltage DAC, see also DAC, IDAC	
WDT	watchdog timer	
WOL	write once latch, see also NVL	
WRES	watchdog timer reset	
XRES	external reset I/O pin	
XTAL	crystal	



Document Conventions

Units of Measure

Table 47. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
dB	decibel
fF	femto farad
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
Khr	kilohour
kHz	kilohertz
kΩ	kilo ohm
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
μA	microampere
μF	microfarad
μH	microhenry
μs	microsecond
μV	microvolt
μW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
sqrtHz	square root of hertz
V	volt



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