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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I <sup>2</sup> C, IrDA, LINbus, Microwire, SmartCard, SPI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, Cap Sense, LCD, LVD, POR, PWM, SmartSense, WDT
Number of I/O	51
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-TQFP (14x14)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4246axi-m445">https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4246axi-m445</a>

## More Information

Cypress provides a wealth of data at [www.cypress.com](http://www.cypress.com) to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article [KBA86521](#), [How to Design with PSoC 3](#), [PSoC 4](#), and [PSoC 5LP](#). Following is an abbreviated list for PSoC 4:

- Overview: [PSoC Portfolio](#), [PSoC Roadmap](#)
- Product Selectors: [PSoC 1](#), [PSoC 3](#), [PSoC 4](#), [PSoC 5LP](#)  
In addition, PSoC Creator includes a device selection tool.
- Application notes: Cypress offers a large number of PSoC application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with PSoC 4 are:
  - [AN79953](#): Getting Started With PSoC 4
  - [AN88619](#): PSoC 4 Hardware Design Considerations
  - [AN86439](#): Using PSoC 4 GPIO Pins
  - [AN57821](#): Mixed Signal Circuit Board Layout
  - [AN81623](#): Digital Design Best Practices
  - [AN73854](#): Introduction To Bootloaders
  - [AN89610](#): ARM Cortex Code Optimization
- Technical Reference Manual (TRM) is in two documents:
  - [Architecture TRM](#) details each PSoC 4 functional block.
  - [Registers TRM](#) describes each of the PSoC 4 registers.
- Development Kits:
  - [CY8CKIT-042](#), PSoC 4 Pioneer Kit, is an easy-to-use and inexpensive development platform. This kit includes connectors for Arduino™ compatible shields and Digilent® Pmod™ daughter cards.
  - [CY8CKIT-049](#) is a very low-cost prototyping platform. It is a low-cost alternative to sampling PSoC 4 devices.
  - [CY8CKIT-001](#) is a common development platform for any one of the PSoC 1, PSoC 3, PSoC 4, or PSoC 5LP families of devices.

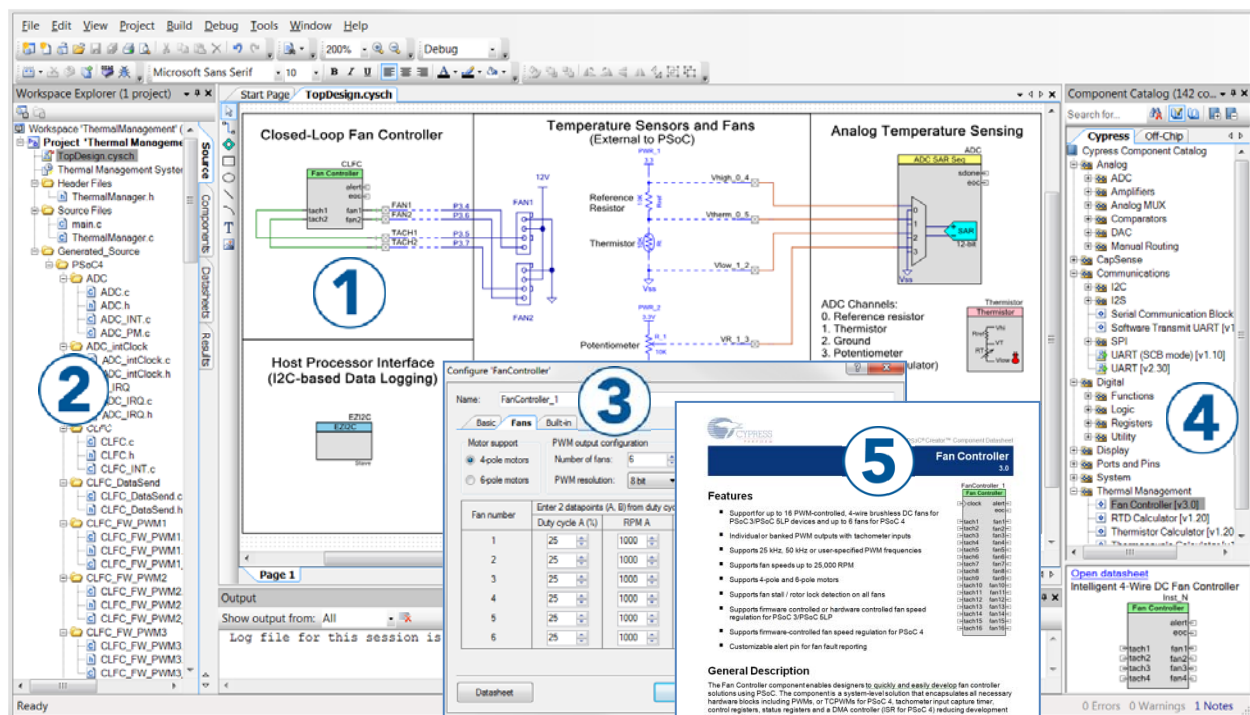
The [MiniProg3](#) device provides an interface for flash programming and debug.

## PSoC Creator

[PSoC Creator](#) is a free Windows-based Integrated Design Environment (IDE). It enables concurrent hardware and firmware design of PSoC 3, PSoC 4, and PSoC 5LP based systems. Create designs using classic, familiar schematic capture supported by over 100 pre-verified, production-ready PSoC Components; see the [list of component datasheets](#). With PSoC Creator, you can:

1. Drag and drop component icons to build your hardware system design in the main design workspace
2. Codesign your application firmware with the PSoC hardware, using the PSoC Creator IDE C compiler
3. Configure components using the configuration tools
4. Explore the library of 100+ components
5. Review component datasheets

**Figure 1. Multiple-Sensor Example Project in PSoC Creator**



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## Functional Definition

### CPU and Memory Subsystem

#### CPU

The Cortex-M0 CPU in the PSoC 4200-M is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. Most instructions are 16 bits in length and execute a subset of the Thumb-2 instruction set. The Cypress implementation includes a hardware multiplier that provides a 32-bit result in one cycle. It includes a nested vectored interrupt controller (NVIC) block with 32 interrupt inputs and also includes a Wakeup Interrupt Controller (WIC), which can wake the processor up from the Deep Sleep mode allowing power to be switched off to the main processor when the chip is in the Deep Sleep mode. The Cortex-M0 CPU provides a Non-Maskable Interrupt (NMI) input, which is made available to the user when it is not in use for system functions requested by the user.

The CPU also includes a debug interface, the serial wire debug (SWD) interface, which is a 2-wire form of JTAG; the debug configuration used for PSoC 4200-M has four break-point (address) comparators and two watchpoint (data) comparators.

#### Flash

The PSoC 4200-M has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The flash accelerator delivers 85% of single-cycle SRAM access performance on average. Part of the flash module can be used to emulate EEPROM operation if required.

#### SRAM

SRAM memory is retained during Hibernate.

#### SROM

A supervisory ROM that contains boot and configuration routines is provided.

#### DMA

A DMA engine, with eight channels, is provided that can do 32-bit transfers and has chainable ping-pong descriptors.

### System Resources

#### Power System

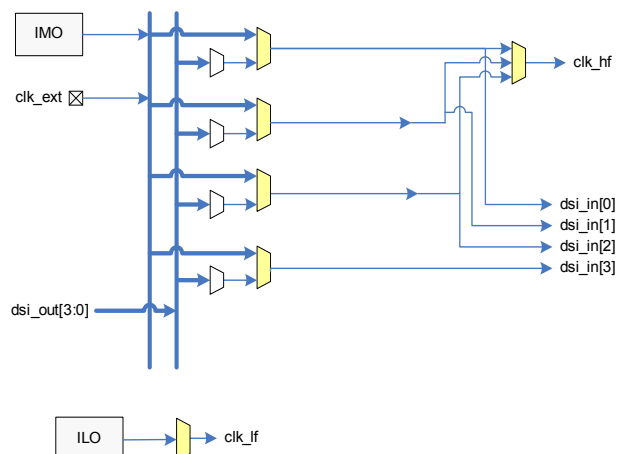
The power system is described in detail in the section [Power on page 14](#). It provides assurance that voltage levels are as required for each respective mode and either delay mode entry (on power-on reset (POR), for example) until voltage levels are as required for proper function or generate resets (brown-out detect (BOD)) or interrupts (low voltage detect (LVD)). The PSoC 4200M operates with a single external supply over the range of 1.71 to 5.5 V and has five different power modes, transitions between which are managed by the power system. The PSoC 4200M provides Sleep, Deep Sleep, Hibernate, and Stop low-power modes.

#### Clock System

The PSoC 4200-M clock system is responsible for providing clocks to all subsystems that require clocks and for switching between different clock sources without glitching. In addition, the clock system ensures that no meta-stable conditions occur.

The clock system for the PSoC 4200-M consists of a Watch Crystal Oscillator (WCO) running at 32 kHz, the IMO (3 to 48 MHz) and the ILO (32-kHz nominal) internal oscillators, and provision for an external clock.

**Figure 2. PSoC 4200M MCU Clocking Architecture**



The clk\_hf signal can be divided down to generate synchronous clocks for the UDBs, and the analog and digital peripherals. There are a total of 16 clock dividers for the PSoC 4200-M, each with 16-bit divide capability; this allows 12 to be used for the fixed-function blocks and four for the UDBs. The analog clock leads the digital clocks to allow analog events to occur before digital clock-related noise is generated. The 16-bit capability allows a lot of flexibility in generating fine-grained frequency values and is fully supported in PSoC Creator.

#### IMO Clock Source

The IMO is the primary source of internal clocking in the PSoC 4200M. It is trimmed during testing to achieve the specified accuracy. Trim values are stored in nonvolatile memory. Trimming can also be done on the fly to allow in-field calibration. The IMO default frequency is 24 MHz and it can be adjusted between 3 to 48 MHz in steps of 1 MHz. IMO tolerance with Cypress-provided calibration settings is  $\pm 2\%$ .

#### ILO Clock Source

The ILO is a very low power oscillator, nominally 32 kHz, which is primarily used to generate clocks for peripheral operation in Deep Sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy. Cypress provides a software component, which does the calibration.

#### Crystal Oscillator

The PSoC 4200M clock subsystem also includes a low-frequency crystal oscillator (32-kHz WCO) that is available during the Deep Sleep mode and can be used for Real-Time Clock (RTC) and Watchdog Timer applications.

### Watchdog Timer

A watchdog timer is implemented in the clock block running from the low-frequency clock; this allows watchdog operation during Deep Sleep and generates a watchdog reset or an interrupt if not serviced before the timeout occurs. The watchdog reset is recorded in the Reset Cause register.

### Reset

The PSoC 4200M can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through reset and allows software to determine the cause of the reset. An XRES pin is reserved for external reset to avoid complications with configuration and multiple pin functions during power-on or reconfiguration.

### Voltage Reference

The PSoC 4200M reference system generates all internally required references. A 1% voltage reference spec is provided for the 12-bit ADC. To allow better signal-to-noise ratios (SNR) and better absolute accuracy, it is possible to add an external bypass capacitor to the internal reference using a GPIO pin or to use an external reference for the SAR.

## Analog Blocks

### 12-bit SAR ADC

The 12-bit 1 MSample/second SAR ADC can operate at a maximum clock rate of 18 MHz and requires a minimum of 18 clocks at that frequency to do a 12-bit conversion.

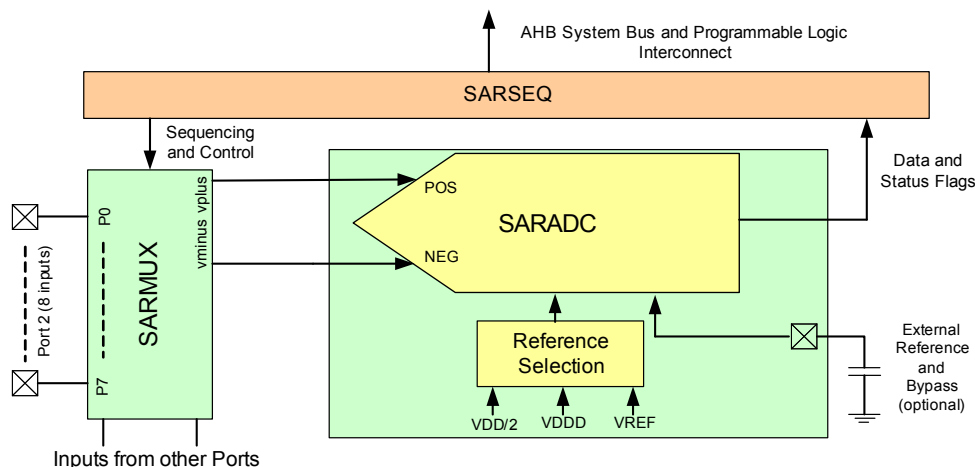
The block functionality is augmented for the user by adding a reference buffer to it (trimmable to  $\pm 1\%$ ) and by providing the choice of three internal voltage references:  $V_{DD}$ ,  $V_{DD}/2$ , and

$V_{REF}$  (nominally 1.024 V) as well as an external reference through a GPIO pin. The Sample-and-Hold (S/H) aperture is programmable allowing the gain bandwidth requirements of the amplifier driving the SAR inputs, which determine its settling time, to be relaxed if required. The system performance will be 65 dB for true 12-bit precision if appropriate references are used and system noise levels permit. To improve performance in noisy conditions, it is possible to provide an external bypass (through a fixed pin location) for the internal reference amplifier.

The SAR is connected to a fixed set of pins through an 8-input sequencer (expandable to 16 inputs). The sequencer cycles through selected channels autonomously (sequencer scan) and does so with zero switching overhead (that is, the aggregate sampling bandwidth is equal to 1 Msps, whether it is for a single channel or distributed over several channels). The sequencer switching is effected through a state machine or through firmware-driven switching. A feature provided by the sequencer is buffering of each channel to reduce CPU interrupt service requirements. To accommodate signals with varying source impedance and frequency, it is possible to have different sample times programmable for each channel. In addition, the signal range specification through a pair of range registers (low and high range values) is implemented with a corresponding out-of-range interrupt if the digitized value exceeds the programmed range; this allows fast detection of out-of-range values without the necessity of having to wait for a sequencer scan to be completed and the CPU to read the values and check for out-of-range values in software.

The SAR is able to digitize the output of the on-board temperature sensor for calibration and other temperature-dependent functions. The SAR is not available in Deep Sleep and Hibernate modes as it requires a high-speed clock (up to 18 MHz). The SAR operating range is 1.71 to 5.5 V.

**Figure 3. SAR ADC System Diagram**





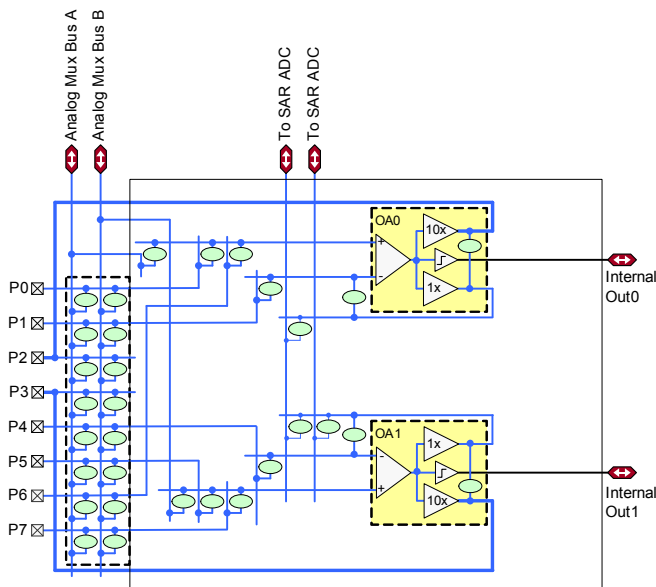
## Analog Multiplex Bus

The PSoC 4200M has two concentric analog buses (Analog Mux Bus A and Analog Mux Bus B) that circumnavigate the periphery of the chip. These buses can transport analog signals from any pin to various analog blocks (including the opamps) and to the CapSense blocks allowing, for instance, the ADC to monitor any pin on the chip. These buses are independent and can also be split into three independent sections. This allows one section to be used for CapSense purposes, one for general analog signal processing, and the third for general-purpose digital peripherals and GPIO.

## Four Opamps

The PSoC 4200M has four opamps with comparator modes, which allow most common analog functions to be performed on-chip eliminating external components; PGAs, voltage buffers, filters, trans-impedance amplifiers, and other functions can be realized with external passives saving power, cost, and space. The on-chip opamps are designed with enough bandwidth to drive the Sample-and-Hold circuit of the ADC without requiring external buffering. The opamps can operate in the Deep Sleep mode at very low power levels. The following diagram shows one of two identical opamp pairs of the opamp subsystem.

**Figure 4. Identical Opamp Pairs in Opamp Subsystem**



The ovals in Figure 4 represent analog switches, which may be controlled via user firmware, the SAR sequencer, or user-defined programmable logic. The opamps (OA0 and OA1) are configurable via these switches to perform all standard opamp functions with appropriate feedback components.

The opamps (OA0 and OA1) are programmable and reconfigurable to provide standard opamp functionality via switchable feedback components, unity gain functionality for driving pins directly, or for internal use (such as buffering SAR ADC inputs as indicated in the diagram), or as true comparators.

The opamp inputs provide highly flexible connectivity and can connect directly to dedicated pins or, via the analog mux buses,

to any pin on the chip. Analog switch connectivity is controllable by user firmware as well as user-defined programmable digital state machines (implemented via UDBs).

The opamps operate in Deep Sleep mode at very low currents allowing analog circuits to remain operational during Deep Sleep.

## Temperature Sensor

The PSoC 4200M has one on-chip temperature sensor. This consists of a diode, which is biased by a current source that can be disabled to save power. The temperature sensor is connected to the ADC, which digitizes the reading and produces a temperature value using Cypress-supplied software that includes calibration and linearization.

## Low-power Comparators

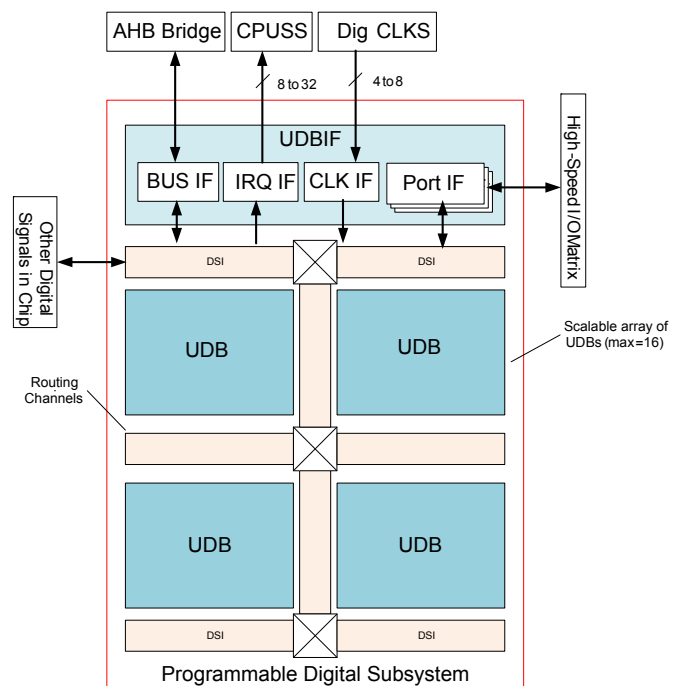
The PSoC 4200M has a pair of low-power comparators, which can also operate in the Deep Sleep and Hibernate modes. This allows the analog system blocks to be disabled while retaining the ability to monitor external voltage levels during low-power modes. The comparator outputs are normally synchronized to avoid meta-stability unless operating in an asynchronous power mode (Hibernate) where the system wake-up circuit is activated by a comparator switch event.

## Programmable Digital

### Universal Digital Blocks (UDBs) and Port Interfaces

The PSoC 4200M has four UDBs; the UDB array also provides a switched Digital System Interconnect (DSI) fabric that allows signals from peripherals and ports to be routed to and through the UDBs for communication and control. The UDB array is shown in the following figure.

**Figure 5. UDB Array**



## GPIO

The PSoC 4200M has 55 GPIOs in the 68-pin QFN package. The GPIO block implements the following:

- Eight drive strength modes including strong push-pull, resistive pull-up and pull-down, weak (resistive) pull-up and pull-down, open drain and open source, input only, and disabled
- Input threshold select (CMOS or LVTTTL)
- Individual control of input and output disables
- Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode and Hibernate modes)
- Selectable slew rates for dV/dt related noise control to improve EMI

The pins are organized in logical entities called ports, which are 8-bit in width. During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin. Pin locations for fixed-function peripherals are also fixed to reduce internal multiplexing complexity (these signals do not go through the DSI network). DSI signals are not affected by this and any pin on Ports 0, 1, 2, and 3 may be routed to any UDB through the DSI network. Only pins on Ports 0, 1, 2, and 3 may be routed through DSI signals.

Data output and pin state registers store, respectively, the values to be driven on the pins and the states of the pins themselves.

Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it (8 for PSoC 4200M).

The Pins of Port 6 (up to 6 depending on the package) are overvoltage tolerant ( $V_{IN}$  can exceed  $V_{DD}$ ). The overvoltage cells will not sink more than 10  $\mu$ A when their inputs exceed  $V_{DDIO}$  in compliance with I<sup>2</sup>C specifications.

## Special Function Peripherals

### LCD Segment Drive

The PSoC 4200M has an LCD controller, which can drive up to four commons and up to 51 segments. Any pin can be either a common or a segment pin. It uses full digital methods to drive the LCD segments requiring no generation of internal LCD voltages.

The two methods used are referred to as digital correlation and PWM.

Digital correlation pertains to modulating the frequency and levels of the common and segment signals to generate the highest RMS voltage across a segment to light it up or to keep the RMS signal zero. This method is good for STN displays but may result in reduced contrast with TN (cheaper) displays.

PWM pertains to driving the panel with PWM signals to effectively use the capacitance of the panel to provide the integration of the modulated pulse-width to generate the desired LCD voltage. This method results in higher power consumption but can result in better results when driving TN displays. LCD operation is supported during Deep Sleep refreshing a small display buffer (4 bits; 1 32-bit register per port).

### CapSense

CapSense is supported on all pins in the PSoC 4200M through a CapSense Sigma-Delta (CSD) block that can be connected to any pin through an analog mux bus that any GPIO pin can be connected to via an Analog switch. CapSense functionality can thus be provided on any pin or group of pins in a system under software control. A component is provided for the CapSense block, which provides automatic hardware tuning (Cypress SmartSense™), to make it easy for the user.

Shield voltage can be driven on another Mux Bus to provide water tolerance capability. Water tolerance is provided by driving the shield electrode in phase with the sense electrode to keep the shield capacitance from attenuating the sensed input.

Each CSD block has two IDACs which can be used for general purposes if CapSense is not being used (both IDACs are available in that case) or if CapSense is used without water tolerance (one IDAC is available). The PSoC 4200M has two CSD blocks which can be used independently; one for CapSense and one providing two IDACs.

The two CapSense blocks are referred to as CSD0 and CSD1. Capacitance sensing inputs on Ports 0, 1, 2, 3, 4, 6, and 7 are sensed by CSD0. Capacitance sensing inputs on Port 5 are sensed by CSD1.

## Pinouts

The following is the pin list for the PSoC 4200M. This shows the power supply and port pins (for example, P0.0 is Pin 0 of Port 0).

68-QFN		64-TQFP		48-TQFP		44-TQFP	
Pin	Name	Pin	Name	Pin	Name	Pin	Name
42	P0.0	39	P0.0	28	P0.0	24	P0.0
43	P0.1	40	P0.1	29	P0.1	25	P0.1
44	P0.2	41	P0.2	30	P0.2	26	P0.2
45	P0.3	42	P0.3	31	P0.3	27	P0.3
46	P0.4	43	P0.4	32	P0.4	28	P0.4
47	P0.5	44	P0.5	33	P0.5	29	P0.5
48	P0.6	45	P0.6	34	P0.6	30	P0.6
49	P0.7	46	P0.7	35	P0.7	31	P0.7
50	XRES	47	XRES	36	XRES	32	XRES
51	VCCD	48	VCCD	37	VCCD	33	VCCD
52	VSSD	49	VSSD	38	VSSD	DN	VSSD
53	VDDD	50	VDDD	39	VDDD	34	VDDD
				40	VDDA	35	VDDA
54	P5.0	51	P5.0				
55	P5.1	52	P5.1				
56	P5.2	53	P5.2				
57	P5.3	54	P5.3				
58	P5.4						
59	P5.5	55	P5.5				
60	VDDA	56	VDDA	40	VDDA	35	VDDA
61	VSSA	57	VSSA	41	VSSA	36	VSSA
62	P1.0	58	P1.0	42	P1.0	37	P1.0
63	P1.1	59	P1.1	43	P1.1	38	P1.1
64	P1.2	60	P1.2	44	P1.2	39	P1.2
65	P1.3	61	P1.3	45	P1.3	40	P1.3
66	P1.4	62	P1.4	46	P1.4	41	P1.4
67	P1.5	63	P1.5	47	P1.5	42	P1.5
68	P1.6	64	P1.6	48	P1.6	43	P1.6
1	P1.7/VREF	1	P1.7/VREF	1	P1.7/VREF	44	P1.7/VREF
						1	VSSD
2	P2.0	2	P2.0	2	P2.0	2	P2.0
3	P2.1	3	P2.1	3	P2.1	3	P2.1
4	P2.2	4	P2.2	4	P2.2	4	P2.2
5	P2.3	5	P2.3	5	P2.3	5	P2.3
6	P2.4	6	P2.4	6	P2.4	6	P2.4
7	P2.5	7	P2.5	7	P2.5	7	P2.5



68-QFN		64-TQFP		48-TQFP		44-TQFP	
Pin	Name	Pin	Name	Pin	Name	Pin	Name
8	P2.6	8	P2.6	8	P2.6	8	P2.6
9	P2.7	9	P2.7	9	P2.7	9	P2.7
10	VSSA	10	VSSA	10	VSSD	10	VSSD
11	VDDA	11	VDDA				
12	P6.0	12	P6.0				
13	P6.1	13	P6.1				
14	P6.2	14	P6.2				
15	P6.3						
16	P6.4	15	P6.4				
17	P6.5	16	P6.5				
18	VSSIO	17	VSSIO	10	VSSD	10	VSSD
19	P3.0	18	P3.0	12	P3.0	11	P3.0
20	P3.1	19	P3.1	13	P3.1	12	P3.1
21	P3.2	20	P3.2	14	P3.2	13	P3.2
22	P3.3	21	P3.3	16	P3.3	14	P3.3
23	P3.4	22	P3.4	17	P3.4	15	P3.4
24	P3.5	23	P3.5	18	P3.5	16	P3.5
25	P3.6	24	P3.6	19	P3.6	17	P3.6
26	P3.7	25	P3.7	20	P3.7	18	P3.7
27	VDDIO	26	VDDIO	21	VDDIO	19	VDDD
28	P4.0	27	P4.0	22	P4.0	20	P4.0
29	P4.1	28	P4.1	23	P4.1	21	P4.1
30	P4.2	29	P4.2	24	P4.2	22	P4.2
31	P4.3	30	P4.3	25	P4.3	23	P4.3
32	P4.4	31	P4.4				
33	P4.5	32	P4.5				
34	P4.6	33	P4.6				
35	P4.7						
39	P7.0	37	P7.0	26	P7.0		
40	P7.1	38	P7.1	27	P7.1		
41	P7.2						

The pins of Port 6 are overvoltage-tolerant. Pins 36, 37, and 38 are No-Connects on the 68-pin QFN. Pins 34, 35, and 36 are No-Connects on the 64-pin TQFP. Pins 11 and 15 are No-connects in the 48-pin TQFP. All VSS pins must be tied together.

The output drivers of I/O Ports P0 and P7 are connected to VDDD. Output drivers of I/O Ports 1, 2, and 5 are connected to VDDA. Output drivers of I/O Ports 3, 4, and 6 are connected to VDDIO.

## Development Support

The PSoC 4200M family has a rich set of documentation, development tools, and online resources to assist you during your development process. Visit [www.cypress.com/go/psoc4](http://www.cypress.com/go/psoc4) to find out more.

### Documentation

A suite of documentation supports the PSoC 4200M family to ensure that you can find answers to your questions quickly. This section contains a list of some of the key documents.

**Software User Guide:** A step-by-step guide for using PSoC Creator. The software user guide shows you how the PSoC Creator build process works in detail, how to use source control with PSoC Creator, and much more.

**Component Datasheets:** The flexibility of PSoC allows the creation of new peripherals (components) long after the device has gone into production. Component data sheets provide all of the information needed to select and use a particular component, including a functional description, API documentation, example code, and AC/DC specifications.

**Application Notes:** PSoC application notes discuss a particular application of PSoC in depth; examples include brushless DC motor control and on-chip filtering. Application notes often include example projects in addition to the application note document.

**Technical Reference Manual:** The Technical Reference Manual (TRM) contains all the technical detail you need to use a PSoC device, including a complete description of all PSoC registers.

### Online

In addition to print documentation, the Cypress PSoC forums connect you with fellow PSoC users and experts in PSoC from around the world, 24 hours a day, 7 days a week.

### Tools

With industry standard cores, programming, and debugging interfaces, the PSoC 4200M family is part of a development tool ecosystem. Visit us at [www.cypress.com/go/psoccreator](http://www.cypress.com/go/psoccreator) for the latest information on the revolutionary, easy to use PSoC Creator IDE, supported third party compilers, programmers, debuggers, and development kits.

## Electrical Specifications

### Absolute Maximum Ratings

**Table 1. Absolute Maximum Ratings<sup>[1]</sup>**

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID1	V <sub>DD_ABS</sub>	Analog or digital supply relative to V <sub>SS</sub> (V <sub>SSD</sub> = V <sub>SSA</sub> )	−0.5	–	6	V	Absolute maximum
SID2	V <sub>CCD_ABS</sub>	Direct digital core voltage input relative to V <sub>SSD</sub>	−0.5	–	1.95	V	Absolute maximum
SID3	V <sub>GPIO_ABS</sub>	GPIO voltage; V <sub>DDD</sub> or V <sub>DDA</sub>	−0.5	–	V <sub>DD</sub> +0.5	V	Absolute maximum
SID4	I <sub>GPIO_ABS</sub>	Current per GPIO	−25	–	25	mA	Absolute maximum
SID5	I <sub>G-PIO_injection</sub>	GPIO injection current per pin	−0.5	–	0.5	mA	Absolute maximum
BID44	ESD_HBM	Electrostatic discharge human body model	2200	–	–	V	
BID45	ESD_CDM	Electrostatic discharge charged device model	500	–	–	V	
BID46	LU	Pin current for latch-up	−140	–	140	mA	

### Device Level Specifications

All specifications are valid for  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 105\text{ }^{\circ}\text{C}$  and  $T_J \leq 125\text{ }^{\circ}\text{C}$ , except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

**Table 2. DC Specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID53	V <sub>DD</sub>	Power Supply Input Voltage (V <sub>DDA</sub> = V <sub>DDD</sub> = V <sub>DD</sub> )	1.8	–	5.5	V	With regulator enabled
SID255	V <sub>DDD</sub>	Power Supply Input Voltage unregulated	1.71	1.8	1.89	V	Internally unregulated Supply
SID54	V <sub>CCD</sub>	Output voltage (for core logic)	–	1.8	–	V	
SID55	C <sub>EFC</sub>	External Regulator voltage bypass	1	1.3	1.6	μF	X5R ceramic or better
SID56	C <sub>EXC</sub>	Power supply decoupling capacitor	–	1	–	μF	X5R ceramic or better
<b>Active Mode, V<sub>DD</sub> = 1.71 V to 5.5 V, −40 °C to +105 °C</b>							
SID6	I <sub>DD1</sub>	Execute from Flash; CPU at 6 MHz	–	2.2	2.8	mA	
SID7	I <sub>DD2</sub>	Execute from Flash; CPU at 12 MHz	–	3.7	4.2	mA	
SID8	I <sub>DD3</sub>	Execute from Flash; CPU at 24 MHz	–	6.7	7.2	mA	
SID9	I <sub>DD4</sub>	Execute from Flash; CPU at 48 MHz	–	13	13.8	mA	
<b>Sleep Mode, −40 °C to +105 °C</b>							
SID21	I <sub>DD16</sub>	I <sup>2</sup> C wakeup, WDT, and Comparators on. Regulator Off.	–	1.75	2.1	mA	V <sub>DD</sub> = 1.71 to 1.89, 6 MHz
SID22	I <sub>DD17</sub>	I <sup>2</sup> C wakeup, WDT, and Comparators on.	–	1.7	2.1	mA	V <sub>DD</sub> = 1.8 to 5.5, 6 MHz
SID23	I <sub>DD18</sub>	I <sup>2</sup> C wakeup, WDT, and Comparators on. Regulator Off.	–	2.35	2.8	mA	V <sub>DD</sub> = 1.71 to 1.89, 12 MHz
SID24	I <sub>DD19</sub>	I <sup>2</sup> C wakeup, WDT, and Comparators on.	–	2.25	2.8	mA	V <sub>DD</sub> = 1.8 to 5.5, 12 MHz

#### Note

- Usage above the absolute maximum conditions listed in Table 1 may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.

**Table 4. GPIO DC Specifications** (continued)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID68	V <sub>HYS</sub> CMOS	Input hysteresis CMOS	0.05 × V <sub>DD</sub>	–	–	mV	
SID69	I <sub>DIODE</sub>	Current through protection diode to V <sub>DD</sub> /V <sub>SS</sub>	–	–	100	μA	Guaranteed by characterization
SID69A	I <sub>TOT_GPIO</sub>	Maximum Total Source or Sink Chip Current	–	–	200	mA	Guaranteed by characterization

**Table 5. GPIO AC Specifications**

(Guaranteed by Characterization)<sup>[3]</sup>

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID70	T <sub>RISE</sub> F	Rise time in fast strong mode	2	–	12	ns	3.3 V V <sub>DD</sub> , Cload = 25 pF
SID71	T <sub>FALL</sub> F	Fall time in fast strong mode	2	–	12	ns	3.3 V V <sub>DD</sub> , Cload = 25 pF
SID72	T <sub>RISE</sub> S	Rise time in slow strong mode	10	–	60	ns	3.3 V V <sub>DD</sub> , Cload = 25 pF
SID73	T <sub>FALL</sub> S	Fall time in slow strong mode	10	–	60	ns	3.3 V V <sub>DD</sub> , Cload = 25 pF
SID74	F <sub>GPIO</sub> OUT1	GPIO Fout; 3.3 V ≤ V <sub>DD</sub> ≤ 5.5 V. Fast strong mode.	–	–	33	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID75	F <sub>GPIO</sub> OUT2	GPIO Fout; 1.7 V ≤ V <sub>DD</sub> ≤ 3.3 V. Fast strong mode.	–	–	16.7	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID76	F <sub>GPIO</sub> OUT3	GPIO Fout; 3.3 V ≤ V <sub>DD</sub> ≤ 5.5 V. Slow strong mode.	–	–	7	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID245	F <sub>GPIO</sub> OUT4	GPIO Fout; 1.7 V ≤ V <sub>DD</sub> ≤ 3.3 V. Slow strong mode.	–	–	3.5	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID246	F <sub>GPIO</sub> IN	GPIO input operating frequency; 1.71 V ≤ V <sub>DD</sub> ≤ 5.5 V	–	–	48	MHz	90/10% V <sub>IO</sub>

## XRES

**Table 6. XRES DC Specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID77	V <sub>IH</sub>	Input voltage high threshold	0.7 × V <sub>DD</sub>	–	–	V	CMOS Input
SID78	V <sub>IL</sub>	Input voltage low threshold	–	–	0.3 × V <sub>DD</sub>	V	CMOS Input
SID79	R <sub>PULLUP</sub>	Pull-up resistor	3.5	5.6	8.5	kΩ	
SID80	C <sub>IN</sub>	Input capacitance	–	3	–	pF	
SID81	V <sub>HYS</sub> XRES	Input voltage hysteresis	–	100	–	mV	Guaranteed by characterization
SID82	I <sub>DIODE</sub>	Current through protection diode to V <sub>DD</sub> /V <sub>SS</sub>	–	–	100	μA	Guaranteed by characterization

**Table 7. XRES AC Specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID83	T <sub>RESET</sub> WIDTH	Reset pulse width	1	–	–	μs	Guaranteed by characterization

### Note

3. Simultaneous switching transitions on many fully-loaded GPIO pins may cause ground perturbations depending on several factors including PCB and decoupling capacitor design. For applications that are very sensitive to ground perturbations, the slower GPIO slew rate setting may be used.

## Analog Peripherals

### Opamp

**Table 8. Opamp Specifications**

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
	$I_{DD}$	Opamp block current. No load.	–	–	–	–	
SID269	$I_{DD\_HI}$	Power = high	–	1100	1850	μA	
SID270	$I_{DD\_MED}$	Power = medium	–	550	950	μA	
SID271	$I_{DD\_LOW}$	Power = low	–	150	350	μA	
	GBW	Load = 20 pF, 0.1 mA. $V_{DDA} = 2.7$ V	–	–	–	–	
SID272	GBW_HI	Power = high	6	–	–	MHz	
SID273	GBW_MED	Power = medium	4	–	–	MHz	
SID274	GBW_LO	Power = low	–	1	–	MHz	
	$I_{OUT\_MAX}$	$V_{DDA} \geq 2.7$ V, 500 mV from rail	–	–	–	–	
SID275	$I_{OUT\_MAX\_HI}$	Power = high	10	–	–	mA	
SID276	$I_{OUT\_MAX\_MID}$	Power = medium	10	–	–	mA	
SID277	$I_{OUT\_MAX\_LO}$	Power = low	–	5	–	mA	
	$I_{OUT}$	$V_{DDA} = 1.71$ V, 500 mV from rail	–	–	–	–	
SID278	$I_{OUT\_MAX\_HI}$	Power = high	4	–	–	mA	
SID279	$I_{OUT\_MAX\_MID}$	Power = medium	4	–	–	mA	
SID280	$I_{OUT\_MAX\_LO}$	Power = low	–	2	–	mA	
SID281	$V_{IN}$	Input voltage range	–0.05	–	$V_{DDA} - 0.2$	V	Charge-pump on, $V_{DDA} \geq 2.7$ V
SID282	$V_{CM}$	Input common mode voltage	–0.05	–	$V_{DDA} - 0.2$	V	Charge-pump on, $V_{DDA} \geq 2.7$ V
	$V_{OUT}$	$V_{DDA} \geq 2.7$ V	–	–	–		
SID283	$V_{OUT\_1}$	Power = high, Iload=10 mA	0.5	–	$V_{DDA} - 0.5$	V	
SID284	$V_{OUT\_2}$	Power = high, Iload=1 mA	0.2	–	$V_{DDA} - 0.2$	V	
SID285	$V_{OUT\_3}$	Power = medium, Iload=1 mA	0.2	–	$V_{DDA} - 0.2$	V	
SID286	$V_{OUT\_4}$	Power = low, Iload=0.1mA	0.2	–	$V_{DDA} - 0.2$	V	
SID288	$V_{OS\_TR}$	Offset voltage, trimmed	1	±0.5	1	mV	High mode
SID288A	$V_{OS\_TR}$	Offset voltage, trimmed	–	±1	–	mV	Medium mode
SID288B	$V_{OS\_TR}$	Offset voltage, trimmed	–	±2	–	mV	Low mode
SID290	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–10	±3	10	μV/°C	High mode. $T_A \leq 85$ °C.
SID290Q	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	15	±3	15	μV/°C	High mode. $T_A \leq 105$ °C
SID290A	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–	±10	–	μV/°C	Medium mode
SID290B	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–	±10	–	μV/°C	Low mode
SID291	CMRR	DC Common mode rejection ratio. High-power mode. Common Model voltage range from 0.5 V to $V_{DDA} - 0.5$ V.	60	70	–	dB	$V_{DD} = 3.6$ V

**Table 8. Opamp Specifications**

(Guaranteed by Characterization) (continued)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID292	PSRR	At 1 kHz, 100-mV ripple	70	85	–	dB	V <sub>DD</sub> = 3.6 V
	Noise		–	–	–	–	
SID293	V <sub>N1</sub>	Input referred, 1 Hz - 1 GHz, power = high	–	94	–	µVrms	
SID294	V <sub>N2</sub>	Input referred, 1 kHz, power = high	–	72	–	nV/rHz	
SID295	V <sub>N3</sub>	Input referred, 10kHz, power = high	–	28	–	nV/rHz	
SID296	V <sub>N4</sub>	Input referred, 100kHz, power = high	–	15	–	nV/rHz	
SID297	Cload	Stable up to maximum load. Performance specs at 50 pF.	–	–	125	pF	
SID298	Slew_rate	Cload = 50 pF, Power = High, V <sub>DDA</sub> ≥ 2.7 V	6	–	–	V/µs	
SID299	T <sub>op_wake</sub>	From disable to enable, no external RC dominating	–	25	–	µs	
SID299A	OL_GAIN	Open Loop Gain	–	90	–	dB	
	Comp_mode	Comparator mode; 50 mV drive, Trise = Tfall (approx.)	–	–	–		
SID300	T <sub>PD1</sub>	Response time; power = high	–	150	–	ns	
SID301	T <sub>PD2</sub>	Response time; power = medium	–	400	–	ns	
SID302	T <sub>PD3</sub>	Response time; power = low	–	2000	–	ns	
SID303	V <sub>hyst_op</sub>	Hysteresis	–	10	–	mV	
<b>Deep Sleep Mode</b>		Mode 2 is lowest current range. Mode 1 has higher GBW.					Deep Sleep mode. V <sub>DDA</sub> ≥ 2.7 V.
SID_DS_1	IDD_HI_M1	Mode 1, High current	–	1400	–	µA	25 °C
SID_DS_2	IDD_MED_M1	Mode 1, Medium current	–	700	–	µA	25 °C
SID_DS_3	IDD_LOW_M1	Mode 1, Low current	–	200	–	µA	25 °C
SID_DS_4	IDD_HI_M2	Mode 2, High current	–	120	–	µA	25 °C
SID_DS_5	IDD_MED_M2	Mode 2, Medium current	–	60	–	µA	25 °C
SID_DS_6	IDD_LOW_M2	Mode 2, Low current	–	15	–	µA	25 °C
SID_DS_7	GBW_HI_M1	Mode 1, High current	–	4	–	MHz	25 °C
SID_DS_8	GBW_MED_M1	Mode 1, Medium current	–	2	–	MHz	25 °C
SID_DS_9	GBW_LOW_M1	Mode 1, Low current	–	0.5	–	MHz	25 °C
SID_DS_10	GBW_HI_M2	Mode 2, High current	–	0.5	–	MHz	20-pF load, no DC load 0.2 V to V <sub>DDA</sub> -1.5 V
SID_DS_11	GBW_MED_M2	Mode 2, Medium current	–	0.2	–	MHz	20-pF load, no DC load 0.2 V to V <sub>DDA</sub> -1.5 V
SID_DS_12	GBW_LOW_M2	Mode 2, Low current	–	0.1	–	MHz	20-pF load, no DC load 0.2 V to V <sub>DDA</sub> -1.5 V
SID_DS_13	VOS_HI_M1	Mode 1, High current	–	5	–	mV	With trim 25 °C, 0.2 V to V <sub>DDA</sub> -1.5 V
SID_DS_14	VOS_MED_M1	Mode 1, Medium current	–	5	–	mV	With trim 25 °C, 0.2 V to V <sub>DDA</sub> -1.5 V



**Table 24. Fixed SPI Master mode AC Specifications**

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID167	T <sub>DMO</sub>	MOSI valid after Sclock driving edge	–	–	15	ns	
SID168	T <sub>DSI</sub>	MISO valid before Sclock capturing edge. Full clock, late MISO Sampling used	20	–	–	ns	
SID169	T <sub>HMO</sub>	Previous MOSI data hold time with respect to capturing edge at Slave	0	–	–	ns	

**Table 25. Fixed SPI Slave mode AC Specifications**

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID170	T <sub>DMI</sub>	MOSI valid before Sclock capturing edge	40	–	–	ns	
SID171	T <sub>DSO</sub>	MISO valid after Sclock driving edge	–	–	42 + 3 × (1/FCPU)	ns	
SID171A	T <sub>DSO_ext</sub>	MISO valid after Sclock driving edge in Ext. Clock mode	–	–	48	ns	
SID172	T <sub>HSO</sub>	Previous MISO data hold time	0	–	–	ns	
SID172A	T <sub>SSELCK</sub>	SSEL Valid to first SCK Valid edge	100	–	–	ns	

## Memory

**Table 26. Flash DC Specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID173	V <sub>PE</sub>	Erase and program voltage	1.71	–	5.5	V	

**Table 27. Flash AC Specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID174	T <sub>ROWWRITE</sub>	Row (block) write time (erase and program)	–	–	20	ms	Row (block) = 128 bytes
SID175	T <sub>ROWERASE</sub>	Row erase time	–	–	13	ms	
SID176	T <sub>ROWPROGRAM</sub>	Row program time after erase	–	–	7	ms	
SID178	T <sub>BULKERASE</sub>	Bulk erase time (128 KB)	–	–	35	ms	
SID179	T <sub>SECTORERASE</sub>	Sector erase time (8 KB)	–	–	15	ms	
SID180	T <sub>DEVPROG</sub>	Total device program time	–	–	15	seconds	Guaranteed by characterization
SID181	F <sub>END</sub>	Flash endurance	100 K	–	–	cycles	Guaranteed by characterization
SID182	F <sub>RET</sub>	Flash retention. T <sub>A</sub> ≤ 55 °C, 100 K P/E cycles	20	–	–	years	Guaranteed by characterization
SID182A		Flash retention. T <sub>A</sub> ≤ 85 °C, 10 K P/E cycles	10	–	–	years	Guaranteed by characterization
SID182B	F <sub>RETQ</sub>	Flash retention. T <sub>A</sub> ≤ 105 °C, 10K P/E cycles, ≤ three years at T <sub>A</sub> ≥ 85 °C	10	20	–	years	Guaranteed by characterization.

**Table 36. ILO AC Specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID234	T <sub>STARTILO1</sub>	ILO startup time	–	–	2	ms	Guaranteed by characterization
SID236	T <sub>ILODUTY</sub>	ILO duty cycle	40	50	60	%	Guaranteed by characterization
SID237	F <sub>ILOTRIM1</sub>	32 kHz trimmed frequency	15	32	50	kHz	Max ILO frequency is 70 kHz if T <sub>A</sub> > 85 °C

**Table 37. External Clock Specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID305	ExtClkFreq	External Clock input Frequency	0	–	48	MHz	Guaranteed by characterization
SID306	ExtClkDuty	Duty cycle; Measured at V <sub>DD/2</sub>	45	–	55	%	Guaranteed by characterization

**Table 38. Watch Crystal Oscillator (WCO) Specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
<b>IMO WCO-PLL calibrated mode</b>							
SID330	IMO <sub>WCO1</sub>	Frequency variation with IMO set to 3 MHz	–0.6	–	0.6	%	Does not include WCO tolerance
SID331	IMO <sub>WCO2</sub>	Frequency variation with IMO set to 5 MHz	–0.4	–	0.4	%	Does not include WCO tolerance
SID332	IMO <sub>WCO3</sub>	Frequency variation with IMO set to 7 MHz or 9 MHz	–0.3	–	0.3	%	Does not include WCO tolerance
SID333	IMO <sub>WCO4</sub>	All other IMO frequency settings	–0.2	–	0.2	%	Does not include WCO tolerance
<b>WCO Specifications</b>							
SID398	F <sub>WCO</sub>	Crystal frequency	–	32.768	–	kHz	
SID399	F <sub>TOL</sub>	Frequency tolerance	–	50	250	ppm	With 20-ppm crystal.
SID400	ESR	Equivalent series resistance	–	50	–	kΩ	
SID401	PD	Drive level	–	–	1	μW	
SID402	T <sub>START</sub>	Startup time	–	–	500	ms	
SID403	C <sub>L</sub>	Crystal load capacitance	6	–	12.5	pF	
SID404	C <sub>0</sub>	Crystal shunt capacitance	–	1.35	–	pF	
SID405	I <sub>WCO1</sub>	Operating current (high power mode)	–	–	8	uA	

**Table 39. UDB AC Specifications**

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
<b>Datapath performance</b>							
SID249	F <sub>MAX-TIMER</sub>	Max frequency of 16-bit timer in a UDB pair	–	–	48	MHz	
SID250	F <sub>MAX-ADDER</sub>	Max frequency of 16-bit adder in a UDB pair	–	–	48	MHz	

## Packaging

The description of the PSoC4200M package dimensions follows.

Spec ID#	Package	Description	Package Dwg #
PKG_1	68-pin QFN	68-pin QFN, 8 mm x 8 mm x 1.0 mm height with 0.4 mm pitch	001-09618
PKG_2	64-pin TQFP	64-pin TQFP, 10 mm x10 mm x 1.4 mm height with 0.5 mm pitch	51-85051
PKG_4	64-pin TQFP	64-pin TQFP, 14 mm x14 mm x 1.4 mm height with 0.8 mm pitch	51-85046
PKG_5	48-pin TQFP	48-pin TQFP, 7 mm x 7 mm x 1.4 mm height with 0.5 mm pitch	51-85135
PKG_6	44-pin TQFP	44-pin TQFP, 10 mm x 10 mm x 1.4 mm height with 0.8 mm pitch	51-85064

**Table 43. Package Characteristics**

Parameter	Description	Conditions	Min	Typ	Max	Units
T <sub>A</sub>	Operating ambient temperature		−40	25	85	°C
T <sub>J</sub>	Operating junction temperature		−40		100	°C
T <sub>JA</sub>	Package $\theta_{JA}$ (68-pin QFN)		−	16.8	−	°C/Watt
T <sub>JC</sub>	Package $\theta_{JC}$ (68-pin QFN)		−	2.9	−	°C/Watt
T <sub>JA</sub>	Package $\theta_{JA}$ (64-pin TQFP, 0.5-mm pitch)		−	56	−	°C/Watt
T <sub>JC</sub>	Package $\theta_{JC}$ (64-pin TQFP, 0.5-mm pitch)		−	19.5	−	°C/Watt
T <sub>JA</sub>	Package $\theta_{JA}$ (64-pin TQFP, 0.8-mm pitch)		−	66.4	−	°C/Watt
T <sub>JC</sub>	Package $\theta_{JC}$ (64-pin TQFP, 0.8-mm pitch)		−	18.2	−	°C/Watt
T <sub>JA</sub>	Package $\theta_{JA}$ (48-pin TQFP, 0.5-mm pitch)		−	67.3	−	°C/Watt
T <sub>JC</sub>	Package $\theta_{JC}$ (48-pin TQFP, 0.5-mm pitch)		−	30.4	−	°C/Watt
T <sub>JA</sub>	Package $\theta_{JA}$ (44-pin TQFP, 0.8-mm pitch)		−	57	−	°C/Watt
T <sub>JC</sub>	Package $\theta_{JC}$ (44-pin TQFP, 0.8-mm pitch)		−	25.9	−	°C/Watt

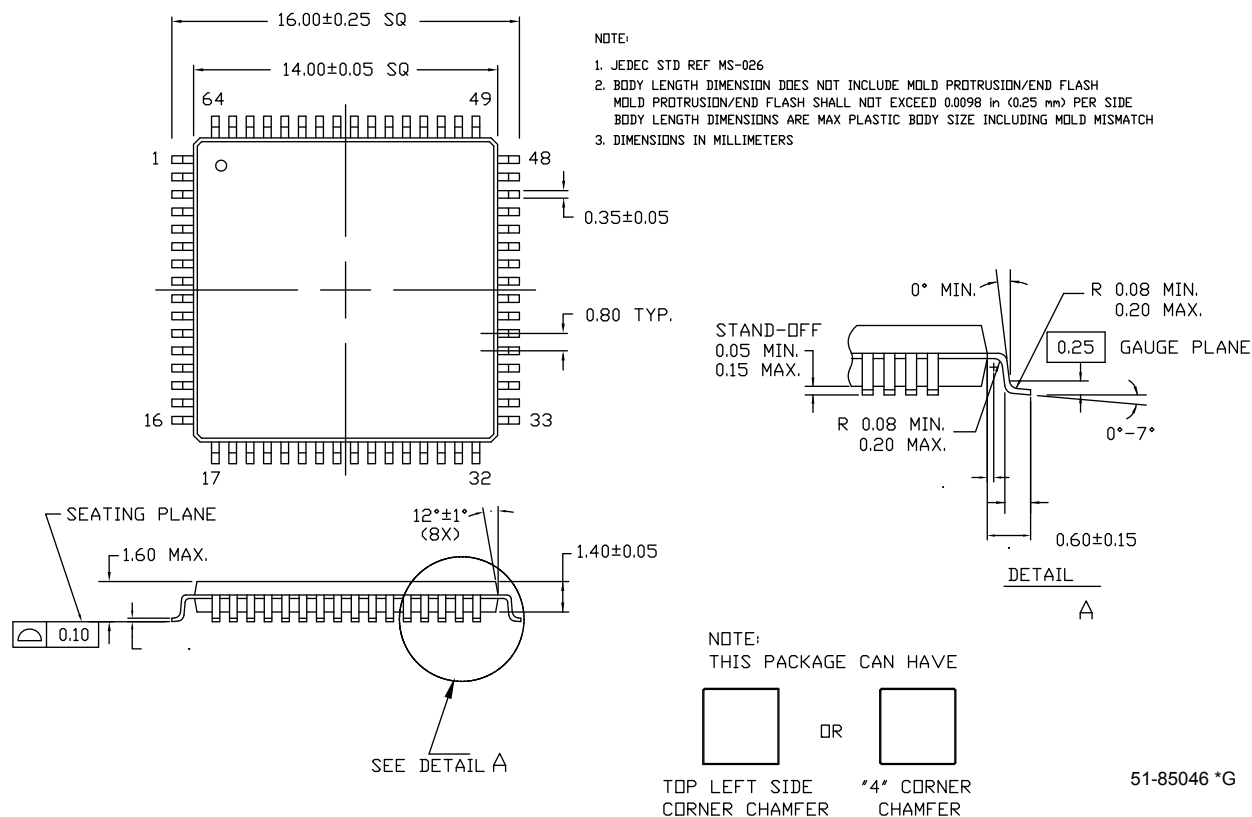
**Table 44. Solder Reflow Peak Temperature**

Package	Maximum Peak Temperature	Maximum Time at Peak Temperature
All packages	260 °C	30 seconds

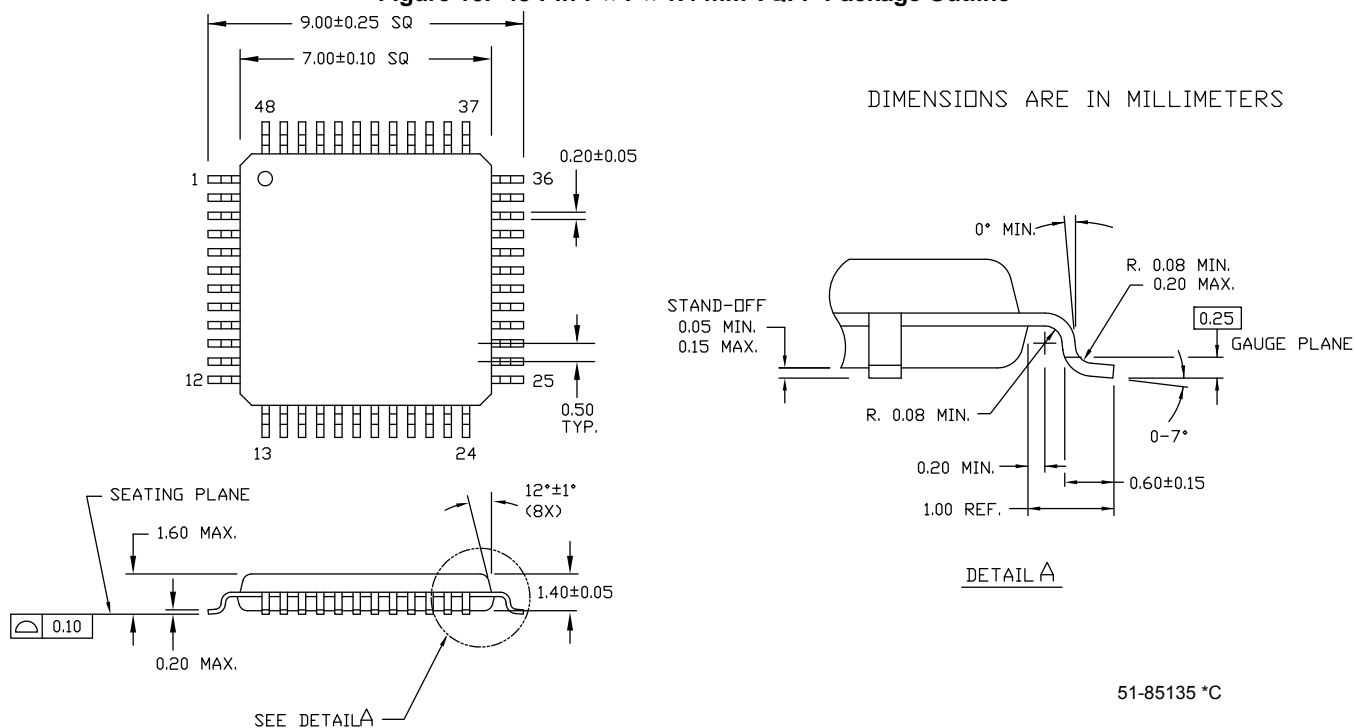
**Table 45. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2**

Package	MSL
All packages	MSL 3

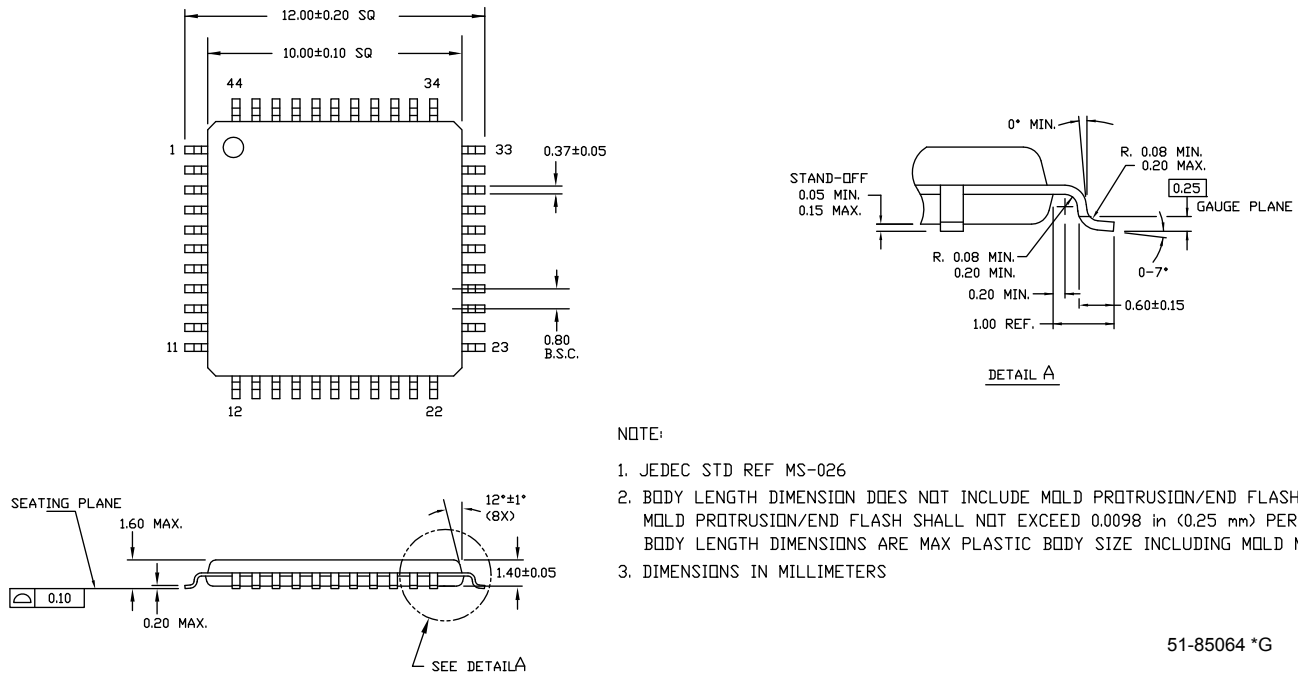
**Figure 9. 64-Pin 14 × 14 × 1.4 mm TQFP Package Outline**



**Figure 10. 48-Pin 7 × 7 × 1.4 mm TQFP Package Outline**



**Figure 11. 44-Pin 10 × 10 × 1.4 mm TQFP Package Outline**



51-85064 \*G

**Table 46. Acronyms Used in this Document** *(continued)*

Acronym	Description
PGA	programmable gain amplifier
PHUB	peripheral hub
PHY	physical layer
PICU	port interrupt control unit
PLA	programmable logic array
PLD	programmable logic device, see also PAL
PLL	phase-locked loop
PMDD	package material declaration data sheet
POR	power-on reset
PRES	precise power-on reset
PRS	pseudo random sequence
PS	port read data register
PSoC®	Programmable System-on-Chip™
PSRR	power supply rejection ratio
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RTL	register transfer language
RTR	remote transmission request
RX	receive
SAR	successive approximation register
SC/CT	switched capacitor/continuous time
SCL	I <sup>2</sup> C serial clock
SDA	I <sup>2</sup> C serial data
S/H	sample and hold
SINAD	signal to noise and distortion ratio
SIO	special input/output, GPIO with advanced features. See GPIO.
SOC	start of conversion
SOF	start of frame
SPI	Serial Peripheral Interface, a communications protocol
SR	slew rate
SRAM	static random access memory
SRES	software reset
SWD	serial wire debug, a test protocol
SWV	single-wire viewer
TD	transaction descriptor, see also DMA

**Table 46. Acronyms Used in this Document** *(continued)*

Acronym	Description
THD	total harmonic distortion
TIA	transimpedance amplifier
TRM	technical reference manual
TTL	transistor-transistor logic
TX	transmit
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UDB	universal digital block
USB	Universal Serial Bus
USBIO	USB input/output, PSoC pins used to connect to a USB port
VDAC	voltage DAC, see also DAC, IDAC
WDT	watchdog timer
WOL	write once latch, see also NVL
WRES	watchdog timer reset
XRES	external reset I/O pin
XTAL	crystal



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