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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, IrDA, LINbus, Microwire, SmartCard, SPI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, Cap Sense, LCD, LVD, POR, PWM, SmartSense, WDT
Number of I/O	55
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x12b SAR; D/A 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	68-VFQFN Exposed Pad
Supplier Device Package	68-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4246lti-m475

Functional Definition

CPU and Memory Subsystem

CPU

The Cortex-M0 CPU in the PSoC 4200-M is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. Most instructions are 16 bits in length and execute a subset of the Thumb-2 instruction set. The Cypress implementation includes a hardware multiplier that provides a 32-bit result in one cycle. It includes a nested vectored interrupt controller (NVIC) block with 32 interrupt inputs and also includes a Wakeup Interrupt Controller (WIC), which can wake the processor up from the Deep Sleep mode allowing power to be switched off to the main processor when the chip is in the Deep Sleep mode. The Cortex-M0 CPU provides a Non-Maskable Interrupt (NMI) input, which is made available to the user when it is not in use for system functions requested by the user.

The CPU also includes a debug interface, the serial wire debug (SWD) interface, which is a 2-wire form of JTAG; the debug configuration used for PSoC 4200-M has four break-point (address) comparators and two watchpoint (data) comparators.

Flash

The PSoC 4200-M has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The flash accelerator delivers 85% of single-cycle SRAM access performance on average. Part of the flash module can be used to emulate EEPROM operation if required.

SRAM

SRAM memory is retained during Hibernate.

SROM

A supervisory ROM that contains boot and configuration routines is provided.

DMA

A DMA engine, with eight channels, is provided that can do 32-bit transfers and has chainable ping-pong descriptors.

System Resources

Power System

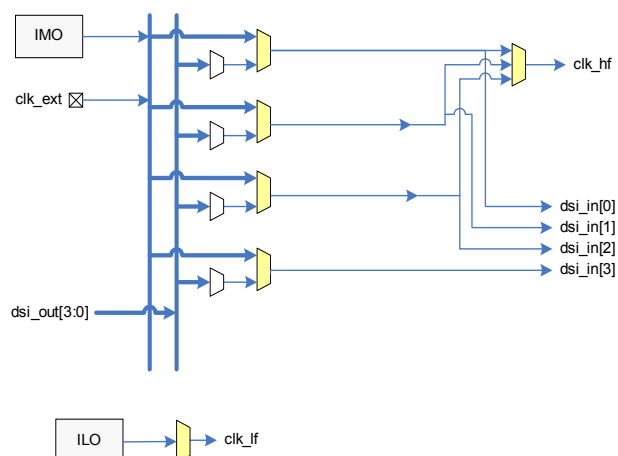
The power system is described in detail in the section [Power on page 14](#). It provides assurance that voltage levels are as required for each respective mode and either delay mode entry (on power-on reset (POR), for example) until voltage levels are as required for proper function or generate resets (brown-out detect (BOD)) or interrupts (low voltage detect (LVD)). The PSoC 4200M operates with a single external supply over the range of 1.71 to 5.5 V and has five different power modes, transitions between which are managed by the power system. The PSoC 4200M provides Sleep, Deep Sleep, Hibernate, and Stop low-power modes.

Clock System

The PSoC 4200-M clock system is responsible for providing clocks to all subsystems that require clocks and for switching between different clock sources without glitching. In addition, the clock system ensures that no meta-stable conditions occur.

The clock system for the PSoC 4200-M consists of a Watch Crystal Oscillator (WCO) running at 32 kHz, the IMO (3 to 48 MHz) and the ILO (32-kHz nominal) internal oscillators, and provision for an external clock.

Figure 2. PSoC 4200M MCU Clocking Architecture



The clk_hf signal can be divided down to generate synchronous clocks for the UDBs, and the analog and digital peripherals. There are a total of 16 clock dividers for the PSoC 4200-M, each with 16-bit divide capability; this allows 12 to be used for the fixed-function blocks and four for the UDBs. The analog clock leads the digital clocks to allow analog events to occur before digital clock-related noise is generated. The 16-bit capability allows a lot of flexibility in generating fine-grained frequency values and is fully supported in PSoC Creator.

IMO Clock Source

The IMO is the primary source of internal clocking in the PSoC 4200M. It is trimmed during testing to achieve the specified accuracy. Trim values are stored in nonvolatile memory. Trimming can also be done on the fly to allow in-field calibration. The IMO default frequency is 24 MHz and it can be adjusted between 3 to 48 MHz in steps of 1 MHz. IMO tolerance with Cypress-provided calibration settings is $\pm 2\%$.

ILO Clock Source

The ILO is a very low power oscillator, nominally 32 kHz, which is primarily used to generate clocks for peripheral operation in Deep Sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy. Cypress provides a software component, which does the calibration.

Crystal Oscillator

The PSoC 4200M clock subsystem also includes a low-frequency crystal oscillator (32-kHz WCO) that is available during the Deep Sleep mode and can be used for Real-Time Clock (RTC) and Watchdog Timer applications.

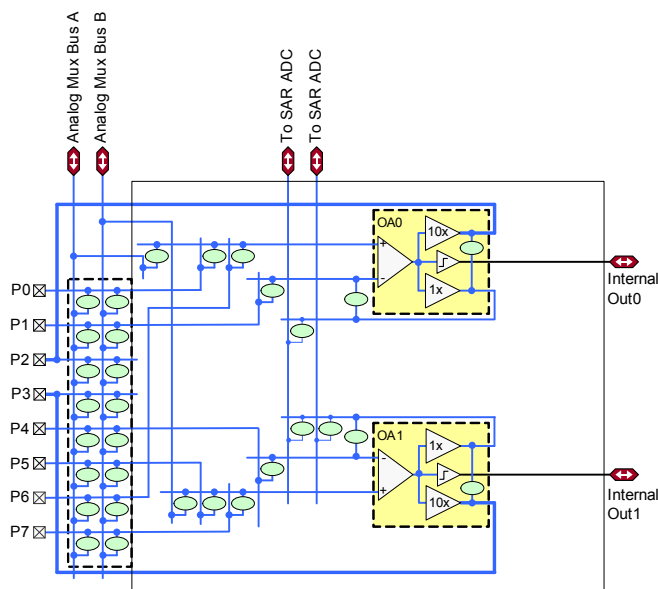
Analog Multiplex Bus

The PSoC 4200M has two concentric analog buses (Analog Mux Bus A and Analog Mux Bus B) that circumnavigate the periphery of the chip. These buses can transport analog signals from any pin to various analog blocks (including the opamps) and to the CapSense blocks allowing, for instance, the ADC to monitor any pin on the chip. These buses are independent and can also be split into three independent sections. This allows one section to be used for CapSense purposes, one for general analog signal processing, and the third for general-purpose digital peripherals and GPIO.

Four Opamps

The PSoC 4200M has four opamps with comparator modes, which allow most common analog functions to be performed on-chip eliminating external components; PGAs, voltage buffers, filters, trans-impedance amplifiers, and other functions can be realized with external passives saving power, cost, and space. The on-chip opamps are designed with enough bandwidth to drive the Sample-and-Hold circuit of the ADC without requiring external buffering. The opamps can operate in the Deep Sleep mode at very low power levels. The following diagram shows one of two identical opamp pairs of the opamp subsystem.

Figure 4. Identical Opamp Pairs in Opamp Subsystem



The ovals in Figure 4 represent analog switches, which may be controlled via user firmware, the SAR sequencer, or user-defined programmable logic. The opamps (OA0 and OA1) are configurable via these switches to perform all standard opamp functions with appropriate feedback components.

The opamps (OA0 and OA1) are programmable and reconfigurable to provide standard opamp functionality via switchable feedback components, unity gain functionality for driving pins directly, or for internal use (such as buffering SAR ADC inputs as indicated in the diagram), or as true comparators.

The opamp inputs provide highly flexible connectivity and can connect directly to dedicated pins or, via the analog mux buses,

to any pin on the chip. Analog switch connectivity is controllable by user firmware as well as user-defined programmable digital state machines (implemented via UDBs).

The opamps operate in Deep Sleep mode at very low currents allowing analog circuits to remain operational during Deep Sleep.

Temperature Sensor

The PSoC 4200M has one on-chip temperature sensor. This consists of a diode, which is biased by a current source that can be disabled to save power. The temperature sensor is connected to the ADC, which digitizes the reading and produces a temperature value using Cypress-supplied software that includes calibration and linearization.

Low-power Comparators

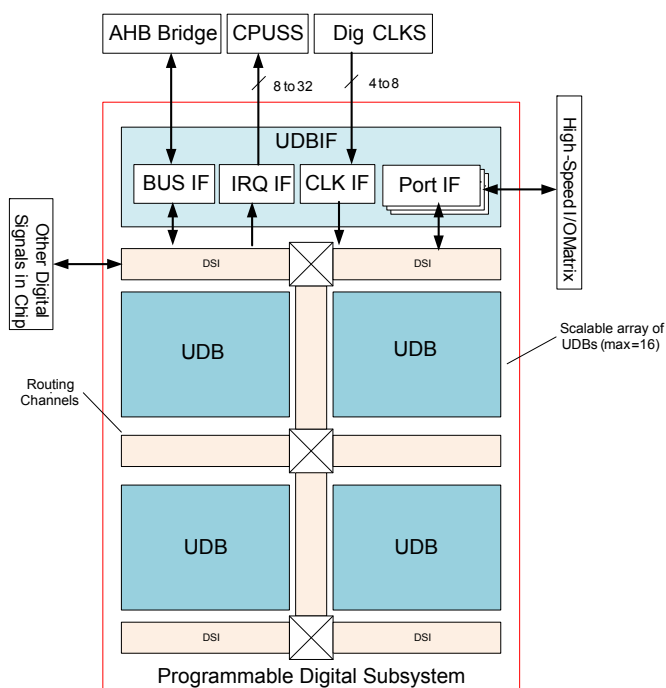
The PSoC 4200M has a pair of low-power comparators, which can also operate in the Deep Sleep and Hibernate modes. This allows the analog system blocks to be disabled while retaining the ability to monitor external voltage levels during low-power modes. The comparator outputs are normally synchronized to avoid meta-stability unless operating in an asynchronous power mode (Hibernate) where the system wake-up circuit is activated by a comparator switch event.

Programmable Digital

Universal Digital Blocks (UDBs) and Port Interfaces

The PSoC 4200M has four UDBs; the UDB array also provides a switched Digital System Interconnect (DSI) fabric that allows signals from peripherals and ports to be routed to and through the UDBs for communication and control. The UDB array is shown in the following figure.

Figure 5. UDB Array



68-QFN		64-TQFP		48-TQFP		44-TQFP	
Pin	Name	Pin	Name	Pin	Name	Pin	Name
8	P2.6	8	P2.6	8	P2.6	8	P2.6
9	P2.7	9	P2.7	9	P2.7	9	P2.7
10	VSSA	10	VSSA	10	VSSD	10	VSSD
11	VDDA	11	VDDA				
12	P6.0	12	P6.0				
13	P6.1	13	P6.1				
14	P6.2	14	P6.2				
15	P6.3						
16	P6.4	15	P6.4				
17	P6.5	16	P6.5				
18	VSSIO	17	VSSIO	10	VSSD	10	VSSD
19	P3.0	18	P3.0	12	P3.0	11	P3.0
20	P3.1	19	P3.1	13	P3.1	12	P3.1
21	P3.2	20	P3.2	14	P3.2	13	P3.2
22	P3.3	21	P3.3	16	P3.3	14	P3.3
23	P3.4	22	P3.4	17	P3.4	15	P3.4
24	P3.5	23	P3.5	18	P3.5	16	P3.5
25	P3.6	24	P3.6	19	P3.6	17	P3.6
26	P3.7	25	P3.7	20	P3.7	18	P3.7
27	VDDIO	26	VDDIO	21	VDDIO	19	VDDD
28	P4.0	27	P4.0	22	P4.0	20	P4.0
29	P4.1	28	P4.1	23	P4.1	21	P4.1
30	P4.2	29	P4.2	24	P4.2	22	P4.2
31	P4.3	30	P4.3	25	P4.3	23	P4.3
32	P4.4	31	P4.4				
33	P4.5	32	P4.5				
34	P4.6	33	P4.6				
35	P4.7						
39	P7.0	37	P7.0	26	P7.0		
40	P7.1	38	P7.1	27	P7.1		
41	P7.2						

The pins of Port 6 are overvoltage-tolerant. Pins 36, 37, and 38 are No-Connects on the 68-pin QFN. Pins 34, 35, and 36 are No-Connects on the 64-pin TQFP. Pins 11 and 15 are No-connects in the 48-pin TQFP. All VSS pins must be tied together.

The output drivers of I/O Ports P0 and P7 are connected to VDDD. Output drivers of I/O Ports 1, 2, and 5 are connected to VDDA. Output drivers of I/O Ports 3, 4, and 6 are connected to VDDIO.

Each of the pins shown in the previous table can have multiple programmable functions as shown in the following table. Column headings refer to Analog and Alternate pin functions.:

Port/Pin	Analog	Alt. Function 1	Alt. Function 2	Alt. Function 3	Alt. Function 4	Alt. Function 5
P0.0	lpcomp.in_p[0]			can[1].can_rx:0		scb[0].spi_select1:0
P0.1	lpcomp.in_n[0]			can[1].can_tx:0		scb[0].spi_select2:0
P0.2	lpcomp.in_p[1]					scb[0].spi_select3:0
P0.3	lpcomp.in_n[1]					
P0.4	wco_in		scb[1].uart_rx:0		scb[1].i2c_scl:0	scb[1].spi_mosi:1
P0.5	wco_out		scb[1].uart_tx:0		scb[1].i2c_sda:0	scb[1].spi_miso:1
P0.6		ext_clk:0	scb[1].uart_cts:0			scb[1].spi_clk:1
P0.7			scb[1].uart_rts:0	can[1].can_tx_enb_n:0	wakeup	scb[1].spi_select0:1
P5.0	ctb1.oa0.inp	tcpwm.line[4]:2	scb[2].uart_rx:0		scb[2].i2c_scl:0	scb[2].spi_mosi:0
P5.1	ctb1.oa0.inm	tcpwm.line_compl[4]:2	scb[2].uart_tx:0		scb[2].i2c_sda:0	scb[2].spi_miso:0
P5.2	ctb1.oa0.out	tcpwm.line[5]:2	scb[2].uart_cts:0		lpcomp.comp[0]:1	scb[2].spi_clk:0
P5.3	ctb1.oa1.out	tcpwm.line_compl[5]:2	scb[2].uart_rts:0		lpcomp.comp[1]:1	scb[2].spi_select0:0
P5.4	ctb1.oa1.inm	tcpwm.line[6]:2				scb[2].spi_select1:0
P5.5	ctb1.oa1.inp	tcpwm.line_compl[6]:2				scb[2].spi_select2:0
P5.6	ctb1.oa0.inp_alt	tcpwm.line[7]:0				scb[2].spi_select3:0
P5.7	ctb1.oa1.inp_alt	tcpwm.line_compl[7]:0				
P1.0	ctb0.oa0.inp	tcpwm.line[2]:1	scb[0].uart_rx:1		scb[0].i2c_scl:0	scb[0].spi_mosi:1
P1.1	ctb0.oa0.inm	tcpwm.line_compl[2]:1	scb[0].uart_tx:1		scb[0].i2c_sda:0	scb[0].spi_miso:1
P1.2	ctb0.oa0.out	tcpwm.line[3]:1	scb[0].uart_cts:1			scb[0].spi_clk:1
P1.3	ctb0.oa1.out	tcpwm.line_compl[3]:1	scb[0].uart_rts:1			scb[0].spi_select0:1
P1.4	ctb0.oa1.inm	tcpwm.line[6]:1				scb[0].spi_select1:1
P1.5	ctb0.oa1.inp	tcpwm.line_compl[6]:1				scb[0].spi_select2:1
P1.6	ctb0.oa0.inp_alt	tcpwm.line[7]:1				scb[0].spi_select3:1
P1.7	ctb0.oa1.inp_alt	tcpwm.line_compl[7]:1				
P2.0	sarmux.0	tcpwm.line[4]:1			scb[1].i2c_scl:1	scb[1].spi_mosi:2
P2.1	sarmux.1	tcpwm.line_compl[4]:1			scb[1].i2c_sda:1	scb[1].spi_miso:2
P2.2	sarmux.2	tcpwm.line[5]:1				scb[1].spi_clk:2
P2.3	sarmux.3	tcpwm.line_compl[5]:1				scb[1].spi_select0:2
P2.4	sarmux.4	tcpwm.line[0]:1				scb[1].spi_select1:1
P2.5	sarmux.5	tcpwm.line_compl[0]:1				scb[1].spi_select2:1
P2.6	sarmux.6	tcpwm.line[1]:1				scb[1].spi_select3:1

Electrical Specifications

Absolute Maximum Ratings

Table 1. Absolute Maximum Ratings^[1]

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID1	V _{DD_ABS}	Analog or digital supply relative to V _{SS} (V _{SSD} = V _{SSA})	−0.5	–	6	V	Absolute maximum
SID2	V _{CCD_ABS}	Direct digital core voltage input relative to V _{SSD}	−0.5	–	1.95	V	Absolute maximum
SID3	V _{GPIO_ABS}	GPIO voltage; V _{DDD} or V _{DDA}	−0.5	–	V _{DD} +0.5	V	Absolute maximum
SID4	I _{GPIO_ABS}	Current per GPIO	−25	–	25	mA	Absolute maximum
SID5	I _{G-PIO_injection}	GPIO injection current per pin	−0.5	–	0.5	mA	Absolute maximum
BID44	ESD_HBM	Electrostatic discharge human body model	2200	–	–	V	
BID45	ESD_CDM	Electrostatic discharge charged device model	500	–	–	V	
BID46	LU	Pin current for latch-up	−140	–	140	mA	

Device Level Specifications

All specifications are valid for $-40\text{ }^{\circ}\text{C} \leq T_A \leq 105\text{ }^{\circ}\text{C}$ and $T_J \leq 125\text{ }^{\circ}\text{C}$, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

Table 2. DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID53	V _{DD}	Power Supply Input Voltage (V _{DDA} = V _{DDD} = V _{DD})	1.8	–	5.5	V	With regulator enabled
SID255	V _{DDD}	Power Supply Input Voltage unregulated	1.71	1.8	1.89	V	Internally unregulated Supply
SID54	V _{CCD}	Output voltage (for core logic)	–	1.8	–	V	
SID55	C _{EFC}	External Regulator voltage bypass	1	1.3	1.6	μF	X5R ceramic or better
SID56	C _{EXC}	Power supply decoupling capacitor	–	1	–	μF	X5R ceramic or better
Active Mode, V_{DD} = 1.71 V to 5.5 V, −40 °C to +105 °C							
SID6	I _{DD1}	Execute from Flash; CPU at 6 MHz	–	2.2	2.8	mA	
SID7	I _{DD2}	Execute from Flash; CPU at 12 MHz	–	3.7	4.2	mA	
SID8	I _{DD3}	Execute from Flash; CPU at 24 MHz	–	6.7	7.2	mA	
SID9	I _{DD4}	Execute from Flash; CPU at 48 MHz	–	13	13.8	mA	
Sleep Mode, −40 °C to +105 °C							
SID21	I _{DD16}	I ² C wakeup, WDT, and Comparators on. Regulator Off.	–	1.75	2.1	mA	V _{DD} = 1.71 to 1.89, 6 MHz
SID22	I _{DD17}	I ² C wakeup, WDT, and Comparators on.	–	1.7	2.1	mA	V _{DD} = 1.8 to 5.5, 6 MHz
SID23	I _{DD18}	I ² C wakeup, WDT, and Comparators on. Regulator Off.	–	2.35	2.8	mA	V _{DD} = 1.71 to 1.89, 12 MHz
SID24	I _{DD19}	I ² C wakeup, WDT, and Comparators on.	–	2.25	2.8	mA	V _{DD} = 1.8 to 5.5, 12 MHz

Note

- Usage above the absolute maximum conditions listed in Table 1 may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.

Table 2. DC Specifications (continued)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
Deep Sleep Mode, -40 °C to + 60 °C							
SID30	I _{DD25}	I ² C wakeup and WDT on. Regulator Off.	–	1.55	20	μA	V _{DD} = 1.71 to 1.89
SID31	I _{DD26}	I ² C wakeup and WDT on.	–	1.35	15	μA	V _{DD} = 1.8 to 3.6
SID32	I _{DD27}	I ² C wakeup and WDT on.	–	1.5	15	μA	V _{DD} = 3.6 to 5.5
Deep Sleep Mode, +85 °C							
SID33	I _{DD28}	I ² C wakeup and WDT on. Regulator Off.	–	–	60	μA	V _{DD} = 1.71 to 1.89
SID34	I _{DD29}	I ² C wakeup and WDT on.	–	–	45	μA	V _{DD} = 1.8 to 3.6
SID35	I _{DD30}	I ² C wakeup and WDT on.	–	–	30	μA	V _{DD} = 3.6 to 5.5
Deep Sleep Mode, +105 °C							
SID33Q	I _{DD28Q}	I ² C wakeup and WDT on. Regulator Off.	–	–	135	μA	V _{DD} = 1.71 to 1.89
SID34Q	I _{DD29Q}	I ² C wakeup and WDT on.	–	–	180	μA	V _{DD} = 1.8 to 3.6
SID35Q	I _{DD30Q}	I ² C wakeup and WDT on.	–	–	140	μA	V _{DD} = 3.6 to 5.5
Hibernate Mode, -40 °C to + 60 °C							
SID39	I _{DD34}	Regulator Off.	–	150	3000	nA	V _{DD} = 1.71 to 1.89
SID40	I _{DD35}		–	150	1000	nA	V _{DD} = 1.8 to 3.6
SID41	I _{DD36}		–	150	1100	nA	V _{DD} = 3.6 to 5.5
Hibernate Mode, +85 °C							
SID42	I _{DD37}	Regulator Off.	–	–	4500	nA	V _{DD} = 1.71 to 1.89
SID43	I _{DD38}		–	–	3500	nA	V _{DD} = 1.8 to 3.6
SID44	I _{DD39}		–	–	3500	nA	V _{DD} = 3.6 to 5.5
Hibernate Mode, +105 °C							
SID42Q	I _{DD37Q}	Regulator Off.	–	–	19.4	μA	V _{DD} = 1.71 to 1.89
SID43Q	I _{DD38Q}		–	–	17	μA	V _{DD} = 1.8 to 3.6
SID44Q	I _{DD39Q}		–	–	16	μA	V _{DD} = 3.6 to 5.5
Stop Mode							
SID304	I _{DD43A}	Stop Mode current; V _{DD} = 3.6 V	–	35	85	nA	T = -40 °C to +60 °C
SID304A	I _{DD43B}	Stop Mode current; V _{DD} = 3.6 V	–	–	1450	nA	T = +85 °C
Stop Mode, +105 °C							
SID304Q	I _{DD43AQ}	Stop Mode current; V _{DD} = 3.6 V	–	–	5645	nA	
XRES current							
SID307	I _{DD_XR}	Supply current while XRES asserted	–	2	5	mA	

Analog Peripherals

Opamp

Table 8. Opamp Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
	I_{DD}	Opamp block current. No load.	–	–	–	–	
SID269	I_{DD_HI}	Power = high	–	1100	1850	μA	
SID270	I_{DD_MED}	Power = medium	–	550	950	μA	
SID271	I_{DD_LOW}	Power = low	–	150	350	μA	
	GBW	Load = 20 pF, 0.1 mA. $V_{DDA} = 2.7$ V	–	–	–	–	
SID272	GBW_HI	Power = high	6	–	–	MHz	
SID273	GBW_MED	Power = medium	4	–	–	MHz	
SID274	GBW_LO	Power = low	–	1	–	MHz	
	I_{OUT_MAX}	$V_{DDA} \geq 2.7$ V, 500 mV from rail	–	–	–	–	
SID275	$I_{OUT_MAX_HI}$	Power = high	10	–	–	mA	
SID276	$I_{OUT_MAX_MID}$	Power = medium	10	–	–	mA	
SID277	$I_{OUT_MAX_LO}$	Power = low	–	5	–	mA	
	I_{OUT}	$V_{DDA} = 1.71$ V, 500 mV from rail	–	–	–	–	
SID278	$I_{OUT_MAX_HI}$	Power = high	4	–	–	mA	
SID279	$I_{OUT_MAX_MID}$	Power = medium	4	–	–	mA	
SID280	$I_{OUT_MAX_LO}$	Power = low	–	2	–	mA	
SID281	V_{IN}	Input voltage range	–0.05	–	$V_{DDA} - 0.2$	V	Charge-pump on, $V_{DDA} \geq 2.7$ V
SID282	V_{CM}	Input common mode voltage	–0.05	–	$V_{DDA} - 0.2$	V	Charge-pump on, $V_{DDA} \geq 2.7$ V
	V_{OUT}	$V_{DDA} \geq 2.7$ V	–	–	–	–	
SID283	V_{OUT_1}	Power = high, Iload=10 mA	0.5	–	$V_{DDA} - 0.5$	V	
SID284	V_{OUT_2}	Power = high, Iload=1 mA	0.2	–	$V_{DDA} - 0.2$	V	
SID285	V_{OUT_3}	Power = medium, Iload=1 mA	0.2	–	$V_{DDA} - 0.2$	V	
SID286	V_{OUT_4}	Power = low, Iload=0.1mA	0.2	–	$V_{DDA} - 0.2$	V	
SID288	V_{OS_TR}	Offset voltage, trimmed	1	±0.5	1	mV	High mode
SID288A	V_{OS_TR}	Offset voltage, trimmed	–	±1	–	mV	Medium mode
SID288B	V_{OS_TR}	Offset voltage, trimmed	–	±2	–	mV	Low mode
SID290	$V_{OS_DR_TR}$	Offset voltage drift, trimmed	–10	±3	10	μV/°C	High mode. $T_A \leq 85$ °C.
SID290Q	$V_{OS_DR_TR}$	Offset voltage drift, trimmed	15	±3	15	μV/°C	High mode. $T_A \leq 105$ °C
SID290A	$V_{OS_DR_TR}$	Offset voltage drift, trimmed	–	±10	–	μV/°C	Medium mode
SID290B	$V_{OS_DR_TR}$	Offset voltage drift, trimmed	–	±10	–	μV/°C	Low mode
SID291	CMRR	DC Common mode rejection ratio. High-power mode. Common Model voltage range from 0.5 V to $V_{DDA} - 0.5$ V.	60	70	–	dB	$V_{DD} = 3.6$ V

Table 8. Opamp Specifications

(Guaranteed by Characterization) (continued)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID292	PSRR	At 1 kHz, 100-mV ripple	70	85	–	dB	$V_{DD} = 3.6\text{ V}$
	Noise		–	–	–	–	
SID293	V_{N1}	Input referred, 1 Hz - 1 GHz, power = high	–	94	–	μV_{rms}	
SID294	V_{N2}	Input referred, 1 kHz, power = high	–	72	–	nV/rtHz	
SID295	V_{N3}	Input referred, 10kHz, power = high	–	28	–	nV/rtHz	
SID296	V_{N4}	Input referred, 100kHz, power = high	–	15	–	nV/rtHz	
SID297	Cload	Stable up to maximum load. Performance specs at 50 pF.	–	–	125	pF	
SID298	Slew_rate	Cload = 50 pF, Power = High, $V_{DDA} \geq 2.7\text{ V}$	6	–	–	V/ μs	
SID299	T_op_wake	From disable to enable, no external RC dominating	–	25	–	μs	
SID299A	OL_GAIN	Open Loop Gain	–	90	–	dB	
	Comp_mode	Comparator mode; 50 mV drive, Trise = Tfall (approx.)	–	–	–		
SID300	T _{PD1}	Response time; power = high	–	150	–	ns	
SID301	T _{PD2}	Response time; power = medium	–	400	–	ns	
SID302	T _{PD3}	Response time; power = low	–	2000	–	ns	
SID303	Vhyst_op	Hysteresis	–	10	–	mV	
Deep Sleep Mode		Mode 2 is lowest current range. Mode 1 has higher GBW.					Deep Sleep mode. $V_{DDA} \geq 2.7\text{ V}$.
SID_DS_1	IDD_HI_M1	Mode 1, High current	–	1400	–	μA	25 °C
SID_DS_2	IDD_MED_M1	Mode 1, Medium current	–	700	–	μA	25 °C
SID_DS_3	IDD_LOW_M1	Mode 1, Low current	–	200	–	μA	25 °C
SID_DS_4	IDD_HI_M2	Mode 2, High current	–	120	–	μA	25 °C
SID_DS_5	IDD_MED_M2	Mode 2, Medium current	–	60	–	μA	25 °C
SID_DS_6	IDD_LOW_M2	Mode 2, Low current	–	15	–	μA	25 °C
SID_DS_7	GBW_HI_M1	Mode 1, High current	–	4	–	MHz	25 °C
SID_DS_8	GBW_MED_M1	Mode 1, Medium current	–	2	–	MHz	25 °C
SID_DS_9	GBW_LOW_M1	Mode 1, Low current	–	0.5	–	MHz	25 °C
SID_DS_10	GBW_HI_M2	Mode 2, High current	–	0.5	–	MHz	20-pF load, no DC load 0.2 V to $V_{DDA}-1.5\text{ V}$
SID_DS_11	GBW_MED_M2	Mode 2, Medium current	–	0.2	–	MHz	20-pF load, no DC load 0.2 V to $V_{DDA}-1.5\text{ V}$
SID_DS_12	GBW_LOW_M2	Mode 2, Low current	–	0.1	–	MHz	20-pF load, no DC load 0.2 V to $V_{DDA}-1.5\text{ V}$
SID_DS_13	VOS_HI_M1	Mode 1, High current	–	5	–	mV	With trim 25 °C, 0.2 V to $V_{DDA}-1.5\text{ V}$
SID_DS_14	VOS_MED_M1	Mode 1, Medium current	–	5	–	mV	With trim 25 °C, 0.2 V to $V_{DDA}-1.5\text{ V}$

Table 13. SAR ADC AC Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID106	A_PSRR	Power supply rejection ratio	70	–	–	dB	
SID107	A_CMRR	Common mode rejection ratio	66	–	–	dB	Measured at 1 V
SID108	A_SAMP_1	Sample rate with external reference bypass cap	–	–	1	Msp/s	
SID108A	A_SAMP_2	Sample rate with no bypass cap. Reference = V_{DD}	–	–	1	Msp/s	
SID108B	A_SAMP_3	Sample rate with no bypass cap. Internal reference	–	–	100	Ksp/s	
SID109	A_SNR	Signal-to-noise and distortion ratio (SINAD)	66	–	–	dB	$F_{IN} = 10$ kHz
SID111	A_INL	Integral non linearity	–1.4	–	+1.4	LSB	$V_{DD} = 1.71$ to 5.5 , 1 Msp/s, $V_{ref} = 1$ to 5.5 .
SID111A	A_INL	Integral non linearity	–1.4	–	+1.4	LSB	$V_{DDD} = 1.71$ to 3.6 , 1 Msp/s, $V_{ref} = 1.71$ to V_{DDD} .
SID111B	A_INL	Integral non linearity	–1.4	–	+1.4	LSB	$V_{DDD} = 1.71$ to 5.5 , 500 ksp/s, $V_{ref} = 1$ to 5.5 .
SID112	A_DNL	Differential non linearity	–0.9	–	+1.35	LSB	$V_{DDD} = 1.71$ to 5.5 , 1 Msp/s, $V_{ref} = 1$ to 5.5 .
SID112A	A_DNL	Differential non linearity	–0.9	–	+1.35	LSB	$V_{DDD} = 1.71$ to 3.6 , 1 Msp/s, $V_{ref} = 1.71$ to V_{DDD} .
SID112B	A_DNL	Differential non linearity	–0.9	–	+1.35	LSB	$V_{DDD} = 1.71$ to 5.5 , 500 ksp/s, $V_{ref} = 1$ to 5.5 .
SID113	A_THD	Total harmonic distortion	–	–	–65	dB	$F_{IN} = 10$ kHz.

CSD

Table 14. CSD Block Specification

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
CSD Specification							
SID308	VCSD	Voltage range of operation	1.71	–	5.5	V	
SID309	IDAC1	DNL for 8-bit resolution	–1	–	1	LSB	
SID310	IDAC1	INL for 8-bit resolution	–3	–	3	LSB	
SID311	IDAC2	DNL for 7-bit resolution	–1	–	1	LSB	
SID312	IDAC2	INL for 7-bit resolution	–3	–	3	LSB	
SID313	SNR	Ratio of counts of finger to noise. Guaranteed by characterization	5	–	–	Ratio	Capacitance range of 9 to 35 pF, 0.1-pF sensitivity
SID314	IDAC1_CRT1	Output current of Idac1 (8-bits) in High range	–	612	–	μ A	
SID314A	IDAC1_CRT2	Output current of Idac1(8-bits) in Low range	–	306	–	μ A	
SID315	IDAC2_CRT1	Output current of Idac2 (7-bits) in High range	–	304.8	–	μ A	
SID315A	IDAC2_CRT2	Output current of Idac2 (7-bits) in Low range	–	152.4	–	μ A	

LCD Direct Drive

Table 18. LCD Direct Drive DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID154	I _{LCDLOW}	Operating current in low power mode	–	5	–	μA	16 × 4 small segment disp. at 50 Hz
SID155	C _{LCDCAP}	LCD capacitance per segment/common driver	–	500	5000	pF	Guaranteed by Design
SID156	LCD _{OFFSET}	Long-term segment offset	–	20	–	mV	
SID157	I _{LCDOP1}	PWM Mode current. 5-V bias. 24-MHz IMO	–	0.6	–	mA	32 × 4 segments. 50 Hz, 25 °C
SID158	I _{LCDOP2}	PWM Mode current. 3.3-V bias. 24-MHz IMO.	–	0.5	–	mA	32 × 4 segments. 50 Hz, 25 °C

Table 19. LCD Direct Drive AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID159	F _{LCD}	LCD frame rate	10	50	150	Hz	

Table 20. Fixed UART DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID160	I _{UART1}	Block current consumption at 100 Kbps	–	–	55	μA	
SID161	I _{UART2}	Block current consumption at 1000 Kbps	–	–	312	μA	

Table 21. Fixed UART AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID162	F _{UART}	Bit rate	–	–	1	Mbps	

SPI Specifications

Table 22. Fixed SPI DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID163	I _{SPI1}	Block current consumption at 1 Mbps	–	–	360	μA	
SID164	I _{SPI2}	Block current consumption at 4 Mbps	–	–	560	μA	
SID165	I _{SPI3}	Block current consumption at 8 Mbps	–	–	600	μA	

Table 23. Fixed SPI AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID166	F _{SPI}	SPI operating frequency (master; 6X oversampling)	–	–	8	MHz	

System Resources

Power-on-Reset (POR) with Brown Out

Table 28. Imprecise Power On Reset (PRES)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID185	V _{RISEIPOR}	Rising trip voltage	0.80	–	1.45	V	Guaranteed by characterization
SID186	V _{FALLIPOR}	Falling trip voltage	0.75	–	1.4	V	Guaranteed by characterization
SID187	V _{IPORHYST}	Hysteresis	15	–	200	mV	Guaranteed by characterization

Table 29. Precise Power On Reset (POR)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID190	V _{FALLPPOR}	BOD trip voltage in active and sleep modes	1.64	–	–	V	Guaranteed by characterization
SID192	V _{FALLDPSLP}	BOD trip voltage in Deep Sleep	1.4	–	–	V	Guaranteed by characterization

Voltage Monitors

Table 30. Voltage Monitors DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID195	V _{LVI1}	LVI_A/D_SEL[3:0] = 0000b	1.71	1.75	1.79	V	
SID196	V _{LVI2}	LVI_A/D_SEL[3:0] = 0001b	1.76	1.80	1.85	V	
SID197	V _{LVI3}	LVI_A/D_SEL[3:0] = 0010b	1.85	1.90	1.95	V	
SID198	V _{LVI4}	LVI_A/D_SEL[3:0] = 0011b	1.95	2.00	2.05	V	
SID199	V _{LVI5}	LVI_A/D_SEL[3:0] = 0100b	2.05	2.10	2.15	V	
SID200	V _{LVI6}	LVI_A/D_SEL[3:0] = 0101b	2.15	2.20	2.26	V	
SID201	V _{LVI7}	LVI_A/D_SEL[3:0] = 0110b	2.24	2.30	2.36	V	
SID202	V _{LVI8}	LVI_A/D_SEL[3:0] = 0111b	2.34	2.40	2.46	V	
SID203	V _{LVI9}	LVI_A/D_SEL[3:0] = 1000b	2.44	2.50	2.56	V	
SID204	V _{LVI10}	LVI_A/D_SEL[3:0] = 1001b	2.54	2.60	2.67	V	
SID205	V _{LVI11}	LVI_A/D_SEL[3:0] = 1010b	2.63	2.70	2.77	V	
SID206	V _{LVI12}	LVI_A/D_SEL[3:0] = 1011b	2.73	2.80	2.87	V	
SID207	V _{LVI13}	LVI_A/D_SEL[3:0] = 1100b	2.83	2.90	2.97	V	
SID208	V _{LVI14}	LVI_A/D_SEL[3:0] = 1101b	2.93	3.00	3.08	V	
SID209	V _{LVI15}	LVI_A/D_SEL[3:0] = 1110b	3.12	3.20	3.28	V	
SID210	V _{LVI16}	LVI_A/D_SEL[3:0] = 1111b	4.39	4.50	4.61	V	
SID211	LVI_IDD	Block current	–	–	100	μA	Guaranteed by characterization

Table 31. Voltage Monitors AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID212	T _{MONTRIP}	Voltage monitor trip time	–	–	1	μs	Guaranteed by characterization

SWD Interface

Table 32. SWD Interface Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID213	F_SWCLK1	$3.3\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	–	–	14	MHz	SWDCLK \leq 1/3 CPU clock frequency
SID214	F_SWCLK2	$1.71\text{ V} \leq V_{DD} \leq 3.3\text{ V}$	–	–	7	MHz	SWDCLK \leq 1/3 CPU clock frequency
SID215	T_SWDI_SETUP	$T = 1/f_{\text{SWDCLK}}$	0.25*T	–	–	ns	Guaranteed by characterization
SID216	T_SWDI_HOLD	$T = 1/f_{\text{SWDCLK}}$	0.25*T	–	–	ns	Guaranteed by characterization
SID217	T_SWDO_VALID	$T = 1/f_{\text{SWDCLK}}$	–	–	0.5*T	ns	Guaranteed by characterization
SID217A	T_SWDO_HOLD	$T = 1/f_{\text{SWDCLK}}$	1	–	–	ns	Guaranteed by characterization

Internal Main Oscillator

Table 33. IMO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID218	I_IMO1	IMO operating current at 48 MHz	–	–	1000	μA	
SID219	I_IMO2	IMO operating current at 24 MHz	–	–	325	μA	
SID220	I_IMO3	IMO operating current at 12 MHz	–	–	225	μA	
SID221	I_IMO4	IMO operating current at 6 MHz	–	–	180	μA	
SID222	I_IMO5	IMO operating current at 3 MHz	–	–	150	μA	

Table 34. IMO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID223	F_IMOTOL1	Frequency variation from 3 to 48 MHz	–	–	±2	%	±3% if $T_A > 85^\circ\text{C}$ and IMO frequency < 24 MHz
SID226	T_STARTIMO	IMO startup time	–	–	12	μs	
SID227	T_JITRMSIMO1	RMS Jitter at 3 MHz	–	156	–	ps	
SID228	T_JITRMSIMO2	RMS Jitter at 24 MHz	–	145	–	ps	
SID229	T_JITRMSIMO3	RMS Jitter at 48 MHz	–	139	–	ps	

Internal Low-Speed Oscillator

Table 35. ILO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID231	I_ILO1	ILO operating current at 32 kHz	–	0.3	1.05	μA	Guaranteed by Characterization
SID233	I_ILOLEAK	ILO leakage current	–	2	15	nA	Guaranteed by Design

Packaging

The description of the PSoC4200M package dimensions follows.

Spec ID#	Package	Description	Package Dwg #
PKG_1	68-pin QFN	68-pin QFN, 8 mm x 8 mm x 1.0 mm height with 0.4 mm pitch	001-09618
PKG_2	64-pin TQFP	64-pin TQFP, 10 mm x10 mm x 1.4 mm height with 0.5 mm pitch	51-85051
PKG_4	64-pin TQFP	64-pin TQFP, 14 mm x14 mm x 1.4 mm height with 0.8 mm pitch	51-85046
PKG_5	48-pin TQFP	48-pin TQFP, 7 mm x 7 mm x 1.4 mm height with 0.5 mm pitch	51-85135
PKG_6	44-pin TQFP	44-pin TQFP, 10 mm x 10 mm x 1.4 mm height with 0.8 mm pitch	51-85064

Table 43. Package Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
T _A	Operating ambient temperature		-40	25	85	°C
T _J	Operating junction temperature		-40		100	°C
T _{JA}	Package θ_{JA} (68-pin QFN)		—	16.8	—	°C/Watt
T _{JC}	Package θ_{JC} (68-pin QFN)		—	2.9	—	°C/Watt
T _{JA}	Package θ_{JA} (64-pin TQFP, 0.5-mm pitch)		—	56	—	°C/Watt
T _{JC}	Package θ_{JC} (64-pin TQFP, 0.5-mm pitch)		—	19.5	—	°C/Watt
T _{JA}	Package θ_{JA} (64-pin TQFP, 0.8-mm pitch)		—	66.4	—	°C/Watt
T _{JC}	Package θ_{JC} (64-pin TQFP, 0.8-mm pitch)		—	18.2	—	°C/Watt
T _{JA}	Package θ_{JA} (48-pin TQFP, 0.5-mm pitch)		—	67.3	—	°C/Watt
T _{JC}	Package θ_{JC} (48-pin TQFP, 0.5-mm pitch)		—	30.4	—	°C/Watt
T _{JA}	Package θ_{JA} (44-pin TQFP, 0.8-mm pitch)		—	57	—	°C/Watt
T _{JC}	Package θ_{JC} (44-pin TQFP, 0.8-mm pitch)		—	25.9	—	°C/Watt

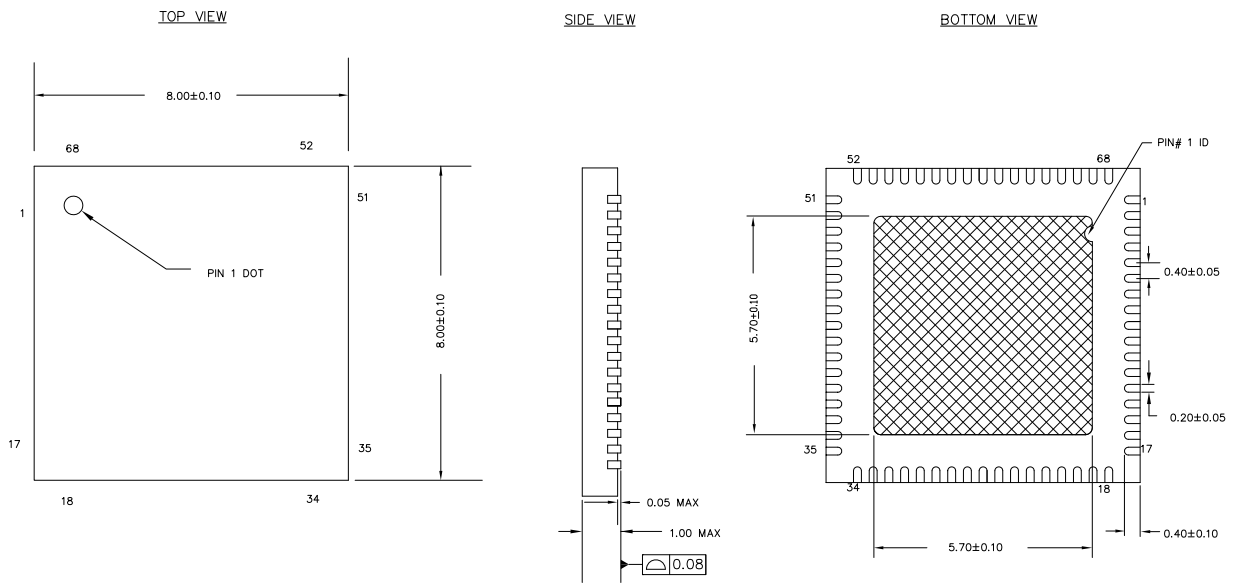
Table 44. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time at Peak Temperature
All packages	260 °C	30 seconds


Table 45. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Package	MSL
All packages	MSL 3

Figure 7. 68-Pin QFN 8 × 8 × 1.0 mm Package Outline

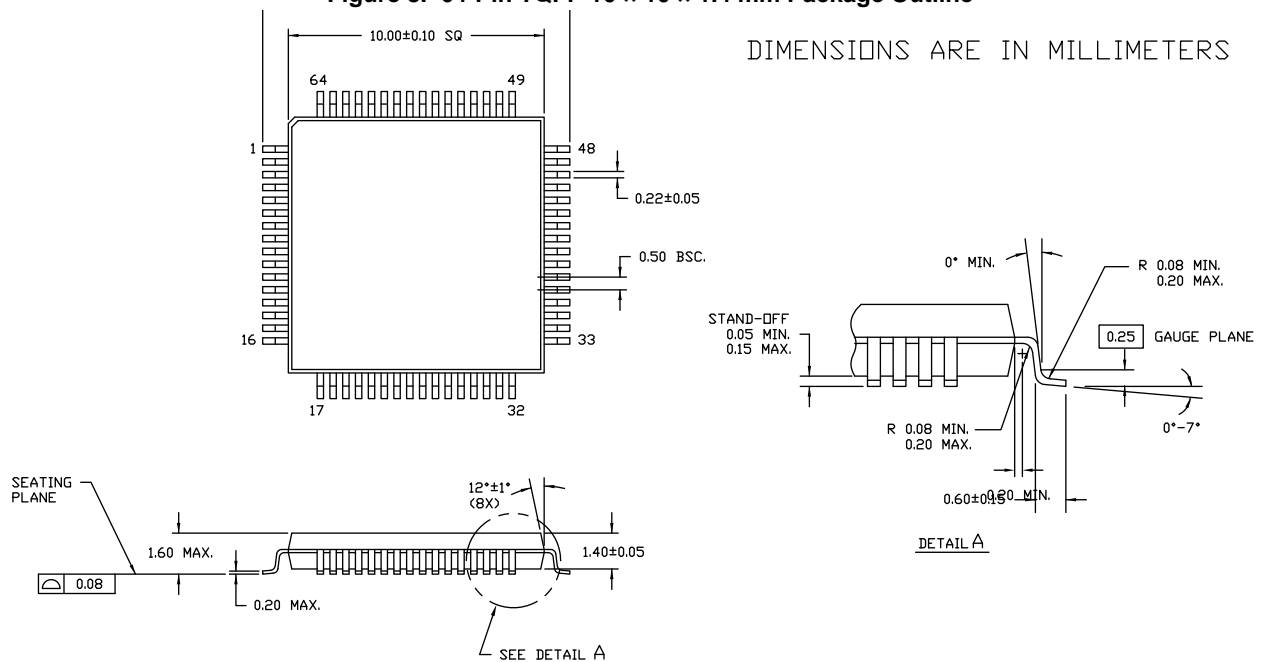


NOTES:

1.  HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: 17 ± 2mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-09618 *E

Figure 8. 64-Pin TQFP 10 × 10 × 1.4 mm Package Outline



51-85051 *D

Figure 9. 64-Pin 14 × 14 × 1.4 mm TQFP Package Outline

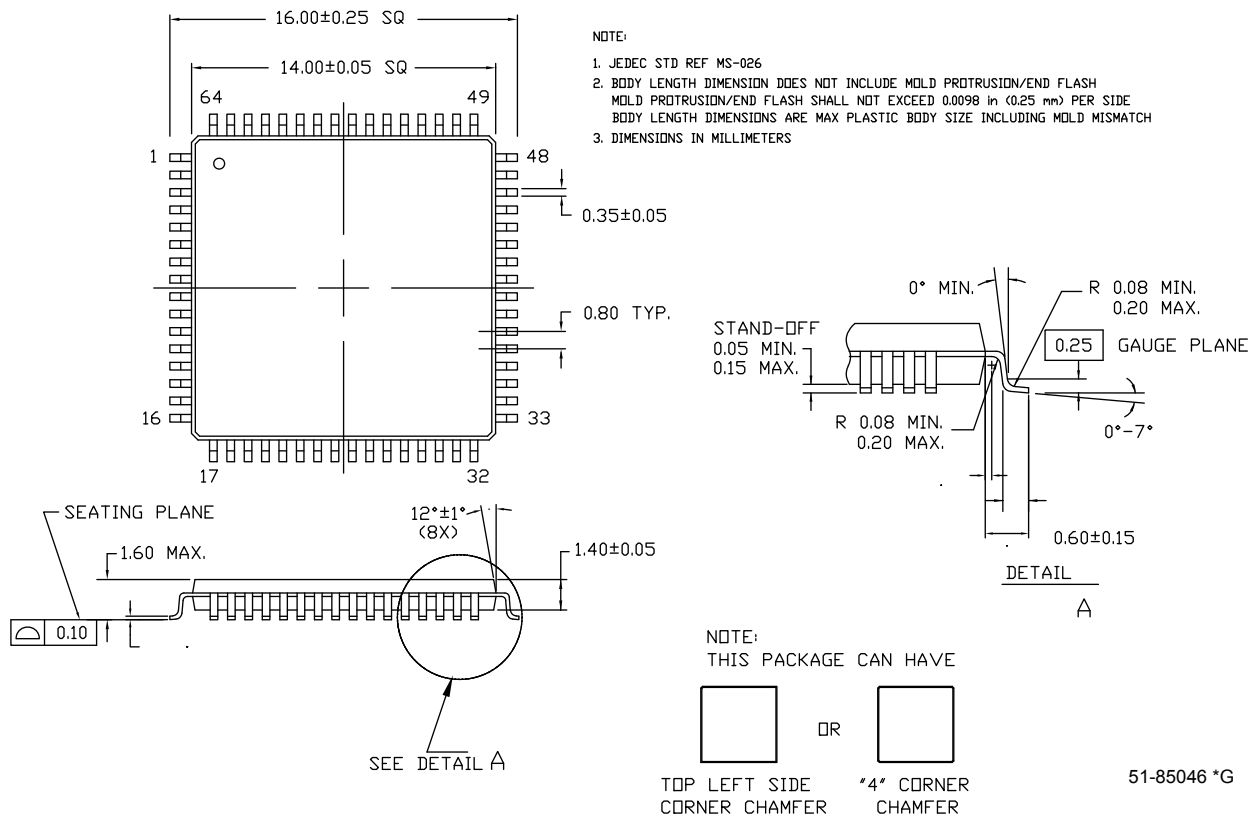


Figure 10. 48-Pin 7 × 7 × 1.4 mm TQFP Package Outline

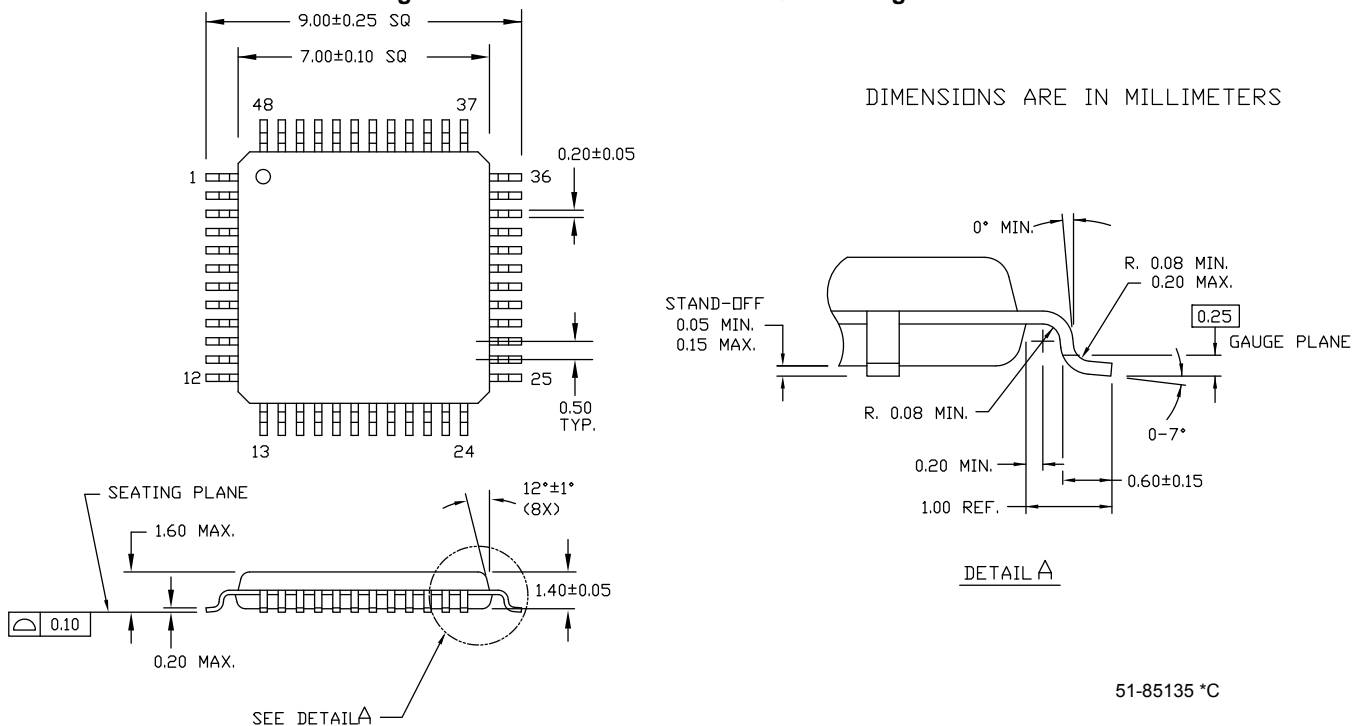
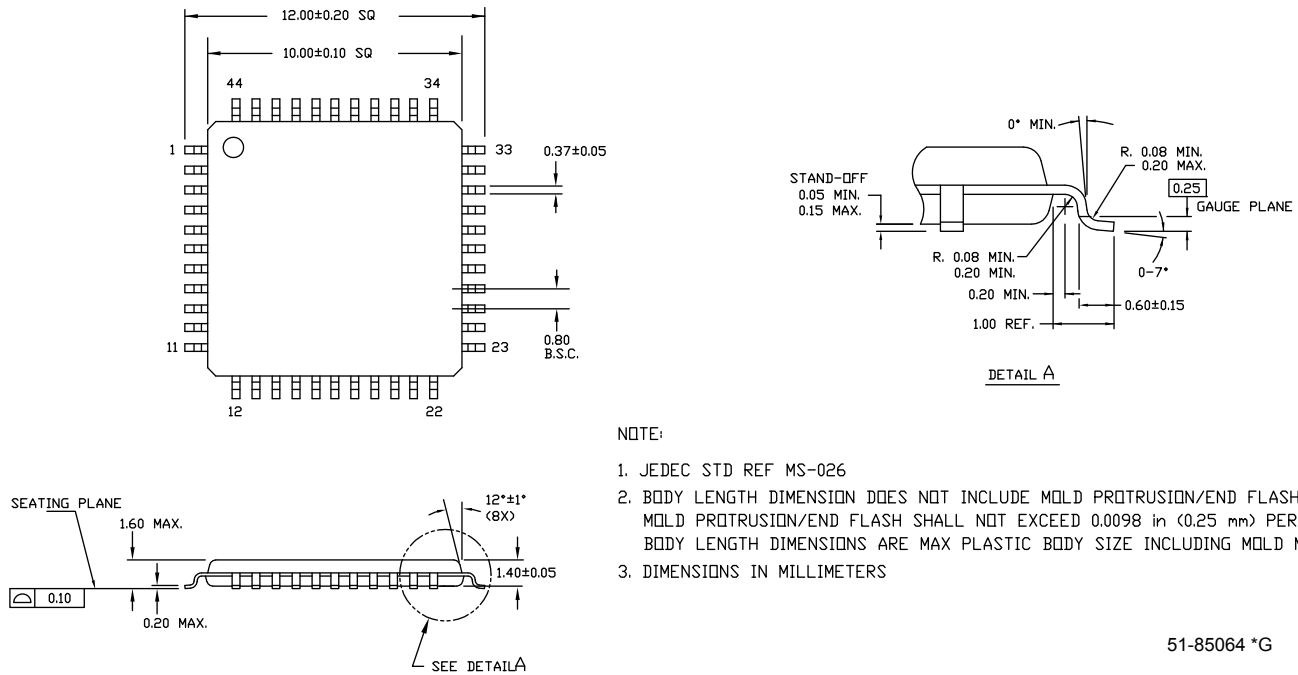


Figure 11. 44-Pin 10 × 10 × 1.4 mm TQFP Package Outline



51-85064 *G

Acronyms

Table 46. Acronyms Used in this Document

Acronym	Description
abus	analog local bus
ADC	analog-to-digital converter
AG	analog global
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an ARM data transfer bus
ALU	arithmetic logic unit
AMUXBUS	analog multiplexer bus
API	application programming interface
APSR	application program status register
ARM®	advanced RISC machine, a CPU architecture
ATM	automatic thump mode
BW	bandwidth
CAN	Controller Area Network, a communications protocol
CMRR	common-mode rejection ratio
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
DAC	digital-to-analog converter, see also IDAC, VDAC
DFB	digital filter block
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DMIPS	Dhrystone million instructions per second
DMA	direct memory access, see also TD
DNL	differential nonlinearity, see also INL
DNU	do not use
DR	port write data registers
DSI	digital system interconnect
DWT	data watchpoint and trace
ECC	error correcting code
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
EMIF	external memory interface
EOC	end of conversion
EOF	end of frame
EPSR	execution program status register
ESD	electrostatic discharge

Table 46. Acronyms Used in this Document *(continued)*

Acronym	Description
ETM	embedded trace macrocell
FIR	finite impulse response, see also IIR
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output, applies to a PSoC pin
HVI	high-voltage interrupt, see also LVI, LVD
IC	integrated circuit
IDAC	current DAC, see also DAC, VDAC
IDE	integrated development environment
I ² C, or IIC	Inter-Integrated Circuit, a communications protocol
IIR	infinite impulse response, see also FIR
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
INL	integral nonlinearity, see also DNL
I/O	input/output, see also GPIO, DIO, SIO, USBIO
IPOR	initial power-on reset
IPSR	interrupt program status register
IRQ	interrupt request
ITM	instrumentation trace macrocell
LCD	liquid crystal display
LIN	Local Interconnect Network, a communications protocol.
LR	link register
LUT	lookup table
LVD	low-voltage detect, see also LVI
LVI	low-voltage interrupt, see also HVI
LVTTL	low-voltage transistor-transistor logic
MAC	multiply-accumulate
MCU	microcontroller unit
MISO	master-in slave-out
NC	no connect
NMI	nonmaskable interrupt
NRZ	non-return-to-zero
NVIC	nested vectored interrupt controller
NVL	nonvolatile latch, see also WOL
opamp	operational amplifier
PAL	programmable array logic, see also PLD
PC	program counter
PCB	printed circuit board

Table 46. Acronyms Used in this Document *(continued)*

Acronym	Description
PGA	programmable gain amplifier
PHUB	peripheral hub
PHY	physical layer
PICU	port interrupt control unit
PLA	programmable logic array
PLD	programmable logic device, see also PAL
PLL	phase-locked loop
PMDD	package material declaration data sheet
POR	power-on reset
PRES	precise power-on reset
PRS	pseudo random sequence
PS	port read data register
PSoC®	Programmable System-on-Chip™
PSRR	power supply rejection ratio
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RTL	register transfer language
RTR	remote transmission request
RX	receive
SAR	successive approximation register
SC/CT	switched capacitor/continuous time
SCL	I ² C serial clock
SDA	I ² C serial data
S/H	sample and hold
SINAD	signal to noise and distortion ratio
SIO	special input/output, GPIO with advanced features. See GPIO.
SOC	start of conversion
SOF	start of frame
SPI	Serial Peripheral Interface, a communications protocol
SR	slew rate
SRAM	static random access memory
SRES	software reset
SWD	serial wire debug, a test protocol
SWV	single-wire viewer
TD	transaction descriptor, see also DMA

Table 46. Acronyms Used in this Document *(continued)*

Acronym	Description
THD	total harmonic distortion
TIA	transimpedance amplifier
TRM	technical reference manual
TTL	transistor-transistor logic
TX	transmit
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UDB	universal digital block
USB	Universal Serial Bus
USBIO	USB input/output, PSoC pins used to connect to a USB port
VDAC	voltage DAC, see also DAC, IDAC
WDT	watchdog timer
WOL	write once latch, see also NVL
WRES	watchdog timer reset
XRES	external reset I/O pin
XTAL	crystal

Revision History

Description Title: PSoC® 4: PSoC 4200M Family Datasheet Programmable System-on-Chip (PSoC®) Document Number: 001-93963				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
*B	4765455	WKA	06/03/2015	Release to web.
*C	4815539	WKA	06/29/2015	Removed note regarding hardware handshaking in the UART Mode section. Changed max value of SID51A to 2 ms. Added "Guaranteed by characterization" note for SID65 and SID65A Updated Ordering Information. Removed the Errata section.
*D	4828234	WKA	07/08/2015	Corrected Block Diagram
*E	4941619	WKA	09/30/2015	Updated CapSense section. Updated the note at the end of the Pinout table. Removed Conditions for spec SID237. Updated Ordering Information.
*F	5026805	WKA	11/25/2015	Added Comparator ULP mode range restrictions and corrected typos.
*G	5408936	WKA	08/19/2016	Added extended industrial temperature range. Added specs SID290Q, SID182A, and SID299A. Updated conditions for SID290, SID223, and SID237. Added 44-pin TQFP package details. Updated Ordering Information.

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