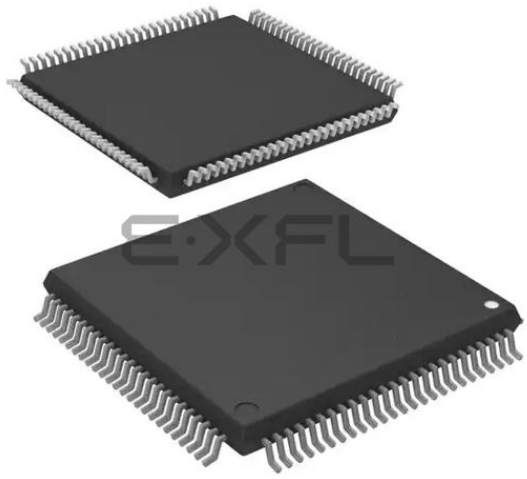

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M16C/60
Core Size	16-Bit
Speed	32MHz
Connectivity	EBI/EMI, I²C, SIO, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	85
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f36506cdfb-v0

1.2 Specifications

The M16C/65C Group includes 128-pin and 100-pin packages. Table 1.1 to Table 1.4 list specifications.

Table 1.1 Specifications for the 128-Pin Package (1/2)

Item	Function	Description
CPU	Central processing unit	M16C/60 Series core (multiplier: 16 bit × 16 bit → 32 bit, multiply and accumulate instruction: 16 bit × 16 bit + 32 bit → 32 bit) • Number of basic instructions: 91 • Minimum instruction execution time: 31.25 ns (f(BCLK) = 32 MHz, VCC1 = VCC2 = 2.7 to 5.5 V) • Operating modes: Single-chip, memory expansion, and microprocessor
Memory	ROM, RAM, data flash	See Table 1.5 “Product List (N-Version)” to Table 1.6 “Product List (D-Version)”.
Voltage Detection	Voltage detector	• Power-on reset • 3 voltage detection points (detection level of voltage detection 0 and 1 selectable)
Clock	Clock generator	• 5 circuits: Main clock, sub clock, low-speed on-chip oscillator (125 kHz), high-speed on-chip oscillator (40 MHz ±5%), PLL frequency synthesizer • Oscillation stop detection: Main clock oscillation stop/restart detection function • Frequency divider circuit: Divide ratio selectable from 1, 2, 4, 8, and 16 • Power saving features: Wait mode, stop mode • Real-time clock
External Bus Expansion	Bus memory expansion	• Address space: 1 MB • External bus interface: 0 to 8 waits inserted, 4 chip select outputs, memory area expansion function (expandable to 4 MB), 3 V and 5 V interfaces • Bus format: Separate bus or multiplexed bus selectable, data bus width selectable (8 or 16 bits), number of address buses selectable (12, 16, or 20)
I/O Ports	Programmable I/O ports	• CMOS I/O ports: 111 (selectable pull-up resistors) • N-channel open drain ports: 3
Interrupts		• Interrupt vectors: 70 • External interrupt inputs: 13 ($\overline{\text{NMI}}$, $\overline{\text{INT}}$ × 8, key input × 4) • Interrupt priority levels: 7
Watchdog Timer		15-bit timer × 1 (with prescaler) Automatic reset start function selectable
DMA	DMAC	• 4 channels, cycle steal mode • Trigger sources: 43 • Transfer modes: 2 (single transfer, repeat transfer)

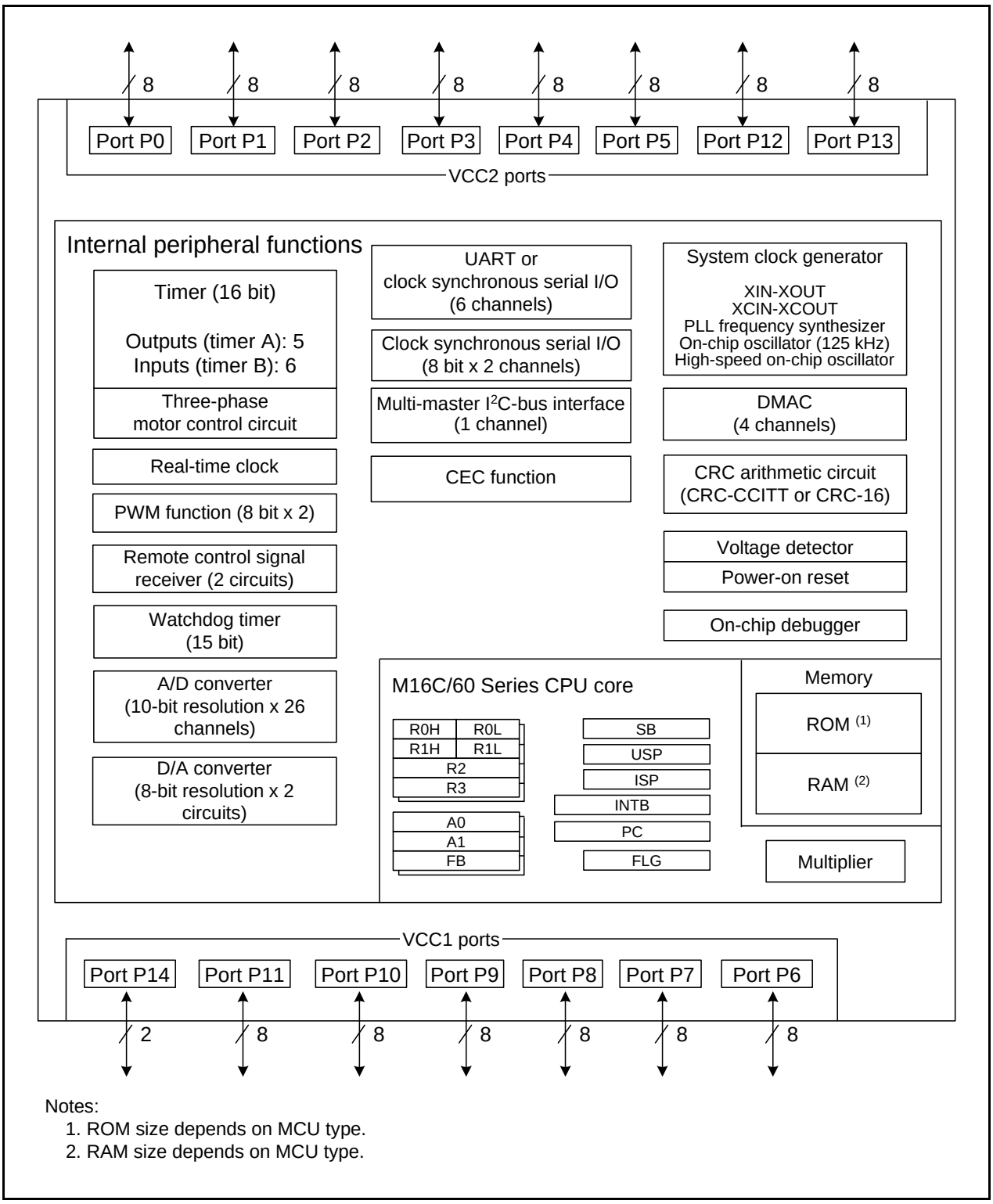
Table 1.2 Specifications for the 128-Pin Package (2/2)

Item	Function	Description
Timers	Timer A	16-bit timer × 5 Timer mode, event counter mode, one-shot timer mode, pulse width modulation (PWM) mode Event counter two-phase pulse signal processing (two-phase encoder input) × 3 Programmable output mode × 3
	Timer B	16-bit timer × 6 Timer mode, event counter mode, pulse period measurement mode, pulse width measurement mode
	Three-phase motor control timer functions	• Three-phase inverter control (timer A1, timer A2, timer A4, timer B2) • On-chip dead time timer
	Real-time clock	Count: seconds, minutes, hours, days of the week
	PWM function	8 bits × 2
	Remote control signal receiver	• 2 circuits • 4 wave pattern matchings (differentiate wave pattern for headers, data 0, data 1, and special data) • 6-byte receive buffer (1 circuit only) • Operating frequency of 32 kHz
Serial Interface	UART0 to UART2, UART5 to UART7	Clock synchronous/asynchronous × 6 channels I^2C-bus, IEBus, special mode 2 SIM (UART2)
	SI/O3, SI/O4	Clock synchronization only × 2 channels
Multi-master I^2C-bus Interface		1 channel
CEC Functions (2)		CEC transmit/receive, arbitration lost detection, ACK automatic output, operation frequency of 32 kHz
A/D Converter		10-bit resolution × 26 channels, including sample and hold function Conversion time: 1.72 µs
D/A Converter		8-bit resolution × 2 circuits
CRC Calculator		CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$), CRC-16 ($X^{16} + X^{15} + X^2 + 1$) compliant
Flash Memory		• Program and erase power supply voltage: 2.7 to 5.5 V • Program and erase cycles: 1,000 times (program ROM 1, program ROM 2), 10,000 times (data flash) • Program security: ROM code protect, ID code check
Debug Functions		On-chip debug, on-board flash rewrite, address match interrupt × 4
Operation Frequency/Supply Voltage		32 MHz/VCC1 = 2.7 to 5.5 V, VCC2 = 2.7 V to VCC1
Current Consumption		Refer to the Electrical Characteristics chapter
Operating Temperature		-20°C to 85°C, -40°C to 85°C (1)
Package		128-pin LQFP: PLQP0128KB-A (Previous package code: 128P6Q-A)

Notes:
1. See Table 1.5 “Product List (N-Version)” to Table 1.6 “Product List (D-Version)” for the operating temperature.
2. The CEC function indicates circuitry which supports the transmission and reception of CEC signals standardized by the High-Definition Multimedia Interface (HDMI). HDMI and High-Definition Multimedia Interface are registered trademarks of HDMI Licensing, LLC.

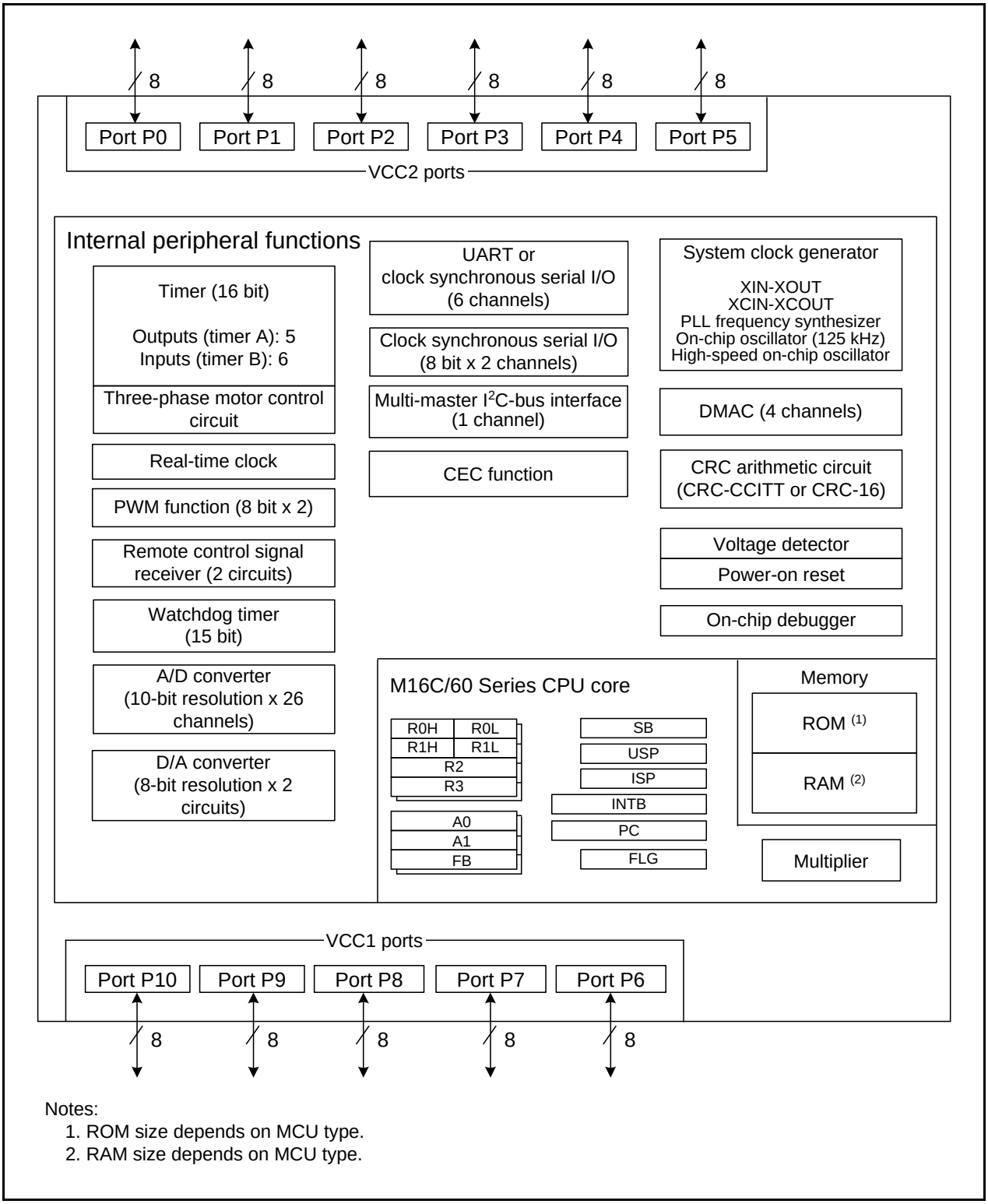
1.4 Block Diagram

Figure 1.3 to Figure 1.4 show block diagrams.



Notes:
1. ROM size depends on MCU type.
2. RAM size depends on MCU type.

Figure 1.3 Block Diagram for the 128-Pin Package

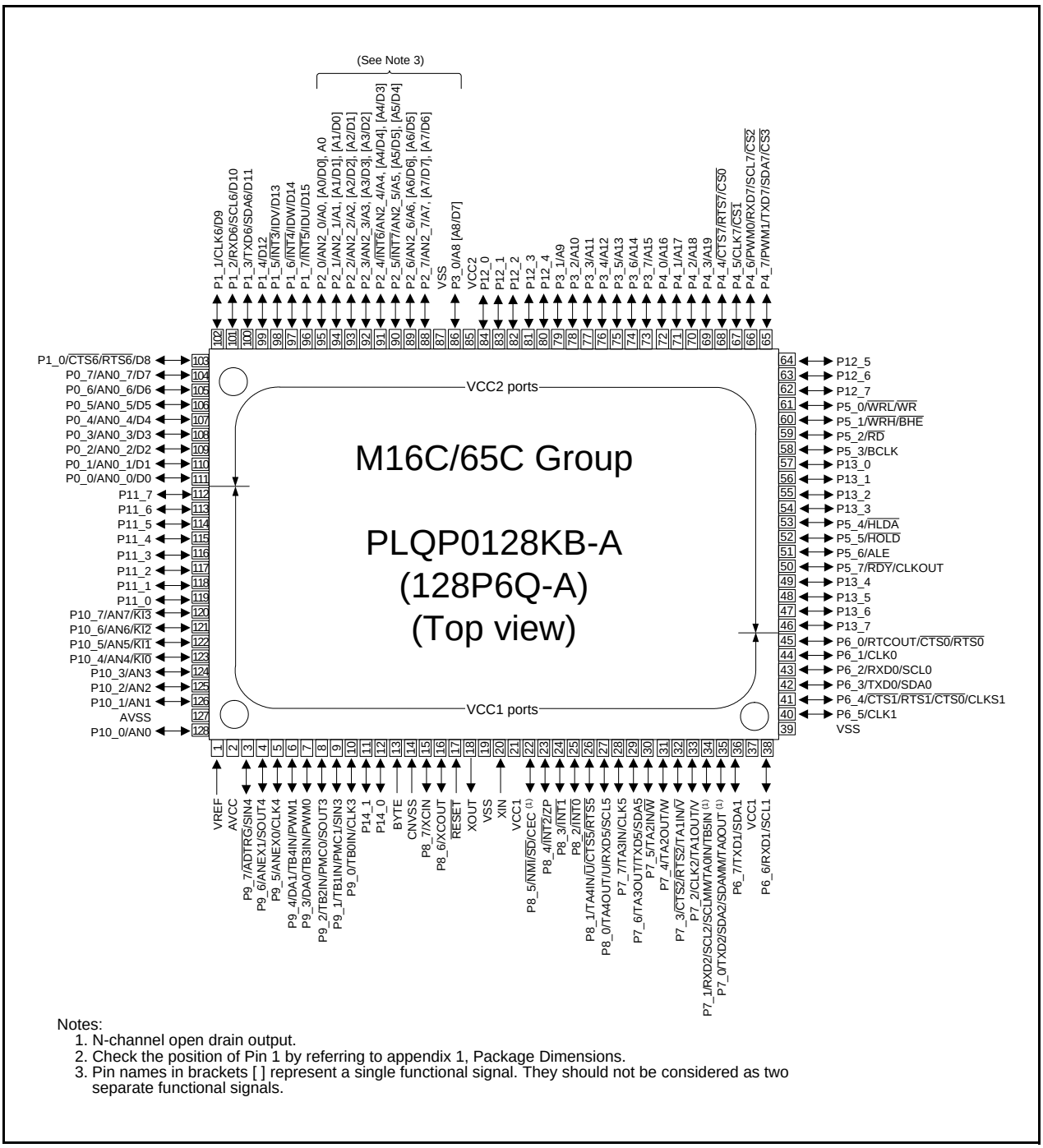


Notes:
1. ROM size depends on MCU type.
2. RAM size depends on MCU type.

Figure 1.4 Block Diagram for the 100-Pin Package

1.5 Pin Assignments

Figure 1.5 to Figure 1.7 show pin assignments. Table 1.7 to Table 1.11 list pin names.



Notes:
1. N-channel open drain output.
2. Check the position of Pin 1 by referring to appendix 1, Package Dimensions.
3. Pin names in brackets [ ] represent a single functional signal. They should not be considered as two separate functional signals.

Figure 1.5 Pin Assignment for the 128-Pin Package

Table 1.10 Pin Names for the 100-Pin Package (1/2)

Pin No.		Control Pin	Port	I/O Pin for Peripheral Function				Bus Control Pin
FA	FB			Interrupt	Timer	Serial interface	A/D converter, D/A converter	
1	99		P9_6			SOUT4	ANEX1	
2	100		P9_5			CLK4	ANEX0	
3	1		P9_4		TB4IN/PWM1		DA1	
4	2		P9_3		TB3IN/PWM0		DA0	
5	3		P9_2		TB2IN/PMC0	SOUT3		
6	4		P9_1		TB1IN/PMC1	SIN3		
7	5		P9_0		TB0IN	CLK3		
8	6	BYTE						
9	7	CNVSS						
10	8	XCIN	P8_7					
11	9	XCOUT	P8_6					
12	10	$\overline{\text{RESET}}$						
13	11	XOUT						
14	12	VSS						
15	13	XIN						
16	14	VCC1						
17	15		P8_5	$\overline{\text{NMI}}$	$\overline{\text{SD}}$	CEC		
18	16		P8_4	$\overline{\text{INT2}}$	ZP			
19	17		P8_3	$\overline{\text{INT1}}$				
20	18		P8_2	$\overline{\text{INT0}}$				
21	19		P8_1		TA4IN/$\overline{\text{U}}$	$\overline{\text{CTS5/RTS5}}$		
22	20		P8_0		TA4OUT/U	RXD5/SCL5		
23	21		P7_7		TA3IN	CLK5		
24	22		P7_6		TA3OUT	TXD5/SDA5		
25	23		P7_5		TA2IN/$\overline{\text{W}}$			
26	24		P7_4		TA2OUT/W			
27	25		P7_3		TA1IN/$\overline{\text{V}}$	$\overline{\text{CTS2/RTS2}}$		
28	26		P7_2		TA1OUT/V	CLK2		
29	27		P7_1		TA0IN/TB5IN	RXD2/SCL2/SCLMM		
30	28		P7_0		TA0OUT	TXD2/SDA2/SDAMM		
31	29		P6_7			TXD1/SDA1		
32	30		P6_6			RXD1/SCL1		
33	31		P6_5			CLK1		
34	32		P6_4			$\overline{\text{CTS1}}$/RTS1/$\overline{\text{CTS0}}$/ CLKS1		
35	33		P6_3			TXD0/SDA0		
36	34		P6_2			RXD0/SCL0		
37	35		P6_1			CLK0		
38	36		P6_0		RTCOUT	$\overline{\text{CTS0/RTS0}}$		
39	37	CLKOUT	P5_7					$\overline{\text{RDY}}$
40	38		P5_6					ALE
41	39		P5_5					$\overline{\text{HOLD}}$
42	40		P5_4					$\overline{\text{HLDA}}$
43	41		P5_3					BCLK
44	42		P5_2					$\overline{\text{RD}}$
45	43		P5_1					$\overline{\text{WRH/BHE}}$
46	44		P5_0					$\overline{\text{WRL/WR}}$
47	45		P4_7		PWM1	TXD7/SDA7		$\overline{\text{CS3}}$
48	46		P4_6		PWM0	RXD7/SCL7		$\overline{\text{CS2}}$
49	47		P4_5			CLK7		$\overline{\text{CS1}}$
50	48		P4_4			$\overline{\text{CTS7/RTS7}}$		$\overline{\text{CS0}}$

Table 1.11 Pin Names for the 100-Pin Package (2/2)

Pin No.		Control Pin	Port	I/O Pin for Peripheral Function				Bus Control Pin
FA	FB			Interrupt	Timer	Serial interface	A/D converter, D/A converter	
51	49		P4_3					A19
52	50		P4_2					A18
53	51		P4_1					A17
54	52		P4_0					A16
55	53		P3_7					A15
56	54		P3_6					A14
57	55		P3_5					A13
58	56		P3_4					A12
59	57		P3_3					A11
60	58		P3_2					A10
61	59		P3_1					A9
62	60	VCC2						
63	61		P3_0					A8, [A8/D7]
64	62	VSS						
65	63		P2_7				AN2_7	A7, [A7/D7], [A7/D6]
66	64		P2_6				AN2_6	A6, [A6/D6], [A6/D5]
67	65		P2_5	$\overline{\text{INT7}}$			AN2_5	A5, [A5/D5], [A5/D4]
68	66		P2_4	$\overline{\text{INT6}}$			AN2_4	A4, [A4/D4], [A4/D3]
69	67		P2_3				AN2_3	A3, [A3/D3], [A3/D2]
70	68		P2_2				AN2_2	A2, [A2/D2], [A2/D1]
71	69		P2_1				AN2_1	A1, [A1/D1], [A1/D0]
72	70		P2_0				AN2_0	A0, [A0/D0], A0
73	71		P1_7	$\overline{\text{INT5}}$	IDU			D15
74	72		P1_6	$\overline{\text{INT4}}$	IDW			D14
75	73		P1_5	$\overline{\text{INT3}}$	IDV			D13
76	74		P1_4					D12
77	75		P1_3			TXD6/SDA6		D11
78	76		P1_2			RXD6/SCL6		D10
79	77		P1_1			CLK6		D9
80	78		P1_0			$\overline{\text{CTS6}}$/$\overline{\text{RTS6}}$		D8
81	79		P0_7				AN0_7	D7
82	80		P0_6				AN0_6	D6
83	81		P0_5				AN0_5	D5
84	82		P0_4				AN0_4	D4
85	83		P0_3				AN0_3	D3
86	84		P0_2				AN0_2	D2
87	85		P0_1				AN0_1	D1
88	86		P0_0				AN0_0	D0
89	87		P10_7	$\overline{\text{KI3}}$			AN7	
90	88		P10_6	$\overline{\text{KI2}}$			AN6	
91	89		P10_5	$\overline{\text{KI1}}$			AN5	
92	90		P10_4	$\overline{\text{KI0}}$			AN4	
93	91		P10_3				AN3	
94	92		P10_2				AN2	
95	93		P10_1				AN1	
96	94	AVSS						
97	95		P10_0				AN0	
98	96	VREF						
99	97	AVCC						
100	98		P9_7			SIN4	$\overline{\text{ADTRG}}$	

Table 1.15 Pin Functions for the 100-Pin Package (1/3)

Signal Name	Pin Name	I/O	Power Supply	Description
Power supply input	VCC1, VCC2, VSS	I	-	Apply 2.7 to 5.5 V to pins VCC1 and VCC2 (VCC1 ≥ VCC2) and 0 V to the VSS pin.
Analog power supply input	AVCC, AVSS	I	VCC1	This is the power supply for the A/D and D/A converters. Connect the AVCC pin to VCC1, and connect the AVSS pin to VSS.
Reset input	$\overline{\text{RESET}}$	I	VCC1	Driving this pin low resets the MCU.
CNVSS	CNVSS	I	VCC1	Input pin to switch processor modes. After a reset, to start operating in single-chip mode, connect the CNVSS pin to VSS via a resistor. To start operating in microprocessor mode, connect the pin to VCC1.
External data bus width select input	BYTE	I	VCC1	Input pin to select the data bus of the external area. The data bus is 16 bits when it is low, and 8 bits when it is high. This pin must be fixed either high or low. Connect the BYTE pin to VSS in single-chip mode.
Bus control pins	D0 to D7	I/O	VCC2	Inputs or outputs data (D0 to D7) while accessing an external area with a separate bus.
	D8 to D15	I/O	VCC2	Inputs or outputs data (D8 to D15) while accessing an external area with a 16-bit separate bus.
	A0 to A19	O	VCC2	Outputs address bits A0 to A19.
	A0/D0 to A7/D7	I/O	VCC2	Inputs or outputs data (D0 to D7) and outputs address bits (A0 to A7) by timesharing, while accessing an external area with an 8-bit multiplexed bus.
	A1/D0 to A8/D7	I/O	VCC2	Inputs or outputs data (D0 to D7) and outputs address bits (A1 to A8) by timesharing, while accessing an external area with a 16-bit multiplexed bus.
	$\overline{\text{CS0}}$ to $\overline{\text{CS3}}$	O	VCC2	Outputs chip-select signals $\overline{\text{CS0}}$ to $\overline{\text{CS3}}$ to specify an external area.
	$\overline{\text{WRL}}$/$\overline{\text{WR}}$ $\overline{\text{WRH}}$/$\overline{\text{BHE}}$ $\overline{\text{RD}}$	O	VCC2	Outputs $\overline{\text{WRL}}$, $\overline{\text{WRH}}$, ($\overline{\text{WR}}$, $\overline{\text{BHE}}$), and $\overline{\text{RD}}$ signals. $\overline{\text{WRL}}$ and $\overline{\text{WRH}}$ can be switched with $\overline{\text{BHE}}$ and $\overline{\text{WR}}$. • $\overline{\text{WRL}}$, $\overline{\text{WRH}}$, and $\overline{\text{RD}}$ selected If the external data bus is 16 bits, data is written to an even address in an external area when $\overline{\text{WRL}}$ is driven low. Data is written to an odd address when $\overline{\text{WRH}}$ is driven low. Data is read when $\overline{\text{RD}}$ is driven low. • $\overline{\text{WR}}$, $\overline{\text{BHE}}$, and $\overline{\text{RD}}$ selected Data is written to an external area when $\overline{\text{WR}}$ is driven low. Data in an external area is read when $\overline{\text{RD}}$ is driven low. An odd address is accessed when $\overline{\text{BHE}}$ is driven low. Select $\overline{\text{WR}}$, $\overline{\text{BHE}}$, and $\overline{\text{RD}}$ when using an 8-bit external data bus.
	ALE	O	VCC2	Outputs an ALE signal to latch the address.
	$\overline{\text{HOLD}}$	I	VCC2	$\overline{\text{HOLD}}$ input is unavailable. Connect the $\overline{\text{HOLD}}$ pin to VCC2 via a resistor (pull-up).
	$\overline{\text{HLDA}}$	O	VCC2	In a hold state, $\overline{\text{HLDA}}$ outputs a low-level signal.
	$\overline{\text{RDY}}$	I	VCC2	The MCU bus is placed in a wait state while the $\overline{\text{RDY}}$ pin is driven low.

Power supply: VCC2 is used to supply power to the external bus associated pins. The dual power supply configuration allows VCC2 to interface at a different voltage than VCC1.

2.1 Data Registers (R0, R1, R2, and R3)

R0, R1, R2, and R3 are 16-bit registers used for transfer, arithmetic, and logic operations. R0 and R1 can be split into upper (R0H/R1H) and lower (R0L/R1L) bits to be used separately as 8-bit data registers. R0 can be combined with R2, and R3 can be combined with R1 and be used as 32-bit data registers R2R0 and R3R1, respectively.

2.2 Address Registers (A0 and A1)

A0 and A1 are 16-bit registers used for indirect addressing, relative addressing, transfer, arithmetic, and logic operations. A0 can be combined with A1 and used as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register that is used for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the start address of a relocatable interrupt vector table.

2.5 Program Counter (PC)

The PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The USP and ISP stack pointers (SP) are each comprised of 16 bits. The U flag is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register used for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register that indicates the CPU state.

2.8.1 Carry Flag (C Flag)

The C flag retains a carry, borrow, or shift-out bit generated by the arithmetic/logic unit.

2.8.2 Debug Flag (D Flag)

The D flag is for debugging only. Set it to 0.

2.8.3 Zero Flag (Z Flag)

The Z flag becomes 1 when an arithmetic operation results in 0. Otherwise, it becomes 0.

2.8.4 Sign Flag (S Flag)

The S flag becomes 1 when an arithmetic operation results in a negative value. Otherwise, it becomes 0.

2.8.5 Register Bank Select Flag (B Flag)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is 1.

2.8.6 Overflow Flag (O Flag)

The O flag becomes 1 when an arithmetic operation results in an overflow. Otherwise, it becomes 0.

3.2 Memory Map

Special function registers (SFRs) are allocated from address 00000h to 003FFh and from 0D000h to 0D7FFh. Peripheral function control registers are located here. All blank areas within SFRs are reserved. Do not access these areas.

Internal RAM is allocated from address 00400h and higher, with 10 KB of internal RAM allocated from 00400h to 02BFFh. Internal RAM is used not only for data storage, but also for the stack area when subroutines are called or when an interrupt request is accepted.

The internal ROM is flash memory. Three internal ROM areas are available: data flash, program ROM 1, and program ROM 2.

The data flash is allocated from 0E000h to 0FFFFh. This data flash area is mostly used for data storage, but can also store programs.

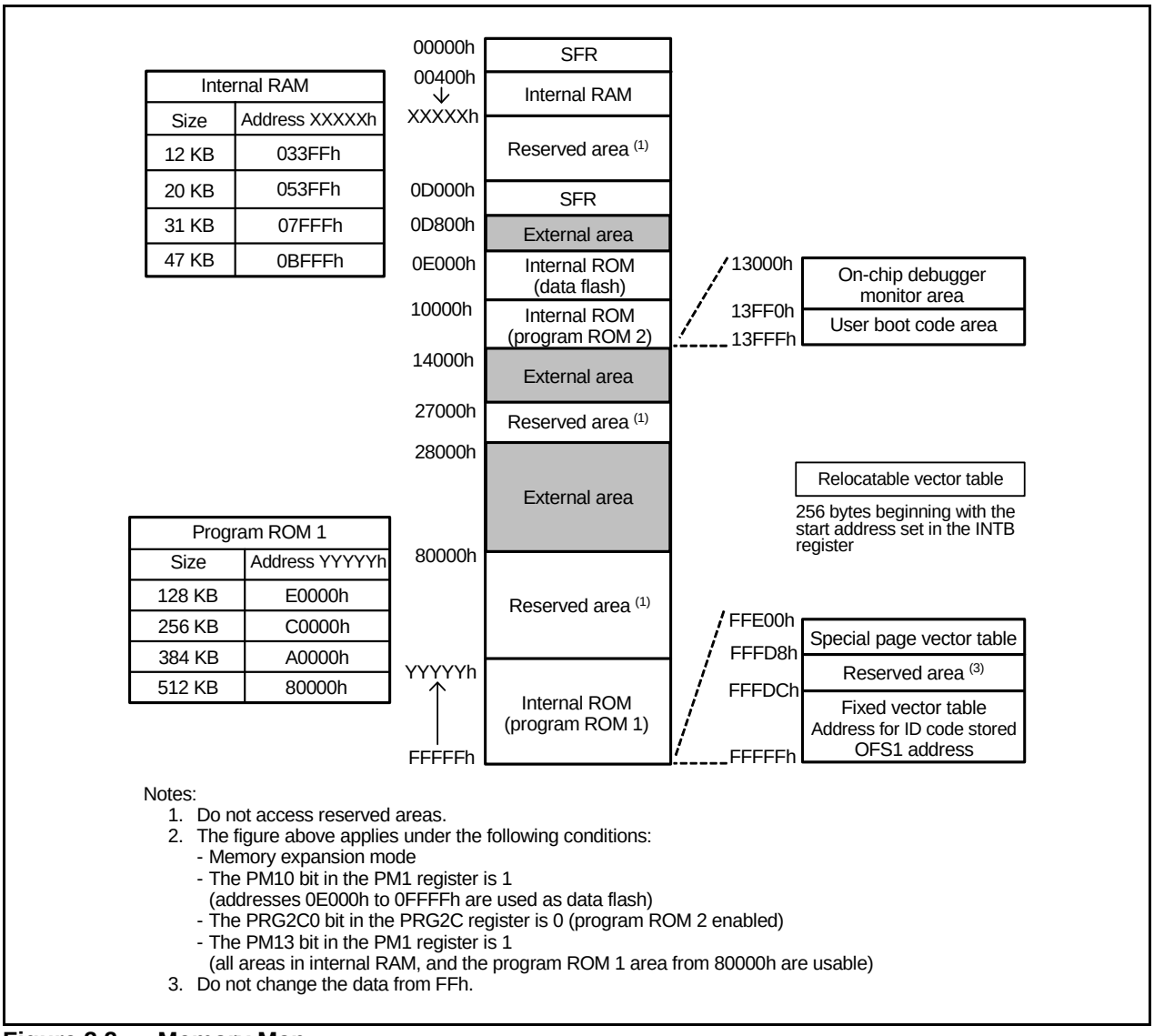
Program ROM 2 is allocated from 10000h to 13FFFh. Program ROM 1 is allocated from FFFFFh and lower, with the 64 KB program ROM 1 area allocated from address F0000h to FFFFFh.

The special page vectors are allocated from FFE00h to FFFD7h. They are used for the JMPS and JSRS instructions. Refer to the M16C/60, M16C/20, M16C/Tiny Series Software Manual for details.

The fixed vector table for interrupts is allocated from FFFDCh to FFFFFh.

The 256 bytes beginning with the start address set in the INTB register compose the relocatable vector table for interrupts.

Figure 3.2 shows the Memory Map.



Notes:
1. Do not access reserved areas.
2. The figure above applies under the following conditions:
   - Memory expansion mode
   - The PM10 bit in the PM1 register is 1
     (addresses 0E000h to 0FFFFh are used as data flash)
   - The PRG2C0 bit in the PRG2C register is 0 (program ROM 2 enabled)
   - The PM13 bit in the PM1 register is 1
     (all areas in internal RAM, and the program ROM 1 area from 80000h are usable)
3. Do not change the data from FFh.

Figure 3.2 Memory Map

Table 4.6 SFR Information (6) (1)

Address	Register	Symbol	Reset Value
01B0h	DMA3 Source Pointer	SAR3	XXh
01B1h			XXh
01B2h			0Xh
01B3h			
01B4h	DMA3 Destination Pointer	DAR3	XXh
01B5h			XXh
01B6h			0Xh
01B7h			
01B8h	DMA3 Transfer Counter	TCR3	XXh
01B9h			XXh
01BAh			
01BBh			
01BCh	DMA3 Control Register	DM3CON	0000 0X00b
01BDh			
01BEh			
01BFh			
01C0h	Timer B0-1 Register	TB01	XXh
01C1h			XXh
01C2h	Timer B1-1 Register	TB11	XXh
01C3h			XXh
01C4h	Timer B2-1 Register	TB21	XXh
01C5h			XXh
01C6h	Pulse Period/Pulse Width Measurement Mode Function Select Register 1	PPWFS1	XXXX X000b
01C7h			
01C8h	Timer B Count Source Select Register 0	TBCS0	00h
01C9h	Timer B Count Source Select Register 1	TBCS1	X0h
01CAh			
01CBh	Timer AB Division Control Register 0	TCKDIVC0	0000 X000b
01CCh			
01CDh			
01CEh			
01CFh			
01D0h	Timer A Count Source Select Register 0	TACS0	00h
01D1h	Timer A Count Source Select Register 1	TACS1	00h
01D2h	Timer A Count Source Select Register 2	TACS2	X0h
01D3h			
01D4h	16-bit Pulse Width Modulation Mode Function Select Register	PWMFS	0XX0 X00Xb
01D5h	Timer A Waveform Output Function Select Register	TAPOFS	XXX0 0000b
01D6h			
01D7h			
01D8h	Timer A Output Waveform Change Enable Register	TAOW	XXX0 X00Xb
01D9h			
01DAh	Three-Phase Protect Control Register	TPRC	00h
01DBh			
01DCh			
01DDh			
01DEh			
01DFh			

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.17 SFR Information (17) (1)

Address	Register	Symbol	Reset Value
03F0h	Port P8 Register	P8	XXh
03F1h	Port P9 Register	P9	XXh
03F2h	Port P8 Direction Register	PD8	00h
03F3h	Port P9 Direction Register	PD9	00h
03F4h	Port P10 Register	P10	XXh
03F5h	Port P11 Register	P11	XXh
03F6h	Port P10 Direction Register	PD10	00h
03F7h	Port P11 Direction Register	PD11	00h
03F8h	Port P12 Register	P12	XXh
03F9h	Port P13 Register	P13	XXh
03FAh	Port P12 Direction Register	PD12	00h
03FBh	Port P13 Direction Register	PD13	00h
03FCh	Port P14 Register	P14	XXh
03FDh			
03FEh	Port P14 Direction Register	PD14	XXXX XX00b
03FFh			

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 5.3 Recommended Operating Conditions (2/3)

V_{CC1} = V_{CC2} = 2.7 to 5.5 V at T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified.

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
$I_{OL(sum)}$	Low peak output current	Sum of $I_{OL(peak)}$ at P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0 to P14_1			80.0	mA
		Sum of $I_{OL(peak)}$ at P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_5, P12_0 to P12_7, P13_0 to P13_7			80.0	mA
$I_{OL(peak)}$	Low peak output current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1			10.0	mA
$I_{OL(avg)}$	Low average output current (1)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1			5.0	mA
$f_{(XIN)}$	Main clock input oscillation frequency	V_{CC1} = 2.7 V to 5.5 V	2		20	MHz
$f_{(XCIN)}$	Sub clock oscillation frequency			32.768	50	kHz
$f_{(PLL)}$	PLL clock oscillation frequency	V_{CC1} = 2.7 V to 5.5 V	10		32	MHz
$f_{(BCLK)}$	CPU operation clock		2		32	MHz
$t_{SU(PLL)}$	PLL frequency synthesizer stabilization wait time	V_{CC1} = 5.0 V			2	ms
		V_{CC1} = 3.0 V			3	ms

Note:
1. The average output current is the mean value within 100 ms.

Table 5.13 Voltage Detector 2 Electrical Characteristics

The measurement condition is V_{CC1} = 2.7 to 5.5 V, T_{opr} = -20°C to 85°C/-40°C to 85°C, unless otherwise specified.

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det2}	Voltage detection level Vdet2_0	When V_{CC1} is falling	3.70	4.00	4.30	V
-	Hysteresis width at the rising of V_{CC1} in voltage detector 2			0.15		V
-	Voltage detector 2 response time (2)	When V_{CC1} falls from 5 V to (Vdet2_0 - 0.1) V			200	µs
-	Voltage detector self power consumption	VC27 = 1, V_{CC1} = 5.0 V		1.7		µA
$t_{d(E-A)}$	Waiting time until voltage detector operation starts (1)				100	µs

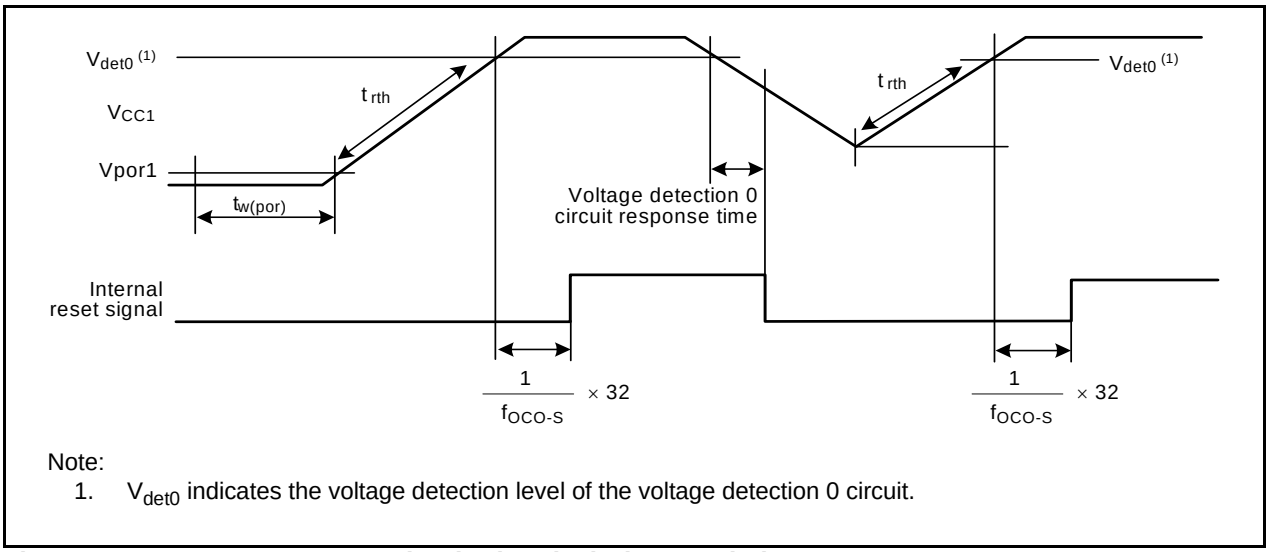
Notes:
1. Necessary time until the voltage detector operates after setting to 1 again after setting the VC27 bit in the VCR2 register to 0.
2. Time from when passing the V_{det2} until when a voltage monitor 2 reset is generated.

Table 5.14 Power-On Reset Circuit

The measurement condition is V_{CC1} = 2.0 to 5.5 V, T_{opr} = -20°C to 85°C/ -40°C to 85°C, unless otherwise specified.

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{por1}	Voltage at which power-on reset enabled (1)				0.5	V
t_{rth}	External power V_{CC1} rise gradient		2.0		50000	mV/ms
$t_{w(por)}$	Time necessary to enable power-on reset		300			ms

Note:
1. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS1 address to 0. Also, set the VDSEL1 bit to 0 (Vdet0_2).



Note:
1. V_{det0} indicates the voltage detection level of the voltage detection 0 circuit.

Figure 5.3 Power-On Reset Circuit Electrical Characteristics

5.2 Electrical Characteristics (V_{CC1} = V_{CC2} = 5 V)

5.2.1 Electrical Characteristics

V_{CC1} = V_{CC2} = 5 V

Table 5.18 Electrical Characteristics (1) [1]

V_{CC1} = V_{CC2} = 4.2 to 5.5 V, V_{SS} = 0 V at T_{opr} = –20°C to 85°C/–40°C to 85°C, $f_{(BCLK)}$ = 32 MHz unless otherwise specified.

Symbol	Parameter		Measuring Condition	Standard			Unit
				Min.	Typ.	Max.	
V_{OH}	High output voltage	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1	I_{OH} = –5 mA	V_{CC1} – 2.0		V_{CC1}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7	I_{OH} = –5 mA	V_{CC2} – 2.0		V_{CC2}	
V_{OH}	High output voltage	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1	I_{OH} = –200 µA	V_{CC1} – 0.3		V_{CC1}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7	I_{OH} = –200 µA	V_{CC2} – 0.3		V_{CC2}	
V_{OH}	High output voltage XOUT	HIGH POWER	I_{OH} = –1 mA	V_{CC1} – 2.0		V_{CC1}	V
		LOW POWER	I_{OH} = –0.5 mA	V_{CC1} – 2.0		V_{CC1}	
	High output voltage XCOUT	HIGH POWER	With no load applied		2.6		V
		LOW POWER	With no load applied		2.2		
V_{OL}	Low output voltage	P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1	I_{OL} = 5 mA			2.0	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7	I_{OL} = 5 mA			2.0	
V_{OL}	Low output voltage	P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1	I_{OL} = 200 µA			0.45	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7	I_{OL} = 200 µA			0.45	
V_{OL}	Low output voltage XOUT	HIGH POWER	I_{OL} = 1 mA			2.0	V
		LOW POWER	I_{OL} = 0.5 mA			2.0	
	Low output voltage XCOUT	HIGH POWER	With no load applied		0		V
		LOW POWER	With no load applied		0		

Note:
1. When $V_{CC1} \neq V_{CC2}$, refer to 5 V or 3 V standard depending on the voltage.

$V_{CC1} = V_{CC2} = 5$ V

Switching Characteristics

($V_{CC1} = V_{CC2} = 5$ V, $V_{SS} = 0$ V, at T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified)

5.2.4.2 In 1 to 3 Waits Setting and When Accessing External Area

Table 5.37 Memory Expansion Mode and Microprocessor Mode (in 1 to 3 Waits Setting and When Accessing External Area)

Symbol	Parameter	Measuring Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	See Figure 5.14		25	ns
$t_{h(BCLK-AD)}$	Address output hold time (in relation to BCLK)		0		ns
$t_{h(RD-AD)}$	Address output hold time (in relation to RD)		0		ns
$t_{h(WR-AD)}$	Address output hold time (in relation to WR)		(Note 2)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			25	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (in relation to BCLK)		0		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time			15	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time		-4		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			25	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			25	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (in relation to BCLK)			40	ns
$t_{d(DB-WR)}$	Data output delay time (in relation to WR)		(Note 1)		ns
$t_{h(WR-DB)}$	Data output hold time (in relation to WR)(3)		(Note 4)		ns

Notes:

1. Calculated according to the BCLK frequency as follows:

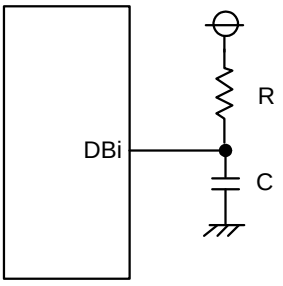
$$\frac{(n-0.5)\times 10^9}{f_{(BCLK)}} - 40[ns]$$

n is 1 for 1 wait setting, 2 for 2 waits setting and 3 for 3 waits setting.
When n = 1, $f_{(BCLK)}$ is 12.5 MHz or less.

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5\times 10^9}{f_{(BCLK)}} - 10[ns]$$

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.
Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.
Hold time of data bus is expressed in
$t = -CR \times \ln(1 - V_{OL}/V_{CC2})$
by a circuit of the right figure.
For example, when $V_{OL} = 0.2V_{CC2}$, C = 30 pF, R = 1 kΩ, hold time of output low level is
$t = -30\text{ pF} \times 1\text{ k}\Omega \times \ln(1 - 0.2V_{CC2}/V_{CC2})$
= 6.7 ns.



4. Calculated according to the BCLK frequency as follows:

$$\frac{0.5\times 10^9}{f_{(BCLK)}} - 20[ns]$$

Hold time is equal to or less than 0 ns when the BCLK frequency exceeds 25 MHz.

$V_{CC1} = V_{CC2} = 5\ V$

Switching Characteristics

($V_{CC1} = V_{CC2} = 5$ V, $V_{SS} = 0$ V, at $T_{opr} = -20°C$ to 85°C/-40°C to 85°C unless otherwise specified)

5.2.4.4 In Wait State Setting 2ϕ + 3ϕ, 2ϕ + 4ϕ, 3ϕ + 4ϕ, and 4ϕ + 5ϕ, and When Accessing External Area

Table 5.39 Memory Expansion Mode and Microprocessor Mode (in Wait State Setting 2 ϕ + 3 ϕ, 2 ϕ + 4ϕ, 3ϕ + 4ϕ, and 4ϕ + 5ϕ, and When Accessing External Area)

Symbol	Parameter	Measuring Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	See Figure 5.14		25	ns
$t_{h(BCLK-AD)}$	Address output hold time (in relation to BCLK)		0		ns
$t_{h(RD-AD)}$	Address output hold time (in relation to RD)		0		ns
$t_{h(WR-AD)}$	Address output hold time (in relation to WR)		(Note 2)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			25	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (in relation to BCLK)		0		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time			15	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time		-4		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			25	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			25	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (in relation to BCLK)			40	ns
$t_{d(DB-WR)}$	Data output delay time (in relation to WR)		(Note 1)		ns
$t_{h(WR-DB)}$	Data output hold time (in relation to WR) (3)		(Note 4)		ns

Notes:

1. Calculated according to the BCLK frequency as follows:

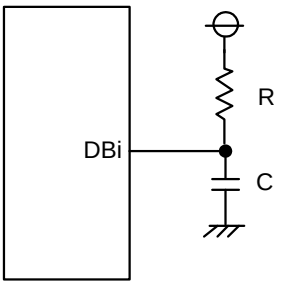
$$\frac{(n-0.5)\times 10^9}{f_{(BCLK)}} - 40[ns]$$

n is 3 for 2ϕ + 3ϕ, 4 for 2ϕ + 4ϕ, 4 for 3ϕ + 4ϕ, and 5 for 4ϕ + 5ϕ.

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5\times 10^9}{f_{(BCLK)}} - 10[ns]$$

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.
Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.
Hold time of data bus is expressed in
$t = -CR \times \ln(1 - V_{OL}/V_{CC2})$
by a circuit of the right figure.
For example, when $V_{OL} = 0.2V_{CC2}$, C = 30 pF, R = 1 kΩ, hold time of output low level is
$t = -30\ pF \times 1\ k\Omega \times \ln(1 - 0.2V_{CC2}/V_{CC2})$
= 6.7 ns.



4. Calculated according to the BCLK frequency as follows: $\frac{0.5\times 10^9}{f_{(BCLK)}} - 20[ns]$
Hold time is equal to or less than 0 ns when the BCLK frequency exceeds 25 MHz.

$V_{CC1} = V_{CC2} = 3\ V$

Table 5.44 Electrical Characteristics (3) (2/2)

R5F3651ECNFC, R5F3651KCNFC, R5F3650KCNFA, R5F3650KCNFB, R5F3651MCNFC, R5F3650MCNFA, R5F3650MCNFB, R5F3651NCNFC, R5F3650NCNFA, R5F3650NCNFB, R5F3651ECDFC, R5F3651KCDFC, R5F3650KCDFA, R5F3650KCDFB, R5F3651MCDFC, R5F3650MCDFA, R5F3650MCDFB, R5F3651NCDFC, R5F3650NCDFA, R5F3650NCDFB

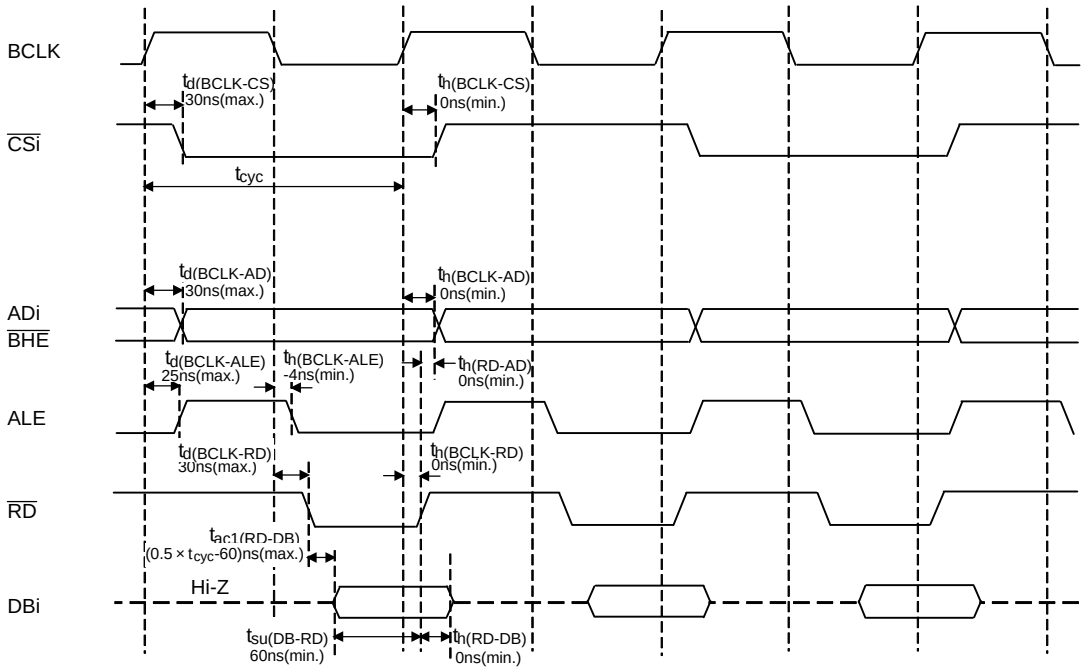
$V_{CC1} = V_{CC2} = 2.7$ to $3.3\ V$, $V_{SS} = 0\ V$ at $T_{opr} = -20°C$ to $85°C/-40°C$ to $85°C$, $f_{(BCLK)} = 32$ MHz unless otherwise specified.

Symbol	Parameter	Measuring Condition		Standard			Unit
				Min.	Typ.	Max.	
I_{CC}	Power supply current In single-chip, mode, the output pin are open and other pins are V_{SS}	Stop mode	Main clock stopped 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator stopped Peripheral clock stopped $T_{opr} = 25°C$		1.6		µA
		During flash memory program	$f_{(BCLK)} = 10$ MHz, PM17 = 1 (one wait) $V_{CC1} = 3.0\ V$		20.0		mA
		During flash memory erase	$f_{(BCLK)} = 10$ MHz, PM17 = 1 (one wait) $V_{CC1} = 3.0\ V$		30.0		mA

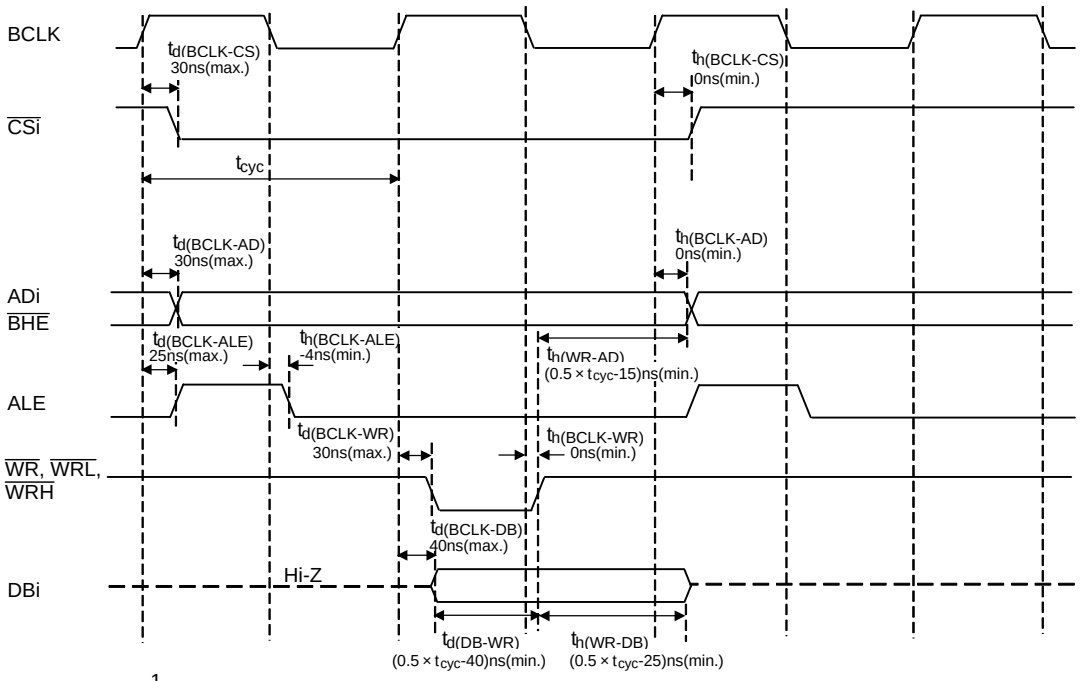
Memory Expansion Mode and Microprocessor Mode
(in no wait state setting)

$V_{CC1} = V_{CC2} = 3V$

Read timing



Write timing



$$t_{cyc} = \frac{1}{f_{(BCLK)}}$$

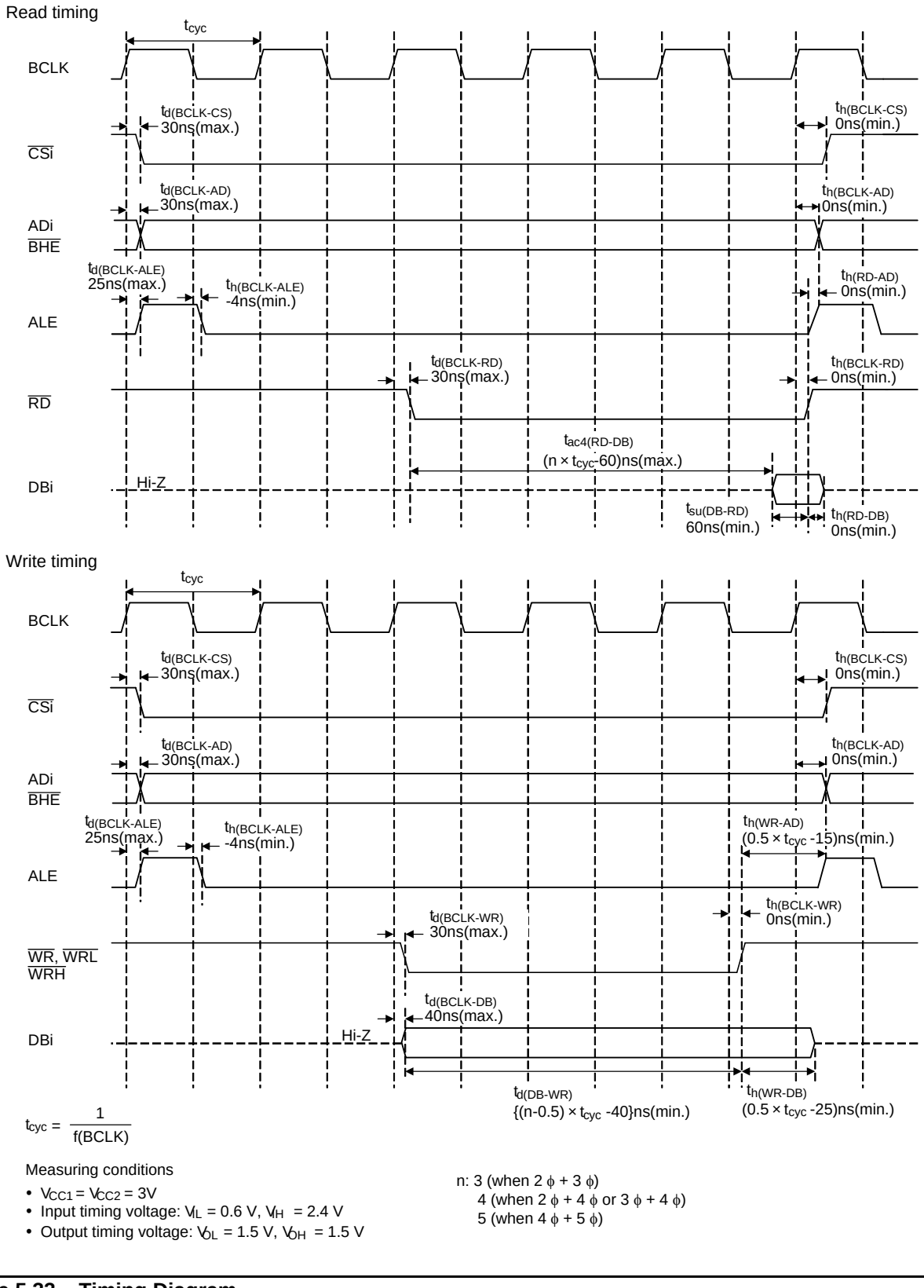
Measuring conditions

- $V_{CC1} = V_{CC2} = 3V$
- Input timing voltage: $V_{IL} = 0.6$ V, $V_{IH} = 2.4$ V
- Output timing voltage: $V_{OL} = 1.5$ V, $V_{OH} = 1.5$ V

Figure 5.30 Timing Diagram

Memory Expansion Mode, Microprocessor Mode
(in wait state setting 2 ϕ + 3 ϕ, 2 ϕ + 4 ϕ, 3ϕ + 4 ϕ, and 4 ϕ + 5 ϕ, and when accessing external area)

$V_{CC1} = V_{CC2} = 3V$



$$t_{cyc} = \frac{1}{f(BCLK)}$$

Measuring conditions

- $V_{CC1} = V_{CC2} = 3V$
- Input timing voltage: $V_{IL} = 0.6$ V, $V_{IH} = 2.4$ V
- Output timing voltage: $V_{OL} = 1.5$ V, $V_{OH} = 1.5$ V

n: 3 (when 2 ϕ + 3 ϕ)
4 (when 2 ϕ + 4 ϕ or 3 ϕ + 4 ϕ)
5 (when 4 ϕ + 5 ϕ)

Figure 5.33 Timing Diagram