Renesas Electronics America Inc - R5F3650KCDFA#V0 Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	M16C/60
Core Size	16-Bit
Speed	32MHz
Connectivity	EBI/EMI, I²C, SIO, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	85
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	31K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f3650kcdfa-v0

Table 1.2 Specifications for the 128-Pin Package (2/2)

Item	Function	Description
Timers	Timer A	16-bit timer × 5 Timer mode, event counter mode, one-shot timer mode, pulse width modulation (PWM) mode Event counter two-phase pulse signal processing (two-phase encoder input) × 3 Programmable output mode × 3
	Timer B	16-bit timer × 6 Timer mode, event counter mode, pulse period measurement mode, pulse width measurement mode
	Three-phase motor control timer functions	• Three-phase inverter control (timer A1, timer A2, timer A4, timer B2) • On-chip dead time timer
	Real-time clock	Count: seconds, minutes, hours, days of the week
	PWM function	8 bits × 2
	Remote control signal receiver	• 2 circuits • 4 wave pattern matchings (differentiate wave pattern for headers, data 0, data 1, and special data) • 6-byte receive buffer (1 circuit only) • Operating frequency of 32 kHz
Serial Interface	UART0 to UART2, UART5 to UART7	Clock synchronous/asynchronous × 6 channels I^2C-bus, IEBus, special mode 2 SIM (UART2)
	SI/O3, SI/O4	Clock synchronization only × 2 channels
Multi-master I^2C-bus Interface		1 channel
CEC Functions (2)		CEC transmit/receive, arbitration lost detection, ACK automatic output, operation frequency of 32 kHz
A/D Converter		10-bit resolution × 26 channels, including sample and hold function Conversion time: 1.72 µs
D/A Converter		8-bit resolution × 2 circuits
CRC Calculator		CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$), CRC-16 ($X^{16} + X^{15} + X^2 + 1$) compliant
Flash Memory		• Program and erase power supply voltage: 2.7 to 5.5 V • Program and erase cycles: 1,000 times (program ROM 1, program ROM 2), 10,000 times (data flash) • Program security: ROM code protect, ID code check
Debug Functions		On-chip debug, on-board flash rewrite, address match interrupt × 4
Operation Frequency/Supply Voltage		32 MHz/VCC1 = 2.7 to 5.5 V, VCC2 = 2.7 V to VCC1
Current Consumption		Refer to the Electrical Characteristics chapter
Operating Temperature		-20°C to 85°C, -40°C to 85°C (1)
Package		128-pin LQFP: PLQP0128KB-A (Previous package code: 128P6Q-A)

Notes:
1. See Table 1.5 “Product List (N-Version)” to Table 1.6 “Product List (D-Version)” for the operating temperature.
2. The CEC function indicates circuitry which supports the transmission and reception of CEC signals standardized by the High-Definition Multimedia Interface (HDMI). HDMI and High-Definition Multimedia Interface are registered trademarks of HDMI Licensing, LLC.

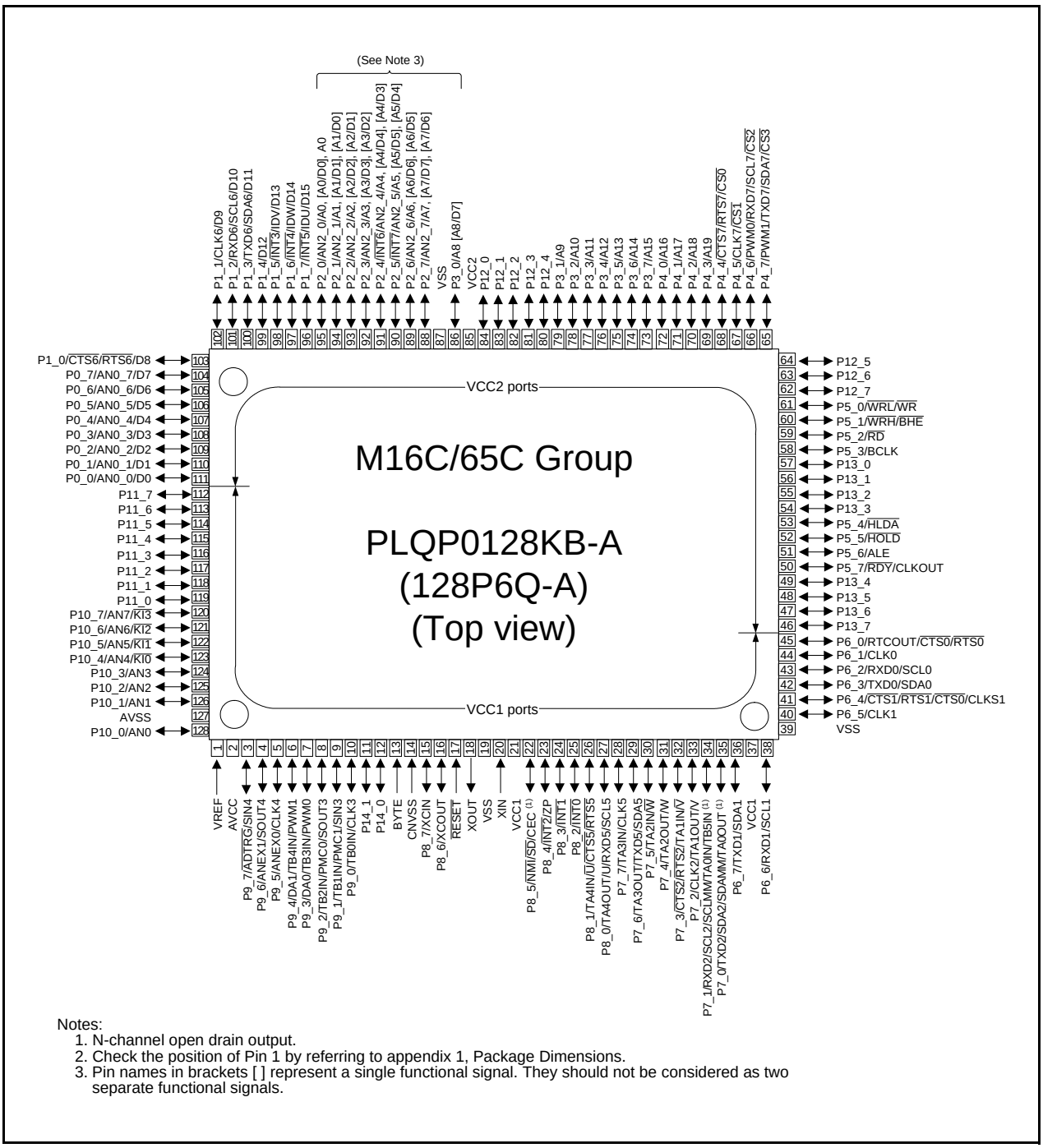
Table 1.4 Specifications for the 100-Pin Package (2/2)

Item	Function	Description
Timers	Timer A	16-bit timer × 5 Timer mode, event counter mode, one-shot timer mode, pulse width modulation (PWM) mode Event counter two-phase pulse signal processing (two-phase encoder input) × 3 Programmable output mode × 3
	Timer B	16-bit timer × 6 Timer mode, event counter mode, pulse period measurement mode, pulse width measurement mode
	Three-phase motor control timer functions	• Three-phase inverter control (timer A1, timer A2, timer A4, timer B2) • On-chip dead time timer
	Real-time clock	Count: seconds, minutes, hours, days of the week
	PWM function	8 bits × 2
	Remote control signal receiver	• 2 circuits • 4 wave pattern matchings (differentiate wave pattern for headers, data 0, data 1, and special data) • 6-byte receive buffer (1 circuit only) • Operating frequency of 32 kHz
Serial Interface	UART0 to UART2, UART5 to UART7	Clock synchronous/asynchronous × 6 channels I^2C-bus, IEBus, special mode 2 SIM (UART2)
	SI/O3, SI/O4	Clock synchronization only × 2 channels
Multi-master I^2C-bus Interface		1 channel
CEC Functions (2)		CEC transmit/receive, arbitration lost detection, ACK automatic output, operation frequency of 32 kHz
A/D Converter		10-bit resolution × 26 channels, including sample and hold function Conversion time: 1.72 µs
D/A Converter		8-bit resolution × 2 circuits
CRC Calculator		CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$), CRC-16 ($X^{16} + X^{15} + X^2 + 1$) compliant
Flash Memory		• Program and erase power supply voltage: 2.7 to 5.5 V • Program and erase cycles: 1,000 times (program ROM 1, program ROM 2), 10,000 times (data flash) • Program security: ROM code protect, ID code check
Debug Functions		On-chip debug, on-board flash rewrite, address match interrupt × 4
Operation Frequency/Supply Voltage		25 MHz/VCC1 = 2.7 to 5.5 V, VCC2 = 2.7 V to VCC1 32 MHz/VCC1 = 2.7 to 5.5 V, VCC2 = 2.7 V to VCC1
Current Consumption		Refer to the Electrical Characteristics chapter
Operating Temperature		-20°C to 85°C, -40°C to 85°C (1)
Package		100-pin QFP: PRQP0100JD-B (Previous package code: 100P6F-A) 100-pin LQFP: PLQP0100KB-A (Previous package code: 100P6Q-A)

Notes:
1. See Table 1.5 “Product List (N-Version)” to Table 1.6 “Product List (D-Version)” for the operating temperature.
2. The CEC function indicates circuitry which supports the transmission and reception of CEC signals standardized by the High-Definition Multimedia Interface (HDMI). HDMI and High-Definition Multimedia Interface are registered trademarks of HDMI Licensing, LLC.

1.5 Pin Assignments

Figure 1.5 to Figure 1.7 show pin assignments. Table 1.7 to Table 1.11 list pin names.



Notes:
1. N-channel open drain output.
2. Check the position of Pin 1 by referring to appendix 1, Package Dimensions.
3. Pin names in brackets [ ] represent a single functional signal. They should not be considered as two separate functional signals.

Figure 1.5 Pin Assignment for the 128-Pin Package

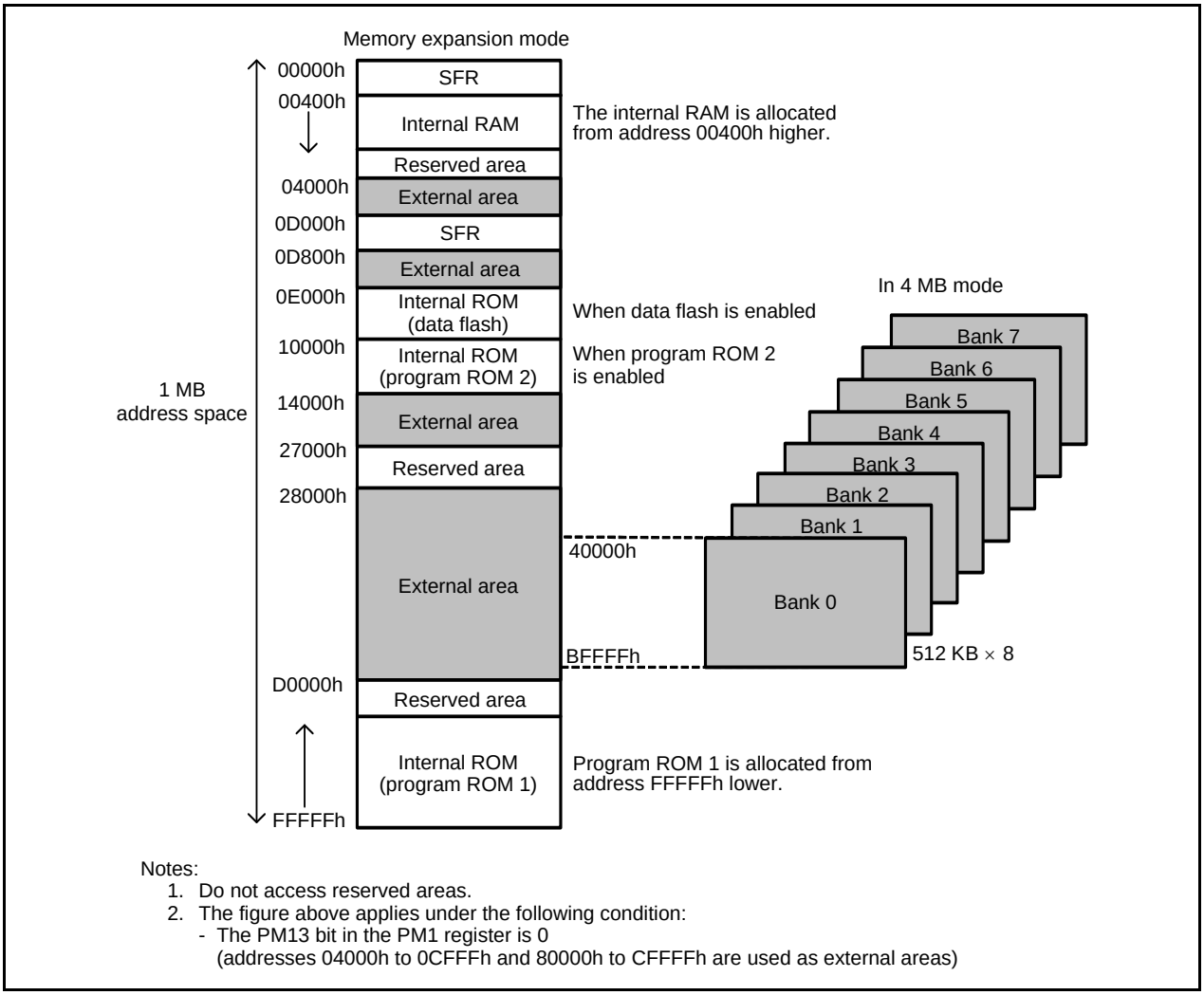
Table 1.14 Pin Functions for the 128-Pin Package (3/3)

Signal Name	Pin Name	I/O	Power Supply	Description
UART0 to UART2, UART5 to UART7 I^2C mode	SDA0 to SDA2, SDA5	I/O	VCC1	Serial data I/O.
	SDA6, SDA7	I/O	VCC2	
	SCL0 to SCL2, SCL5	I/O	VCC1	Transmit/receive clock I/O.
	SCL6, SCL7	I/O	VCC2	
Serial interface SI/O3, SI/O4	CLK3, CLK4	I/O	VCC1	Transmit/receive clock I/O.
	SIN3, SIN4	I	VCC1	Serial data input.
	SOUT3, SOUT4	O	VCC1	Serial data output.
Multi-master I^2C-bus interface	SDAMM	I/O	VCC1	Serial data I/O (N-channel open drain output).
	SCLMM	I/O	VCC1	Transmit/receive clock I/O (N-channel open drain output).
CEC I/O	CEC	I/O	VCC1	CEC I/O (N-channel open drain output).
Reference voltage input	VREF	I	VCC1	Reference voltage input for the A/D and D/A converters.
A/D converter	AN0 to AN7	I	VCC1	Analog input.
	AN0_0 to AN0_7 AN2_0 to AN2_7	I	VCC2	
	$\overline{\text{ADTRG}}$	I	VCC1	External trigger input.
	ANEX0, ANEX1	I	VCC1	Extended analog input.
D/A converter	DA0, DA1	O	VCC1	Output pin the D/A converter.
I/O ports	P0_0 to P0_7 P1_0 to P1_7 P2_0 to P2_7 P3_0 to P3_7 P4_0 to P4_7 P5_0 to P5_7 P12_0 to P12_7 P13_0 to P13_7	I/O	VCC2	8-bit CMOS I/O ports. A direction register determines whether each pin is used as an input port or an output port. A pull-up resistor may be enabled or disabled for input ports in 4-bit units.
	P6_0 to P6_7 P7_0 to P7_7 P8_0 to P8_7 P9_0 to P9_7 P10_0 to P10_7 P11_0 to P11_7	I/O	VCC1	8-bit I/O ports having equivalent functions to P0. However, P7_0, P7_1, and P8_5 are N-channel open drain output ports. No pull-up resistor is provided. P8_5 is an input port for verifying the $\overline{\text{NMI}}$ pin level and shares a pin with $\overline{\text{NMI}}$.
	P14_0, P14_1	I/O	VCC1	I/O ports having equivalent functions to P0.

3. Address Space

3.1 Address Space

The M16C/65C Group has a 1 MB address space from 00000h to FFFFFh. Address space is expandable to 4 MB with the memory area expansion function. Addresses 40000h to BFFFFh can be used as external areas from bank 0 to bank 7. Figure 3.1 shows the Address Space. Areas that can be accessed vary depending on processor mode and the status of each control bit.



Notes:
1. Do not access reserved areas.
2. The figure above applies under the following condition:
   - The PM13 bit in the PM1 register is 0
     (addresses 04000h to 0CFFFh and 80000h to CFFFFh are used as external areas)

Figure 3.1 Address Space

Table 4.3 SFR Information (3) (1)

Address	Register	Symbol	Reset Value
0040h			
0041h			
0042h	$\overline{\text{INT7}}$ Interrupt Control Register	INT7IC	XX00 X000b
0043h	$\overline{\text{INT6}}$ Interrupt Control Register	INT6IC	XX00 X000b
0044h	$\overline{\text{INT3}}$ Interrupt Control Register	INT3IC	XX00 X000b
0045h	Timer B5 Interrupt Control Register	TB5IC	XXXX X000b
0046h	Timer B4 Interrupt Control Register UART1 Bus Collision Detection Interrupt Control Register	TB4IC U1BCNIC	XXXX X000b
0047h	Timer B3 Interrupt Control Register UART0 Bus Collision Detection Interrupt Control Register	TB3IC U0BCNIC	XXXX X000b
0048h	SI/O4 Interrupt Control Register $\overline{\text{INT5}}$ Interrupt Control Register	S4IC INT5IC	XX00 X000b
0049h	SI/O3 Interrupt Control Register $\overline{\text{INT4}}$ Interrupt Control Register	S3IC INT4IC	XX00 X000b
004Ah	UART2 Bus Collision Detection Interrupt Control Register	BCNIC	XXXX X000b
004Bh	DMA0 Interrupt Control Register	DM0IC	XXXX X000b
004Ch	DMA1 Interrupt Control Register	DM1IC	XXXX X000b
004Dh	Key Input Interrupt Control Register	KUPIC	XXXX X000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXX X000b
004Fh	UART2 Transmit Interrupt Control Register	S2TIC	XXXX X000b
0050h	UART2 Receive Interrupt Control Register	S2RIC	XXXX X000b
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXX X000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXX X000b
0053h	UART1 Transmit Interrupt Control Register	S1TIC	XXXX X000b
0054h	UART1 Receive Interrupt Control Register	S1RIC	XXXX X000b
0055h	Timer A0 Interrupt Control Register	TA0IC	XXXX X000b
0056h	Timer A1 Interrupt Control Register	TA1IC	XXXX X000b
0057h	Timer A2 Interrupt Control Register	TA2IC	XXXX X000b
0058h	Timer A3 Interrupt Control Register	TA3IC	XXXX X000b
0059h	Timer A4 Interrupt Control Register	TA4IC	XXXX X000b
005Ah	Timer B0 Interrupt Control Register	TB0IC	XXXX X000b
005Bh	Timer B1 Interrupt Control Register	TB1IC	XXXX X000b
005Ch	Timer B2 Interrupt Control Register	TB2IC	XXXX X000b
005Dh	$\overline{\text{INT0}}$ Interrupt Control Register	INT0IC	XX00 X000b
005Eh	$\overline{\text{INT1}}$ Interrupt Control Register	INT1IC	XX00 X000b
005Fh	$\overline{\text{INT2}}$ Interrupt Control Register	INT2IC	XX00 X000b

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.5 SFR Information (5) (1)

Address	Register	Symbol	Reset Value
0180h	DMA0 Source Pointer	SAR0	XXh
0181h			XXh
0182h			0Xh
0183h			
0184h	DMA0 Destination Pointer	DAR0	XXh
0185h			XXh
0186h			0Xh
0187h			
0188h	DMA0 Transfer Counter	TCR0	XXh
0189h			XXh
018Ah			
018Bh			
018Ch	DMA0 Control Register	DM0CON	0000 0X00b
018Dh			
018Eh			
018Fh			
0190h	DMA1 Source Pointer	SAR1	XXh
0191h			XXh
0192h			0Xh
0193h			
0194h	DMA1 Destination Pointer	DAR1	XXh
0195h			XXh
0196h			0Xh
0197h			
0198h	DMA1 Transfer Counter	TCR1	XXh
0199h			XXh
019Ah			
019Bh			
019Ch	DMA1 Control Register	DM1CON	0000 0X00b
019Dh			
019Eh			
019Fh			
01A0h	DMA2 Source Pointer	SAR2	XXh
01A1h			XXh
01A2h			0Xh
01A3h			
01A4h	DMA2 Destination Pointer	DAR2	XXh
01A5h			XXh
01A6h			0Xh
01A7h			
01A8h	DMA2 Transfer Counter	TCR2	XXh
01A9h			XXh
01AAh			
01ABh			
01ACh	DMA2 Control Register	DM2CON	0000 0X00b
01ADh			
01AEh			
01AFh			

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.9 SFR Information (9) (1)

Address	Register	Symbol	Reset Value
0240h			
0241h			
0242h			
0243h			
0244h	UART0 Special Mode Register 4	U0SMR4	00h
0245h	UART0 Special Mode Register 3	U0SMR3	000X 0X0Xb
0246h	UART0 Special Mode Register 2	U0SMR2	X000 0000b
0247h	UART0 Special Mode Register	U0SMR	X000 0000b
0248h	UART0 Transmit/Receive Mode Register	U0MR	00h
0249h	UART0 Bit Rate Register	U0BRG	XXh
024Ah	UART0 Transmit Buffer Register	U0TB	XXh
024Bh			XXh
024Ch	UART0 Transmit/Receive Control Register 0	U0C0	0000 1000b
024Dh	UART0 Transmit/Receive Control Register 1	U0C1	00XX 0010b
024Eh	UART0 Receive Buffer Register	U0RB	XXh
024Fh			XXh
0250h	UART Transmit/Receive Control Register 2	UCON	X000 0000b
0251h			
0252h	UART Clock Select Register	UCLKSEL0	X0h
0253h			
0254h	UART1 Special Mode Register 4	U1SMR4	00h
0255h	UART1 Special Mode Register 3	U1SMR3	000X 0X0Xb
0256h	UART1 Special Mode Register 2	U1SMR2	X000 0000b
0257h	UART1 Special Mode Register	U1SMR	X000 0000b
0258h	UART1 Transmit/Receive Mode Register	U1MR	00h
0259h	UART1 Bit Rate Register	U1BRG	XXh
025Ah	UART1 Transmit Buffer Register	U1TB	XXh
025Bh			XXh
025Ch	UART1 Transmit/Receive Control Register 0	U1C0	0000 1000b
025Dh	UART1 Transmit/Receive Control Register 1	U1C1	00XX 0010b
025Eh	UART1 Receive Buffer Register	U1RB	XXh
025Fh			XXh
0260h			
0261h			
0262h			
0263h			
0264h	UART2 Special Mode Register 4	U2SMR4	00h
0265h	UART2 Special Mode Register 3	U2SMR3	000X 0X0Xb
0266h	UART2 Special Mode Register 2	U2SMR2	X000 0000b
0267h	UART2 Special Mode Register	U2SMR	X000 0000b
0268h	UART2 Transmit/Receive Mode Register	U2MR	00h
0269h	UART2 Bit Rate Register	U2BRG	XXh
026Ah	UART2 Transmit Buffer Register	U2TB	XXh
026Bh			XXh
026Ch	UART2 Transmit/Receive Control Register 0	U2C0	0000 1000b
026Dh	UART2 Transmit/Receive Control Register 1	U2C1	0000 0010b
026Eh	UART2 Receive Buffer Register	U2RB	XXh
026Fh			XXh

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.11 SFR Information (11) (1)

Address	Register	Symbol	Reset Value
02A0h			
02A1h			
02A2h			
02A3h			
02A4h	UART7 Special Mode Register 4	U7SMR4	00h
02A5h	UART7 Special Mode Register 3	U7SMR3	000X 0X0Xb
02A6h	UART7 Special Mode Register 2	U7SMR2	X000 0000b
02A7h	UART7 Special Mode Register	U7SMR	X000 0000b
02A8h	UART7 Transmit/Receive Mode Register	U7MR	00h
02A9h	UART7 Bit Rate Register	U7BRG	XXh
02AAh	UART7 Transmit Buffer Register	U7TB	XXh
02ABh			XXh
02ACh	UART7 Transmit/Receive Control Register 0	U7C0	0000 1000b
02ADh	UART7 Transmit/Receive Control Register 1	U7C1	0000 0010b
02AEh	UART7 Receive Buffer Register	U7RB	XXh
02AFh			XXh
02B0h	I2C0 Data Shift Register	S00	XXh
02B1h			
02B2h	I2C0 Address Register 0	S0D0	0000 000Xb
02B3h	I2C0 Control Register 0	S1D0	00h
02B4h	I2C0 Clock Control Register	S20	00h
02B5h	I2C0 Start/Stop Condition Control Register	S2D0	0001 1010b
02B6h	I2C0 Control Register 1	S3D0	0011 0000b
02B7h	I2C0 Control Register 2	S4D0	00h
02B8h	I2C0 Status Register 0	S10	0001 000Xb
02B9h	I2C0 Status Register 1	S11	XXXX X000b
02BAh	I2C0 Address Register 1	S0D1	0000 000Xb
02BBh	I2C0 Address Register 2	S0D2	0000 000Xb
02BCh			
02BDh			
02BEh			
02BFh			
02C0h to 02FFh			

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

5.1.5 Flash Memory Electrical Characteristics

Table 5.8 CPU Clock When Operating Flash Memory ($f_{(BCLK)}$)

V_{CC1} = 2.7 to 5.5 V, T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified.

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
-	CPU rewrite mode				10 (1)	MHz
f(SLOW_R)	Slow read mode				5 (3)	MHz
-	Low current consumption read mode			fC(32.768)	35	kHz
-	Data flash read	2.7 V ≤ V_{CC1} ≤ 3.0 V			16 (2)	MHz
		3.0 V < V_{CC1} ≤ 5.5 V			20 (2)	MHz

Notes:
1. Set the PM17 bit in the PM1 register to 1 (one wait).
2. When the frequency is over this value, set the FMR17 bit in the FMR1 register to 0 (one wait) or the PM17 bit in the PM1 register to 1 (one wait)
3. Set the PM17 bit in the PM1 register to 1 (one wait). When using 125 kHz on-chip oscillator clock or sub clock as the CPU clock source, a wait is not necessary.

Table 5.9 Flash Memory (Program ROM 1, 2) Electrical Characteristics

V_{CC1} = 2.7 to 5.5 V at T_{opr} = 0°C to 60°C (option: -40°C to 85°C), unless otherwise specified.

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
-	Program and erase cycles (1), (3), (4)	V_{CC1} = 3.3 V, T_{opr} = 25°C	1,000 (2)			times
-	2 word program time	V_{CC1} = 3.3 V, T_{opr} = 25°C		150	4000	µs
-	Lock bit program time	V_{CC1} = 3.3 V, T_{opr} = 25°C		70	3000	µs
-	Block erase time	V_{CC1} = 3.3 V, T_{opr} = 25°C		0.2	3.0	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend				$5 + \frac{3}{f_{(BCLK)}}$	ms
-	Interval from erase start/restart until following suspend request		0			µs
-	Suspend interval necessary for auto-erasure to complete (7)		20			ms
-	Time from suspend until erase restart				$30 + \frac{1}{f_{(BCLK)}}$	µs
-	Program, erase voltage		2.7		5.5	V
-	Read voltage	T_{opr}= -20°C to 85°C/-40°C to 85°C	2.7		5.5	V
-	Program, erase temperature		0		60	°C
t_{PS}	Flash memory circuit stabilization wait time				50	µs
-	Data hold time (6)	Ambient temperature = 55°C	20			year

Notes:
1. Definition of program and erase cycles:
   The program and erase cycles refer to the number of per-block erasures. If the program and erase cycles are n (n = 1,000), each block can be erased n times. For example, if a block is erased after writing 2 word data 16,384 times, each to a different address, this counts as one program and erase cycles. Data cannot be written to the same address more than once without erasing the block (rewrite prohibited).
2. Cycles to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
3. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. It is advisable to retain data on the erasure cycles of each block and limit the number of erase operations to a certain number.
4. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
5. Customers desiring program/erase failure rate information should contact a Renesas Electronics sales office.
6. The data hold time includes time that the power supply is off or the clock is not supplied.
7. After an erase start or erase restart, if an interval of at least 20 ms is not set before the next suspend request, the erase sequence cannot be completed.

5.1.6 Voltage Detector and Power Supply Circuit Electrical Characteristics

Table 5.11 Voltage Detector 0 Electrical Characteristics

The measurement condition is V_{CC1} = 2.7 to 5.5 V, T_{opr} = -20°C to 85°C/-40°C to 85°C, unless otherwise specified.

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det0}	Voltage detection level Vdet0_0 (1)	When V_{CC1} is falling.	1.80	1.90	2.10	V
	Voltage detection level Vdet0_2 (1)	When V_{CC1} is falling.	2.70	2.85	3.00	V
-	Voltage detector 0 response time (3)	When V_{CC1} falls from 5 V to (Vdet0_0 - 0.1) V			200	µs
-	Voltage detector self power consumption	VC25 = 1, V_{CC1} = 5.0 V		1.5		µA
$t_{d(E-A)}$	Waiting time until voltage detector operation starts (2)				100	µs

Notes:
1. Select the voltage detection level with the VDSEL1 bit in the OFS1 address.
2. Necessary time until the voltage detector operates when setting to 1 again after setting the VC25 bit in the VCR2 register to 0.
3. Time from when passing the V_{det0} until when a voltage monitor 0 reset is generated.

Table 5.12 Voltage Detector 1 Electrical Characteristics

The measurement condition is V_{CC1} = 2.7 to 5.5 V, T_{opr} = -20°C to 85°C/-40°C to 85°C, unless otherwise specified.

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det1}	Voltage detection level Vdet1_6 (1)	When V_{CC1} is falling.	2.80	3.10	3.40	V
	Voltage detection level Vdet1_B (1)	When V_{CC1} is falling.	3.55	3.85	4.15	V
	Voltage detection level Vdet1_F (1)	When V_{CC1} is falling.	4.15	4.45	4.75	V
-	Hysteresis width when V_{CC1} of voltage detector 1 is rising			0.15		V
-	Voltage detector 1 response time (3)	When V_{CC1} falls from 5 V to (Vdet1_0 - 0.1) V			200	µs
-	Voltage detector self power consumption	VC26 = 1, V_{CC1} = 5.0 V		1.7		µA
$t_{d(E-A)}$	Waiting time until voltage detector operation starts (2)				100	µs

Notes:
1. Select the voltage detection level with bits VD1S0 to VD1S3 in the VD1LS register.
2. Necessary time until the voltage detector operates when setting to 1 again after setting the VC26 bit in the VCR2 register to 0.
3. Time from when passing the V_{det1} until when a voltage monitor 1 reset is generated.

$V_{CC1} = V_{CC2} = 5\ V$

Table 5.19 Electrical Characteristics (2) (1)

$V_{CC1} = V_{CC2} = 4.2$ to 5.5 V, $V_{SS} = 0$ V at $T_{opr} = -20°C$ to 85°C/–40°C to 85°C, $f_{(BCLK)}$ = 32 MHz unless otherwise specified.

Symbol	Parameter		Measuring Condition	Standard			Unit
				Min.	Typ.	Max.	
$V_{T+} - V_{T-}$	Hysteresis	$\overline{HOLD}$, $\overline{RDY}$, TA0IN to TA4IN, TB0IN to TB5IN, $\overline{INT0}$ to $\overline{INT7}$, $\overline{NMI}$, $\overline{ADTRG}$, $\overline{CTS0}$ to $\overline{CTS2}$, $\overline{CTS5}$ to $\overline{CTS7}$, SCL0 to SCL2, SCL5 to SCL7, SDA0 to SDA2, SDA5 to SDA7, CLK0 to CLK7, TA0OUT to TA4OUT, $\overline{KI0}$ to $\overline{KI3}$, RXD0 to RXD2, RXD5 to RXD7, SIN3, SIN4, $\overline{SD}$, PMC0, PMC1, SCLMM, SDAMM, CEC, ZP, IDU, IDV, IDW		0.5		2.0	V
$V_{T+} - V_{T-}$	Hysteresis	$\overline{RESET}$		0.5		2.5	V
I_{IH}	High input current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1 XIN, $\overline{RESET}$, CNVSS, BYTE	V_I = 5 V			5.0	µA
I_{IL}	Low input current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1 XIN, $\overline{RESET}$, CNVSS, BYTE	V_I = 0 V			–5.0	µA
R_{PULLUP}	Pull-up resistance	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1	V_I = 0 V	30	50	100	kΩ
R_{fXIN}	Feedback resistance XIN				1.5		MΩ
V_{RAM}	RAM retention voltage		In stop mode	1.8			V

Note:
1. When $V_{CC1} \neq V_{CC2}$, refer to 5 V or 3 V standard depending on the voltage.

$V_{CC1} = V_{CC2} = 5\ V$

Table 5.21 Electrical Characteristics (4)

R5F3651ECNFC, R5F3651KCNFC, R5F3650KCNFA, R5F3650KCNFB, R5F3651MCNFC, R5F3650MCNFA, R5F3650MCNFB, R5F3651NCNFC, R5F3650NCNFA, R5F3650NCNFB, R5F3651ECDFC, R5F3651KCDFC, R5F3650KCDFA, R5F3650KCDFB, R5F3651MCDFC, R5F3650MCDFA, R5F3650MCDFB, R5F3651NCDFC, R5F3650NCDFA, R5F3650NCDFB

$V_{CC1} = V_{CC2} = 4.2$ to 5.5 V, $V_{SS} = 0$ V at $T_{opr} = -20°C$ to 85°C/−40°C to 85°C, $f_{(BCLK)} = 32$ MHz unless otherwise specified.

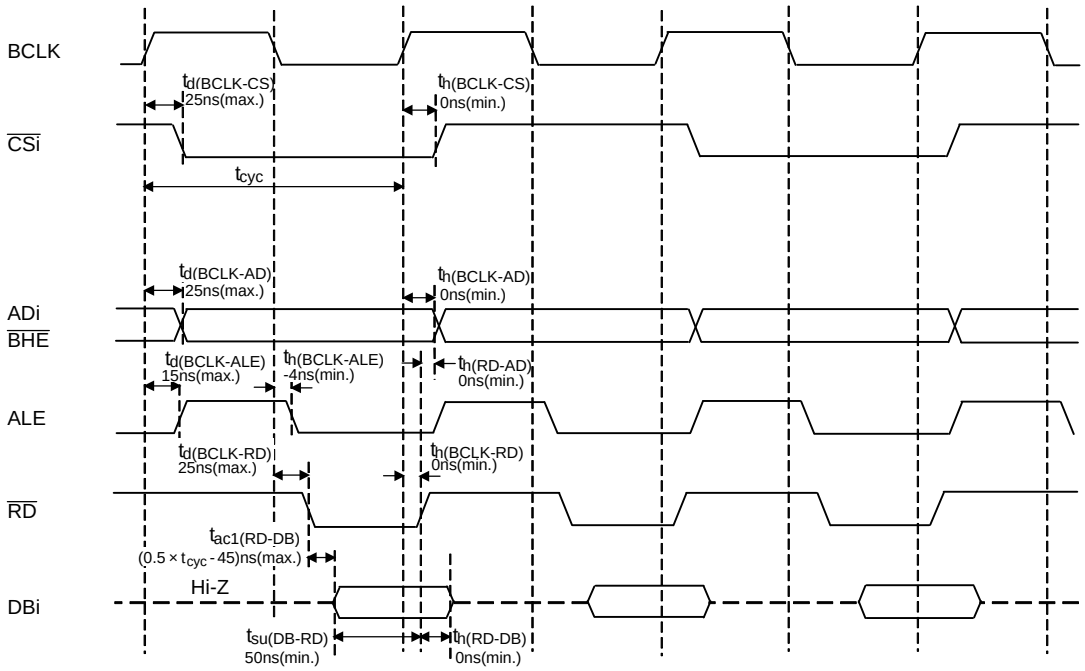
Symbol	Parameter	Measuring Condition		Standard			Unit
				Min.	Typ.	Max.	
R_{fXCIN}	Feedback resistance XCIN				8		MΩ
I_{CC}	Power supply current In single-chip, mode, the output pin are open and other pins are V_{SS}	High-speed mode	$f_{(BCLK)}$ = 32 MHz XIN = 4 MHz (square wave), PLL multiplied by 8 125 kHz on-chip oscillator stopped		26.0		mA
			$f_{(BCLK)}$ = 32 MHz, A/D conversion XIN = 4 MHz (square wave), PLL multiplied by 8 125 kHz on-chip oscillator stopped		27.0		mA
			$f_{(BCLK)}$ = 20 MHz XIN = 20 MHz (square wave) 125 kHz on-chip oscillator stopped		17.0		mA
		40 MHz on-chip oscillator mode	Main clock stopped 40 MHz on-chip oscillator on, divide-by-4 (f(BCLK) = 10 MHz) 125 kHz on-chip oscillator stopped		18.0		mA
		125 kHz on-chip oscillator mode	Main clock stopped 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator on, no division FMR22 = 1 (slow read mode)		550.0		μA
		Low-power mode	$f_{(BCLK)}$ = 32 kHz In low-power mode FMR22 = FMR23 = 1 on flash memory (1)		170.0		μA
			$f_{(BCLK)}$ = 32 kHz In low-power mode on RAM (1)		45.0		μA
		Wait mode	Main clock stopped 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator on Peripheral clock operating T_{opr} = 25°C		20.5		μA
			$f_{(BCLK)}$ = 32 kHz (oscillation capacity High) 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator stopped Peripheral clock operating T_{opr} = 25°C		11.0		μA
			$f_{(BCLK)}$ = 32 kHz (oscillation capacity low) 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator stopped Peripheral clock operating T_{opr} = 25°C		6.0		μA
			XIN = 6 MHz 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator stopped Peripheral clock f1 provision disabled except timers (PCKSTP1A = 1) Main clock as a timer clock source (PCKSTP11 = 0, PCKSTP17 = 1) A given timer operating		1.2		mA
		Stop mode	Main clock stopped 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator stopped Peripheral clock stopped T_{opr} = 25°C		1.7		μA
		During flash memory program	$f_{(BCLK)}$ = 10 MHz, PM17 = 1 (one wait) V_{CC1} = 5.0 V		20.0		mA
		During flash memory erase	$f_{(BCLK)}$ = 10 MHz, PM17 = 1 (one wait) V_{CC1} = 5.0 V		30.0		mA

Note:
1. This indicates the memory in which the program to be executed exists.

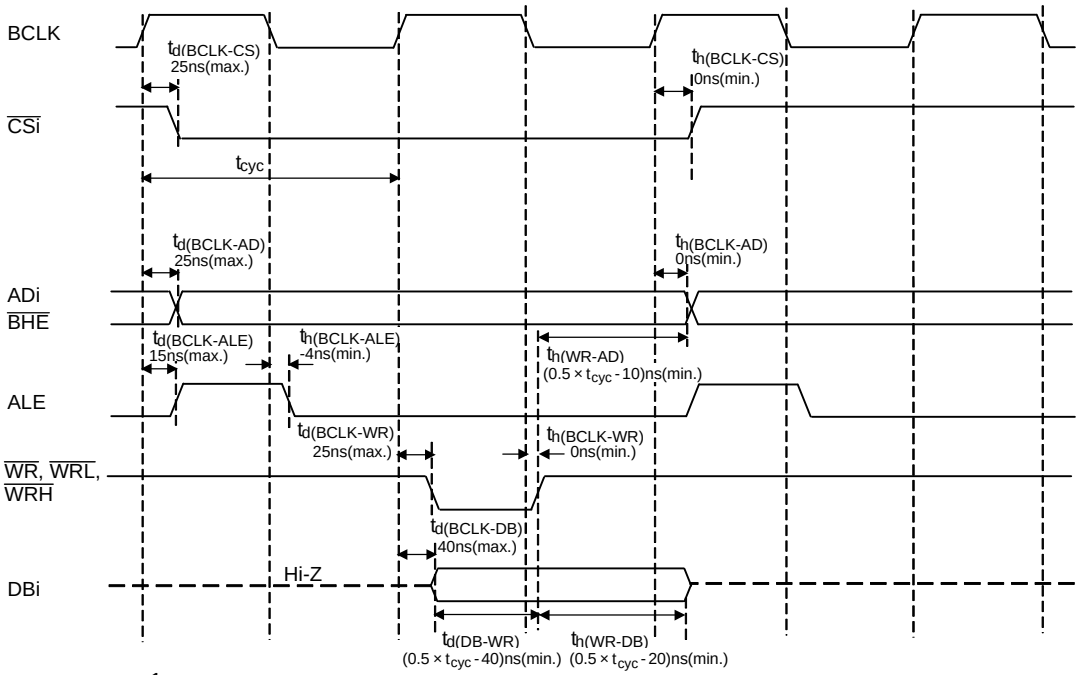
Memory Expansion Mode and Microprocessor Mode
(in no wait state setting)

$V_{CC1} = V_{CC2} = 5V$

Read timing



Write timing



$$t_{cyc} = \frac{1}{f_{(BCLK)}}$$

Measuring conditions

- $V_{CC1} = V_{CC2} = 5V$
- Input timing voltage: $V_{IL} = 0.8$ V, $V_{IH} = 2.0$ V
- Output timing voltage: $V_{OL} = 0.4$ V, $V_{OH} = 2.4$ V

Figure 5.15 Timing Diagram

$V_{CC1} = V_{CC2} = 5\ V$

Switching Characteristics

($V_{CC1} = V_{CC2} = 5$ V, $V_{SS} = 0$ V, at T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified)

5.2.4.3 In 2 or 3 Waits Setting, and When Accessing External Area and Using Multiplexed Bus

Table 5.38 Memory Expansion Mode and Microprocessor Mode (in 2 or 3 Waits Setting, and When Accessing External Area and Using Multiplexed Bus) (5)

Symbol	Parameter	Measuring Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	See Figure 5.14		25	ns
$t_{h(BCLK-AD)}$	Address output hold time (in relation to BCLK)		0		ns
$t_{h(RD-AD)}$	Address output hold time (in relation to RD)		(Note 1)		ns
$t_{h(WR-AD)}$	Address output hold time (in relation to WR)		(Note 1)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			25	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (in relation to BCLK)		0		ns
$t_{h(RD-CS)}$	Chip select output hold time (in relation to RD)		(Note 1)		ns
$t_{h(WR-CS)}$	Chip select output hold time (in relation to WR)		(Note 1)		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			25	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			25	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (in relation to BCLK)			40	ns
$t_{d(DB-WR)}$	Data output delay time (in relation to WR)		(Note 2)		ns
$t_{h(WR-DB)}$	Data output hold time (in relation to WR)		(Note 6)		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time (in relation to BCLK)			15	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time (in relation to BCLK)		–4		ns
$t_{d(AD-ALE)}$	ALE signal output delay time (in relation to Address)		(Note 3)		ns
$t_{h(AD-ALE)}$	ALE signal output hold time (in relation to Address)		(Note 4)		ns
$t_{d(AD-RD)}$	RD signal output delay from the end of address		0		ns
$t_{d(AD-WR)}$	WR signal output delay from the end of address		0		ns
$t_{dz(RD-AD)}$	Address output floating start time			8	ns

Notes:

1. Calculated according to the BCLK frequency as follows:
$$\frac{0.5 \times 10^9}{f_{(BCLK)}} - 10[ns]$$
2. Calculated according to the BCLK frequency as follows:
$$\frac{(n - 0.5) \times 10^9}{f_{(BCLK)}} - 40[ns]$$
n is 2 for 2-wait setting, 3 for 3-wait setting.
3. Calculated according to the BCLK frequency as follows:
$$\frac{0.5 \times 10^9}{f_{(BCLK)}} - 25[ns]$$
4. Calculated according to the BCLK frequency as follows:
$$\frac{0.5 \times 10^9}{f_{(BCLK)}} - 15[ns]$$
5. When using multiplex bus, set $f_{(BCLK)}$ 12.5 MHz or less.
6. Calculated according to the BCLK frequency as follows: $\frac{0.5 \times 10^9}{f_{(BCLK)}} - 20[ns]$

$V_{CC1} = V_{CC2} = 3\ V$

5.3.4 Switching Characteristics (Memory Expansion Mode and Microprocessor Mode)

($V_{CC1} = V_{CC2} = 3$ V, $V_{SS} = 0$ V, at T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified)

5.3.4.1 In No Wait State Setting

Table 5.59 Memory Expansion and Microprocessor Modes (in No Wait State Setting)

Symbol	Parameter	Measuring Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	See Figure 5.29		30	ns
$t_{h(BCLK-AD)}$	Address output hold time (in relation to BCLK)		0		ns
$t_{h(RD-AD)}$	Address output hold time (in relation to RD)		0		ns
$t_{h(WR-AD)}$	Address output hold time (in relation to WR)		(Note 2)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			30	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (in relation to BCLK)		0		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time			25	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time		–4		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			30	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			30	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (in relation to BCLK)			40	ns
$t_{d(DB-WR)}$	Data output delay time (in relation to WR)		(Note 1)		ns
$t_{h(WR-DB)}$	Data output hold time (in relation to WR) (3)		(Note 4)		ns

Notes:

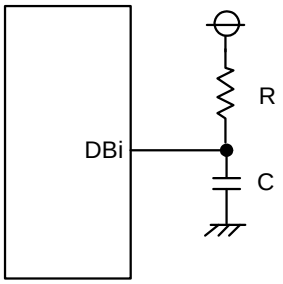
1. Calculated according to the BCLK frequency as follows:

   $\frac{0.5 \times 10^9}{f_{(BCLK)}} - 40[ns]$ $f_{(BCLK)}$ is 12.5 MHz or less.

2. Calculated according to the BCLK frequency as follows:

   $\frac{0.5 \times 10^9}{f_{(BCLK)}} - 15[ns]$

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.
   Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.
   Hold time of data bus is expressed in
   $t = -CR \times \ln(1 - V_{OL}/V_{CC2})$
   by a circuit of the right figure.
   For example, when $V_{OL} = 0.2V_{CC2}$, C = 30 pF, R = 1 kΩ,
   hold time of output low level is
   $t = -30\ pF \times 1\ k\Omega \times \ln(1 - 0.2V_{CC2}/V_{CC2})$
   = 6.7 ns.



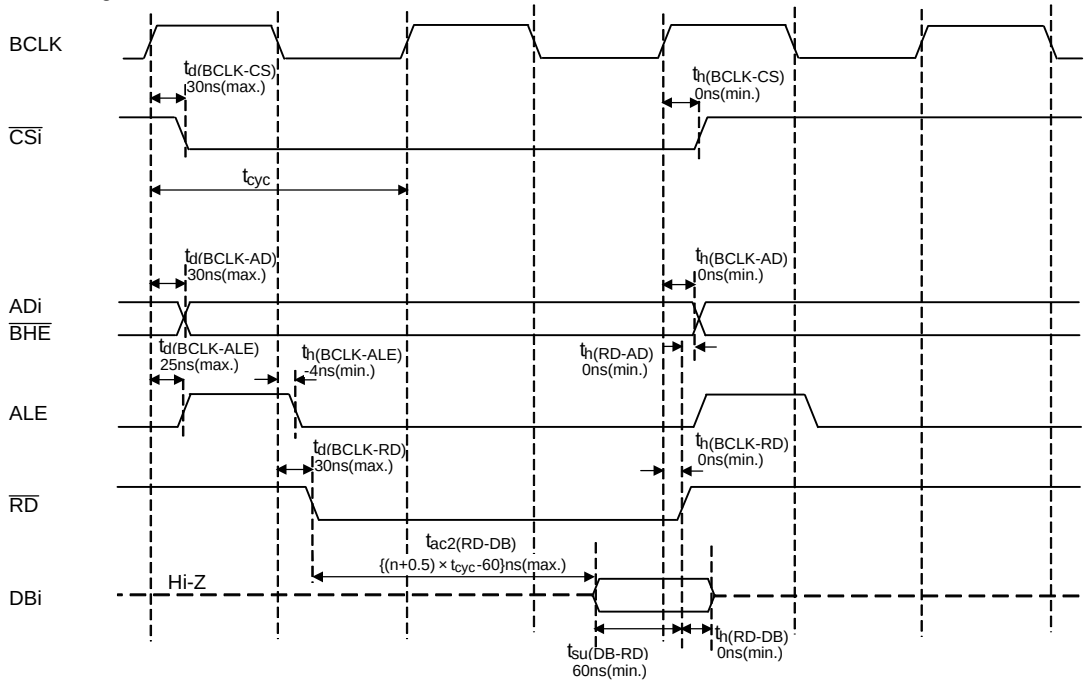
4. Calculated according to the BCLK frequency as follows:

   $\frac{0.5 \times 10^9}{f_{(BCLK)}} - 25[ns]$
   Hold time is equal to or less than 0 ns when the BCLK frequency exceeds 20 MHz.

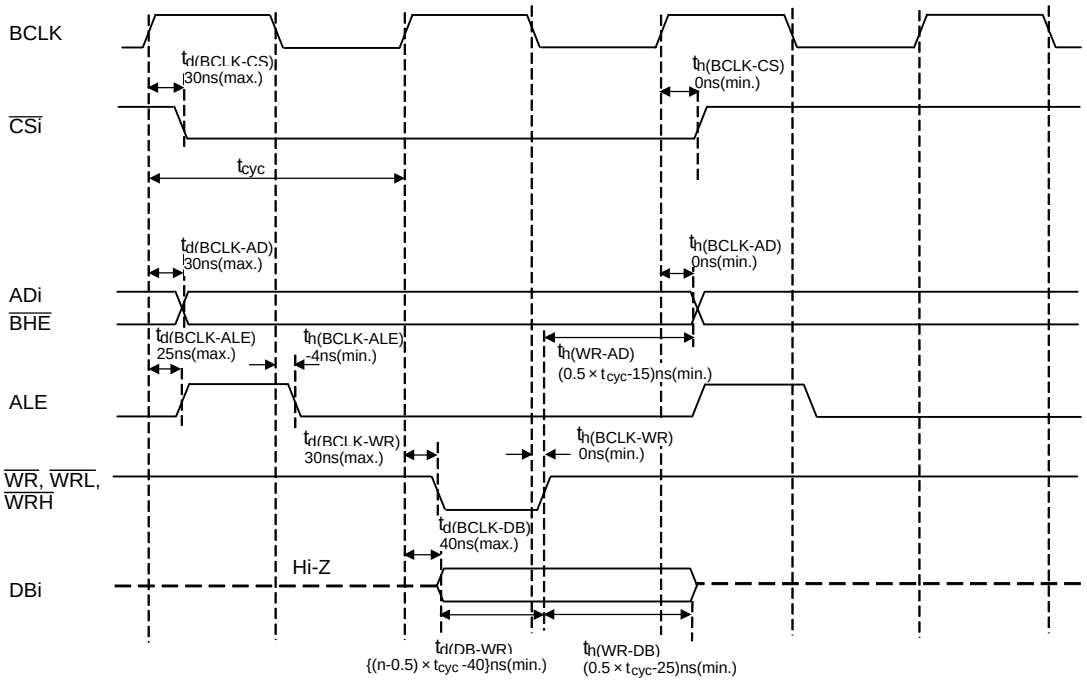
Memory Expansion Mode and Microprocessor Mode
(in 1 to 3 waits setting and when accessing external area)

$V_{CC1} = V_{CC2} = 3V$

Read timing



Write timing



$$t_{cyc} = \frac{1}{f_{(BCLK)}}$$

Measuring conditions

- $V_{CC1} = V_{CC2} = 3V$
- Input timing voltage: $V_{IL} = 0.6$ V, $V_{IH} = 2.4$ V
- Output timing voltage: $V_{OL} = 1.5$ V, $V_{OH} = 1.5$ V

n: 1 (when 1 wait)
2 (when 2 waits)
3 (when 3 waits)

Figure 5.31 Timing Diagram

$V_{CC1} = V_{CC2} = 3\ V$

Switching Characteristics

($V_{CC1} = V_{CC2} = 3\ V$, $V_{SS} = 0\ V$, at T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified)

5.3.4.5 In Wait State Setting 2φ + 3φ, 2φ + 4φ, 3φ + 4φ, and 4φ + 5φ, and Inserting 1 to 3 Recovery Cycles and Accessing External Area

Table 5.63 Memory Expansion Mode and Microprocessor Mode (in Wait State Setting 2φ + 3φ, 2φ + 4φ, 3φ + 4φ, and 4φ + 5φ, and Inserting 1 to 3 Recovery Cycles and Accessing External Area)

Symbol	Parameter	Measuring Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	See Figure 5.29		30	ns
$t_{h(BCLK-AD)}$	Address output hold time (in relation to BCLK)		0		ns
$t_{h(RD-AD)}$	Address output hold time (in relation to RD)		(Note 4)		ns
$t_{h(WR-AD)}$	Address output hold time (in relation to WR)		(Note 2)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			30	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (in relation to BCLK)		0		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time			25	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time		-4		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			30	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			30	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (in relation to BCLK)			40	ns
$t_{d(DB-WR)}$	Data output delay time (in relation to WR)		(Note 1)		ns
$t_{h(WR-DB)}$	Data output hold time (in relation to WR) (3)		(Note 5)		ns

Notes:

1. Calculated according to the BCLK frequency as follows:

$$\frac{n \times 10^9}{f_{(BCLK)}} - 40[ns]$$

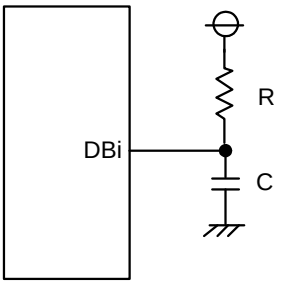
n is 3 for 2φ + 3φ, 4 for 2φ + 4φ, 4 for 3φ + 4φ, and 5 for 4φ + 5φ.

2. Calculated according to the BCLK frequency as follows:

$$\frac{m \times 10^9}{f_{(BCLK)}} - 15[ns]$$

m is 1 when 1 recovery cycle is inserted, 2 when 2 recovery cycles are inserted, and 3 when 3 recovery cycles are inserted.

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.
Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.
Hold time of data bus is expressed in
$t = -CR \times \ln(1 - V_{OL}/V_{CC2})$
by a circuit of the right figure.
For example, when $V_{OL} = 0.2V_{CC2}$, C = 30 pF, R = 1 kΩ, hold time of output low level is
$t = -30\ pF \times 1\ k\Omega \times \ln(1 - 0.2V_{CC2}/V_{CC2})$
= 6.7 ns.



4. Calculated according to the BCLK frequency as follows:

$$\frac{m \times 10^9}{f_{(BCLK)}} + 0[ns]$$

m is 1 when 1 recovery cycle is inserted, 2 when 2 recovery cycles are inserted, and 3 when 3 recovery cycles are inserted.

5. Calculated according to the BCLK frequency as follows:

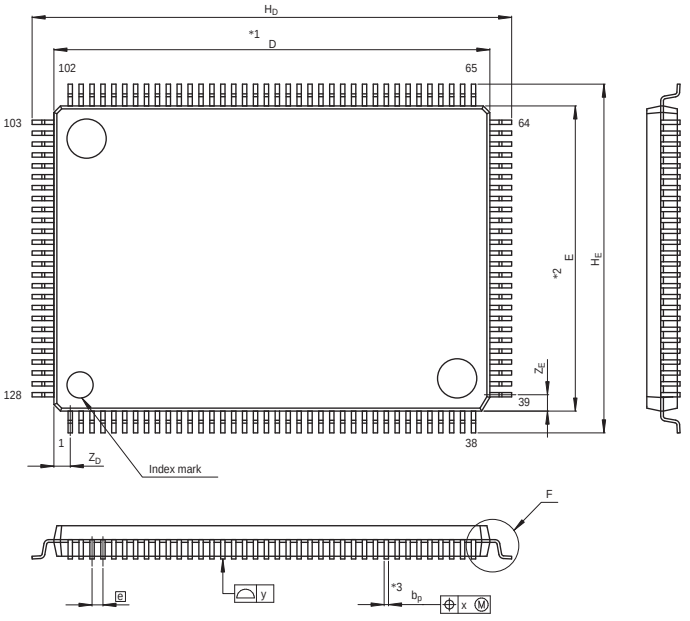
$$\frac{m \times 10^9}{f_{(BCLK)}} - 25[ns]$$

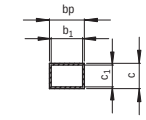
m is 1 when 1 recovery cycle is inserted, 2 when 2 recovery cycles are inserted, and 3 when 3 recovery cycles are inserted.

Appendix 1. Package Dimensions

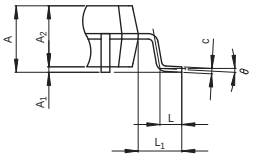
The information on the latest package dimensions or packaging may be obtained from “Packages“ on the Renesas Electronics website.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP128-14x20-0.50	PLQP0128KB-A	128P6Q-A	0.9g





Terminal cross section

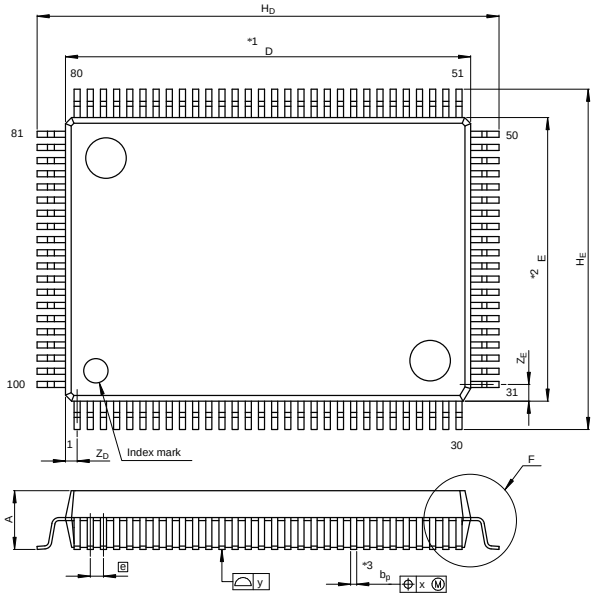


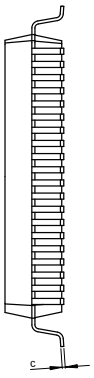
DetailF

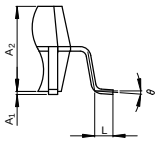
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	19.9	20.0	20.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	21.8	22.0	22.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	0.125	0.2
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.10
y	—	—	0.10
Z_D	—	0.75	—
Z_E	—	0.75	—
L	0.35	0.5	0.65
L_1	—	1.0	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-QFP100-14x20-0.65	PRQP0100JD-B	100P6F-A	1.8g







Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	19.8	20.0	20.2
E	13.8	14.0	14.2
A_2	—	2.8	—
H_D	22.5	22.8	23.1
H_E	16.5	16.8	17.1
A	—	—	3.05
A_1	0	0.1	0.2
b_p	0.25	0.3	0.4
c	0.13	0.15	0.2
θ	0°	—	10°
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z_D	—	0.575	—
Z_E	—	0.825	—
L	0.4	0.6	0.8

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.