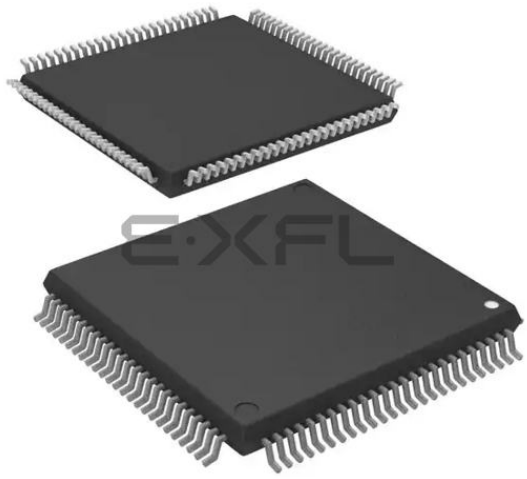
Renesas Electronics America Inc - R5F3650KCDFB#V0 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M16C/60
Core Size	16-Bit
Speed	32MHz
Connectivity	EBI/EMI, I²C, SIO, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	85
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	31K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f3650kcdfb-v0

Table 1.2 Specifications for the 128-Pin Package (2/2)

Item	Function	Description
Timers	Timer A	16-bit timer × 5 Timer mode, event counter mode, one-shot timer mode, pulse width modulation (PWM) mode Event counter two-phase pulse signal processing (two-phase encoder input) × 3 Programmable output mode × 3
	Timer B	16-bit timer × 6 Timer mode, event counter mode, pulse period measurement mode, pulse width measurement mode
	Three-phase motor control timer functions	• Three-phase inverter control (timer A1, timer A2, timer A4, timer B2) • On-chip dead time timer
	Real-time clock	Count: seconds, minutes, hours, days of the week
	PWM function	8 bits × 2
	Remote control signal receiver	• 2 circuits • 4 wave pattern matchings (differentiate wave pattern for headers, data 0, data 1, and special data) • 6-byte receive buffer (1 circuit only) • Operating frequency of 32 kHz
Serial Interface	UART0 to UART2, UART5 to UART7	Clock synchronous/asynchronous × 6 channels I^2C-bus, IEBus, special mode 2 SIM (UART2)
	SI/O3, SI/O4	Clock synchronization only × 2 channels
Multi-master I^2C-bus Interface		1 channel
CEC Functions (2)		CEC transmit/receive, arbitration lost detection, ACK automatic output, operation frequency of 32 kHz
A/D Converter		10-bit resolution × 26 channels, including sample and hold function Conversion time: 1.72 µs
D/A Converter		8-bit resolution × 2 circuits
CRC Calculator		CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$), CRC-16 ($X^{16} + X^{15} + X^2 + 1$) compliant
Flash Memory		• Program and erase power supply voltage: 2.7 to 5.5 V • Program and erase cycles: 1,000 times (program ROM 1, program ROM 2), 10,000 times (data flash) • Program security: ROM code protect, ID code check
Debug Functions		On-chip debug, on-board flash rewrite, address match interrupt × 4
Operation Frequency/Supply Voltage		32 MHz/VCC1 = 2.7 to 5.5 V, VCC2 = 2.7 V to VCC1
Current Consumption		Refer to the Electrical Characteristics chapter
Operating Temperature		-20°C to 85°C, -40°C to 85°C (1)
Package		128-pin LQFP: PLQP0128KB-A (Previous package code: 128P6Q-A)

Notes:
1. See Table 1.5 “Product List (N-Version)” to Table 1.6 “Product List (D-Version)” for the operating temperature.
2. The CEC function indicates circuitry which supports the transmission and reception of CEC signals standardized by the High-Definition Multimedia Interface (HDMI). HDMI and High-Definition Multimedia Interface are registered trademarks of HDMI Licensing, LLC.

1.3 Product List

Table 1.5 and Table 1.6 list product information. Figure 1.1 shows the Part No., with Memory Size and Package, and Figure 1.2 shows the Marking Diagram (Top View).

Table 1.5 Product List (N-Version) As of July, 2012

Part No.	ROM Capacity			RAM Capacity	Package Code	Remarks
	Program ROM 1	Program ROM 2	Data flash			
R5F36506CNFA	128 KB	16 KB	4 KB × 2 blocks	12 KB	PRQP0100JD-B	Operating temperature -20°C to 85°C
R5F36506CNFB					PLQP0100KB-A	
R5F3651ECNFC	256 KB	16 KB	4 KB × 2 blocks	20 KB	PLQP0128KB-A	
R5F3650ECNFA					PRQP0100JD-B	
R5F3650ECNFB					PLQP0100KB-A	
R5F3651KCNFC	384 KB	16 KB	4 KB × 2 blocks	31 KB	PLQP0128KB-A	
R5F3650KCNFA					PRQP0100JD-B	
R5F3650KCNFB					PLQP0100KB-A	
R5F3651MCNFC	512 KB	16 KB	4 KB × 2 blocks	31 KB	PLQP0128KB-A	
R5F3650MCNFA					PRQP0100JD-B	
R5F3650MCNFB					PLQP0100KB-A	
R5F3651NCNFC	512 KB	16 KB	4 KB × 2 blocks	47 KB	PLQP0128KB-A	
R5F3650NCNFA					PRQP0100JD-B	
R5F3650NCNFB					PLQP0100KB-A	

(D): Under development
(P): Planning
Note:
1. Previous package codes are as follows:
PLQP0128KB-A: 128P6Q-A, PRQP0100JD-B: 100P6F-A, PLQP0100KB-A: 100P6Q-A

Table 1.6 Product List (D-Version) As of July, 2012

Part No.	ROM Capacity			RAM Capacity	Package Code	Remarks
	Program ROM 1	Program ROM 2	Data flash			
R5F36506CDFA	128 KB	16 KB	4 KB × 2 blocks	12 KB	PRQP0100JD-B	Operating temperature -40°C to 85°C
R5F36506CDFB					PLQP0100KB-A	
R5F3651ECDFC	256 KB	16 KB	4 KB × 2 blocks	20 KB	PLQP0128KB-A	
R5F3650ECDFA					PRQP0100JD-B	
R5F3650ECDFB					PLQP0100KB-A	
R5F3651KCDFC	384 KB	16 KB	4 KB × 2 blocks	31 KB	PLQP0128KB-A	
R5F3650KCDFA					PRQP0100JD-B	
R5F3650KCDFB					PLQP0100KB-A	
R5F3651MCDFC	512 KB	16 KB	4 KB × 2 blocks	31 KB	PLQP0128KB-A	
R5F3650MCDFA					PRQP0100JD-B	
R5F3650MCDFB					PLQP0100KB-A	
R5F3651NCDFC	512 KB	16 KB	4 KB × 2 blocks	47 KB	PLQP0128KB-A	
R5F3650NCDFA					PRQP0100JD-B	
R5F3650NCDFB					PLQP0100KB-A	

(D): Under development
(P): Planning
Note:
1. Previous package codes are as follows:
PLQP0128KB-A: 128P6Q-A, PRQP0100JD-B: 100P6F-A, PLQP0100KB-A: 100P6Q-A

1.6 Pin Functions

Table 1.12 Pin Functions for the 128-Pin Package (1/3)

Signal Name	Pin Name	I/O	Power Supply	Description
Power supply input	VCC1, VCC2, VSS	I	-	Apply 2.7 to 5.5 V to pins VCC1 and VCC2 (VCC1 ≥ VCC2), and 0 V to the VSS pin.
Analog power supply input	AVCC, AVSS	I	VCC1	This is the power supply for the A/D and D/A converters. Connect the AVCC pin to VCC1, and connect the AVSS pin to VSS.
Reset input	$\overline{\text{RESET}}$	I	VCC1	Driving this pin low resets the MCU.
CNVSS	CNVSS	I	VCC1	Input pin to switch processor modes. After a reset, to start operating in single-chip mode, connect the CNVSS pin to VSS via a resistor. To start operating in microprocessor mode, connect the pin to VCC1.
External data bus width select input	BYTE	I	VCC1	Input pin to select the data bus of the external area. The data bus is 16 bits when it is low and 8 bits when it is high. This pin must be fixed either high or low. Connect the BYTE pin to VSS in single-chip mode.
Bus control pins	D0 to D7	I/O	VCC2	Inputs or outputs data (D0 to D7) while accessing an external area with a separate bus.
	D8 to D15	I/O	VCC2	Inputs or outputs data (D8 to D15) while accessing an external area with a 16-bit separate bus.
	A0 to A19	O	VCC2	Outputs address bits A0 to A19.
	A0/D0 to A7/D7	I/O	VCC2	Inputs or outputs data (D0 to D7) and outputs address bits (A0 to A7) by timesharing, while accessing an external area with an 8-bit multiplexed bus.
	A1/D0 to A8/D7	I/O	VCC2	Inputs or outputs data (D0 to D7) and outputs address bits (A1 to A8) by timesharing, while accessing an external area with a 16-bit multiplexed bus.
	$\overline{\text{CS0}}$ to $\overline{\text{CS3}}$	O	VCC2	Outputs chip-select signals $\overline{\text{CS0}}$ to $\overline{\text{CS3}}$ to specify an external area.
	$\overline{\text{WRL}}$/$\overline{\text{WR}}$ $\overline{\text{WRH}}$/$\overline{\text{BHE}}$ $\overline{\text{RD}}$	O	VCC2	Outputs $\overline{\text{WRL}}$, $\overline{\text{WRH}}$, ($\overline{\text{WR}}$, $\overline{\text{BHE}}$), and $\overline{\text{RD}}$ signals. $\overline{\text{WRL}}$ and $\overline{\text{WRH}}$ can be switched with $\overline{\text{BHE}}$ and $\overline{\text{WR}}$. • $\overline{\text{WRL}}$, $\overline{\text{WRH}}$, and $\overline{\text{RD}}$ selected If the external data bus is 16 bits, data is written to an even address in an external area when $\overline{\text{WRL}}$ is driven low. Data is written to an odd address when $\overline{\text{WRH}}$ is driven low. Data is read when $\overline{\text{RD}}$ is driven low. • $\overline{\text{WR}}$, $\overline{\text{BHE}}$, and $\overline{\text{RD}}$ selected Data is written to an external area when $\overline{\text{WR}}$ is driven low. Data in an external area is read when $\overline{\text{RD}}$ is driven low. An odd address is accessed when $\overline{\text{BHE}}$ is driven low. Select $\overline{\text{WR}}$, $\overline{\text{BHE}}$, and $\overline{\text{RD}}$ when using an 8-bit external data bus.
	ALE	O	VCC2	Outputs an ALE signal to latch the address.
	$\overline{\text{HOLD}}$	I	VCC2	$\overline{\text{HOLD}}$ input is unavailable. Connect the $\overline{\text{HOLD}}$ pin to VCC2 via a resistor (pull-up).
	$\overline{\text{HLDA}}$	O	VCC2	In a hold state, $\overline{\text{HLDA}}$ outputs a low-level signal.
	$\overline{\text{RDY}}$	I	VCC2	The MCU bus is placed in wait state while the $\overline{\text{RDY}}$ pin is driven low.

Power supply: VCC2 is used to supply power to the external bus associated pins. The dual power supply configuration allows VCC2 to interface at a different voltage than VCC1.

2.1 Data Registers (R0, R1, R2, and R3)

R0, R1, R2, and R3 are 16-bit registers used for transfer, arithmetic, and logic operations. R0 and R1 can be split into upper (R0H/R1H) and lower (R0L/R1L) bits to be used separately as 8-bit data registers. R0 can be combined with R2, and R3 can be combined with R1 and be used as 32-bit data registers R2R0 and R3R1, respectively.

2.2 Address Registers (A0 and A1)

A0 and A1 are 16-bit registers used for indirect addressing, relative addressing, transfer, arithmetic, and logic operations. A0 can be combined with A1 and used as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register that is used for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the start address of a relocatable interrupt vector table.

2.5 Program Counter (PC)

The PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The USP and ISP stack pointers (SP) are each comprised of 16 bits. The U flag is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register used for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register that indicates the CPU state.

2.8.1 Carry Flag (C Flag)

The C flag retains a carry, borrow, or shift-out bit generated by the arithmetic/logic unit.

2.8.2 Debug Flag (D Flag)

The D flag is for debugging only. Set it to 0.

2.8.3 Zero Flag (Z Flag)

The Z flag becomes 1 when an arithmetic operation results in 0. Otherwise, it becomes 0.

2.8.4 Sign Flag (S Flag)

The S flag becomes 1 when an arithmetic operation results in a negative value. Otherwise, it becomes 0.

2.8.5 Register Bank Select Flag (B Flag)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is 1.

2.8.6 Overflow Flag (O Flag)

The O flag becomes 1 when an arithmetic operation results in an overflow. Otherwise, it becomes 0.

Table 4.3 SFR Information (3) (1)

Address	Register	Symbol	Reset Value
0040h			
0041h			
0042h	$\overline{\text{INT7}}$ Interrupt Control Register	INT7IC	XX00 X000b
0043h	$\overline{\text{INT6}}$ Interrupt Control Register	INT6IC	XX00 X000b
0044h	$\overline{\text{INT3}}$ Interrupt Control Register	INT3IC	XX00 X000b
0045h	Timer B5 Interrupt Control Register	TB5IC	XXXX X000b
0046h	Timer B4 Interrupt Control Register UART1 Bus Collision Detection Interrupt Control Register	TB4IC U1BCNIC	XXXX X000b
0047h	Timer B3 Interrupt Control Register UART0 Bus Collision Detection Interrupt Control Register	TB3IC U0BCNIC	XXXX X000b
0048h	SI/O4 Interrupt Control Register $\overline{\text{INT5}}$ Interrupt Control Register	S4IC INT5IC	XX00 X000b
0049h	SI/O3 Interrupt Control Register $\overline{\text{INT4}}$ Interrupt Control Register	S3IC INT4IC	XX00 X000b
004Ah	UART2 Bus Collision Detection Interrupt Control Register	BCNIC	XXXX X000b
004Bh	DMA0 Interrupt Control Register	DM0IC	XXXX X000b
004Ch	DMA1 Interrupt Control Register	DM1IC	XXXX X000b
004Dh	Key Input Interrupt Control Register	KUPIC	XXXX X000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXX X000b
004Fh	UART2 Transmit Interrupt Control Register	S2TIC	XXXX X000b
0050h	UART2 Receive Interrupt Control Register	S2RIC	XXXX X000b
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXX X000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXX X000b
0053h	UART1 Transmit Interrupt Control Register	S1TIC	XXXX X000b
0054h	UART1 Receive Interrupt Control Register	S1RIC	XXXX X000b
0055h	Timer A0 Interrupt Control Register	TA0IC	XXXX X000b
0056h	Timer A1 Interrupt Control Register	TA1IC	XXXX X000b
0057h	Timer A2 Interrupt Control Register	TA2IC	XXXX X000b
0058h	Timer A3 Interrupt Control Register	TA3IC	XXXX X000b
0059h	Timer A4 Interrupt Control Register	TA4IC	XXXX X000b
005Ah	Timer B0 Interrupt Control Register	TB0IC	XXXX X000b
005Bh	Timer B1 Interrupt Control Register	TB1IC	XXXX X000b
005Ch	Timer B2 Interrupt Control Register	TB2IC	XXXX X000b
005Dh	$\overline{\text{INT0}}$ Interrupt Control Register	INT0IC	XX00 X000b
005Eh	$\overline{\text{INT1}}$ Interrupt Control Register	INT1IC	XX00 X000b
005Fh	$\overline{\text{INT2}}$ Interrupt Control Register	INT2IC	XX00 X000b

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.6 SFR Information (6) (1)

Address	Register	Symbol	Reset Value
01B0h	DMA3 Source Pointer	SAR3	XXh
01B1h			XXh
01B2h			0Xh
01B3h			
01B4h	DMA3 Destination Pointer	DAR3	XXh
01B5h			XXh
01B6h			0Xh
01B7h			
01B8h	DMA3 Transfer Counter	TCR3	XXh
01B9h			XXh
01BAh			
01BBh			
01BCh	DMA3 Control Register	DM3CON	0000 0X00b
01BDh			
01BEh			
01BFh			
01C0h	Timer B0-1 Register	TB01	XXh
01C1h			XXh
01C2h	Timer B1-1 Register	TB11	XXh
01C3h			XXh
01C4h	Timer B2-1 Register	TB21	XXh
01C5h			XXh
01C6h	Pulse Period/Pulse Width Measurement Mode Function Select Register 1	PPWFS1	XXXX X000b
01C7h			
01C8h	Timer B Count Source Select Register 0	TBCS0	00h
01C9h	Timer B Count Source Select Register 1	TBCS1	X0h
01CAh			
01CBh	Timer AB Division Control Register 0	TCKDIVC0	0000 X000b
01CCh			
01CDh			
01CEh			
01CFh			
01D0h	Timer A Count Source Select Register 0	TACS0	00h
01D1h	Timer A Count Source Select Register 1	TACS1	00h
01D2h	Timer A Count Source Select Register 2	TACS2	X0h
01D3h			
01D4h	16-bit Pulse Width Modulation Mode Function Select Register	PWMFS	0XX0 X00Xb
01D5h	Timer A Waveform Output Function Select Register	TAPOFS	XXX0 0000b
01D6h			
01D7h			
01D8h	Timer A Output Waveform Change Enable Register	TAOW	XXX0 X00Xb
01D9h			
01DAh	Three-Phase Protect Control Register	TPRC	00h
01DBh			
01DCh			
01DDh			
01DEh			
01DFh			

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.9 SFR Information (9) (1)

Address	Register	Symbol	Reset Value
0240h			
0241h			
0242h			
0243h			
0244h	UART0 Special Mode Register 4	U0SMR4	00h
0245h	UART0 Special Mode Register 3	U0SMR3	000X 0X0Xb
0246h	UART0 Special Mode Register 2	U0SMR2	X000 0000b
0247h	UART0 Special Mode Register	U0SMR	X000 0000b
0248h	UART0 Transmit/Receive Mode Register	U0MR	00h
0249h	UART0 Bit Rate Register	U0BRG	XXh
024Ah	UART0 Transmit Buffer Register	U0TB	XXh
024Bh			XXh
024Ch	UART0 Transmit/Receive Control Register 0	U0C0	0000 1000b
024Dh	UART0 Transmit/Receive Control Register 1	U0C1	00XX 0010b
024Eh	UART0 Receive Buffer Register	U0RB	XXh
024Fh			XXh
0250h	UART Transmit/Receive Control Register 2	UCON	X000 0000b
0251h			
0252h	UART Clock Select Register	UCLKSEL0	X0h
0253h			
0254h	UART1 Special Mode Register 4	U1SMR4	00h
0255h	UART1 Special Mode Register 3	U1SMR3	000X 0X0Xb
0256h	UART1 Special Mode Register 2	U1SMR2	X000 0000b
0257h	UART1 Special Mode Register	U1SMR	X000 0000b
0258h	UART1 Transmit/Receive Mode Register	U1MR	00h
0259h	UART1 Bit Rate Register	U1BRG	XXh
025Ah	UART1 Transmit Buffer Register	U1TB	XXh
025Bh			XXh
025Ch	UART1 Transmit/Receive Control Register 0	U1C0	0000 1000b
025Dh	UART1 Transmit/Receive Control Register 1	U1C1	00XX 0010b
025Eh	UART1 Receive Buffer Register	U1RB	XXh
025Fh			XXh
0260h			
0261h			
0262h			
0263h			
0264h	UART2 Special Mode Register 4	U2SMR4	00h
0265h	UART2 Special Mode Register 3	U2SMR3	000X 0X0Xb
0266h	UART2 Special Mode Register 2	U2SMR2	X000 0000b
0267h	UART2 Special Mode Register	U2SMR	X000 0000b
0268h	UART2 Transmit/Receive Mode Register	U2MR	00h
0269h	UART2 Bit Rate Register	U2BRG	XXh
026Ah	UART2 Transmit Buffer Register	U2TB	XXh
026Bh			XXh
026Ch	UART2 Transmit/Receive Control Register 0	U2C0	0000 1000b
026Dh	UART2 Transmit/Receive Control Register 1	U2C1	0000 0010b
026Eh	UART2 Receive Buffer Register	U2RB	XXh
026Fh			XXh

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.12 SFR Information (12) (1)

Address	Register	Symbol	Reset Value
0300h	Timer B3/B4/B5 Count Start Flag	TBSR	000X XXXXb
0301h			
0302h	Timer A1-1 Register	TA11	XXh
0303h			XXh
0304h	Timer A2-1 Register	TA21	XXh
0305h			XXh
0306h	Timer A4-1 Register	TA41	XXh
0307h			XXh
0308h	Three-Phase PWM Control Register 0	INVC0	00h
0309h	Three-Phase PWM Control Register 1	INVC1	00h
030Ah	Three-Phase Output Buffer Register 0	IDB0	XX11 1111b
030Bh	Three-Phase Output Buffer Register 1	IDB1	XX11 1111b
030Ch	Dead Time Timer	DTT	XXh
030Dh	Timer B2 Interrupt Generation Frequency Set Counter	ICTB2	XXh
030Eh	Position-Data-Retain Function Control Register	PDRF	XXXX 0000b
030Fh			
0310h	Timer B3 Register	TB3	XXh
0311h			XXh
0312h	Timer B4 Register	TB4	XXh
0313h			XXh
0314h	Timer B5 Register	TB5	XXh
0315h			XXh
0316h			
0317h			
0318h	Port Function Control Register	PFCR	0011 1111b
0319h			
031Ah			
031Bh	Timer B3 Mode Register	TB3MR	00XX 0000b
031Ch	Timer B4 Mode Register	TB4MR	00XX 0000b
031Dh	Timer B5 Mode Register	TB5MR	00XX 0000b
031Eh			
031Fh			
0320h	Count Start Flag	TABSR	00h
0321h			
0322h	One-Shot Start Flag	ONSF	00h
0323h	Trigger Select Register	TRGSR	00h
0324h	Increment/Decrement Flag	UDF	00h
0325h			
0326h	Timer A0 Register	TA0	XXh
0327h			XXh
0328h	Timer A1 Register	TA1	XXh
0329h			XXh
032Ah	Timer A2 Register	TA2	XXh
032Bh			XXh
032Ch	Timer A3 Register	TA3	XXh
032Dh			XXh
032Eh	Timer A4 Register	TA4	XXh
032Fh			XXh

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

5.1.3 A/D Conversion Characteristics

Table 5.5 A/D Conversion Characteristics (1/2) (1)

V_{CC1} = AV_{CC} = 3.0 to 5.5 V ≥ V_{CC2} ≥ V_{REF}, V_{SS} = AV_{SS} = 0 V at T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified.

Symbol	Parameter		Measuring Condition		Standard			Unit
					Min.	Typ.	Max.	
-	Resolution		AV_{CC} = V_{CC1} ≥ V_{CC2} ≥ V_{REF}				10	Bits
I_{NL}	Integral non-linearity error	10 bits	V_{CC1} = 5.0 V	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input (Note 2)			±3	LSB
			V_{CC1} = 3.3 V	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input (Note 2)			±3	LSB
			V_{CC1} = 3.0 V	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input (Note 2)			±3	LSB
-	Absolute accuracy	10 bits	V_{CC1} = 5.0 V	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input (Note 2)			±3	LSB
			V_{CC1} = 3.3 V	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input (Note 2)			±3	LSB
			V_{CC1} = 3.0 V	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input (Note 2)			±3	LSB

Notes:
1. Use when AV_{CC} = V_{CC1}.
2. Flash memory rewrite disabled. Except for the analog input pin, set the pins to be measured as input ports and connect them to V_{SS}. See Figure 5.2 “A/D Accuracy Measure Circuit”.

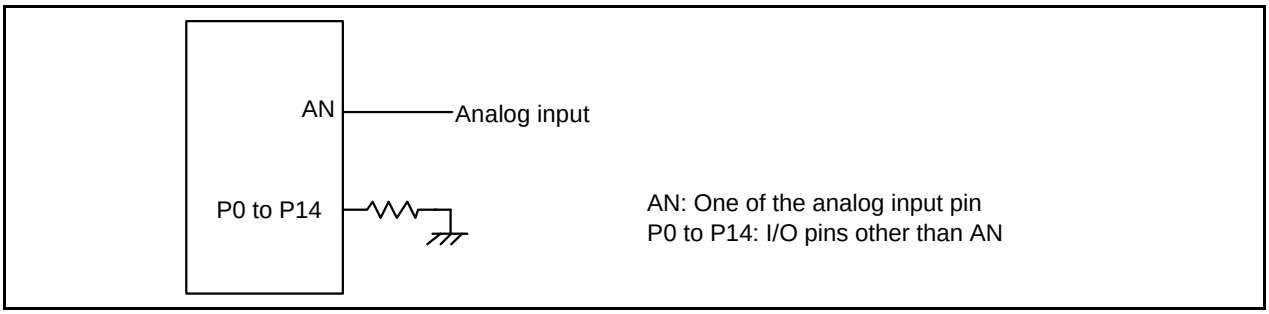


Figure 5.2 A/D Accuracy Measure Circuit

Table 5.13 Voltage Detector 2 Electrical Characteristics

The measurement condition is V_{CC1} = 2.7 to 5.5 V, T_{opr} = -20°C to 85°C/-40°C to 85°C, unless otherwise specified.

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det2}	Voltage detection level Vdet2_0	When V_{CC1} is falling	3.70	4.00	4.30	V
-	Hysteresis width at the rising of V_{CC1} in voltage detector 2			0.15		V
-	Voltage detector 2 response time (2)	When V_{CC1} falls from 5 V to (Vdet2_0 - 0.1) V			200	µs
-	Voltage detector self power consumption	VC27 = 1, V_{CC1} = 5.0 V		1.7		µA
$t_{d(E-A)}$	Waiting time until voltage detector operation starts (1)				100	µs

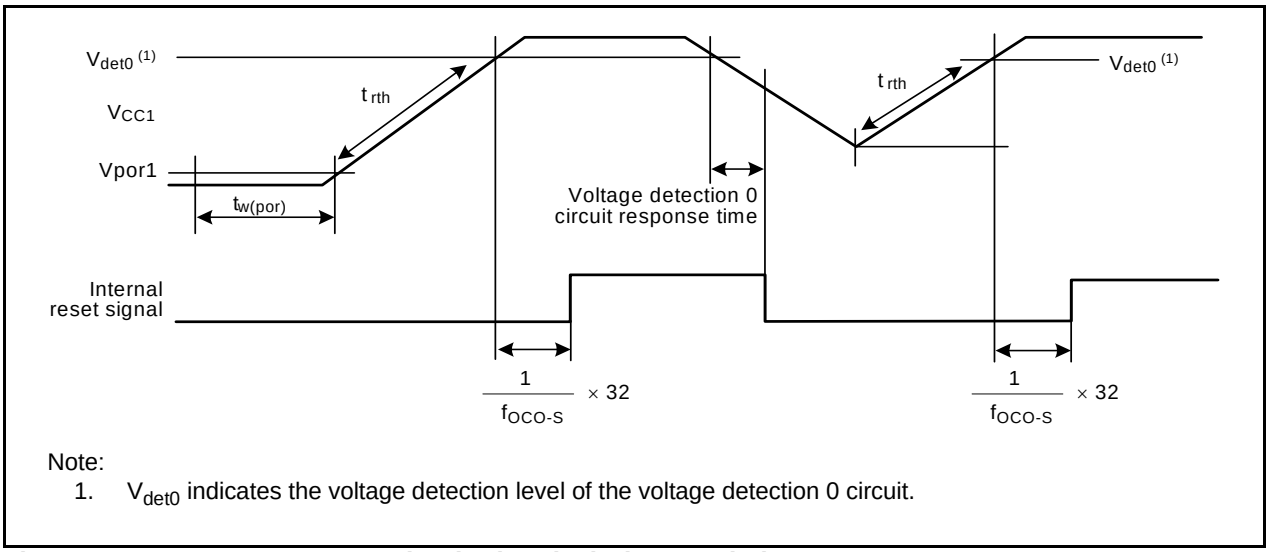
Notes:
1. Necessary time until the voltage detector operates after setting to 1 again after setting the VC27 bit in the VCR2 register to 0.
2. Time from when passing the V_{det2} until when a voltage monitor 2 reset is generated.

Table 5.14 Power-On Reset Circuit

The measurement condition is V_{CC1} = 2.0 to 5.5 V, T_{opr} = -20°C to 85°C/ -40°C to 85°C, unless otherwise specified.

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{por1}	Voltage at which power-on reset enabled (1)				0.5	V
t_{rth}	External power V_{CC1} rise gradient		2.0		50000	mV/ms
$t_{w(por)}$	Time necessary to enable power-on reset		300			ms

Note:
1. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS1 address to 0. Also, set the VDSEL1 bit to 0 (Vdet0_2).



Note:
1. V_{det0} indicates the voltage detection level of the voltage detection 0 circuit.

Figure 5.3 Power-On Reset Circuit Electrical Characteristics

$V_{CC1} = V_{CC2} = 5\ V$

Timing Requirements

($V_{CC1} = V_{CC2} = 5$ V, $V_{SS} = 0$ V, at $T_{opr} = -20°C$ to 85°C/-40°C to 85°C unless otherwise specified)

5.2.2.3 Timer A Input

Table 5.24 Timer A Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	100		ns
$t_{w(TAH)}$	TAiIN input high pulse width	40		ns
$t_{w(TAL)}$	TAiIN input low pulse width	40		ns

Table 5.25 Timer A Input (Gating Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	400		ns
$t_{w(TAH)}$	TAiIN input high pulse width	200		ns
$t_{w(TAL)}$	TAiIN input low pulse width	200		ns

Table 5.26 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	200		ns
$t_{w(TAH)}$	TAiIN input high pulse width	100		ns
$t_{w(TAL)}$	TAiIN input low pulse width	100		ns

Table 5.27 Timer A Input (External Trigger Input in Pulse Width Modulation Mode and Programmable Output Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiIN input high pulse width	100		ns
$t_{w(TAL)}$	TAiIN input low pulse width	100		ns

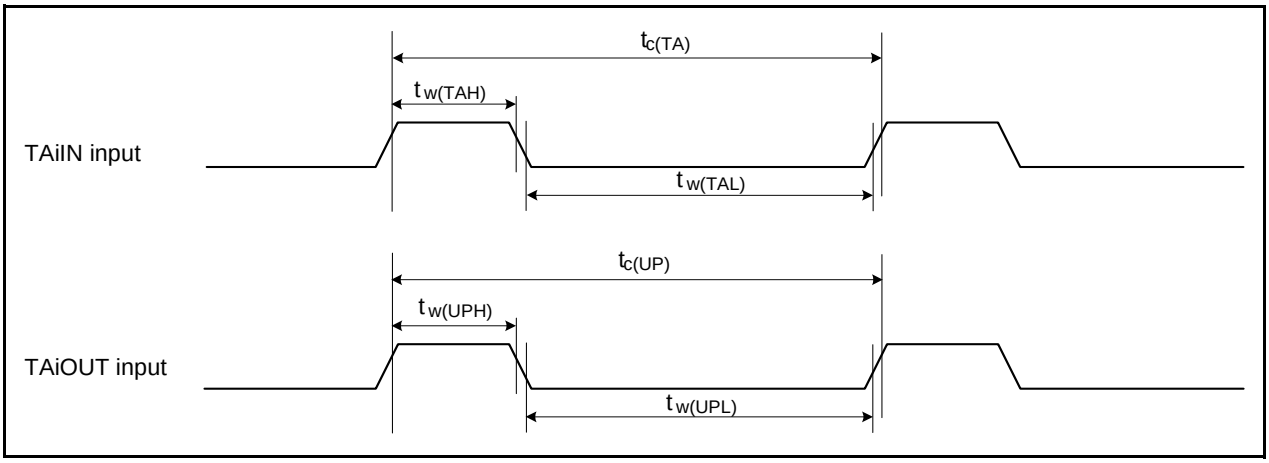


Figure 5.7 Timer A Input

$V_{CC1} = V_{CC2} = 5\ V$

Timing Requirements

($V_{CC1} = V_{CC2} = 5$ V, $V_{SS} = 0$ V, at $T_{opr} = -20°C$ to 85°C/-40°C to 85°C unless otherwise specified)

5.2.2.4 Timer B Input

Table 5.29 Timer B Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time (counted on one edge)	100		ns
$t_{w(TBH)}$	TBiIN input high pulse width (counted on one edge)	40		ns
$t_{w(TBL)}$	TBiIN input low pulse width (counted on one edge)	40		ns
$t_{c(TB)}$	TBiIN input cycle time (counted on both edges)	200		ns
$t_{w(TBH)}$	TBiIN input high pulse width (counted on both edges)	80		ns
$t_{w(TBL)}$	TBiIN input low pulse width (counted on both edges)	80		ns

Table 5.30 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	400		ns
$t_{w(TBH)}$	TBiIN input high pulse width	200		ns
$t_{w(TBL)}$	TBiIN input low pulse width	200		ns

Table 5.31 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	400		ns
$t_{w(TBH)}$	TBiIN input high pulse width	200		ns
$t_{w(TBL)}$	TBiIN input low pulse width	200		ns

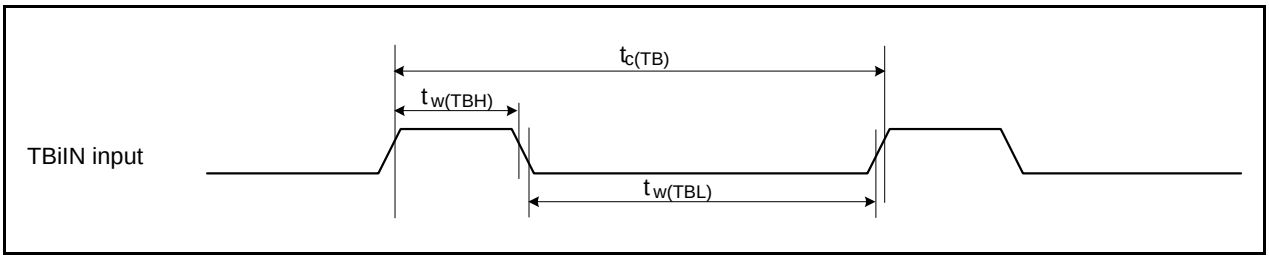
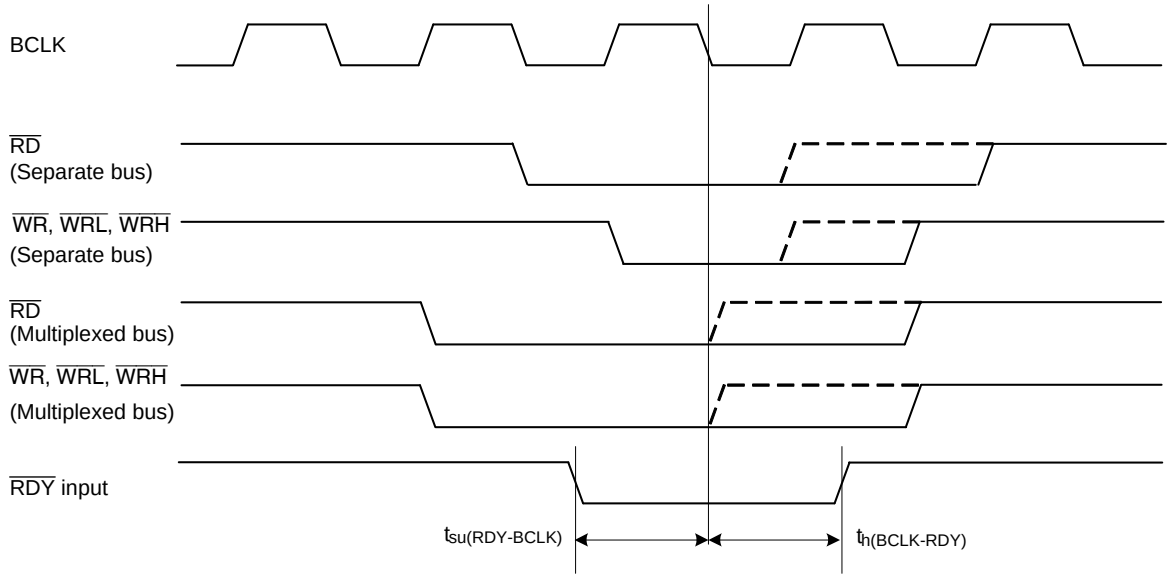


Figure 5.9 Timer B Input

Memory Expansion Mode and Microprocessor Mode

$V_{CC1} = V_{CC2} = 5\ V$

(Effective in wait state setting**)**



Measuring conditions

- $V_{CC1} = V_{CC2} = 5\ V$
- Input timing voltage: $V_{IL} = 1.0\ V$, $V_{IH} = 4.0\ V$
- Output timing voltage: $V_{OL} = 2.5\ V$, $V_{OH} = 2.5\ V$

Figure 5.13 Timing Diagram

5.3 Electrical Characteristics (V_{CC1} = V_{CC2} = 3 V)

5.3.1 Electrical Characteristics

VCC1 = VCC2 = 3 V

Table 5.41 Electrical Characteristics (1) [1]

V_{CC1} = V_{CC2} = 2.7 to 3.3 V, V_{SS} = 0 V at T_{opr} = -20°C to 85°C/-40°C to 85°C, $f_{(BCLK)}$ = 32 MHz unless otherwise specified.

Symbol	Parameter			Measuring Condition	Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	High output voltage	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1		I_{OH} = –1 mA	V_{CC1} – 0.5		V_{CC1}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7		I_{OH} = –1 mA	V_{CC2} – 0.5		V_{CC2}	
V_{OH}	High output voltage XOUT		HIGH POWER	I_{OH} = –0.1 mA	V_{CC1} – 0.5		V_{CC1}	V
			LOW POWER	I_{OH} = –50 µA	V_{CC1} – 0.5		V_{CC1}	
	High output voltage XCOUT		HIGH POWER	With no load applied		2.6		V
			LOW POWER	With no load applied		2.2		
V_{OL}	Low output voltage	P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1		I_{OL} = 1 mA			0.5	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7		I_{OL} = 1 mA			0.5	
		CEC		I_{OL} = 1 mA		0	0.5	V
V_{OL}	Low output voltage XOUT		HIGH POWER	I_{OL} = 0.1 mA			0.5	V
			LOW POWER	I_{OL} = 50 µA			0.5	
	Low output voltage XCOUT		HIGH POWER	With no load applied		0		V
			LOW POWER	With no load applied		0		
V_{T+}-V_{T-}	Hysteresis	$\overline{HOLD}$, $\overline{RDY}$, TA0IN to TA4IN, TB0IN to TB5IN, $\overline{INT0}$ to $\overline{INT7}$, $\overline{NMI}$, $\overline{ADTRG}$, $\overline{CTS0}$ to $\overline{CTS2}$, $\overline{CTS5}$ to $\overline{CTS7}$, SCL0 to SCL2, SCL5 to SCL7, SDA0 to SDA2, SDA5 to SDA7, CLK0 to CLK7, TA0OUT to TA4OUT, $\overline{KI0}$ to $\overline{KI3}$, RXD0 to RXD2, RXD5 to RXD7, SIN3, SIN4, $\overline{SD}$, PMC0, PMC1, SCLMM, SDAMM, ZP, IDU, IDV, IDW			0.2		1.0	V
		CEC			0.2	0.5	1.0	V
		$\overline{RESET}$			0.2		1.8	V
I_{IH}	High input current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1 XIN, $\overline{RESET}$, CNVSS, BYTE		V_I = 3 V			4.0	µA
–	Leakage current in powered-off state		CEC	V_{CC1} = 0 V			1.8	µA
I_{IL}	Low input current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1 XIN, $\overline{RESET}$, CNVSS, BYTE		V_I = 0 V			–4.0	µA
R_{PULLUP}	Pull-up resistance	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1		V_I = 0 V	50	80	150	kΩ
R_{fXIN}	Feedback resistance XIN					3.0		MΩ
V_{RAM}	RAM retention voltage			In stop mode	1.8			V

Note:
1. When $V_{CC1} \neq V_{CC2}$, refer to 5 V or 3 V standard depending on the voltage.

$V_{CC1} = V_{CC2} = 3\ V$

Timing Requirements

($V_{CC1} = V_{CC2} = 3$ V, $V_{SS} = 0$ V, at $T_{opr} = -20°C$ to 85°C/-40°C to 85°C unless otherwise specified)

5.3.2.4 Timer B Input

Table 5.52 Timer B Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time (counted on one edge)	150		ns
$t_{w(TBH)}$	TBiIN input high pulse width (counted on one edge)	60		ns
$t_{w(TBL)}$	TBiIN input low pulse width (counted on one edge)	60		ns
$t_{c(TB)}$	TBiIN input cycle time (counted on both edges)	300		ns
$t_{w(TBH)}$	TBiIN input high pulse width (counted on both edges)	120		ns
$t_{w(TBL)}$	TBiIN input low pulse width (counted on both edges)	120		ns

Table 5.53 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	600		ns
$t_{w(TBH)}$	TBiIN input high pulse width	300		ns
$t_{w(TBL)}$	TBiIN input low pulse width	300		ns

Table 5.54 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	600		ns
$t_{w(TBH)}$	TBiIN input high pulse width	300		ns
$t^{w(TBL)}$	TBiIN input low pulse width	300		ns

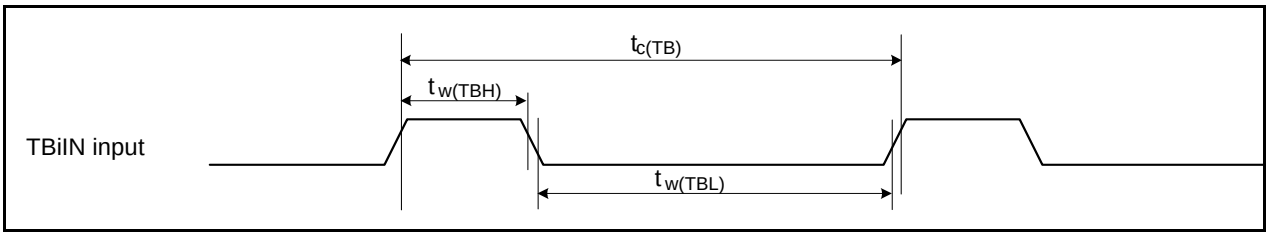


Figure 5.24 Timer B Input

$V_{CC1} = V_{CC2} = 3\ V$

Timing Requirements

($V_{CC1} = V_{CC2} = 3$ V, $V_{SS} = 0$ V, at T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified)

5.3.2.5 Serial Interface

Table 5.55 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300		ns
$t_{w(CKH)}$	CLKi input high pulse width	150		ns
$t_{w(CKL)}$	CLKi input low pulse width	150		ns
$t_{d(C-Q)}$	TXDi output delay time		160	ns
$t_{h(C-Q)}$	TXDi hold time	0		ns
$t_{su(D-C)}$	RXDi input setup time	100		ns
$t_{h(C-D)}$	RXDi input hold time	90		ns

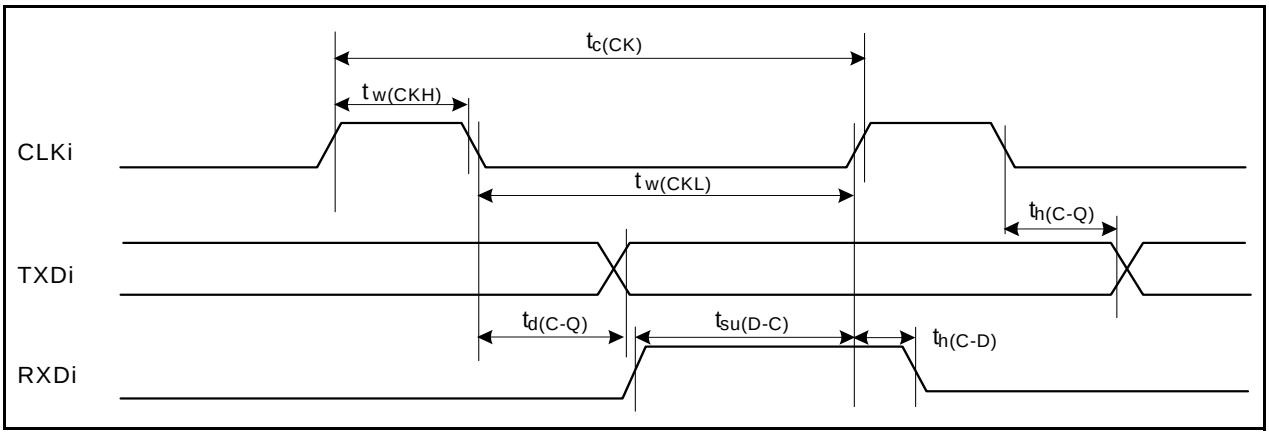


Figure 5.25 Serial Interface

5.3.2.6 External Interrupt $\overline{INTi}$ Input

Table 5.56 External Interrupt $\overline{INTi}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input high pulse width	380		ns
$t_{w(INL)}$	$\overline{INTi}$ input low pulse width	380		ns

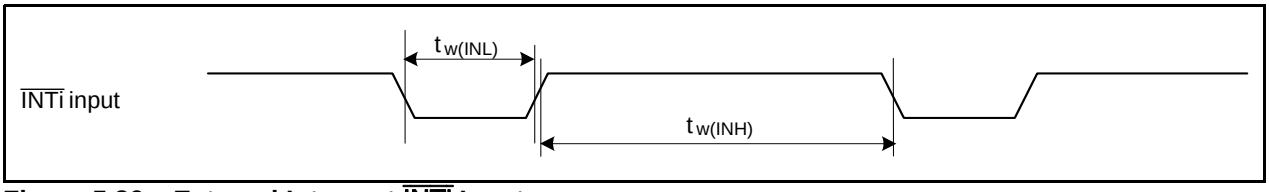


Figure 5.26 External Interrupt $\overline{INTi}$ Input

$V_{CC1} = V_{CC2} = 3\ V$

Timing Requirements

($V_{CC1} = V_{CC2} = 3$ V, $V_{SS} = 0$ V, at T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified)

5.3.3 Timing Requirements (Memory Expansion Mode and Microprocessor Mode)

Table 5.58 Memory Expansion Mode and Microprocessor Mode

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{ac1(RD-DB)}$	Data input access time (for setting with no wait)		(Note 1)	ns
$t_{ac2(RD-DB)}$	Data input access time (for setting with wait)		(Note 2)	ns
$t_{ac3(RD-DB)}$	Data input access time (when accessing multiplex bus area)		(Note 3)	ns
$t_{ac4(RD-DB)}$	Data input access time (for setting with 2 ϕ + 3 ϕ or more)		(Note 4)	ns
$t_{su(DB-RD)}$	Data input setup time	60		ns
$t_{su(RDY-BCLK)}$	$\overline{RDY}$ input setup time	85		ns
$t_{h(RD-DB)}$	Data input hold time	0		ns
$t_{h(BCLK-RDY)}$	$\overline{RDY}$ input hold time	0		ns

Notes:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f_{(BCLK)}} - 60[ns]$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{(n + 0.5) \times 10^9}{f_{(BCLK)}} - 60[ns]$$ n is 1 for 1 wait setting, 2 for 2 waits setting and 3 for 3 waits setting.

3. Calculated according to the BCLK frequency as follows:

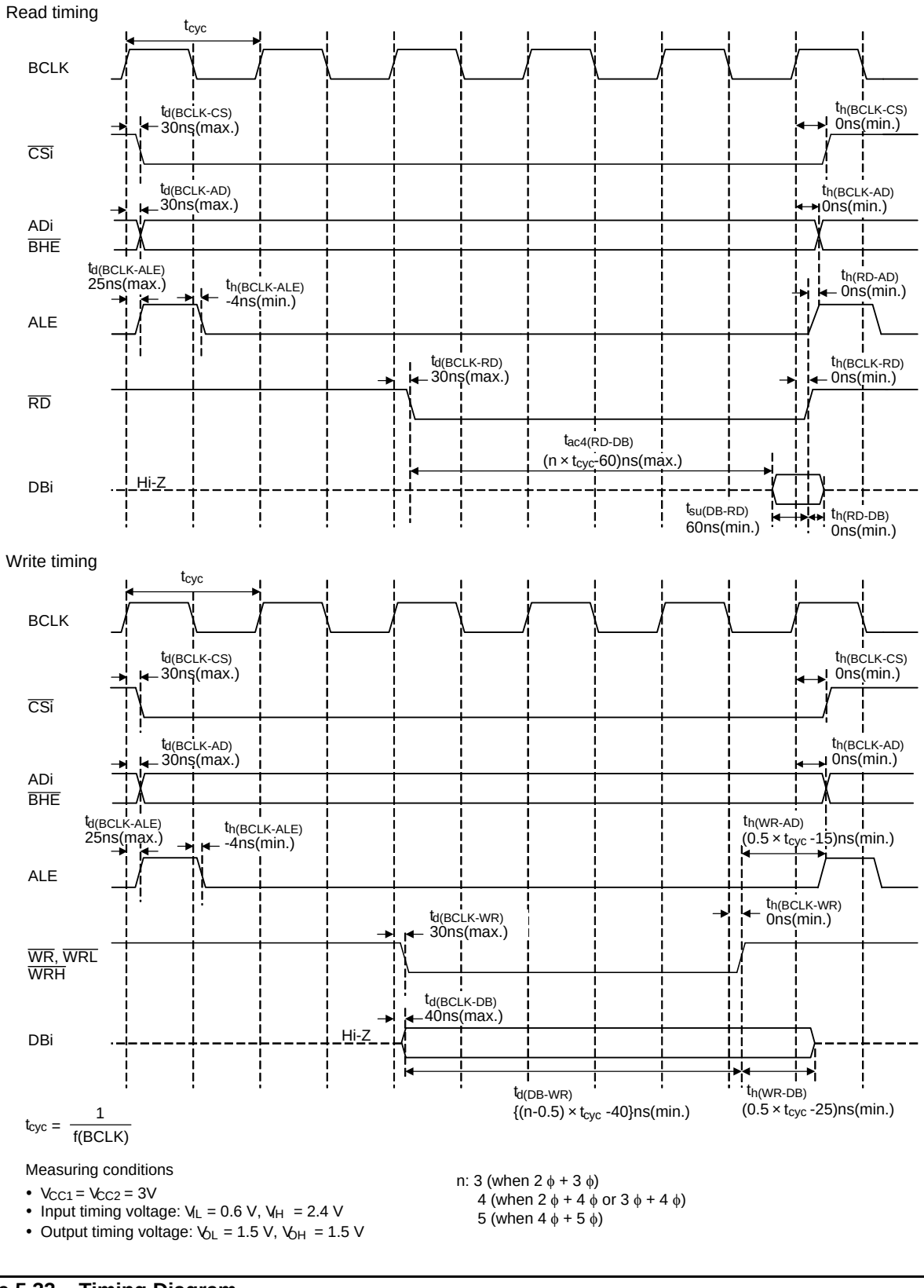
$$\frac{(n - 0.5) \times 10^9}{f_{(BCLK)}} - 60[ns]$$ n is 2 for 2 waits setting, 3 for 3 waits setting.

4. Calculated according to the BCLK frequency as follows:

$$\frac{n \times 10^9}{f_{(BCLK)}} - 60[ns]$$ n is 3 for 2 ϕ + 3 ϕ, 4 for 2 ϕ + 4 ϕ, 4 for 3 ϕ + 4 ϕ, 5 for 4 ϕ + 5 ϕ,.

Memory Expansion Mode, Microprocessor Mode
(in wait state setting 2 ϕ + 3 ϕ, 2 ϕ + 4 ϕ, 3ϕ + 4 ϕ, and 4 ϕ + 5 ϕ, and when accessing external area)

$V_{CC1} = V_{CC2} = 3V$



$$t_{cyc} = \frac{1}{f(BCLK)}$$

Measuring conditions

- $V_{CC1} = V_{CC2} = 3V$
- Input timing voltage: $V_{IL} = 0.6$ V, $V_{IH} = 2.4$ V
- Output timing voltage: $V_{OL} = 1.5$ V, $V_{OH} = 1.5$ V

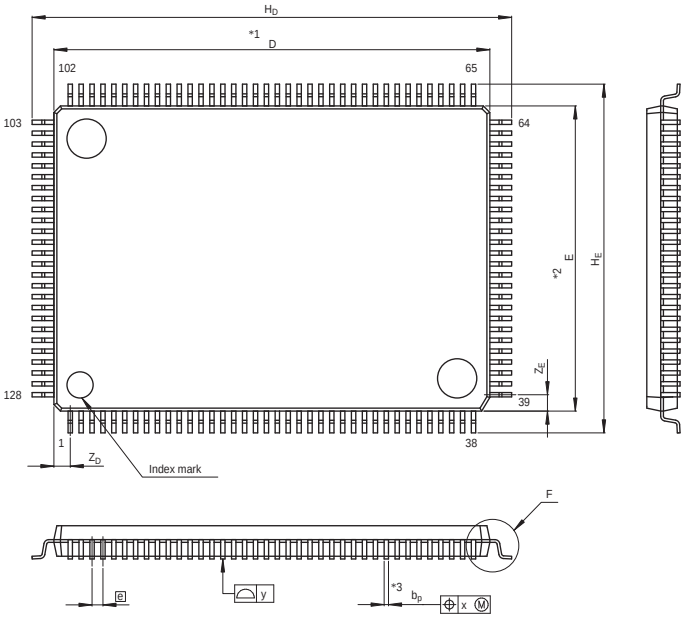
n: 3 (when 2 ϕ + 3 ϕ)
4 (when 2 ϕ + 4 ϕ or 3 ϕ + 4 ϕ)
5 (when 4 ϕ + 5 ϕ)

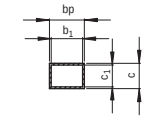
Figure 5.33 Timing Diagram

Appendix 1. Package Dimensions

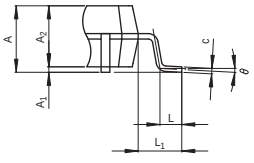
The information on the latest package dimensions or packaging may be obtained from “Packages“ on the Renesas Electronics website.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP128-14x20-0.50	PLQP0128KB-A	128P6Q-A	0.9g





Terminal cross section

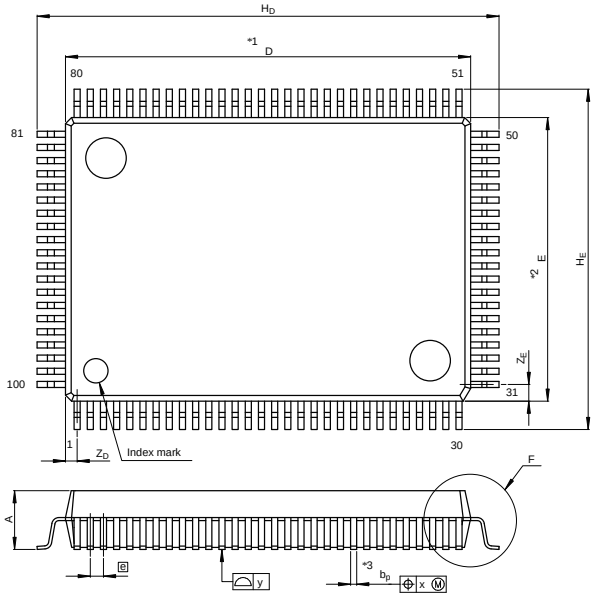


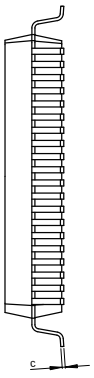
DetailF

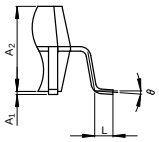
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	19.9	20.0	20.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	21.8	22.0	22.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	0.125	0.2
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.10
y	—	—	0.10
Z_D	—	0.75	—
Z_E	—	0.75	—
L	0.35	0.5	0.65
L_1	—	1.0	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-QFP100-14x20-0.65	PRQP0100JD-B	100P6F-A	1.8g







Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	19.8	20.0	20.2
E	13.8	14.0	14.2
A_2	—	2.8	—
H_D	22.5	22.8	23.1
H_E	16.5	16.8	17.1
A	—	—	3.05
A_1	0	0.1	0.2
b_p	0.25	0.3	0.4
c	0.13	0.15	0.2
θ	0°	—	10°
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z_D	—	0.575	—
Z_E	—	0.825	—
L	0.4	0.6	0.8

REVISION HISTORY	M16C/65C Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.10	Oct 29, 2010	-	First Edition issued.
1.00	Feb 07, 2011	Overall	Changed terminologies are as follows: • “oscillation/oscillator circuit” to “oscillator” • “oscillator” to “a crystal/ceramic resonator” • “oscillator manufacturer” to “manufacturer of crystal/ceramic resonator” • “on-chip oscillator oscillation circuit” to “on-chip oscillator”
		Overview	
		3, 5	Table 1.2 Specifications for the 128-Pin Package (2/2), Table 1.4 Specifications for the 100-Pin Package (2/2): Changed the Description column of the Current Consumption row.
		6	Table 1.5 Product List (N-Version), Table 1.6 Product List (D-Version): Changed the development status.
		Electrical Characteristics	
		VCC = 5 V	
		64, 65	Table 5.20 Electrical Characteristics (3), Table 5.21 Electrical Characteristics (4): Added conditions with XIN is 6MHz to the Wait mode measuring condition.
		74, 77, 79, 81, 83	In Switching Characteristics (Memory Expansion Mode and Microprocessor Mode), Table 5.36, Table 5.37, Table 5.38, Table 5.39, Table 5.40: • Deleted the th(BCLK-DB) row. • Changed the formula of th(WR-DB) for minimum standard.
		76, 78, 80, 82, 84	Figure 5.15, Figure 5.16, Figure 5.17, Figure 5.18, Figure 5.19: Deleted the description of th(BCLK-DB), and changed the formula of th(WR-DB) in the Write timing.
		VCC = 3 V	
		86, 87	Table 5.42 Electrical Characteristics (2), Table 5.43 Electrical Characteristics (3) (1/2): Added conditions with XIN is 6MHz to the Wait mode measuring condition.
		95, 97, 100, 102, 104	In Switching Characteristics (Memory Expansion Mode and Microprocessor Mode), Table 5.58, Table 5.59, Table 5.60, Table 5.61, Table 5.62: • Deleted the th(BCLK-DB) row. • Changed the formula of th(WR-AD) for minimum standard. • Changed the formula of th(WR-DB) for minimum standard.
		99, 101, 103, 105, 107	Figure 5.30, Figure 5.31, Figure 5.32, Figure 5.33, Figure 5.34: • Deleted the description of th(BCLK-DB), and changed the formulas of th(WR-AD) and th(WR-DB) in the Write timing.
1.10	Jul 31, 2012	**Overview**	
		6	Table 1.5 Product List (N-Version), Table 1.6 Product List (D-Version): Changed development statuses.
		Electrical Characteristics	
		Vcc = 5 V	
		64, 65	Table 5.20 Electrical Characteristics (3) and Table 5.21 Electrical Characteristics (4): Changed the Measuring Condition column of 40 MHz on-chip oscillator for the 40 MHz on-chip oscillator mode in the I_{CC}.
		Vcc = 3 V	
		86, 87	Table 5.42 Electrical Characteristics (2) and Table 5.43 Electrical Characteristics (3) (1/2): Changed the Measuring Condition column of 40 MHz on-chip oscillator for the 40 MHz on-chip oscillator mode in the I_{CC}.