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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	M16C/60
Core Size	16-Bit
Speed	32MHz
Connectivity	EBI/EMI, I ² C, SIO, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	85
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	31K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f3650mcdfb-v0

1.4 Block Diagram

Figure 1.3 to Figure 1.4 show block diagrams.

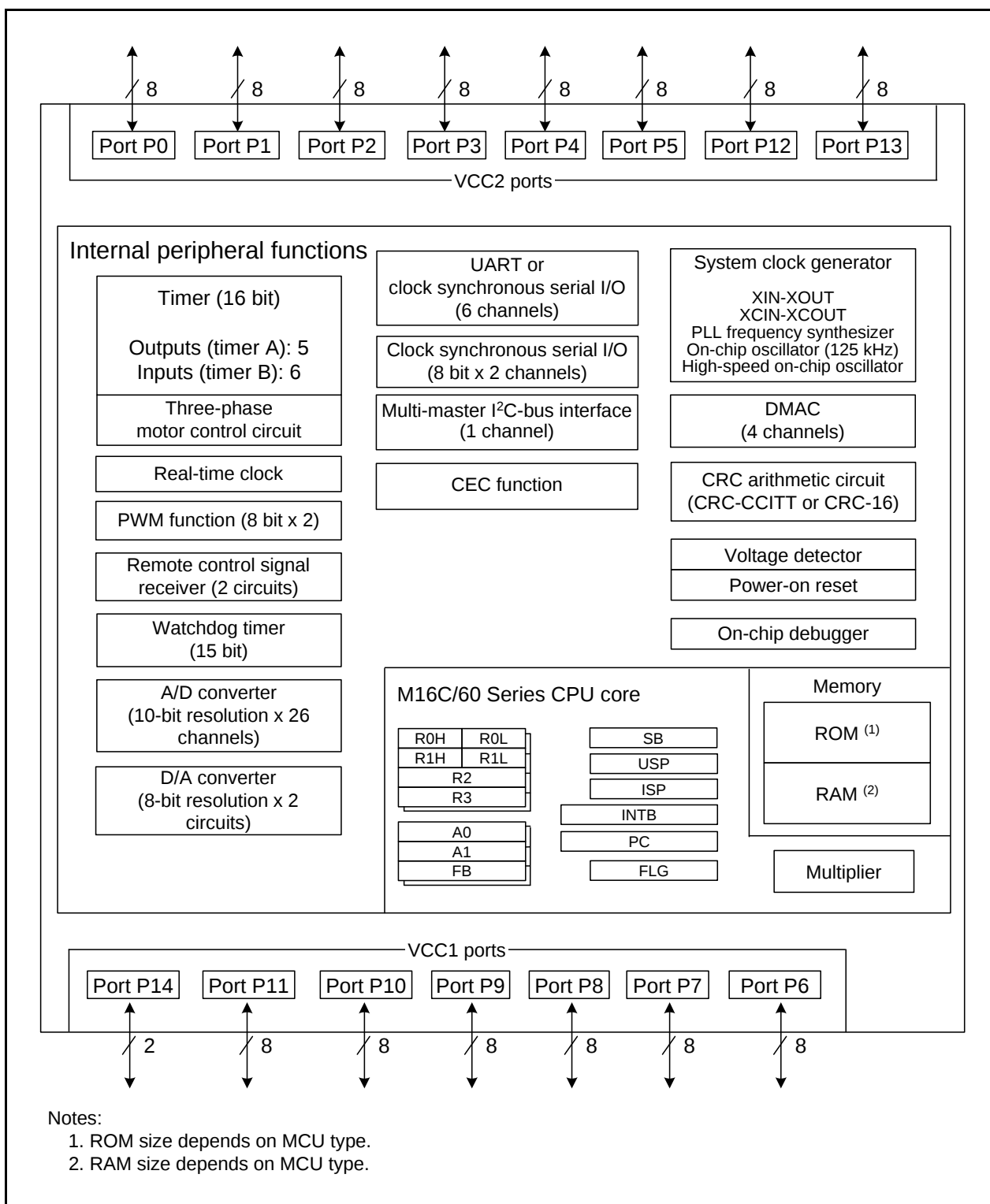


Figure 1.3 Block Diagram for the 128-Pin Package

Table 1.9 Pin Names for the 128-Pin Package (3/3)

Pin No.	Control Pin	Port	I/O Pin for Peripheral Function				Bus Control Pin
			Interrupt	Timer	Serial interface	A/D converter, D/A converter	
101		P1_2			RXD6/SCL6		D10
102		P1_1			CLK6		D9
103		P1_0			CTS6/RTS6		D8
104		P0_7				AN0_7	D7
105		P0_6				AN0_6	D6
106		P0_5				AN0_5	D5
107		P0_4				AN0_4	D4
108		P0_3				AN0_3	D3
109		P0_2				AN0_2	D2
110		P0_1				AN0_1	D1
111		P0_0				AN0_0	D0
112		P11_7					
113		P11_6					
114		P11_5					
115		P11_4					
116		P11_3					
117		P11_2					
118		P11_1					
119		P11_0					
120		P10_7	KI3			AN7	
121		P10_6	KI2			AN6	
122		P10_5	KI1			AN5	
123		P10_4	KI0			AN4	
124		P10_3				AN3	
125		P10_2				AN2	
126		P10_1				AN1	
127	AVSS						
128		P10_0				AN0	

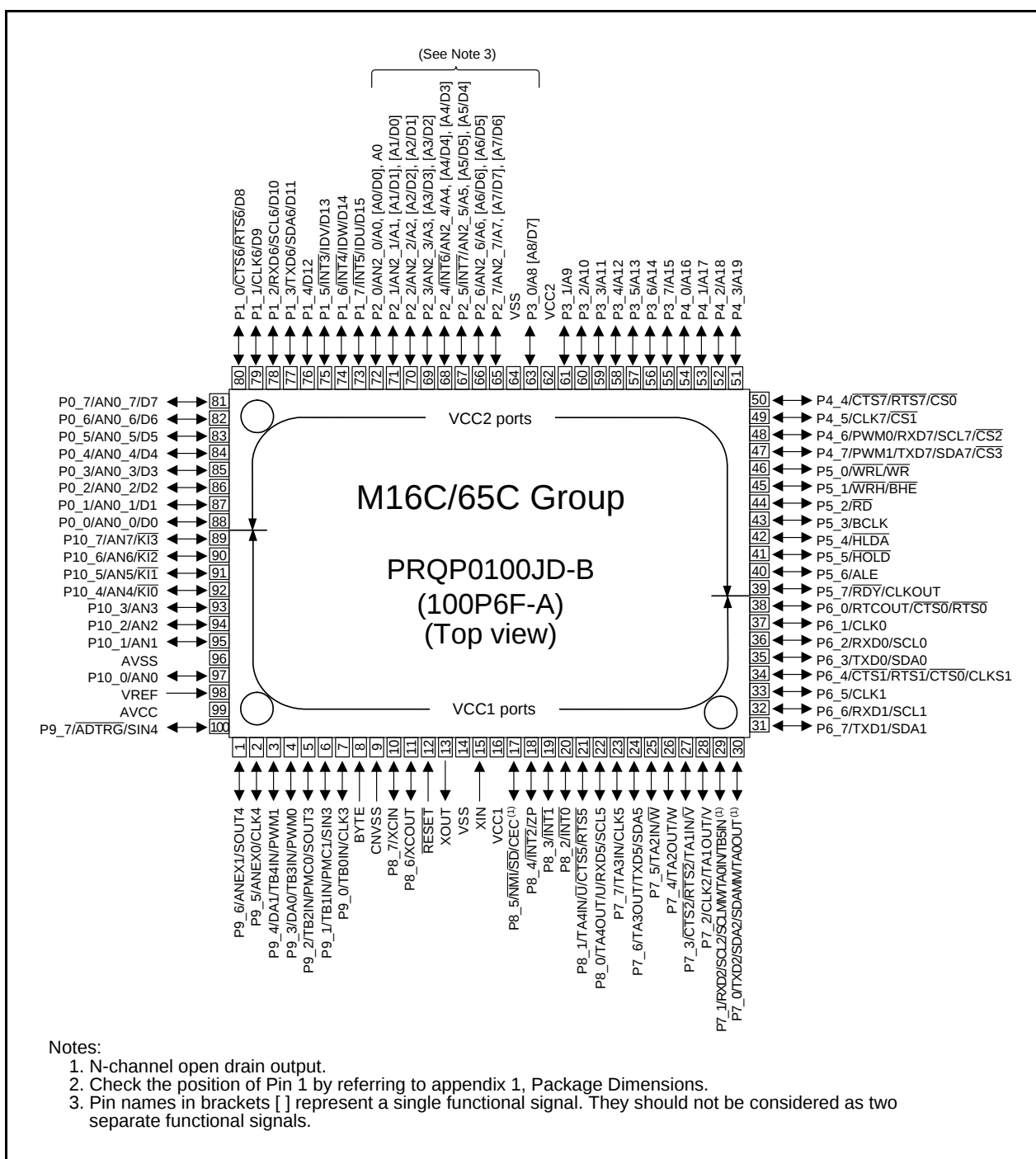


Figure 1.6 Pin Assignment for the 100-Pin Package

Table 4.9 SFR Information (9) ⁽¹⁾

Address	Register	Symbol	Reset Value
0240h			
0241h			
0242h			
0243h			
0244h	UART0 Special Mode Register 4	U0SMR4	00h
0245h	UART0 Special Mode Register 3	U0SMR3	000X 0X0Xb
0246h	UART0 Special Mode Register 2	U0SMR2	X000 0000b
0247h	UART0 Special Mode Register	U0SMR	X000 0000b
0248h	UART0 Transmit/Receive Mode Register	U0MR	00h
0249h	UART0 Bit Rate Register	U0BRG	XXh
024Ah	UART0 Transmit Buffer Register	U0TB	XXh
024Bh			XXh
024Ch	UART0 Transmit/Receive Control Register 0	U0C0	0000 1000b
024Dh	UART0 Transmit/Receive Control Register 1	U0C1	00XX 0010b
024Eh	UART0 Receive Buffer Register	U0RB	XXh
024Fh			XXh
0250h	UART Transmit/Receive Control Register 2	UCON	X000 0000b
0251h			
0252h	UART Clock Select Register	UCLKSEL0	X0h
0253h			
0254h	UART1 Special Mode Register 4	U1SMR4	00h
0255h	UART1 Special Mode Register 3	U1SMR3	000X 0X0Xb
0256h	UART1 Special Mode Register 2	U1SMR2	X000 0000b
0257h	UART1 Special Mode Register	U1SMR	X000 0000b
0258h	UART1 Transmit/Receive Mode Register	U1MR	00h
0259h	UART1 Bit Rate Register	U1BRG	XXh
025Ah	UART1 Transmit Buffer Register	U1TB	XXh
025Bh			XXh
025Ch	UART1 Transmit/Receive Control Register 0	U1C0	0000 1000b
025Dh	UART1 Transmit/Receive Control Register 1	U1C1	00XX 0010b
025Eh	UART1 Receive Buffer Register	U1RB	XXh
025Fh			XXh
0260h			
0261h			
0262h			
0263h			
0264h	UART2 Special Mode Register 4	U2SMR4	00h
0265h	UART2 Special Mode Register 3	U2SMR3	000X 0X0Xb
0266h	UART2 Special Mode Register 2	U2SMR2	X000 0000b
0267h	UART2 Special Mode Register	U2SMR	X000 0000b
0268h	UART2 Transmit/Receive Mode Register	U2MR	00h
0269h	UART2 Bit Rate Register	U2BRG	XXh
026Ah	UART2 Transmit Buffer Register	U2TB	XXh
026Bh			XXh
026Ch	UART2 Transmit/Receive Control Register 0	U2C0	0000 1000b
026Dh	UART2 Transmit/Receive Control Register 1	U2C1	0000 0010b
026Eh	UART2 Receive Buffer Register	U2RB	XXh
026Fh			XXh

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 4.20 Read-Modify-Write Instructions

Function	Mnemonic
Transfer	<i>MOVDir</i>
Bit processing	BCLR, BMCnd, BNOT, BSET, BTSTC, and BTSTS
Shifting	ROL, ROR, ROT, SHA, and SHL
Arithmetic operation	ABS, ADC, ADCF, ADD, DEC, DIV, DIVU, DIVX, EXTS, INC, MUL, MULU, NEG, SBB, and SUB
Decimal operation	DADC, DADD, DSBB, and DSUB
Logical operation	AND, NOT, OR, and XOR
Jump	ADJNZ, SBJNZ

5.1.3 A/D Conversion Characteristics

Table 5.5 A/D Conversion Characteristics (1/2) ⁽¹⁾

$V_{CC1} = AV_{CC} = 3.0$ to 5.5 V $\geq V_{CC2} \geq V_{REF}$, $V_{SS} = AV_{SS} = 0$ V at $T_{opr} = -20^{\circ}\text{C}$ to $85^{\circ}\text{C}/-40^{\circ}\text{C}$ to 85°C unless otherwise specified.

Symbol	Parameter		Measuring Condition		Standard			Unit
					Min.	Typ.	Max.	
-	Resolution		$AV_{CC} = V_{CC1} \geq V_{CC2} \geq V_{REF}$				10	Bits
I_{NL}	Integral non-linearity error	10 bits	$V_{CC1} = 5.0$ V	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input (Note 2)			± 3	LSB
			$V_{CC1} = 3.3$ V	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input (Note 2)			± 3	LSB
			$V_{CC1} = 3.0$ V	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input (Note 2)			± 3	LSB
-	Absolute accuracy	10 bits	$V_{CC1} = 5.0$ V	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input (Note 2)			± 3	LSB
			$V_{CC1} = 3.3$ V	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input (Note 2)			± 3	LSB
			$V_{CC1} = 3.0$ V	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input (Note 2)			± 3	LSB

Notes:

1. Use when $AV_{CC} = V_{CC1}$.
2. Flash memory rewrite disabled. Except for the analog input pin, set the pins to be measured as input ports and connect them to V_{SS} . See Figure 5.2 "A/D Accuracy Measure Circuit".

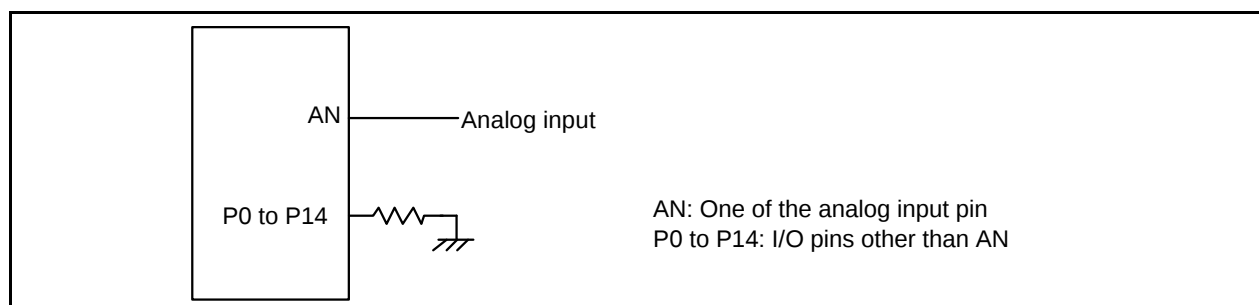

Figure 5.2 A/D Accuracy Measure Circuit

Table 5.6 A/D Conversion Characteristics (2/2) ⁽¹⁾

$V_{CC1} = AV_{CC} = 3.0 \text{ to } 5.5 \text{ V} \geq V_{CC2} \geq V_{REF}$, $V_{SS} = AV_{SS} = 0 \text{ V}$ at $T_{opr} = -20^\circ\text{C to } 85^\circ\text{C}/-40^\circ\text{C to } 85^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter		Measuring Condition	Standard			Unit	
				Min.	Typ.	Max.		
φAD	A/D operating clock frequency	AN0 to AN7 input, ANEX0 to ANEX1 input	4.0 V ≤ V _{CC1} ≤ 5.5 V	2		25	MHz	
			3.2 V ≤ V _{CC1} ≤ 4.0 V	2		16	MHz	
			3.0 V ≤ V _{CC1} ≤ 3.2 V	2		10	MHz	
		AN0_0 to AN0_7 input, AN2_0 to AN2_7 input	4.0 V ≤ V _{CC2} ≤ 5.5 V	2		25	MHz	
			3.2 V ≤ V _{CC2} ≤ 4.0 V	2		16	MHz	
			3.0 V ≤ V _{CC2} ≤ 3.2 V	2		10	MHz	
-	Tolerance level impedance				3		kΩ	
D _{NL}	Differential non-linearity error		(4)			±1	LSB	
-	Offset error		(4)				±3	LSB
-	Gain error		(4)				±3	LSB
t _{CONV}	10-bit conversion time		V _{CC1} = 5 V, φAD = 25 MHz	1.60				μs
t _{SAMP}	Sampling time			0.60				μs
V _{REF}	Reference voltage			3.0			V _{CC1}	V
V _{IA}	Analog input voltage ^{(2), (3)}			0			V _{REF}	V

Notes:

1. Use when $AV_{CC} = V_{CC1}$.
2. When $V_{CC1} \geq V_{CC2}$, set as below:
Analog input voltage (AN0 to AN7, ANEX0, and ANEX1) $\leq V_{CC1}$
Analog input voltage (AN0_0 to AN0_7 and AN2_0 to AN2_7) $\leq V_{CC2}$.
3. When analog input voltage is over reference voltage, the result of A/D conversion is 3FFh.
4. Flash memory rewrite disabled. Except for the analog input pin, set the pins to be measured as input ports and connect them to V_{SS} . See Figure 5.2 "A/D Accuracy Measure Circuit".

5.1.4 D/A Conversion Characteristics

Table 5.7 D/A Conversion Characteristics

$V_{CC1} = AV_{CC} = V_{REF} = 3.0 \text{ to } 5.5 \text{ V}$, $V_{SS} = AV_{SS} = 0 \text{ V}$ at $T_{opr} = -20^\circ\text{C to } 85^\circ\text{C}/-40^\circ\text{C to } 85^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Measuring Condition	Standard			Unit
			Min.	Typ.	Max.	
-	Resolution				8	Bits
-	Absolute Accuracy				2.5	LSB
t_{SU}	Setup Time				3	μs
R_O	Output Resistance		5	6	8.2	k Ω
I_{VREF}	Reference Power Supply Input Current	See Notes ¹ and ²			1.5	mA

Notes:

1. This applies when using one D/A converter, with the D/A register for the unused D/A converter set to 00h.
2. The current consumption of the A/D converter is not included. Also, the I_{VREF} of the D/A converter will flow even if the ADSTBY bit in the ADCON1 register is 0 (A/D operation stopped (standby)).

5.1.6 Voltage Detector and Power Supply Circuit Electrical Characteristics

Table 5.11 Voltage Detector 0 Electrical Characteristics

The measurement condition is $V_{CC1} = 2.7$ to 5.5 V, $T_{opr} = -20^{\circ}\text{C}$ to $85^{\circ}\text{C}/-40^{\circ}\text{C}$ to 85°C , unless otherwise specified.

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det0}	Voltage detection level V_{det0_0} ⁽¹⁾	When V_{CC1} is falling.	1.80	1.90	2.10	V
	Voltage detection level V_{det0_2} ⁽¹⁾	When V_{CC1} is falling.	2.70	2.85	3.00	V
-	Voltage detector 0 response time ⁽³⁾	When V_{CC1} falls from 5 V to $(V_{det0_0} - 0.1)$ V			200	μs
-	Voltage detector self power consumption	$VC25 = 1$, $V_{CC1} = 5.0$ V		1.5		μA
$t_{d(E-A)}$	Waiting time until voltage detector operation starts ⁽²⁾				100	μs

Notes:

1. Select the voltage detection level with the VDSEL1 bit in the OFS1 address.
2. Necessary time until the voltage detector operates when setting to 1 again after setting the VC25 bit in the VCR2 register to 0.
3. Time from when passing the V_{det0} until when a voltage monitor 0 reset is generated.

Table 5.12 Voltage Detector 1 Electrical Characteristics

The measurement condition is $V_{CC1} = 2.7$ to 5.5 V, $T_{opr} = -20^{\circ}\text{C}$ to $85^{\circ}\text{C}/-40^{\circ}\text{C}$ to 85°C , unless otherwise specified.

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det1}	Voltage detection level V_{det1_6} ⁽¹⁾	When V_{CC1} is falling.	2.80	3.10	3.40	V
	Voltage detection level V_{det1_B} ⁽¹⁾	When V_{CC1} is falling.	3.55	3.85	4.15	V
	Voltage detection level V_{det1_F} ⁽¹⁾	When V_{CC1} is falling.	4.15	4.45	4.75	V
-	Hysteresis width when V_{CC1} of voltage detector 1 is rising			0.15		V
-	Voltage detector 1 response time ⁽³⁾	When V_{CC1} falls from 5 V to $(V_{det1_0} - 0.1)$ V			200	μs
-	Voltage detector self power consumption	$VC26 = 1$, $V_{CC1} = 5.0$ V		1.7		μA
$t_{d(E-A)}$	Waiting time until voltage detector operation starts ⁽²⁾				100	μs

Notes:

1. Select the voltage detection level with bits VD1S0 to VD1S3 in the VD1LS register.
2. Necessary time until the voltage detector operates when setting to 1 again after setting the VC26 bit in the VCR2 register to 0.
3. Time from when passing the V_{det1} until when a voltage monitor 1 reset is generated.

Table 5.13 Voltage Detector 2 Electrical Characteristics

The measurement condition is $V_{CC1} = 2.7$ to 5.5 V, $T_{opr} = -20^{\circ}\text{C}$ to $85^{\circ}\text{C}/-40^{\circ}\text{C}$ to 85°C , unless otherwise specified.

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det2}	Voltage detection level V_{det2_0}	When V_{CC1} is falling	3.70	4.00	4.30	V
-	Hysteresis width at the rising of V_{CC1} in voltage detector 2			0.15		V
-	Voltage detector 2 response time ⁽²⁾	When V_{CC1} falls from 5 V to $(V_{det2_0} - 0.1)$ V			200	μs
-	Voltage detector self power consumption	$VC27 = 1$, $V_{CC1} = 5.0$ V		1.7		μA
$t_{d(E-A)}$	Waiting time until voltage detector operation starts ⁽¹⁾				100	μs

Notes:

1. Necessary time until the voltage detector operates after setting to 1 again after setting the VC27 bit in the VCR2 register to 0.
2. Time from when passing the V_{det2} until when a voltage monitor 2 reset is generated.

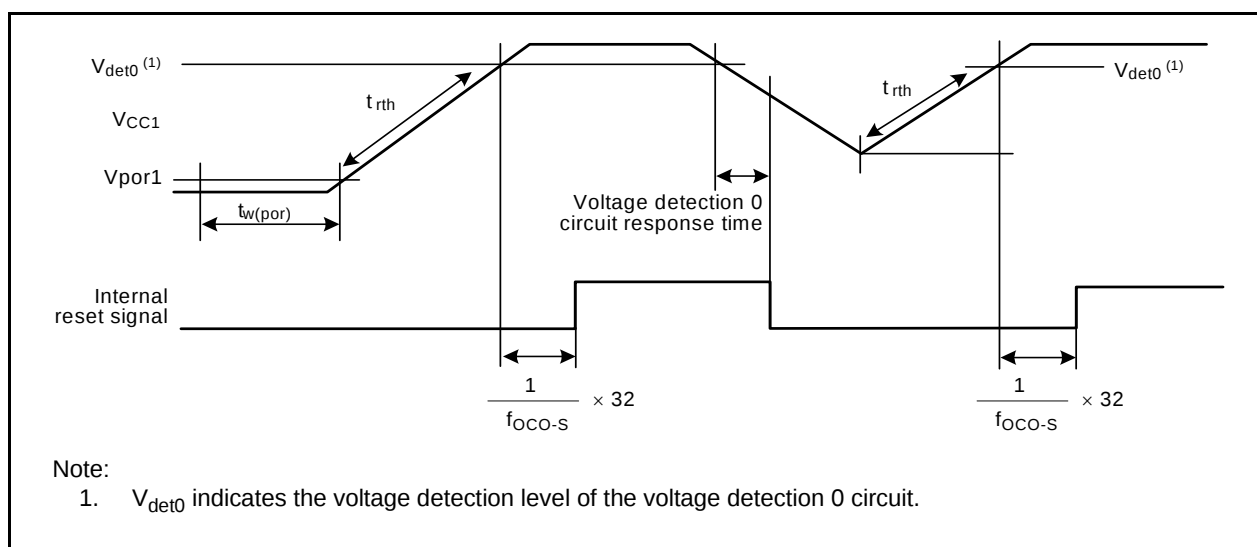
Table 5.14 Power-On Reset Circuit

The measurement condition is $V_{CC1} = 2.0$ to 5.5 V, $T_{opr} = -20^{\circ}\text{C}$ to $85^{\circ}\text{C}/-40^{\circ}\text{C}$ to 85°C , unless otherwise specified.

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{por1}	Voltage at which power-on reset enabled ⁽¹⁾				0.5	V
t_{rth}	External power V_{CC1} rise gradient		2.0		50000	mV/ms
$t_{w(por)}$	Time necessary to enable power-on reset		300			ms

Note:

1. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS1 address to 0. Also, set the VDSEL1 bit to 0 (V_{det0_2}).

**Figure 5.3 Power-On Reset Circuit Electrical Characteristics**

$$V_{CC1} = V_{CC2} = 5 \text{ V}$$

Table 5.19 Electrical Characteristics (2) (1)

$V_{CC1} = V_{CC2} = 4.2 \text{ to } 5.5 \text{ V}$, $V_{SS} = 0 \text{ V}$ at $T_{opr} = -20^\circ\text{C to } 85^\circ\text{C}/-40^\circ\text{C to } 85^\circ\text{C}$, $f_{(CLK)} = 32 \text{ MHz}$ unless otherwise specified.

Symbol	Parameter		Measuring Condition	Standard			Unit
				Min.	Typ.	Max.	
V _{T+} - V _{T-}	Hysteresis	HOLD, RDY, TA0IN to TA4IN, TB0IN to TB5IN, INT0 to INT7, NMI, ADTRG, CTS0 to CTS2, CTS5 to CTS7, SCL0 to SCL2, SCL5 to SCL7, SDA0 to SDA2, SDA5 to SDA7, CLK0 to CLK7, TA0OUT to TA4OUT, KI0 to KI3, RXD0 to RXD2, RXD5 to RXD7, SIN3, SIN4, SD, PMC0, PMC1, SCLMM, SDAMM, CEC, ZP, IDU, IDV, IDW		0.5		2.0	V
V _{T+} - V _{T-}	Hysteresis	RESET		0.5		2.5	V
I _{IH}	High input current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1 XIN, RESET, CNVSS, BYTE	V _I = 5 V			5.0	μA
I _{IL}	Low input current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1 XIN, RESET, CNVSS, BYTE	V _I = 0 V			−5.0	μA
R _{PULLUP}	Pull-up resistance	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1	V _I = 0 V	30	50	100	kΩ
R _{fXIN}	Feedback resistance XIN				1.5		MΩ
V _{RAM}	RAM retention voltage		In stop mode	1.8			V

Note:

1. When $V_{CC1} \neq V_{CC2}$, refer to 5 V or 3 V standard depending on the voltage.

$$V_{CC1} = V_{CC2} = 5 \text{ V}$$

Table 5.21 Electrical Characteristics (4)

R5F3651ECNFC, R5F3651KCNFC, R5F3650KCNFA, R5F3650KCNFB, R5F3651MCNFC, R5F3650MCNFA, R5F3650MCNFB, R5F3651NCNFC, R5F3650NCNFA, R5F3650NCNFB, R5F3651ECDFC, R5F3651KCDFC, R5F3650KCDFA, R5F3650KCDFB, R5F3651MCDFC, R5F3650MCDFA, R5F3650MCDFB, R5F3651NCDFC, R5F3650NCDFA, R5F3650NCDFB

$V_{CC1} = V_{CC2} = 4.2 \text{ to } 5.5 \text{ V}$, $V_{SS} = 0 \text{ V}$ at $T_{opr} = -20^\circ\text{C}$ to 85°C / -40°C to 85°C , $f_{(BCLK)} = 32 \text{ MHz}$ unless otherwise specified.

Symbol	Parameter	Measuring Condition	Standard			Unit
			Min.	Typ.	Max.	
R_{FXCIN}	Feedback resistance XCIN			8		MΩ
I_{CC}	Power supply current In single-chip, mode, the output pin are open and other pins are V_{SS}	High-speed mode	$f_{(BCLK)} = 32 \text{ MHz}$ XIN = 4 MHz (square wave), PLL multiplied by 8 125 kHz on-chip oscillator stopped	26.0		mA
			$f_{(BCLK)} = 32 \text{ MHz}$, A/D conversion XIN = 4 MHz (square wave), PLL multiplied by 8 125 kHz on-chip oscillator stopped	27.0		mA
			$f_{(BCLK)} = 20 \text{ MHz}$ XIN = 20 MHz (square wave) 125 kHz on-chip oscillator stopped	17.0		mA
		40 MHz on-chip oscillator mode	Main clock stopped 40 MHz on-chip oscillator on, divide-by-4 ($f_{(BCLK)} = 10 \text{ MHz}$) 125 kHz on-chip oscillator stopped	18.0		mA
		125 kHz on-chip oscillator mode	Main clock stopped 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator on, no division FMR22 = 1 (slow read mode)	550.0		μA
		Low-power mode	$f_{(BCLK)} = 32 \text{ kHz}$ In low-power mode FMR22 = FMR23 = 1 on flash memory ⁽¹⁾	170.0		μA
			$f_{(BCLK)} = 32 \text{ kHz}$ In low-power mode on RAM ⁽¹⁾	45.0		μA
		Wait mode	Main clock stopped 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator on Peripheral clock operating $T_{opr} = 25^\circ\text{C}$	20.5		μA
			$f_{(BCLK)} = 32 \text{ kHz}$ (oscillation capacity High) 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator stopped Peripheral clock operating $T_{opr} = 25^\circ\text{C}$	11.0		μA
			$f_{(BCLK)} = 32 \text{ kHz}$ (oscillation capacity low) 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator stopped Peripheral clock operating $T_{opr} = 25^\circ\text{C}$	6.0		μA
			XIN = 6 MHz 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator stopped Peripheral clock f1 provision disabled except timers (PCKSTP1A = 1) Main clock as a timer clock source (PCKSTP11 = 0, PCKSTP17 = 1) A given timer operating	1.2		mA
		Stop mode	Main clock stopped 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator stopped Peripheral clock stopped $T_{opr} = 25^\circ\text{C}$	1.7		μA
		During flash memory program	$f_{(BCLK)} = 10 \text{ MHz}$, PM17 = 1 (one wait) $V_{CC1} = 5.0 \text{ V}$	20.0		mA
		During flash memory erase	$f_{(BCLK)} = 10 \text{ MHz}$, PM17 = 1 (one wait) $V_{CC1} = 5.0 \text{ V}$	30.0		mA

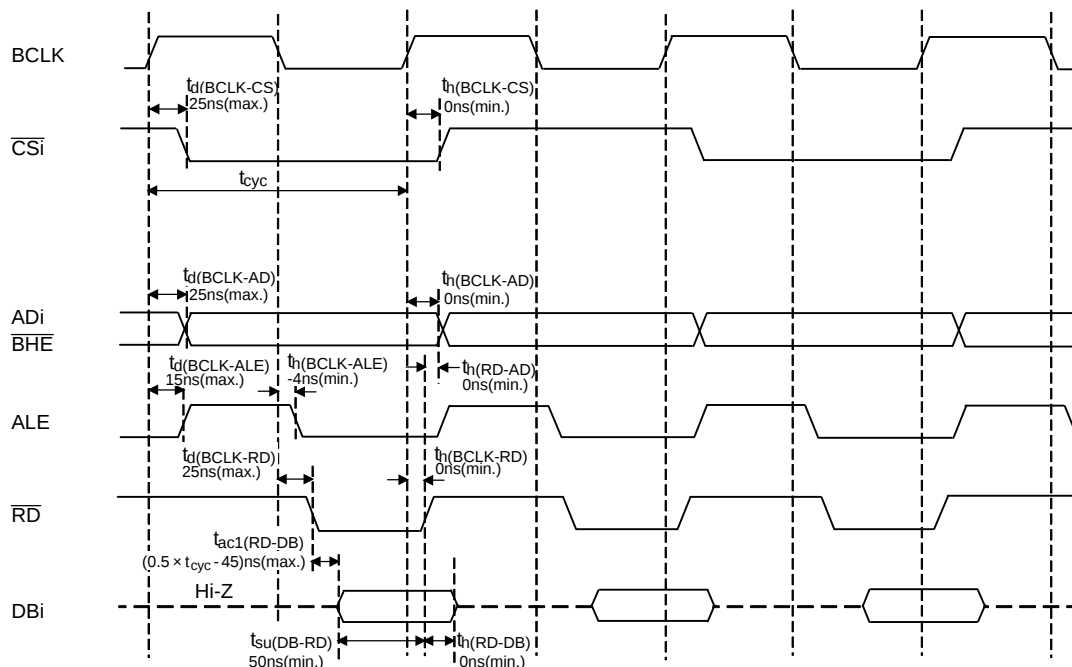
Note:

- This indicates the memory in which the program to be executed exists.

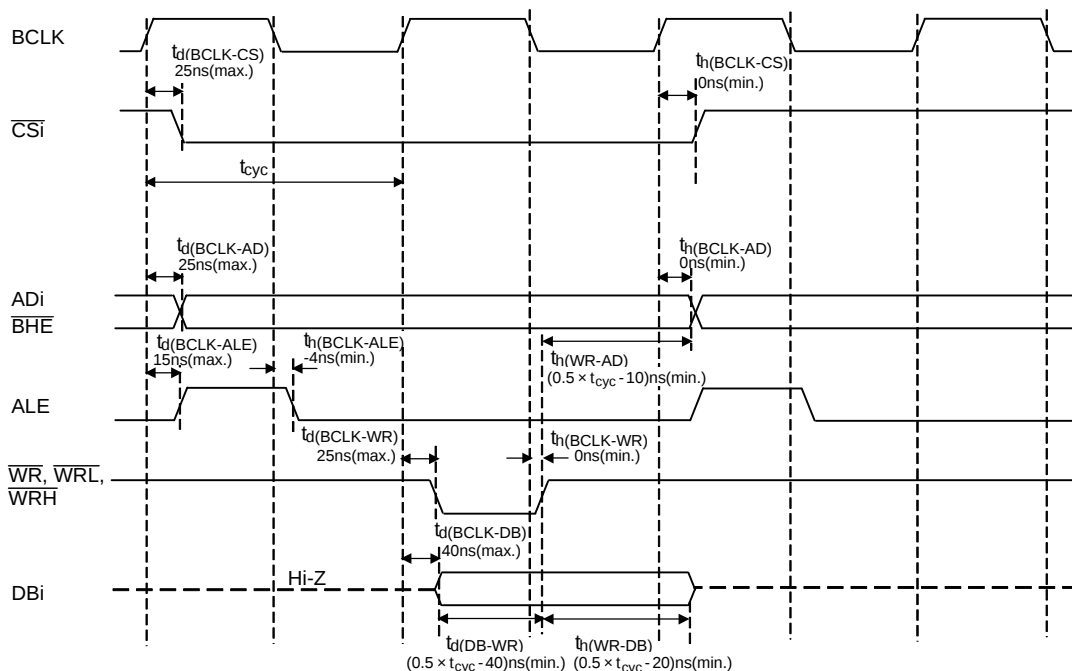
Memory Expansion Mode and Microprocessor Mode
(in no wait state setting)

$$V_{CC1} = V_{CC2} = 5V$$

Read timing



Write timing



$$t_{cyc} = \frac{1}{f(\text{BCLK})}$$

Measuring conditions

- $V_{CC1} = V_{CC2} = 5V$
- Input timing voltage: $V_L = 0.8V$, $V_H = 2.0V$
- Output timing voltage: $V_L = 0.4V$, $V_H = 2.4V$

Figure 5.15 Timing Diagram

$$V_{CC1} = V_{CC2} = 5 \text{ V}$$

Switching Characteristics

($V_{CC1} = V_{CC2} = 5 \text{ V}$, $V_{SS} = 0 \text{ V}$, at $T_{opr} = -20^{\circ}\text{C}$ to $85^{\circ}\text{C}/-40^{\circ}\text{C}$ to 85°C unless otherwise specified)

5.2.4.2 In 1 to 3 Waits Setting and When Accessing External Area**Table 5.37 Memory Expansion Mode and Microprocessor Mode (in 1 to 3 Waits Setting and When Accessing External Area)**

Symbol	Parameter	Measuring Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	See Figure 5.14		25	ns
$t_{h(BCLK-AD)}$	Address output hold time (in relation to BCLK)		0		ns
$t_{h(RD-AD)}$	Address output hold time (in relation to RD)		0		ns
$t_{h(WR-AD)}$	Address output hold time (in relation to WR)		(Note 2)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			25	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (in relation to BCLK)		0		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time			15	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time		-4		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			25	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			25	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (in relation to BCLK)			40	ns
$t_{d(DB-WR)}$	Data output delay time (in relation to WR)		(Note 1)		ns
$t_{h(WR-DB)}$	Data output hold time (in relation to WR) ⁽³⁾		(Note 4)		ns

Notes:

1. Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5) \times 10^9}{f_{(BCLK)}} - 40 [ns] \quad \begin{array}{l} n \text{ is 1 for 1 wait setting, 2 for 2 waits setting and 3 for 3 waits setting.} \\ \text{When } n = 1, f_{(BCLK)} \text{ is 12.5 MHz or less.} \end{array}$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f_{(BCLK)}} - 10 [ns]$$

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.
Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.

Hold time of data bus is expressed in

$$t = -CR \times \ln(1 - V_{OL}/V_{CC2})$$

by a circuit of the right figure.

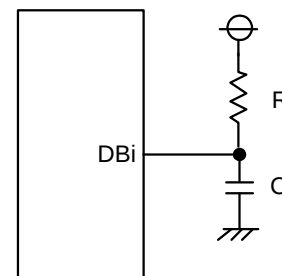
For example, when $V_{OL} = 0.2V_{CC2}$, $C = 30 \text{ pF}$, $R = 1 \text{ k}\Omega$, hold time of output low level is

$$t = -30 \text{ pF} \times 1 \text{ k}\Omega \times \ln(1 - 0.2V_{CC2}/V_{CC2}) = 6.7 \text{ ns.}$$

4. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f_{(BCLK)}} - 20 [ns]$$

Hold time is equal to or less than 0 ns when the BCLK frequency exceeds 25 MHz.



$$V_{CC1} = V_{CC2} = 3 \text{ V}$$

Table 5.42 Electrical Characteristics (2)

R5F36506CNFA, R5F36506CNFB, R5F36506CDFA, R5F36506CDFB, R5F3650ECNFA, R5F3650ECNFB,
R5F3650ECDFA, R5F3650ECDFB

$V_{CC1} = V_{CC2} = 2.7$ to 3.3 V , $V_{SS} = 0 \text{ V}$ at $T_{opr} = -20^{\circ}\text{C}$ to $85^{\circ}\text{C}/-40^{\circ}\text{C}$ to 85°C , $f_{(BCLK)} = 32 \text{ MHz}$ unless otherwise specified.

Symbol	Parameter	Measuring Condition	Standard			Unit
			Min.	Typ.	Max.	
R_{FXCIN}	Feedback resistance XCIN			16		$M\Omega$
I_{CC}	Power supply current In single-chip, mode, the output pin are open and other pins are V_{SS}	High-speed mode	$f_{(BCLK)} = 32 \text{ MHz}$ XIN = 4 MHz (square wave), PLL multiplied by 8 125 kHz on-chip oscillator stopped	24.0		mA
			$f_{(BCLK)} = 32 \text{ MHz}$, A/D conversion XIN = 4 MHz (square wave), PLL multiplied by 8 125 kHz on-chip oscillator stopped	24.7		mA
			$f_{(BCLK)} = 20 \text{ MHz}$ XIN = 20 MHz (square wave) 125 kHz on-chip oscillator stopped	16.0		mA
		40 MHz on-chip oscillator mode	Main clock stopped 40 MHz on-chip oscillator on, divide-by-4 ($f_{(BCLK)} = 10 \text{ MHz}$) 125 kHz on-chip oscillator stopped	17.0		mA
		125 kHz on-chip oscillator mode	Main clock stopped 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator on, no division FMR22 = 1 (slow read mode)	450.0		μA
		Low-power mode	$f_{(BCLK)} = 32 \text{ MHz}$ In low-power mode FMR 22 = FMR23 = 1 On flash memory ⁽¹⁾	160.0		μA
			$f_{(BCLK)} = 32 \text{ MHz}$ In low-power mode On RAM ⁽¹⁾	40.0		μA
		Wait mode	Main clock stopped 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator on Peripheral clock operating $T_{opr} = 25^{\circ}\text{C}$	20.0		μA
			$f_{(BCLK)} = 32 \text{ MHz}$ (oscillation capacity High) 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator stopped Peripheral clock operating $T_{opr} = 25^{\circ}\text{C}$	8.0		μA
			$f_{(BCLK)} = 32 \text{ kHz}$ (oscillation capacity Low) 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator stopped Peripheral clock operating $T_{opr} = 25^{\circ}\text{C}$	4.0		μA
			XIN = 6 MHz 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator stopped Peripheral clock f1 provision disabled except timers (PCKSTP1A = 1) Main clock as a timer clock source (PCKSTP11 = 0, PCKSTP17 = 1) A given timer operating	0.5		mA
		Stop mode	Main clock stopped 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator stopped Peripheral clock stopped $T_{opr} = 25^{\circ}\text{C}$	1.6		μA
		During flash memory program	$f_{(BCLK)} = 10 \text{ MHz}$, PM17 = 1 (one wait) $V_{CC1} = 3.0 \text{ V}$	20.0		mA
		During flash memory erase	$f_{(BCLK)} = 10 \text{ MHz}$, PM17 = 1 (one wait) $V_{CC1} = 3.0 \text{ V}$	30.0		mA

Note:

1. This indicates the memory in which the program to be executed exists.

$$V_{CC1} = V_{CC2} = 3\text{ V}$$

Timing Requirements

($V_{CC1} = V_{CC2} = 3\text{ V}$, $V_{SS} = 0\text{ V}$, at $T_{opr} = -20^{\circ}\text{C}$ to $85^{\circ}\text{C}/-40^{\circ}\text{C}$ to 85°C unless otherwise specified)

5.3.2.4 Timer B Input**Table 5.52 Timer B Input (Counter Input in Event Counter Mode)**

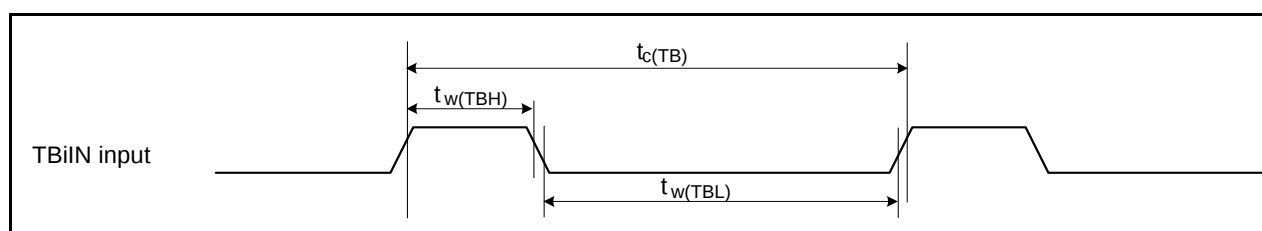
Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time (counted on one edge)	150		ns
$t_{w(TBH)}$	TBiIN input high pulse width (counted on one edge)	60		ns
$t_{w(TBL)}$	TBiIN input low pulse width (counted on one edge)	60		ns
$t_{c(TB)}$	TBiIN input cycle time (counted on both edges)	300		ns
$t_{w(TBH)}$	TBiIN input high pulse width (counted on both edges)	120		ns
$t_{w(TBL)}$	TBiIN input low pulse width (counted on both edges)	120		ns

Table 5.53 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	600		ns
$t_{w(TBH)}$	TBiIN input high pulse width	300		ns
$t_{w(TBL)}$	TBiIN input low pulse width	300		ns

Table 5.54 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	600		ns
$t_{w(TBH)}$	TBiIN input high pulse width	300		ns
$t_{w(TBL)}$	TBiIN input low pulse width	300		ns

**Figure 5.24 Timer B Input**

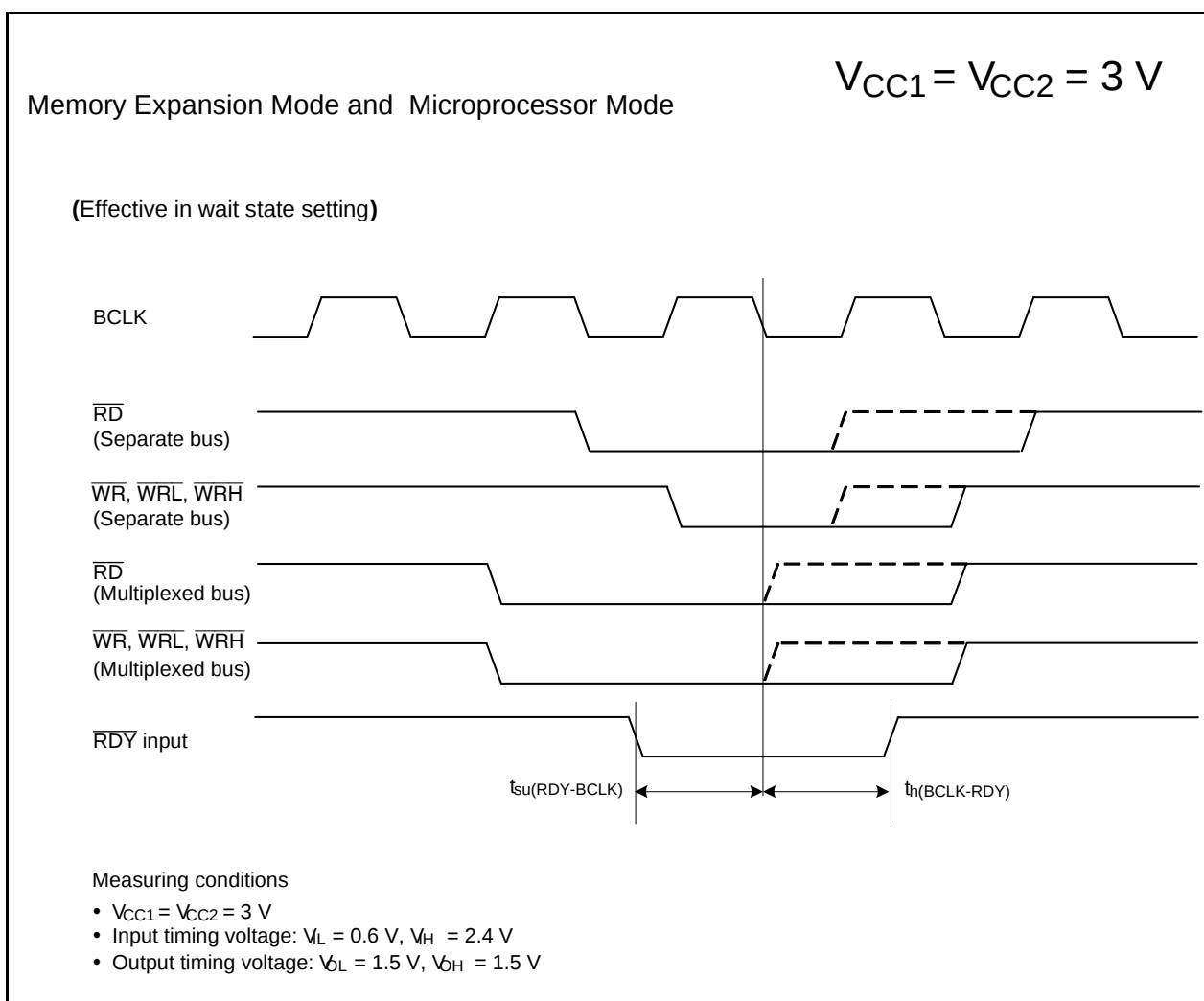


Figure 5.28 Timing Diagram

$$V_{CC1} = V_{CC2} = 3 \text{ V}$$

5.3.4 Switching Characteristics (Memory Expansion Mode and Microprocessor Mode)

($V_{CC1} = V_{CC2} = 3 \text{ V}$, $V_{SS} = 0 \text{ V}$, at $T_{opr} = -20^{\circ}\text{C}$ to $85^{\circ}\text{C}/-40^{\circ}\text{C}$ to 85°C unless otherwise specified)

5.3.4.1 In No Wait State Setting

Table 5.59 Memory Expansion and Microprocessor Modes (in No Wait State Setting)

Symbol	Parameter	Measuring Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	See Figure 5.29		30	ns
$t_{h(BCLK-AD)}$	Address output hold time (in relation to BCLK)		0		ns
$t_{h(RD-AD)}$	Address output hold time (in relation to RD)		0		ns
$t_{h(WR-AD)}$	Address output hold time (in relation to WR)		(Note 2)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			30	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (in relation to BCLK)		0		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time			25	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time		-4		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			30	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			30	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (in relation to BCLK)			40	ns
$t_{d(DB-WR)}$	Data output delay time (in relation to WR)		(Note 1)		ns
$t_{h(WR-DB)}$	Data output hold time (in relation to WR) ⁽³⁾		(Note 4)		ns

Notes:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f_{(BCLK)}} - 40 [\text{ns}] \quad f_{(BCLK)} \text{ is } 12.5 \text{ MHz or less.}$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f_{(BCLK)}} - 15 [\text{ns}]$$

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.
Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.

Hold time of data bus is expressed in

$$t = -CR \times \ln(1 - V_{OL}/V_{CC2})$$

by a circuit of the right figure.

For example, when $V_{OL} = 0.2V_{CC2}$, $C = 30 \text{ pF}$, $R = 1 \text{ k}\Omega$,

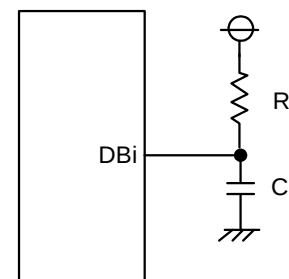
hold time of output low level is

$$t = -30 \text{ pF} \times 1 \text{ k}\Omega \times \ln(1 - 0.2V_{CC2}/V_{CC2}) = 6.7 \text{ ns.}$$

4. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f_{(BCLK)}} - 25 [\text{ns}]$$

Hold time is equal to or less than 0 ns when the BCLK frequency exceeds 20 MHz.



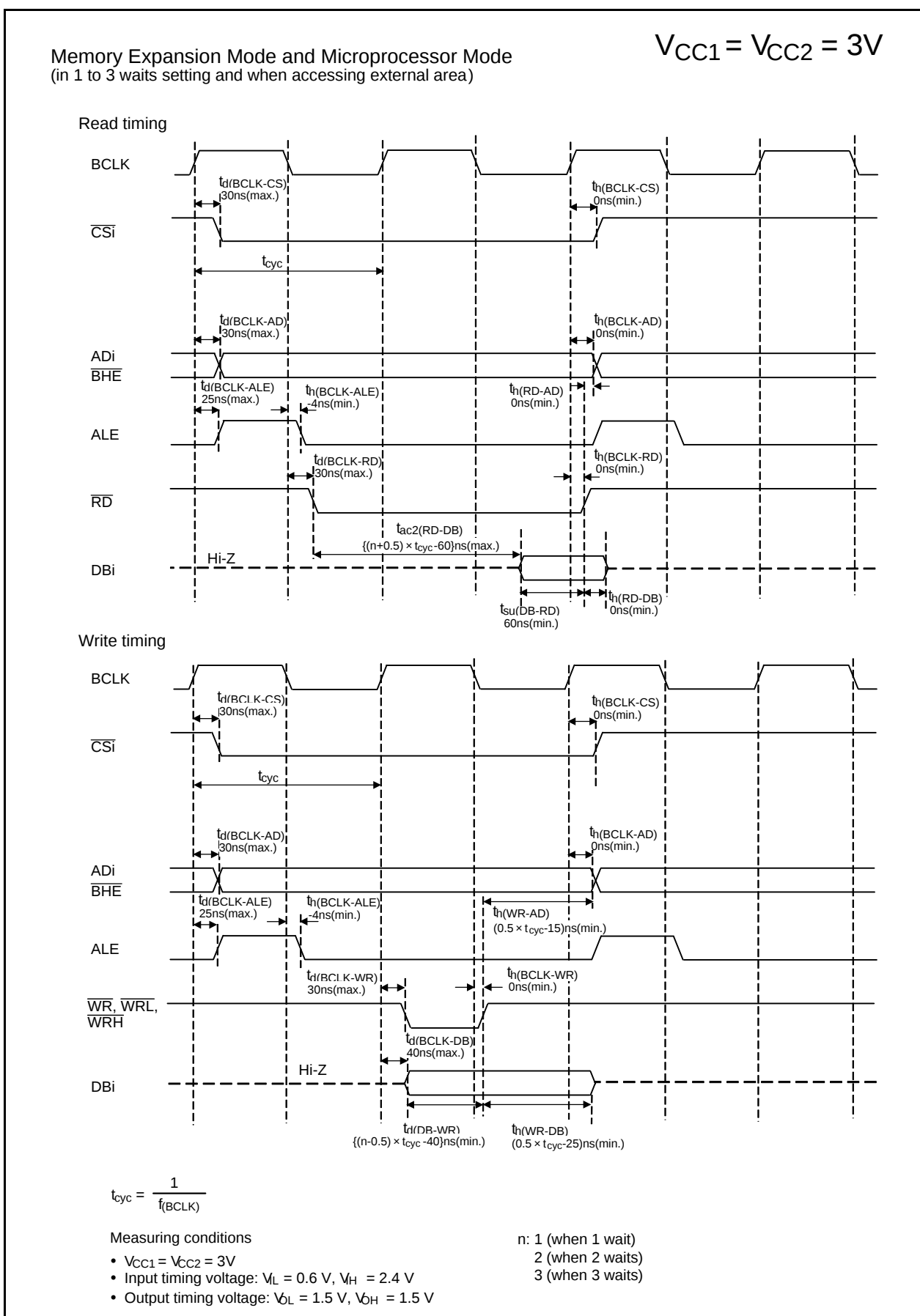


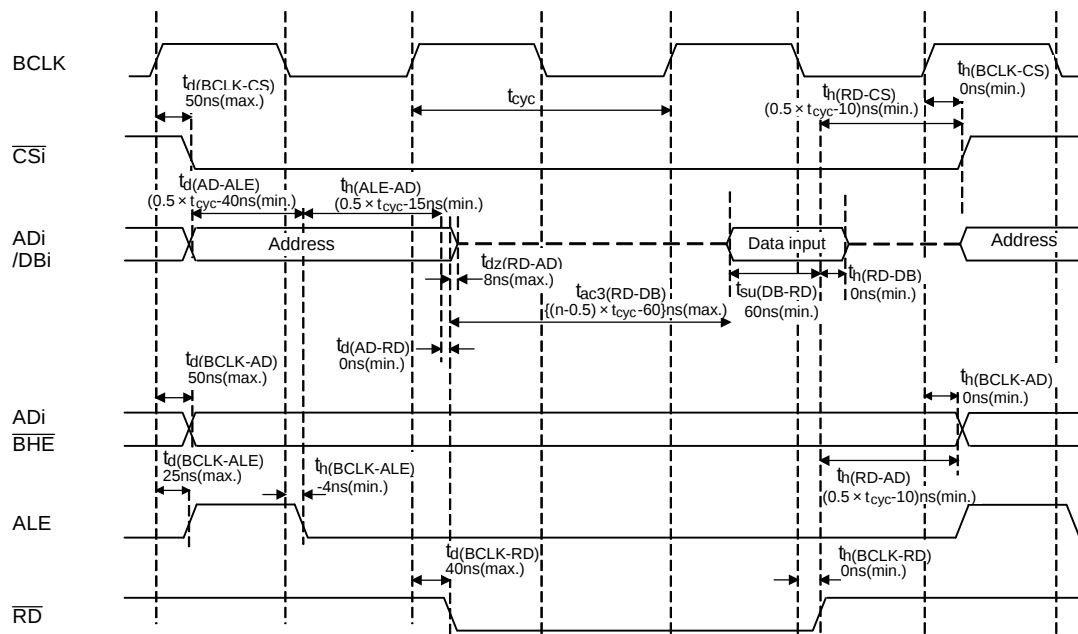
Figure 5.31 Timing Diagram

Memory Expansion Mode and Microprocessor Mode

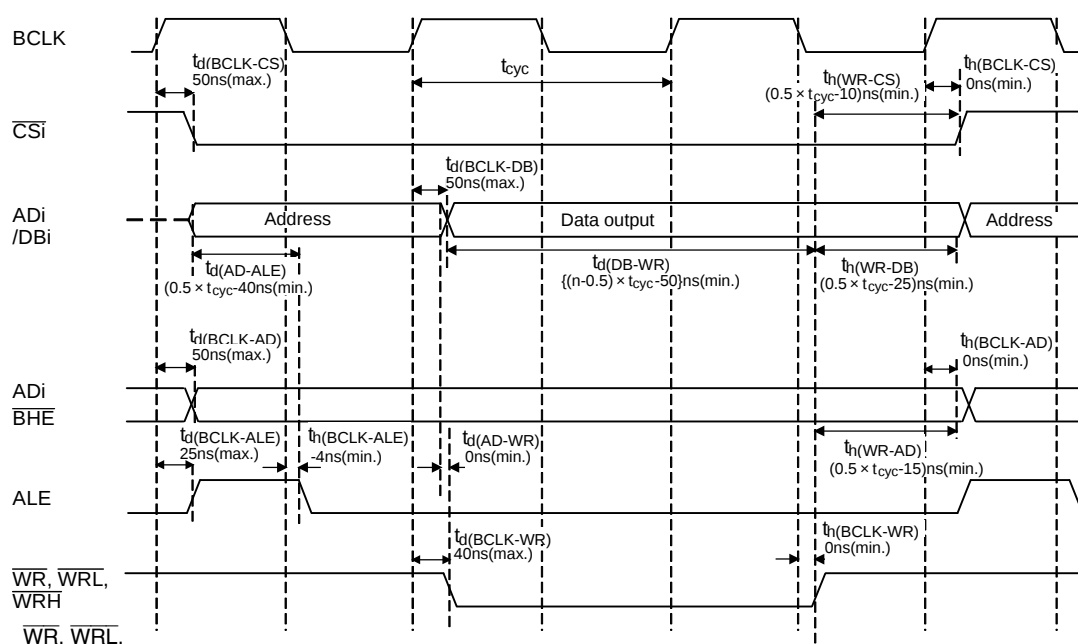
(in 2 or 3 waits setting, and when accessing external area and using multiplexed bus)

$$V_{CC1} = V_{CC2} = 3V$$

Read timing



Write timing



$$t_{cyc} = \frac{1}{f_{BCLK}}$$

Measuring conditions

- $V_{CC1} = V_{CC2} = 3V$
- Input timing voltage: $V_L = 0.6V$, $V_H = 2.4V$
- Output timing voltage: $V_{OL} = 1.5V$, $V_{OH} = 1.5V$

n: 2 (when 2 waits)
3 (when 3 waits)

Figure 5.32 Timing Diagram

