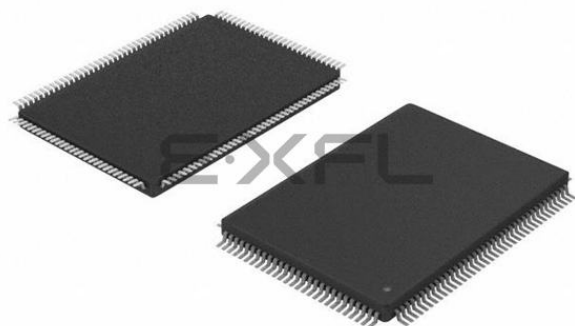




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Details

Product Status	Obsolete
Core Processor	M16C/60
Core Size	16-Bit
Speed	32MHz
Connectivity	EBI/EMI, I ² C, SIO, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	111
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	31K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	128-LQFP
Supplier Device Package	128-LFQFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f3651mcnfc-v0

1.2 Specifications

The M16C/65C Group includes 128-pin and 100-pin packages. Table 1.1 to Table 1.4 list specifications.

Table 1.1 Specifications for the 128-Pin Package (1/2)

Item	Function	Description
CPU	Central processing unit	M16C/60 Series core (multiplier: 16 bit × 16 bit → 32 bit, multiply and accumulate instruction: 16 bit × 16 bit + 32 bit → 32 bit) • Number of basic instructions: 91 • Minimum instruction execution time: 31.25 ns (f(BCLK) = 32 MHz, VCC1 = VCC2 = 2.7 to 5.5 V) • Operating modes: Single-chip, memory expansion, and microprocessor
Memory	ROM, RAM, data flash	See Table 1.5 "Product List (N-Version)" to Table 1.6 "Product List (D-Version)".
Voltage Detection	Voltage detector	• Power-on reset • 3 voltage detection points (detection level of voltage detection 0 and 1 selectable)
Clock	Clock generator	• 5 circuits: Main clock, sub clock, low-speed on-chip oscillator (125 kHz), high-speed on-chip oscillator (40 MHz ±5%), PLL frequency synthesizer • Oscillation stop detection: Main clock oscillation stop/restart detection function • Frequency divider circuit: Divide ratio selectable from 1, 2, 4, 8, and 16 • Power saving features: Wait mode, stop mode • Real-time clock
External Bus Expansion	Bus memory expansion	• Address space: 1 MB • External bus interface: 0 to 8 waits inserted, 4 chip select outputs, memory area expansion function (expandable to 4 MB), 3 V and 5 V interfaces • Bus format: Separate bus or multiplexed bus selectable, data bus width selectable (8 or 16 bits), number of address buses selectable (12, 16, or 20)
I/O Ports	Programmable I/O ports	• CMOS I/O ports: 111 (selectable pull-up resistors) • N-channel open drain ports: 3
Interrupts		• Interrupt vectors: 70 • External interrupt inputs: 13 ($\overline{\text{NMI}}$, $\overline{\text{INT}} \times 8$, key input × 4) • Interrupt priority levels: 7
Watchdog Timer		15-bit timer × 1 (with prescaler) Automatic reset start function selectable
DMA	DMAC	• 4 channels, cycle steal mode • Trigger sources: 43 • Transfer modes: 2 (single transfer, repeat transfer)

1.5 Pin Assignments

Figure 1.5 to Figure 1.7 show pin assignments. Table 1.7 to Table 1.11 list pin names.

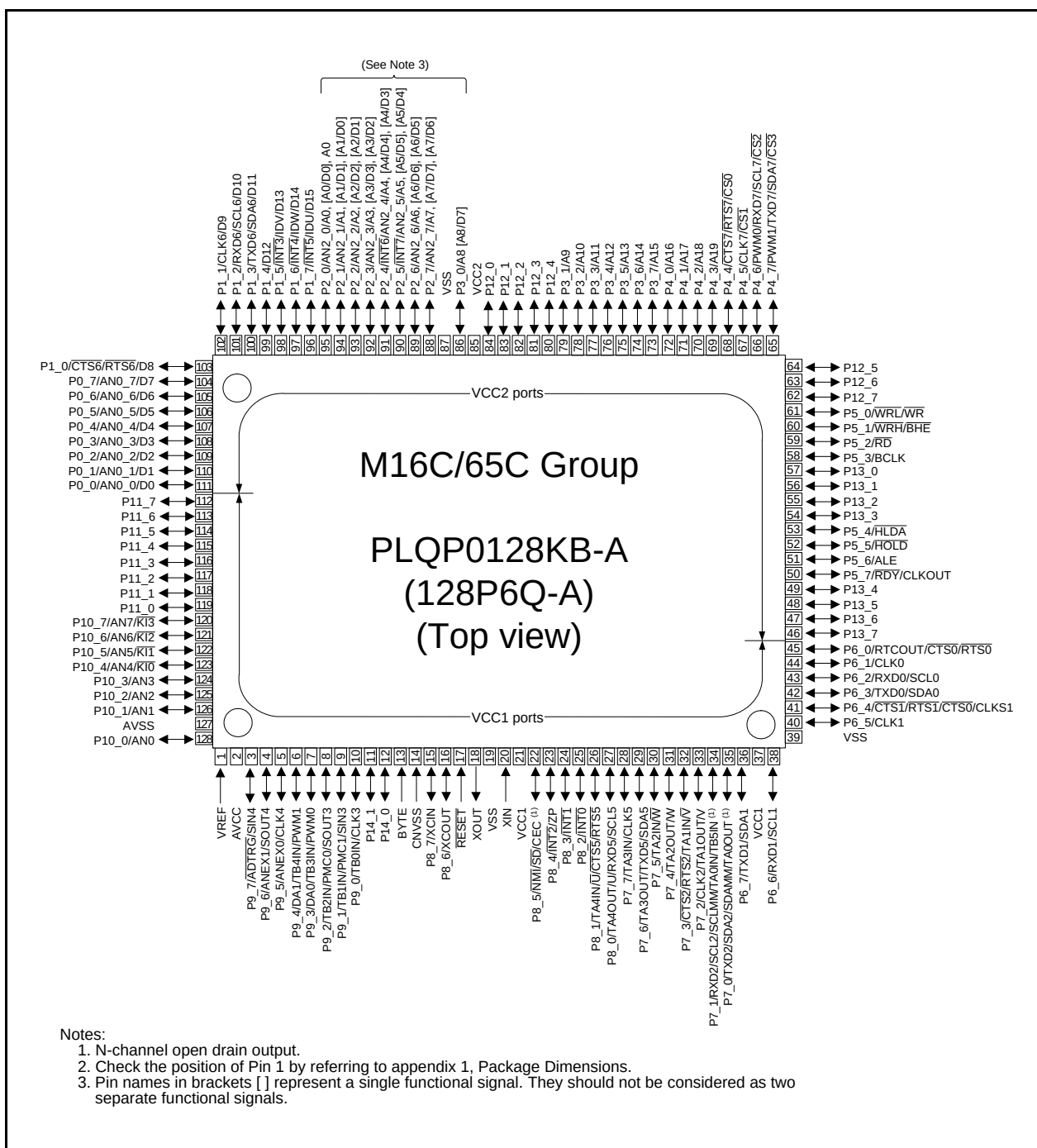


Figure 1.5 Pin Assignment for the 128-Pin Package

Table 1.9 Pin Names for the 128-Pin Package (3/3)

Pin No.	Control Pin	Port	I/O Pin for Peripheral Function				Bus Control Pin
			Interrupt	Timer	Serial interface	A/D converter, D/A converter	
101		P1_2			RXD6/SCL6		D10
102		P1_1			CLK6		D9
103		P1_0			CTS6/RTS6		D8
104		P0_7				AN0_7	D7
105		P0_6				AN0_6	D6
106		P0_5				AN0_5	D5
107		P0_4				AN0_4	D4
108		P0_3				AN0_3	D3
109		P0_2				AN0_2	D2
110		P0_1				AN0_1	D1
111		P0_0				AN0_0	D0
112		P11_7					
113		P11_6					
114		P11_5					
115		P11_4					
116		P11_3					
117		P11_2					
118		P11_1					
119		P11_0					
120		P10_7	KI3			AN7	
121		P10_6	KI2			AN6	
122		P10_5	KI1			AN5	
123		P10_4	KI0			AN4	
124		P10_3				AN3	
125		P10_2				AN2	
126		P10_1				AN1	
127	AVSS						
128		P10_0				AN0	

Table 1.16 Pin Functions for the 100-Pin Package (2/3)

Signal Name	Pin Name	I/O	Power Supply	Description
Main clock input	XIN	I	VCC1	I/O for the main clock oscillator. Connect a ceramic resonator or crystal between pins XIN and XOUT. ⁽¹⁾ Input an external clock to XIN pin and leave XOUT pin open.
Main clock output	XOUT	O	VCC1	
Sub clock input	XCIN	I	VCC1	I/O for a sub clock oscillator. Connect a crystal between XCIN pin and XCOUT pin. ⁽¹⁾ Input an external clock to XCIN pin and leave XCOUT pin open.
Sub clock output	XCOUT	O	VCC1	
BCLK output	BCLK	O	VCC2	Outputs the BCLK signal.
Clock output	CLKOUT	O	VCC2	Outputs a clock with the same frequency as f _C , f ₁ , f ₈ , or f ₃₂ .
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT2}}$	I	VCC1	Input for the $\overline{\text{INT}}$ interrupt.
	$\overline{\text{INT3}}$ to $\overline{\text{INT7}}$	I	VCC2	
$\overline{\text{NMI}}$ interrupt input	$\overline{\text{NMI}}$	I	VCC1	Input for the $\overline{\text{NMI}}$ interrupt.
Key input interrupt input	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	VCC1	Input for the key input interrupt.
Timer A	TA0OUT to TA4OUT	I/O	VCC1	I/O for timers A0 to A4 (TA0OUT is N-channel open drain output).
	TA0IN to TA4IN	I	VCC1	Input for timers A0 to A4.
	ZP	I	VCC1	Input for Z-phase.
Timer B	TB0IN to TB5IN	I	VCC1	Input for timers B0 to B5.
Three-phase motor control timer	U, $\overline{\text{U}}$, V, $\overline{\text{V}}$, W, $\overline{\text{W}}$	O	VCC1	Output for the three-phase motor control timer.
	$\overline{\text{SD}}$	I	VCC1	Forced cutoff input.
	IDU, IDV, IDW	I	VCC2	Input for the position data.
Real-time clock output	RTCOUT	O	VCC1	Output for the real-time clock.
PWM output	PWM0, PWM1	O	VCC1, VCC2	PWM output.
Remote control signal receiver input	PMC0, PMC1	I	VCC1	Input for the remote control signal receiver.
Serial interface UART0 to UART2, UART5 to UART7	CTS0 to CTS2, CTS5	I	VCC1	Input pins to control data transmission.
	CTS6, CTS7	I	VCC2	
	RTS0 to RTS2, RTS5	O	VCC1	Output pins to control data reception.
	RTS6, RTS7	O	VCC2	
	CLK0 to CLK2, CLK5	I/O	VCC1	Transmit/receive clock I/O.
	CLK6, CLK7	I/O	VCC2	
	RXD0 to RXD2, RXD5	I	VCC1	Serial data input.
	RXD6, RXD7	I	VCC2	
	TXD0 to TXD2, TXD5	O	VCC1	Serial data output. ⁽²⁾
	TXD6, TXD7	O	VCC2	
	CLKS1	O	VCC1	Output for the transmit/receive clock multiple-pin output function.

Notes:

- Contact the manufacturer of crystal/ceramic resonator regarding the oscillation characteristics.
- TXD2, SDA2, and SCL2 are N-channel open drain output pins. TXDi (i = 0, 1, 5 to 7), SDAi, and SCLi can be selected as CMOS output pins or N-channel open drain output pins.

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers. Seven registers (R0, R1, R2, R3, A0, A1, and FB) out of 13 compose a register bank, and there are two register banks.

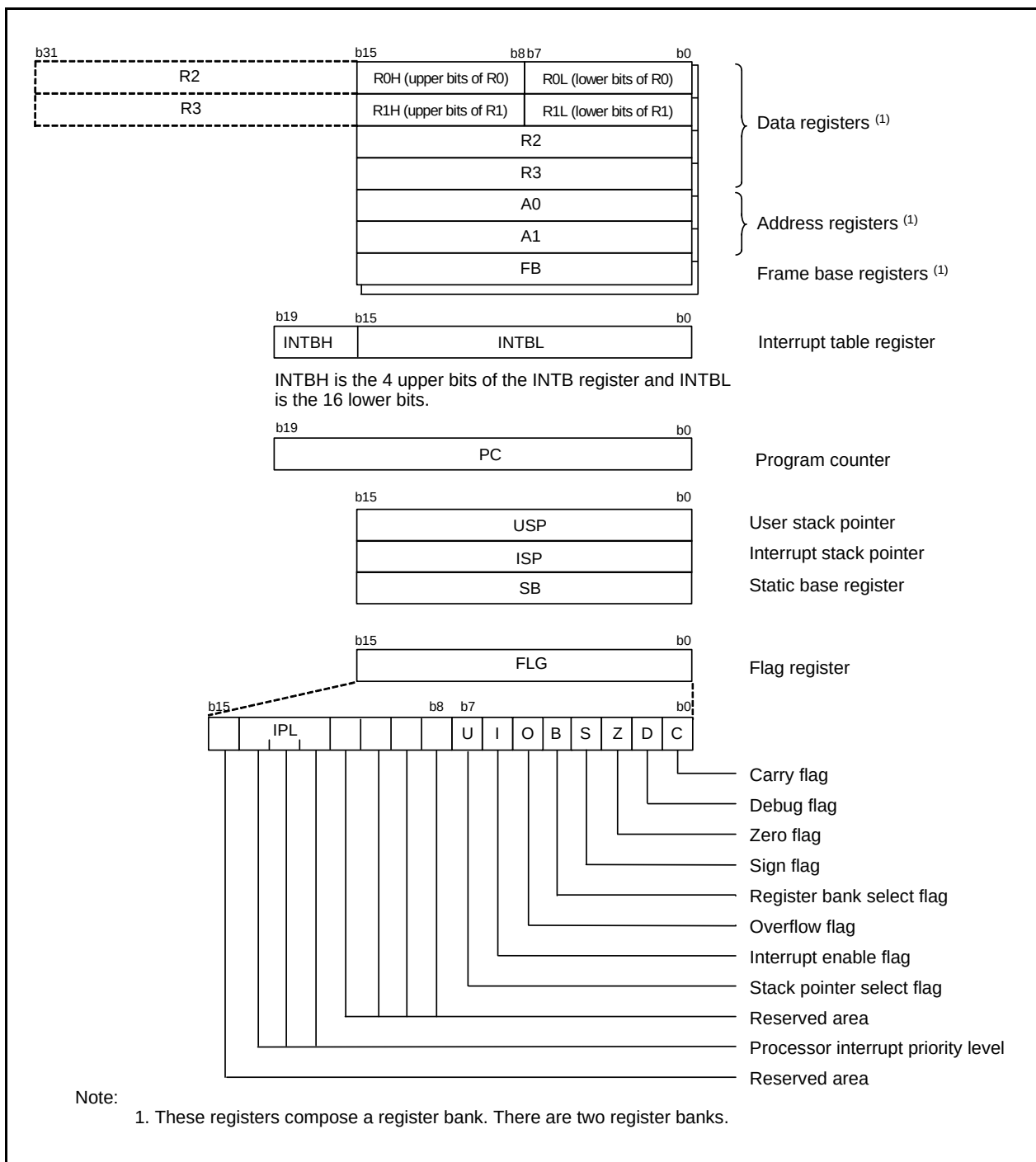


Figure 2.1 CPU Registers

3. Address Space

3.1 Address Space

The M16C/65C Group has a 1 MB address space from 00000h to FFFFFh. Address space is expandable to 4 MB with the memory area expansion function. Addresses 40000h to BFFFFh can be used as external areas from bank 0 to bank 7. Figure 3.1 shows the Address Space. Areas that can be accessed vary depending on processor mode and the status of each control bit.

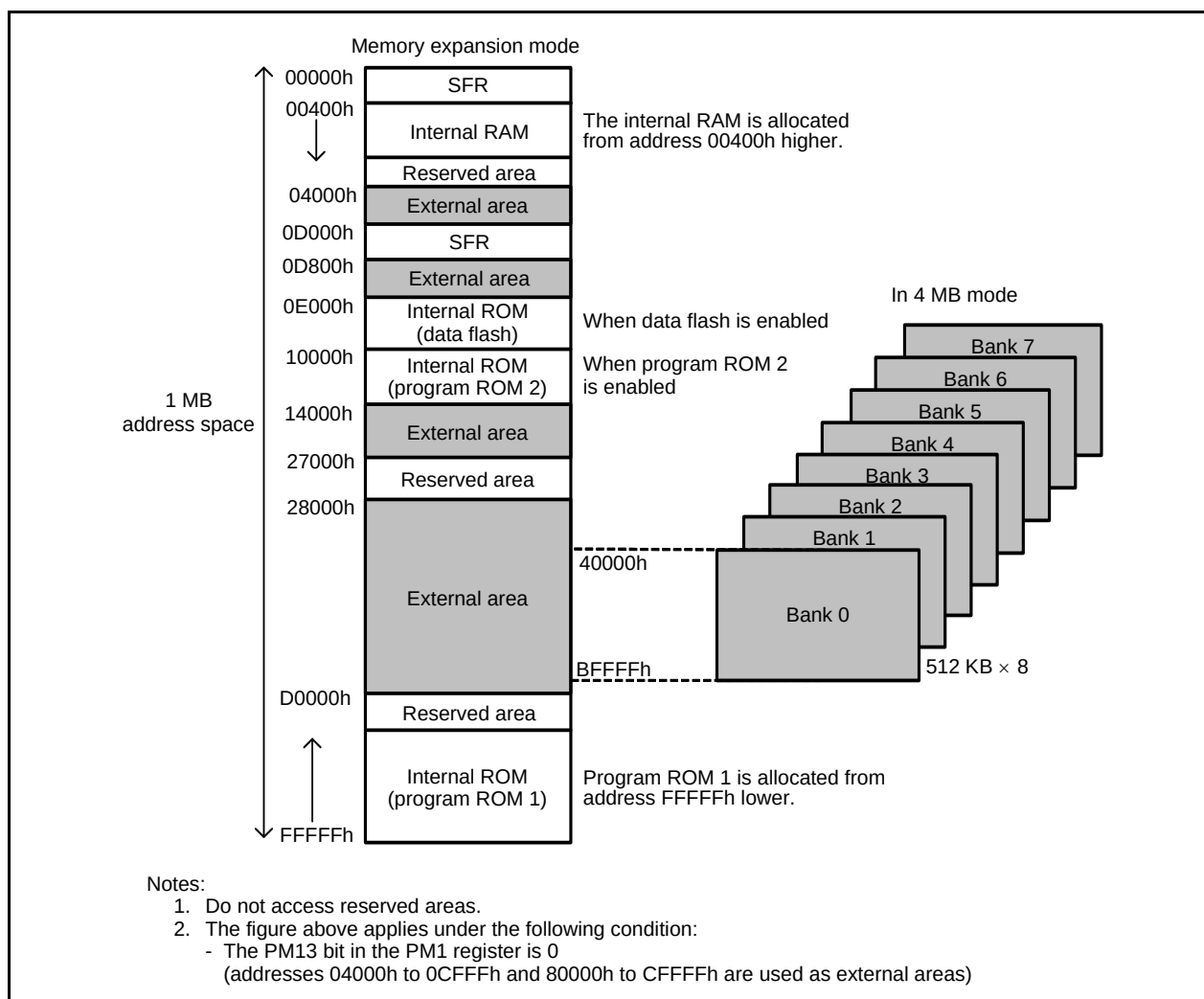


Figure 3.1 Address Space

3.2 Memory Map

Special function registers (SFRs) are allocated from address 00000h to 003FFh and from 0D000h to 0D7FFh. Peripheral function control registers are located here. All blank areas within SFRs are reserved. Do not access these areas.

Internal RAM is allocated from address 00400h and higher, with 10 KB of internal RAM allocated from 00400h to 02BFFh. Internal RAM is used not only for data storage, but also for the stack area when subroutines are called or when an interrupt request is accepted.

The internal ROM is flash memory. Three internal ROM areas are available: data flash, program ROM 1, and program ROM 2.

The data flash is allocated from 0E000h to 0FFFFh. This data flash area is mostly used for data storage, but can also store programs.

Program ROM 2 is allocated from 10000h to 13FFFh. Program ROM 1 is allocated from FFFFFh and lower, with the 64 KB program ROM 1 area allocated from address F0000h to FFFFFh.

The special page vectors are allocated from FFE00h to FFFD7h. They are used for the JMPS and JSRS instructions. Refer to the M16C/60, M16C/20, M16C/Tiny Series Software Manual for details.

The fixed vector table for interrupts is allocated from FFFDCh to FFFFFh.

The 256 bytes beginning with the start address set in the INTB register compose the relocatable vector table for interrupts.

Figure 3.2 shows the Memory Map.

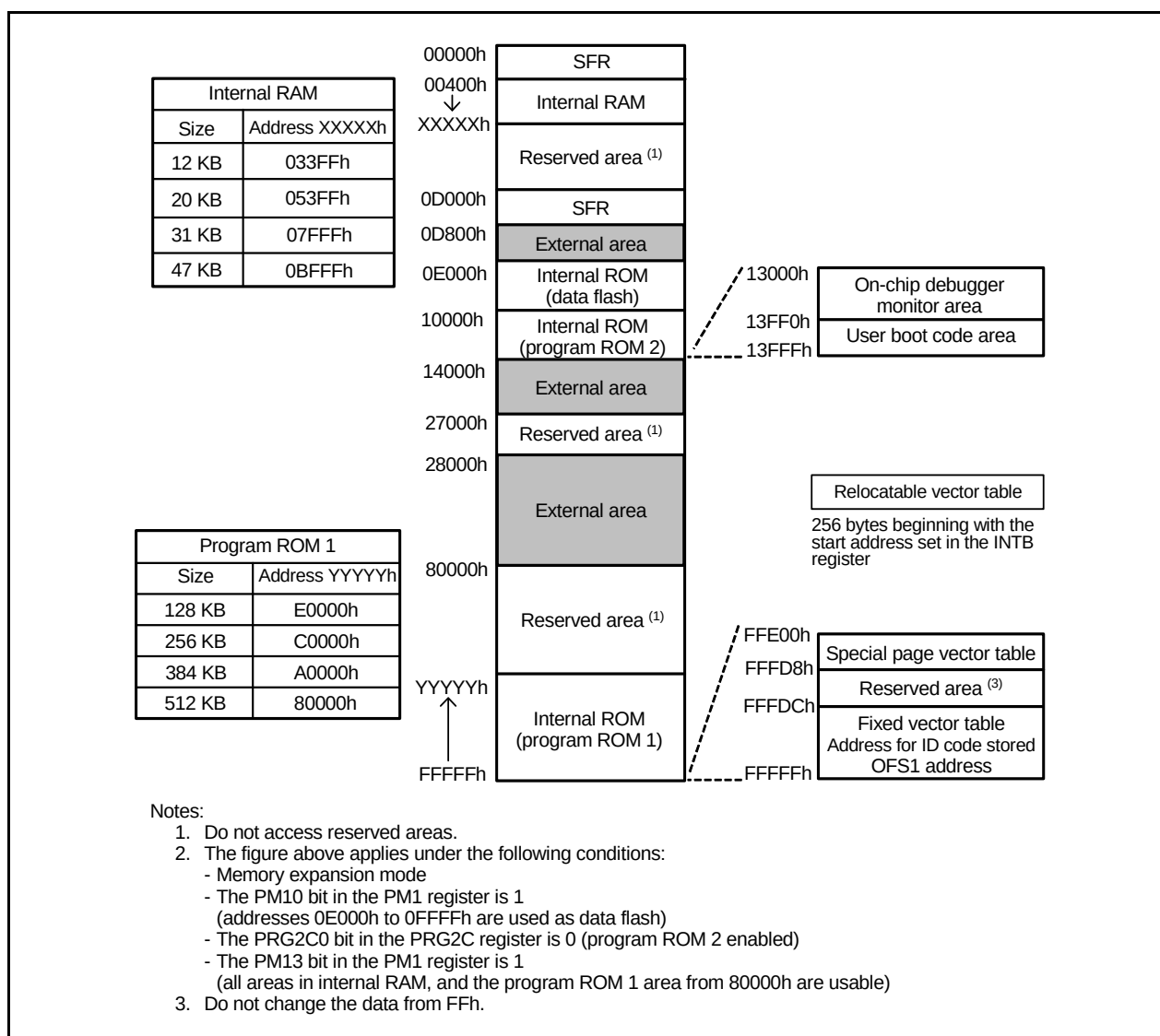


Figure 3.2 Memory Map

Table 4.4 SFR Information (4) ⁽¹⁾

Address	Register	Symbol	Reset Value
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h	DMA2 Interrupt Control Register	DM2IC	XXXX X000b
006Ah	DMA3 Interrupt Control Register	DM3IC	XXXX X000b
006Bh	UART5 Bus Collision Detection Interrupt Control Register CEC1 Interrupt Control Register	U5BCNIC CEC1IC	XXXX X000b
006Ch	UART5 Transmit Interrupt Control Register CEC2 Interrupt Control Register	S5TIC CEC2IC	XXXX X000b
006Dh	UART5 Receive Interrupt Control Register	S5RIC	XXXX X000b
006Eh	UART6 Bus Collision Detection Interrupt Control Register Real-Time Clock Periodic Interrupt Control Register	U6BCNIC RTCTIC	XXXX X000b
006Fh	UART6 Transmit Interrupt Control Register Real-Time Clock Compare Interrupt Control Register	S6TIC RTCCIC	XXXX X000b
0070h	UART6 Receive Interrupt Control Register	S6RIC	XXXX X000b
0071h	UART7 Bus Collision Detection Interrupt Control Register Remote Control Signal Receiver 0 Interrupt Control Register	U7BCNIC PMC0IC	XXXX X000b
0072h	UART7 Transmit Interrupt Control Register Remote Control Signal Receiver 1 Interrupt Control Register	S7TIC PMC1IC	XXXX X000b
0073h	UART7 Receive Interrupt Control Register	S7RIC	XXXX X000b
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh	I2C-bus Interface Interrupt Control Register	IICIC	XXXX X000b
007Ch	SCL/SDA Interrupt Control Register	SCLDAIC	XXXX X000b
007Dh			
007Eh			
007Fh			
0080h to 017Fh			

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 4.6 SFR Information (6) ⁽¹⁾

Address	Register	Symbol	Reset Value
01B0h	DMA3 Source Pointer	SAR3	XXh
01B1h			XXh
01B2h			0Xh
01B3h			
01B4h	DMA3 Destination Pointer	DAR3	XXh
01B5h			XXh
01B6h			0Xh
01B7h			
01B8h	DMA3 Transfer Counter	TCR3	XXh
01B9h			XXh
01BAh			
01BBh			
01BCh	DMA3 Control Register	DM3CON	0000 0X00b
01BDh			
01BEh			
01BFh			
01C0h	Timer B0-1 Register	TB01	XXh
01C1h			XXh
01C2h	Timer B1-1 Register	TB11	XXh
01C3h			XXh
01C4h	Timer B2-1 Register	TB21	XXh
01C5h			XXh
01C6h	Pulse Period/Pulse Width Measurement Mode Function Select Register 1	PPWFS1	XXXX X000b
01C7h			
01C8h	Timer B Count Source Select Register 0	TBCS0	00h
01C9h	Timer B Count Source Select Register 1	TBCS1	X0h
01CAh			
01CBh	Timer AB Division Control Register 0	TCKDIVC0	0000 X000b
01CCh			
01CDh			
01CEh			
01CFh			
01D0h	Timer A Count Source Select Register 0	TACS0	00h
01D1h	Timer A Count Source Select Register 1	TACS1	00h
01D2h	Timer A Count Source Select Register 2	TACS2	X0h
01D3h			
01D4h	16-bit Pulse Width Modulation Mode Function Select Register	PWMFS	0XX0 X00Xb
01D5h	Timer A Waveform Output Function Select Register	TAPOFS	XXX0 0000b
01D6h			
01D7h			
01D8h	Timer A Output Waveform Change Enable Register	TAOW	XXX0 X00Xb
01D9h			
01DAh	Three-Phase Protect Control Register	TPRC	00h
01DBh			
01DCh			
01DDh			
01DEh			
01DFh			

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 4.8 SFR Information (8) ⁽¹⁾

Address	Register	Symbol	Reset Value
0210h	Address Match Interrupt Register 0	RMAD0	00h
0211h			00h
0212h			X0h
0213h			
0214h	Address Match Interrupt Register 1	RMAD1	00h
0215h			00h
0216h			X0h
0217h			
0218h	Address Match Interrupt Register 2	RMAD2	00h
0219h			00h
021Ah			X0h
021Bh			
021Ch	Address Match Interrupt Register 3	RMAD3	00h
021Dh			00h
021Eh			X0h
021Fh			
0220h	Flash Memory Control Register 0	FMR0	0000 0001b (Other than user boot mode) 0010 0001b (User boot mode)
0221h	Flash Memory Control Register 1	FMR1	00X0 XX0Xb
0222h	Flash Memory Control Register 2	FMR2	XXXX 0000b
0223h	Flash Memory Control Register 3	FMR3	XXXX 0000b
0224h			
0225h			
0226h			
0227h			
0228h			
0229h			
022Ah			
022Bh			
022Ch			
022Dh			
022Eh			
022Fh			
0230h	Flash Memory Control Register 6	FMR6	XX0X XX00b
0231h			
0232h			
0233h			
0234h			
0235h			
0236h			
0237h			
0238h			
0239h			
023Ah			
023Bh			
023Ch			
023Dh			
023Eh			
023Fh			

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 4.11 SFR Information (11) ⁽¹⁾

Address	Register	Symbol	Reset Value
02A0h			
02A1h			
02A2h			
02A3h			
02A4h	UART7 Special Mode Register 4	U7SMR4	00h
02A5h	UART7 Special Mode Register 3	U7SMR3	000X 0X0Xb
02A6h	UART7 Special Mode Register 2	U7SMR2	X000 0000b
02A7h	UART7 Special Mode Register	U7SMR	X000 0000b
02A8h	UART7 Transmit/Receive Mode Register	U7MR	00h
02A9h	UART7 Bit Rate Register	U7BRG	XXh
02AAh	UART7 Transmit Buffer Register	U7TB	XXh
02ABh			XXh
02ACh	UART7 Transmit/Receive Control Register 0	U7C0	0000 1000b
02ADh	UART7 Transmit/Receive Control Register 1	U7C1	0000 0010b
02AEh	UART7 Receive Buffer Register	U7RB	XXh
02AFh			XXh
02B0h	I2C0 Data Shift Register	S00	XXh
02B1h			
02B2h	I2C0 Address Register 0	S0D0	0000 000Xb
02B3h	I2C0 Control Register 0	S1D0	00h
02B4h	I2C0 Clock Control Register	S20	00h
02B5h	I2C0 Start/Stop Condition Control Register	S2D0	0001 1010b
02B6h	I2C0 Control Register 1	S3D0	0011 0000b
02B7h	I2C0 Control Register 2	S4D0	00h
02B8h	I2C0 Status Register 0	S10	0001 000Xb
02B9h	I2C0 Status Register 1	S11	XXXX X000b
02BAh	I2C0 Address Register 1	S0D1	0000 000Xb
02BBh	I2C0 Address Register 2	S0D2	0000 000Xb
02BCh			
02BDh			
02BEh			
02BFh			
02C0h to 02FFh			

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 4.14 SFR Information (14) ⁽¹⁾

Address	Register	Symbol	Reset Value
0360h	Pull-Up Control Register 0	PUR0	00h
0361h	Pull-Up Control Register 1	PUR1	0000 0000b ⁽²⁾ 0000 0010b
0362h	Pull-Up Control Register 2	PUR2	00h
0363h	Pull-Up Control Register 3	PUR3	00h
0364h			
0365h			
0366h	Port Control Register	PCR	0000 0XX0b
0367h			
0368h			
0369h	NMI/SD Digital Filter Register	NMIDF	XXXX X000b
036Ah			
036Bh			
036Ch			
036Dh			
036Eh			
036Fh			
0370h	PWM Control Register 0	PWMCON0	00h
0371h			
0372h	PWM0 Prescaler	PWMPRE0	00h
0373h	PWM0 Register	PWMREG0	00h
0374h	PWM1 Prescaler	PWMPRE1	00h
0375h	PWM1 Register	PWMREG1	00h
0376h	PWM Control Register 1	PWMCON1	00h
0377h			
0378h			
0379h			
037Ah			
037Bh			
037Ch	Count Source Protection Mode Register	CSPR	00h ⁽³⁾
037Dh	Watchdog Timer Refresh Register	WDTR	XXh
037Eh	Watchdog Timer Start Register	WDTS	XXh
037Fh	Watchdog Timer Control Register	WDC	00XX XXXXb
0380h to 038Fh			

X: Undefined

Notes:

- The blank areas are reserved. No access is allowed.
- Values after hardware reset, power-on reset, or voltage monitor 0 reset are as follows:
 - 00000000b when a low-level signal is input to the CNVSS pin
 - 00000010b when a high-level signal is input to the CNVSS pin
 Values after voltage monitor 1 reset, voltage monitor 2 reset, software reset, watchdog timer reset, or oscillation stop detect reset are as follows:
 - 00000000b when bits PM01 and PM00 in the PM0 register are 00b (single-chip mode).
 - 00000010b when bits PM01 and PM00 in the PM0 register are 01b (memory expansion mode) or 11b (microprocessor mode).
- When the CSPROINI bit in the OFS1 address is 0, the reset value is 1000 0000b.

5.1.7 Oscillator Electrical Characteristics

Table 5.16 40 MHz On-Chip Oscillator Electrical Characteristics (1/2)

$V_{CC1} = 2.7$ to 5.5 V, $T_{opr} = -20^{\circ}\text{C}$ to $85^{\circ}\text{C}/-40^{\circ}\text{C}$ to 85°C , unless otherwise specified.

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
f_{OCO40M}	40 MHz on-chip oscillator frequency	Average frequency in a 10 ms period	38	40	42	MHz
$tsu(f_{OCO40M})$	Wait time until 40 MHz on-chip oscillator stabilizes				2	ms

Table 5.17 125 kHz On-Chip Oscillator Electrical Characteristics

$V_{CC1} = 2.7$ to 5.5 V, $T_{opr} = -20^{\circ}\text{C}$ to $85^{\circ}\text{C}/-40^{\circ}\text{C}$ to 85°C , unless otherwise specified.

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
f_{OCO-S}	125 kHz on-chip oscillator frequency	Average frequency in a 10 ms period	100	125	150	kHz
$tsu(f_{OCO-S})$	Wait time until 125 kHz on-chip oscillator stabilizes				20	μs

$$V_{CC1} = V_{CC2} = 5 \text{ V}$$

Table 5.19 Electrical Characteristics (2) (1)

$V_{CC1} = V_{CC2} = 4.2 \text{ to } 5.5 \text{ V}$, $V_{SS} = 0 \text{ V}$ at $T_{opr} = -20^\circ\text{C to } 85^\circ\text{C}/-40^\circ\text{C to } 85^\circ\text{C}$, $f_{(CLK)} = 32 \text{ MHz}$ unless otherwise specified.

Symbol	Parameter		Measuring Condition	Standard			Unit
				Min.	Typ.	Max.	
V _{T+} - V _{T-}	Hysteresis	HOLD, RDY, TA0IN to TA4IN, TB0IN to TB5IN, INT0 to INT7, NMI, ADTRG, CTS0 to CTS2, CTS5 to CTS7, SCL0 to SCL2, SCL5 to SCL7, SDA0 to SDA2, SDA5 to SDA7, CLK0 to CLK7, TA0OUT to TA4OUT, K10 to K13, RXD0 to RXD2, RXD5 to RXD7, SIN3, SIN4, SD, PMC0, PMC1, SCLMM, SDAMM, CEC, ZP, IDU, IDV, IDW		0.5		2.0	V
V _{T+} - V _{T-}	Hysteresis	RESET		0.5		2.5	V
I _{IH}	High input current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1 XIN, RESET, CNVSS, BYTE	V _I = 5 V			5.0	μA
I _{IL}	Low input current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1 XIN, RESET, CNVSS, BYTE	V _I = 0 V			−5.0	μA
R _{PULLUP}	Pull-up resistance	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1	V _I = 0 V	30	50	100	kΩ
R _{fXIN}	Feedback resistance XIN				1.5		MΩ
V _{RAM}	RAM retention voltage		In stop mode	1.8			V

Note:

1. When $V_{CC1} \neq V_{CC2}$, refer to 5 V or 3 V standard depending on the voltage.

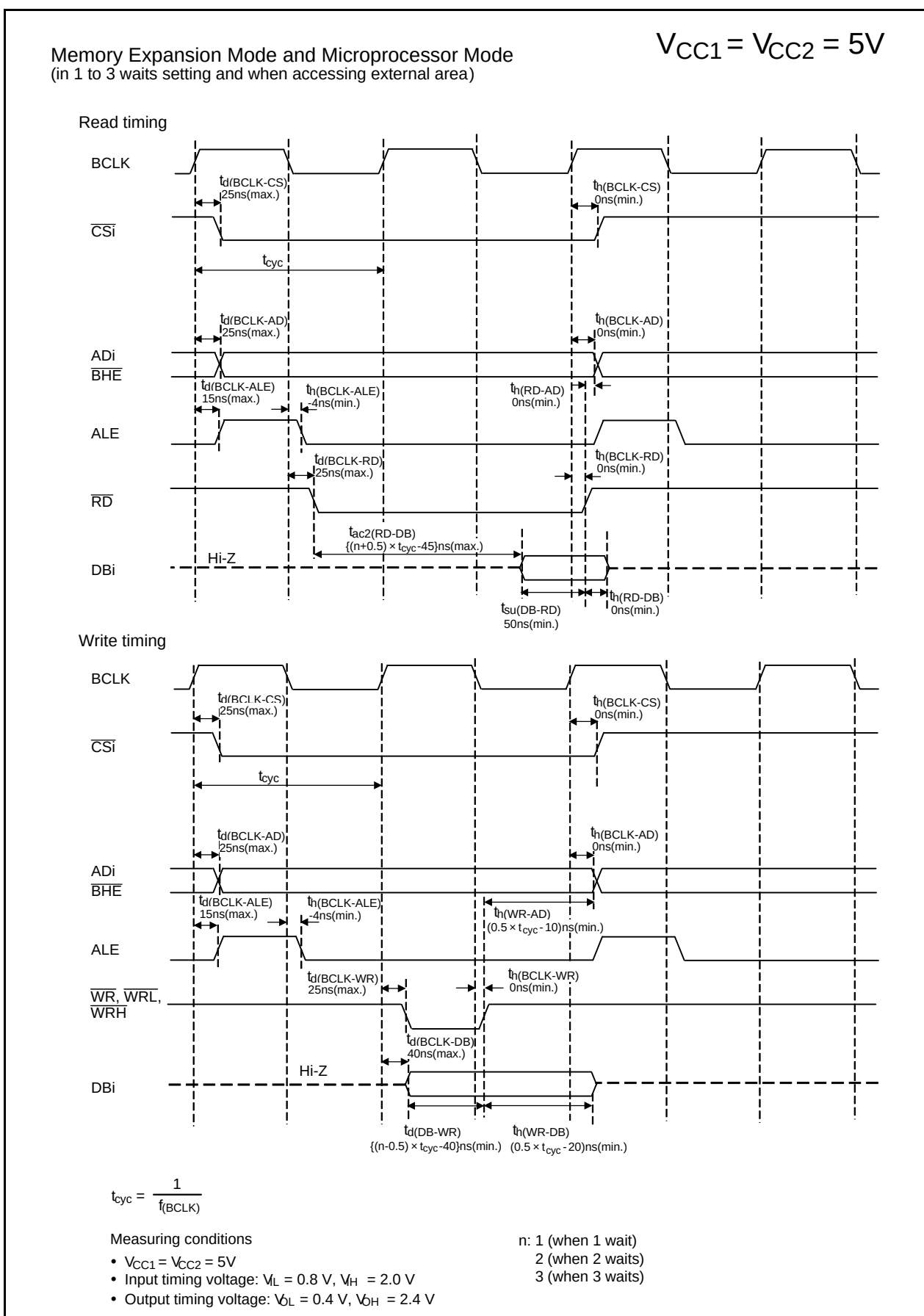


Figure 5.16 Timing Diagram

$$V_{CC1} = V_{CC2} = 3\text{ V}$$

Table 5.44 Electrical Characteristics (3) (2/2)

R5F3651ECNFC, R5F3651KCNFC, R5F3650KCNFA, R5F3650KCNFB, R5F3651MCNFC, R5F3650MCNFA,
 R5F3650MCNFB, R5F3651NCNFC, R5F3650NCNFA, R5F3650NCNFB,
 R5F3651ECDFC, R5F3651KCDFC, R5F3650KCDFA, R5F3650KCDFB, R5F3651MCDFC, R5F3650MCDFA,
 R5F3650MCDFB, R5F3651NCDFC, R5F3650NCDFA, R5F3650NCDFB

$V_{CC1} = V_{CC2} = 2.7$ to 3.3 V , $V_{SS} = 0\text{ V}$ at $T_{opr} = -20^{\circ}\text{C}$ to $85^{\circ}\text{C}/-40^{\circ}\text{C}$ to 85°C , $f_{(BCLK)} = 32\text{ MHz}$ unless otherwise specified.

Symbol	Parameter	Measuring Condition		Standard			Unit
				Min.	Typ.	Max.	
I_{CC}	Power supply current In single-chip, mode, the output pin are open and other pins are V_{SS}	Stop mode	Main clock stopped 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator stopped Peripheral clock stopped $T_{opr} = 25^{\circ}\text{C}$		1.6		μA
		During flash memory program	$f_{(BCLK)} = 10\text{ MHz}$, PM17 = 1 (one wait) $V_{CC1} = 3.0\text{ V}$		20.0		mA
		During flash memory erase	$f_{(BCLK)} = 10\text{ MHz}$, PM17 = 1 (one wait) $V_{CC1} = 3.0\text{ V}$		30.0		mA

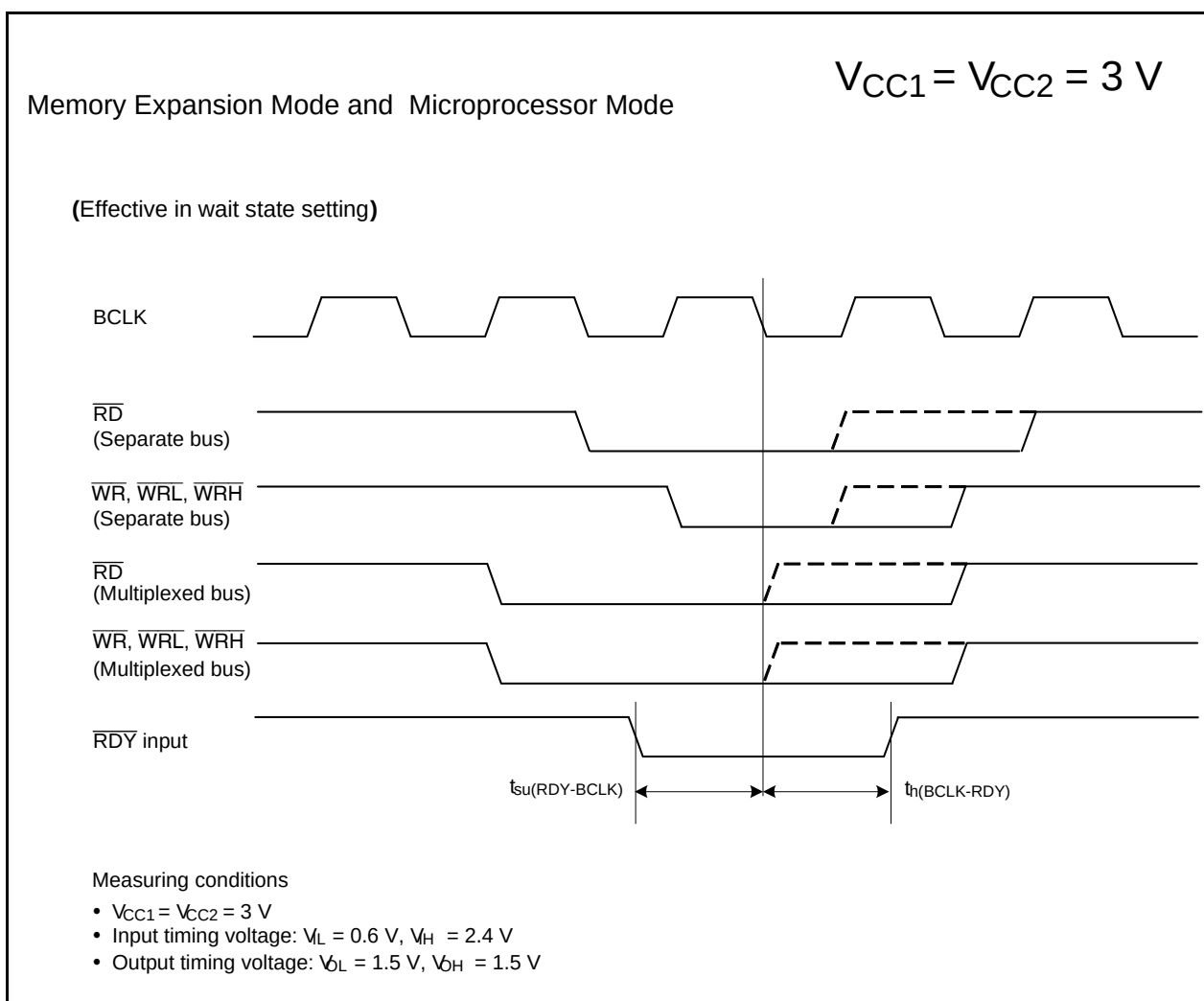
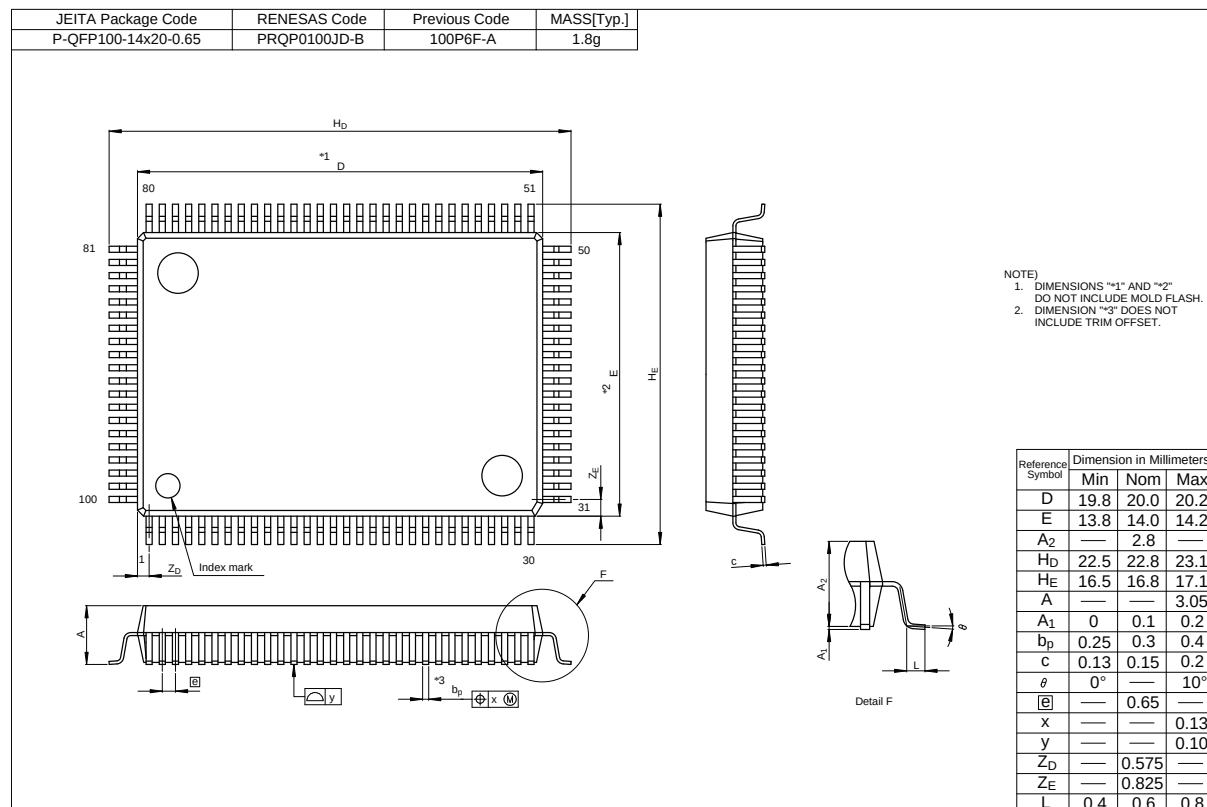
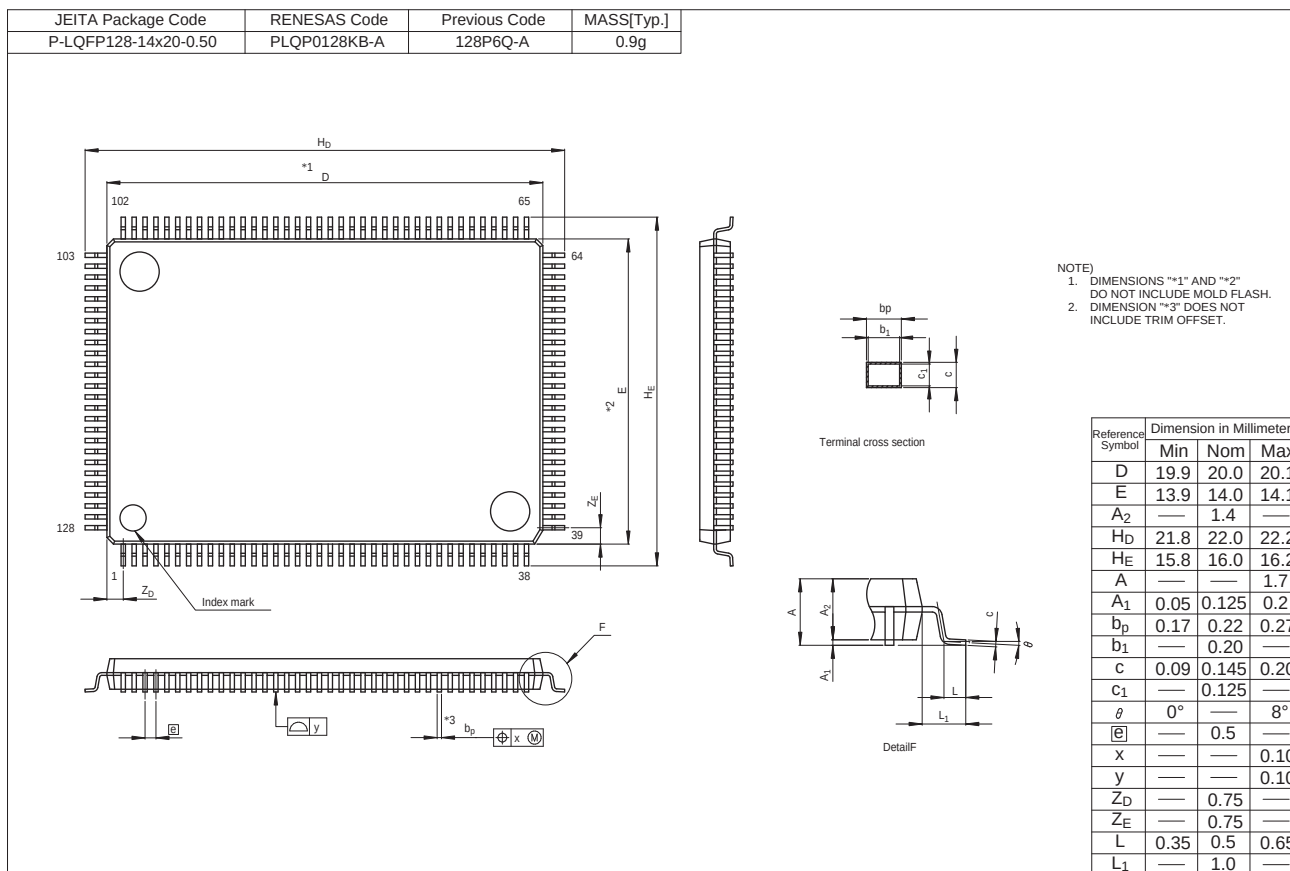
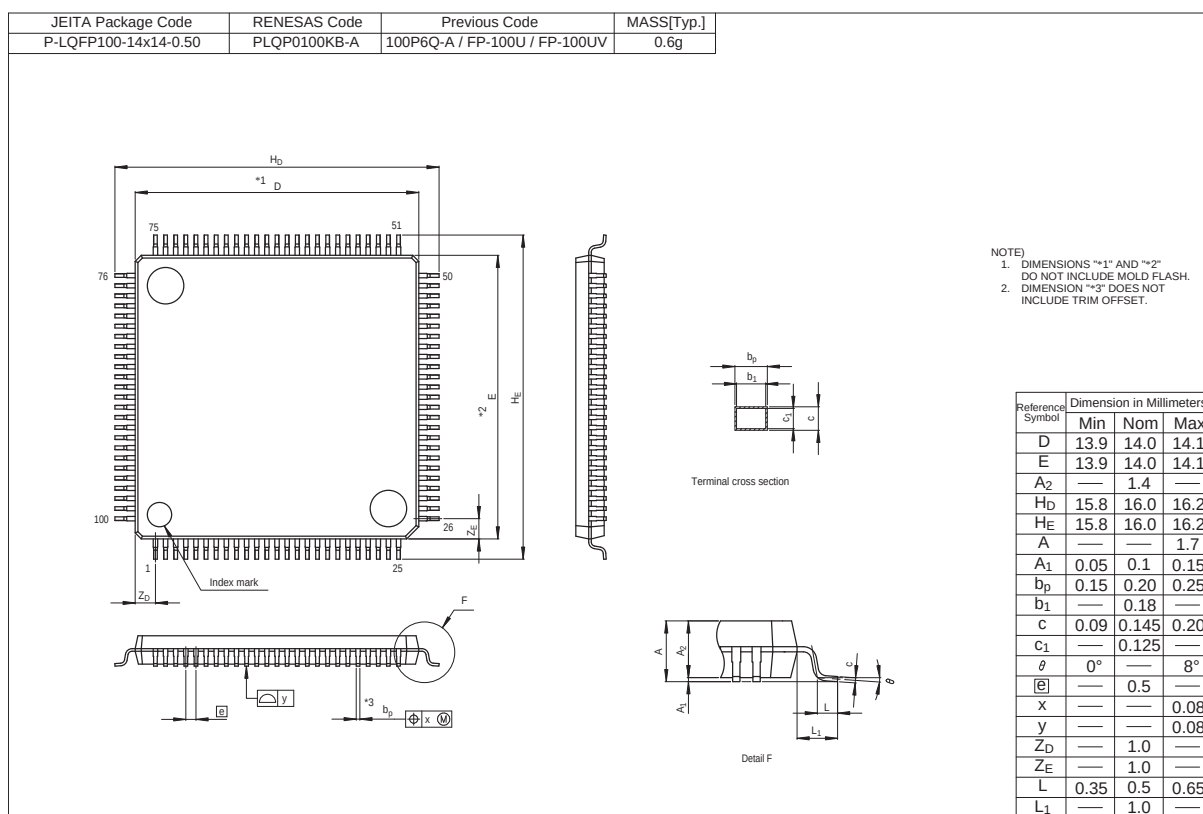


Figure 5.28 Timing Diagram

Appendix 1. Package Dimensions

The information on the latest package dimensions or packaging may be obtained from "Packages" on the Renesas Electronics website.





General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

- The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.