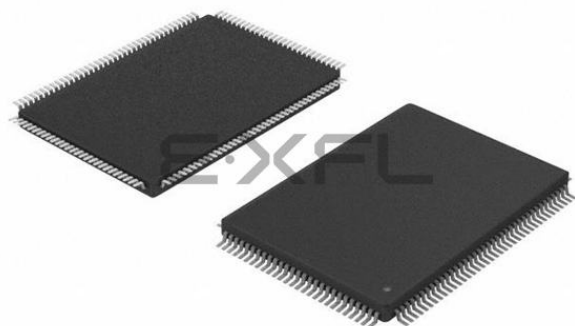




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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	M16C/60
Core Size	16-Bit
Speed	32MHz
Connectivity	EBI/EMI, I ² C, SIO, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	111
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	47K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	128-LQFP
Supplier Device Package	128-LFQFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f3651ncdfc-v0

Table 1.8 Pin Names for the 128-Pin Package (2/3)

Pin No.	Control Pin	Port	I/O Pin for Peripheral Function				Bus Control Pin
			Interrupt	Timer	Serial interface	A/D converter, D/A converter	
51		P5_6					ALE
52		P5_5					HOLD
53		P5_4					HLDA
54		P13_3					
55		P13_2					
56		P13_1					
57		P13_0					
58		P5_3					BCLK
59		P5_2					RD
60		P5_1					WRH/BHE
61		P5_0					WRL/WR
62		P12_7					
63		P12_6					
64		P12_5					
65		P4_7		PWM1	TXD7/SDA7		CS3
66		P4_6		PWM0	RXD7/SCL7		CS2
67		P4_5			CLK7		CS1
68		P4_4			CTS7/RTS7		CS0
69		P4_3					A19
70		P4_2					A18
71		P4_1					A17
72		P4_0					A16
73		P3_7					A15
74		P3_6					A14
75		P3_5					A13
76		P3_4					A12
77		P3_3					A11
78		P3_2					A10
79		P3_1					A9
80		P12_4					
81		P12_3					
82		P12_2					
83		P12_1					
84		P12_0					
85	VCC2						
86		P3_0					A8, [A8/D7]
87	VSS						
88		P2_7				AN2_7	A7, [A7/D7], [A7/D6]
89		P2_6				AN2_6	A6, [A6/D6], [A6/D5]
90		P2_5	INT7			AN2_5	A5, [A5/D5], [A5/D4]
91		P2_4	INT6			AN2_4	A4[A4/D4], [A4/D3]
92		P2_3				AN2_3	A3, [A3/D3], [A3/D2]
93		P2_2				AN2_2	A2, [A2/D2], [A2/D1]
94		P2_1				AN2_1	A1, [A1/D1], [A1/D0]
95		P2_0				AN2_0	A0, [A0/D0], A0
96		P1_7	INT5	IDU			D15
97		P1_6	INT4	IDW			D14
98		P1_5	INT3	IDV			D13
99		P1_4					D12
100		P1_3			TXD6/SDA6		D11

Table 1.16 Pin Functions for the 100-Pin Package (2/3)

Signal Name	Pin Name	I/O	Power Supply	Description
Main clock input	XIN	I	VCC1	I/O for the main clock oscillator. Connect a ceramic resonator or crystal between pins XIN and XOUT. ⁽¹⁾ Input an external clock to XIN pin and leave XOUT pin open.
Main clock output	XOUT	O	VCC1	
Sub clock input	XCIN	I	VCC1	I/O for a sub clock oscillator. Connect a crystal between XCIN pin and XCOUT pin. ⁽¹⁾ Input an external clock to XCIN pin and leave XCOUT pin open.
Sub clock output	XCOUT	O	VCC1	
BCLK output	BCLK	O	VCC2	Outputs the BCLK signal.
Clock output	CLKOUT	O	VCC2	Outputs a clock with the same frequency as f _C , f ₁ , f ₈ , or f ₃₂ .
INT interrupt input	INT0 to INT2	I	VCC1	Input for the INT interrupt.
	INT3 to INT7	I	VCC2	
NMI interrupt input	NMI	I	VCC1	Input for the NMI interrupt.
Key input interrupt input	KI0 to KI3	I	VCC1	Input for the key input interrupt.
Timer A	TA0OUT to TA4OUT	I/O	VCC1	I/O for timers A0 to A4 (TA0OUT is N-channel open drain output).
	TA0IN to TA4IN	I	VCC1	Input for timers A0 to A4.
	ZP	I	VCC1	Input for Z-phase.
Timer B	TB0IN to TB5IN	I	VCC1	Input for timers B0 to B5.
Three-phase motor control timer	U, $\bar{U}$, V, $\bar{V}$, W, $\bar{W}$	O	VCC1	Output for the three-phase motor control timer.
	$\bar{SD}$	I	VCC1	Forced cutoff input.
	IDU, IDV, IDW	I	VCC2	Input for the position data.
Real-time clock output	RTCOUT	O	VCC1	Output for the real-time clock.
PWM output	PWM0, PWM1	O	VCC1, VCC2	PWM output.
Remote control signal receiver input	PMC0, PMC1	I	VCC1	Input for the remote control signal receiver.
Serial interface UART0 to UART2, UART5 to UART7	CTS0 to CTS2, CTS5	I	VCC1	Input pins to control data transmission.
	CTS6, CTS7	I	VCC2	
	RTS0 to RTS2, RTS5	O	VCC1	Output pins to control data reception.
	RTS6, RTS7	O	VCC2	
	CLK0 to CLK2, CLK5	I/O	VCC1	Transmit/receive clock I/O.
	CLK6, CLK7	I/O	VCC2	
	RXD0 to RXD2, RXD5	I	VCC1	Serial data input.
	RXD6, RXD7	I	VCC2	
	TXD0 to TXD2, TXD5	O	VCC1	Serial data output. ⁽²⁾
	TXD6, TXD7	O	VCC2	
	CLKS1	O	VCC1	Output for the transmit/receive clock multiple-pin output function.

Notes:

- Contact the manufacturer of crystal/ceramic resonator regarding the oscillation characteristics.
- TXD2, SDA2, and SCL2 are N-channel open drain output pins. TXDi (i = 0, 1, 5 to 7), SDAi, and SCLi can be selected as CMOS output pins or N-channel open drain output pins.

2.1 Data Registers (R0, R1, R2, and R3)

R0, R1, R2, and R3 are 16-bit registers used for transfer, arithmetic, and logic operations. R0 and R1 can be split into upper (R0H/R1H) and lower (R0L/R1L) bits to be used separately as 8-bit data registers. R0 can be combined with R2, and R3 can be combined with R1 and be used as 32-bit data registers R2R0 and R3R1, respectively.

2.2 Address Registers (A0 and A1)

A0 and A1 are 16-bit registers used for indirect addressing, relative addressing, transfer, arithmetic, and logic operations. A0 can be combined with A1 and used as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register that is used for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the start address of a relocatable interrupt vector table.

2.5 Program Counter (PC)

The PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The USP and ISP stack pointers (SP) are each comprised of 16 bits. The U flag is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register used for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register that indicates the CPU state.

2.8.1 Carry Flag (C Flag)

The C flag retains a carry, borrow, or shift-out bit generated by the arithmetic/logic unit.

2.8.2 Debug Flag (D Flag)

The D flag is for debugging only. Set it to 0.

2.8.3 Zero Flag (Z Flag)

The Z flag becomes 1 when an arithmetic operation results in 0. Otherwise, it becomes 0.

2.8.4 Sign Flag (S Flag)

The S flag becomes 1 when an arithmetic operation results in a negative value. Otherwise, it becomes 0.

2.8.5 Register Bank Select Flag (B Flag)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is 1.

2.8.6 Overflow Flag (O Flag)

The O flag becomes 1 when an arithmetic operation results in an overflow. Otherwise, it becomes 0.

2.8.7 Interrupt Enable Flag (I Flag)

The I flag enables maskable interrupts.

Maskable interrupts are disabled when the I flag is 0, and enabled when it is 1. The I flag becomes 0 when an interrupt request is accepted.

2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is 0. USP is selected when the U flag is 1.

The U flag becomes 0 when a hardware interrupt request is accepted, or the INT instruction of software interrupt number 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from 0 to 7.

If a requested interrupt has higher priority than IPL, the interrupt request is enabled.

2.8.10 Reserved Areas

Only set these bits to 0. The read value is undefined.

Table 4.3 SFR Information (3) ⁽¹⁾

Address	Register	Symbol	Reset Value
0040h			
0041h			
0042h	INT7 Interrupt Control Register	INT7IC	XX00 X000b
0043h	INT6 Interrupt Control Register	INT6IC	XX00 X000b
0044h	INT3 Interrupt Control Register	INT3IC	XX00 X000b
0045h	Timer B5 Interrupt Control Register	TB5IC	XXXX X000b
0046h	Timer B4 Interrupt Control Register UART1 Bus Collision Detection Interrupt Control Register	TB4IC U1BCNIC	XXXX X000b
0047h	Timer B3 Interrupt Control Register UART0 Bus Collision Detection Interrupt Control Register	TB3IC U0BCNIC	XXXX X000b
0048h	SI/O4 Interrupt Control Register INT5 Interrupt Control Register	S4IC INT5IC	XX00 X000b
0049h	SI/O3 Interrupt Control Register INT4 Interrupt Control Register	S3IC INT4IC	XX00 X000b
004Ah	UART2 Bus Collision Detection Interrupt Control Register	BCNIC	XXXX X000b
004Bh	DMA0 Interrupt Control Register	DM0IC	XXXX X000b
004Ch	DMA1 Interrupt Control Register	DM1IC	XXXX X000b
004Dh	Key Input Interrupt Control Register	KUPIC	XXXX X000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXX X000b
004Fh	UART2 Transmit Interrupt Control Register	S2TIC	XXXX X000b
0050h	UART2 Receive Interrupt Control Register	S2RIC	XXXX X000b
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXX X000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXX X000b
0053h	UART1 Transmit Interrupt Control Register	S1TIC	XXXX X000b
0054h	UART1 Receive Interrupt Control Register	S1RIC	XXXX X000b
0055h	Timer A0 Interrupt Control Register	TA0IC	XXXX X000b
0056h	Timer A1 Interrupt Control Register	TA1IC	XXXX X000b
0057h	Timer A2 Interrupt Control Register	TA2IC	XXXX X000b
0058h	Timer A3 Interrupt Control Register	TA3IC	XXXX X000b
0059h	Timer A4 Interrupt Control Register	TA4IC	XXXX X000b
005Ah	Timer B0 Interrupt Control Register	TB0IC	XXXX X000b
005Bh	Timer B1 Interrupt Control Register	TB1IC	XXXX X000b
005Ch	Timer B2 Interrupt Control Register	TB2IC	XXXX X000b
005Dh	INT0 Interrupt Control Register	INT0IC	XX00 X000b
005Eh	INT1 Interrupt Control Register	INT1IC	XX00 X000b
005Fh	INT2 Interrupt Control Register	INT2IC	XX00 X000b

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 4.9 SFR Information (9) ⁽¹⁾

Address	Register	Symbol	Reset Value
0240h			
0241h			
0242h			
0243h			
0244h	UART0 Special Mode Register 4	U0SMR4	00h
0245h	UART0 Special Mode Register 3	U0SMR3	000X 0X0Xb
0246h	UART0 Special Mode Register 2	U0SMR2	X000 0000b
0247h	UART0 Special Mode Register	U0SMR	X000 0000b
0248h	UART0 Transmit/Receive Mode Register	U0MR	00h
0249h	UART0 Bit Rate Register	U0BRG	XXh
024Ah	UART0 Transmit Buffer Register	U0TB	XXh
024Bh			XXh
024Ch	UART0 Transmit/Receive Control Register 0	U0C0	0000 1000b
024Dh	UART0 Transmit/Receive Control Register 1	U0C1	00XX 0010b
024Eh	UART0 Receive Buffer Register	U0RB	XXh
024Fh			XXh
0250h	UART Transmit/Receive Control Register 2	UCON	X000 0000b
0251h			
0252h	UART Clock Select Register	UCLKSEL0	X0h
0253h			
0254h	UART1 Special Mode Register 4	U1SMR4	00h
0255h	UART1 Special Mode Register 3	U1SMR3	000X 0X0Xb
0256h	UART1 Special Mode Register 2	U1SMR2	X000 0000b
0257h	UART1 Special Mode Register	U1SMR	X000 0000b
0258h	UART1 Transmit/Receive Mode Register	U1MR	00h
0259h	UART1 Bit Rate Register	U1BRG	XXh
025Ah	UART1 Transmit Buffer Register	U1TB	XXh
025Bh			XXh
025Ch	UART1 Transmit/Receive Control Register 0	U1C0	0000 1000b
025Dh	UART1 Transmit/Receive Control Register 1	U1C1	00XX 0010b
025Eh	UART1 Receive Buffer Register	U1RB	XXh
025Fh			XXh
0260h			
0261h			
0262h			
0263h			
0264h	UART2 Special Mode Register 4	U2SMR4	00h
0265h	UART2 Special Mode Register 3	U2SMR3	000X 0X0Xb
0266h	UART2 Special Mode Register 2	U2SMR2	X000 0000b
0267h	UART2 Special Mode Register	U2SMR	X000 0000b
0268h	UART2 Transmit/Receive Mode Register	U2MR	00h
0269h	UART2 Bit Rate Register	U2BRG	XXh
026Ah	UART2 Transmit Buffer Register	U2TB	XXh
026Bh			XXh
026Ch	UART2 Transmit/Receive Control Register 0	U2C0	0000 1000b
026Dh	UART2 Transmit/Receive Control Register 1	U2C1	0000 0010b
026Eh	UART2 Receive Buffer Register	U2RB	XXh
026Fh			XXh

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 4.12 SFR Information (12) ⁽¹⁾

Address	Register	Symbol	Reset Value
0300h	Timer B3/B4/B5 Count Start Flag	TBSR	000X XXXXb
0301h			
0302h	Timer A1-1 Register	TA11	XXh
0303h			XXh
0304h	Timer A2-1 Register	TA21	XXh
0305h			XXh
0306h	Timer A4-1 Register	TA41	XXh
0307h			XXh
0308h	Three-Phase PWM Control Register 0	INVC0	00h
0309h	Three-Phase PWM Control Register 1	INVC1	00h
030Ah	Three-Phase Output Buffer Register 0	IDB0	XX11 1111b
030Bh	Three-Phase Output Buffer Register 1	IDB1	XX11 1111b
030Ch	Dead Time Timer	DTT	XXh
030Dh	Timer B2 Interrupt Generation Frequency Set Counter	ICTB2	XXh
030Eh	Position-Data-Retain Function Control Register	PDRF	XXXX 0000b
030Fh			
0310h	Timer B3 Register	TB3	XXh
0311h			XXh
0312h	Timer B4 Register	TB4	XXh
0313h			XXh
0314h	Timer B5 Register	TB5	XXh
0315h			XXh
0316h			
0317h			
0318h	Port Function Control Register	PFCR	0011 1111b
0319h			
031Ah			
031Bh	Timer B3 Mode Register	TB3MR	00XX 0000b
031Ch	Timer B4 Mode Register	TB4MR	00XX 0000b
031Dh	Timer B5 Mode Register	TB5MR	00XX 0000b
031Eh			
031Fh			
0320h	Count Start Flag	TABSR	00h
0321h			
0322h	One-Shot Start Flag	ONSF	00h
0323h	Trigger Select Register	TRGSR	00h
0324h	Increment/Decrement Flag	UDF	00h
0325h			
0326h	Timer A0 Register	TA0	XXh
0327h			XXh
0328h	Timer A1 Register	TA1	XXh
0329h			XXh
032Ah	Timer A2 Register	TA2	XXh
032Bh			XXh
032Ch	Timer A3 Register	TA3	XXh
032Dh			XXh
032Eh	Timer A4 Register	TA4	XXh
032Fh			XXh

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 4.16 SFR Information (16) ⁽¹⁾

Address	Register	Symbol	Reset Value
03C0h	A/D Register 0	AD0	XXXX XXXXb
03C1h			0000 00XXb
03C2h	A/D Register 1	AD1	XXXX XXXXb
03C3h			0000 00XXb
03C4h	A/D Register 2	AD2	XXXX XXXXb
03C5h			0000 00XXb
03C6h	A/D Register 3	AD3	XXXX XXXXb
03C7h			0000 00XXb
03C8h	A/D Register 4	AD4	XXXX XXXXb
03C9h			0000 00XXb
03CAh	A/D Register 5	AD5	XXXX XXXXb
03CBh			0000 00XXb
03CCh	A/D Register 6	AD6	XXXX XXXXb
03CDh			0000 00XXb
03CEh	A/D Register 7	AD7	XXXX XXXXb
03CFh			0000 00XXb
03D0h			
03D1h			
03D2h			
03D3h			
03D4h	A/D Control Register 2	ADCON2	0000 X00Xb
03D5h			
03D6h	A/D Control Register 0	ADCON0	0000 0XXXb
03D7h	A/D Control Register 1	ADCON1	0000 X000b
03D8h	D/A0 Register	DA0	00h
03D9h			
03DAh	D/A1 Register	DA1	00h
03DBh			
03DCh	D/A Control Register	DACON	00h
03DDh			
03DEh			
03DFh			
03E0h	Port P0 Register	P0	XXh
03E1h	Port P1 Register	P1	XXh
03E2h	Port P0 Direction Register	PD0	00h
03E3h	Port P1 Direction Register	PD1	00h
03E4h	Port P2 Register	P2	XXh
03E5h	Port P3 Register	P3	XXh
03E6h	Port P2 Direction Register	PD2	00h
03E7h	Port P3 Direction Register	PD3	00h
03E8h	Port P4 Register	P4	XXh
03E9h	Port P5 Register	P5	XXh
03EAh	Port P4 Direction Register	PD4	00h
03EBh	Port P5 Direction Register	PD5	00h
03ECh	Port P6 Register	P6	XXh
03EDh	Port P7 Register	P7	XXh
03EEh	Port P6 Direction Register	PD6	00h
03EFh	Port P7 Direction Register	PD7	00h

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

4.2 Notes on SFRs

4.2.1 Register Settings

Table 4.19 lists Registers with Write-Only Bits and registers whose function differs between reading and writing. Set these registers with immediate values. Do not use read-modify-write instructions. When establishing the next value by altering the existing value, write the existing value to the RAM as well as to the register. Transfer the next value to the register after making changes in the RAM. Read-modify-write instructions can be used when writing to the no register bits.

Table 4.19 Registers with Write-Only Bits

Address	Register	Symbol
0249h	UART0 Bit Rate Register	U0BRG
024Bh to 024Ah	UART0 Transmit Buffer Register	U0TB
0259h	UART1 Bit Rate Register	U1BRG
025Bh to 025Ah	UART1 Transmit Buffer Register	U1TB
0269h	UART2 Bit Rate Register	U2BRG
026Bh to 026Ah	UART2 Transmit Buffer Register	U2TB
0273h	SI/O3 Bit Rate Register	S3BRG
0277h	SI/O4 Bit Rate Register	S4BRG
0289h	UART5 Bit Rate Register	U5BRG
028Bh to 028Ah	UART5 Transmit Buffer Register	U5TB
0299h	UART6 Bit Rate Register	U6BRG
029Bh to 029Ah	UART6 Transmit Buffer Register	U6TB
02A9h	UART7 Bit Rate Register	U7BRG
02ABh to 02AAh	UART7 Transmit Buffer Register	U7TB
02B6h	I2C0 Control Register 1	S3D0
02B8h	I2C0 Status Register 0	S10
0303h to 0302h	Timer A1-1 Register	TA11
0305h to 0304h	Timer A2-1 Register	TA21
0307h to 0306h	Timer A4-1 Register	TA41
030Ah	Three-Phase Output Buffer Register 0	IDB0
030Bh	Three-Phase Output Buffer Register 1	IDB1
030Ch	Dead Time Timer	DTT
030Dh	Timer B2 Interrupt Generation Frequency Set Counter	ICTB2
0327h to 0326h	Timer A0 Register	TA0
0329h to 0328h	Timer A1 Register	TA1
032Bh to 032Ah	Timer A2 Register	TA2
032Dh to 032Ch	Timer A3 Register	TA3
032Fh to 032Eh	Timer A4 Register	TA4
037Dh	Watchdog Timer Refresh Register	WDTR
037Eh	Watchdog Timer Start Register	WDTS

5.1.3 A/D Conversion Characteristics

Table 5.5 A/D Conversion Characteristics (1/2) ⁽¹⁾

$V_{CC1} = AV_{CC} = 3.0 \text{ to } 5.5 \text{ V} \geq V_{CC2} \geq V_{REF}$, $V_{SS} = AV_{SS} = 0 \text{ V}$ at $T_{opr} = -20^\circ\text{C to } 85^\circ\text{C}/-40^\circ\text{C to } 85^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter		Measuring Condition		Standard			Unit
					Min.	Typ.	Max.	
-	Resolution		$AV_{CC} = V_{CC1} \geq V_{CC2} \geq V_{REF}$				10	Bits
I_{NL}	Integral non-linearity error	10 bits	$V_{CC1} = 5.0 \text{ V}$	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input (Note 2)			± 3	LSB
			$V_{CC1} = 3.3 \text{ V}$	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input (Note 2)			± 3	LSB
			$V_{CC1} = 3.0 \text{ V}$	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input (Note 2)			± 3	LSB
-	Absolute accuracy	10 bits	$V_{CC1} = 5.0 \text{ V}$	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input (Note 2)			± 3	LSB
			$V_{CC1} = 3.3 \text{ V}$	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input (Note 2)			± 3	LSB
			$V_{CC1} = 3.0 \text{ V}$	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input (Note 2)			± 3	LSB

Notes:

1. Use when $AV_{CC} = V_{CC1}$.
2. Flash memory rewrite disabled. Except for the analog input pin, set the pins to be measured as input ports and connect them to V_{SS} . See Figure 5.2 "A/D Accuracy Measure Circuit".

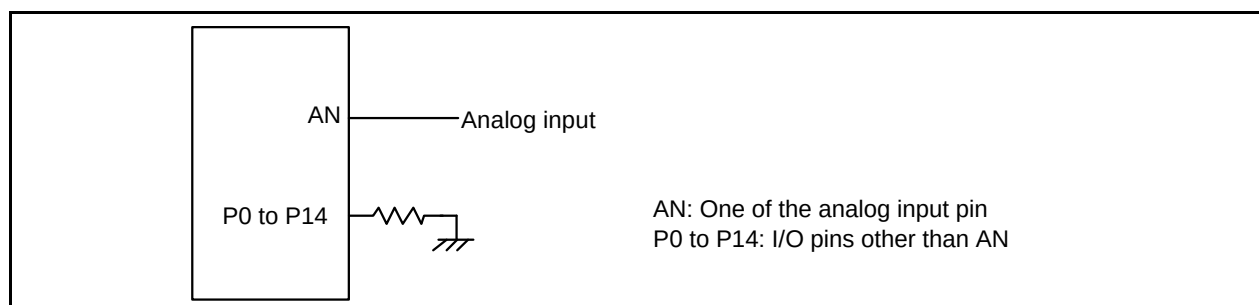

Figure 5.2 A/D Accuracy Measure Circuit

Table 5.6 A/D Conversion Characteristics (2/2) ⁽¹⁾

$V_{CC1} = AV_{CC} = 3.0 \text{ to } 5.5 \text{ V} \geq V_{CC2} \geq V_{REF}$, $V_{SS} = AV_{SS} = 0 \text{ V}$ at $T_{opr} = -20^\circ\text{C to } 85^\circ\text{C}/-40^\circ\text{C to } 85^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter		Measuring Condition	Standard			Unit	
				Min.	Typ.	Max.		
φAD	A/D operating clock frequency	AN0 to AN7 input, ANEX0 to ANEX1 input	4.0 V ≤ V _{CC1} ≤ 5.5 V	2		25	MHz	
			3.2 V ≤ V _{CC1} ≤ 4.0 V	2		16	MHz	
			3.0 V ≤ V _{CC1} ≤ 3.2 V	2		10	MHz	
		AN0_0 to AN0_7 input, AN2_0 to AN2_7 input	4.0 V ≤ V _{CC2} ≤ 5.5 V	2		25	MHz	
			3.2 V ≤ V _{CC2} ≤ 4.0 V	2		16	MHz	
			3.0 V ≤ V _{CC2} ≤ 3.2 V	2		10	MHz	
-	Tolerance level impedance				3		kΩ	
D _{NL}	Differential non-linearity error		(4)			±1	LSB	
-	Offset error		(4)				±3	LSB
-	Gain error		(4)				±3	LSB
t _{CONV}	10-bit conversion time		V _{CC1} = 5 V, φAD = 25 MHz	1.60				μs
t _{SAMP}	Sampling time			0.60				μs
V _{REF}	Reference voltage			3.0			V _{CC1}	V
V _{IA}	Analog input voltage ^{(2), (3)}			0			V _{REF}	V

Notes:

1. Use when $AV_{CC} = V_{CC1}$.
2. When $V_{CC1} \geq V_{CC2}$, set as below:
Analog input voltage (AN0 to AN7, ANEX0, and ANEX1) $\leq V_{CC1}$
Analog input voltage (AN0_0 to AN0_7 and AN2_0 to AN2_7) $\leq V_{CC2}$.
3. When analog input voltage is over reference voltage, the result of A/D conversion is 3FFh.
4. Flash memory rewrite disabled. Except for the analog input pin, set the pins to be measured as input ports and connect them to V_{SS} . See Figure 5.2 "A/D Accuracy Measure Circuit".

5.1.4 D/A Conversion Characteristics

Table 5.7 D/A Conversion Characteristics

$V_{CC1} = AV_{CC} = V_{REF} = 3.0 \text{ to } 5.5 \text{ V}$, $V_{SS} = AV_{SS} = 0 \text{ V}$ at $T_{opr} = -20^\circ\text{C to } 85^\circ\text{C}/-40^\circ\text{C to } 85^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Measuring Condition	Standard			Unit
			Min.	Typ.	Max.	
-	Resolution				8	Bits
-	Absolute Accuracy				2.5	LSB
t_{SU}	Setup Time				3	μs
R_O	Output Resistance		5	6	8.2	k Ω
I_{VREF}	Reference Power Supply Input Current	See Notes ¹ and ²			1.5	mA

Notes:

1. This applies when using one D/A converter, with the D/A register for the unused D/A converter set to 00h.
2. The current consumption of the A/D converter is not included. Also, the I_{VREF} of the D/A converter will flow even if the ADSTBY bit in the ADCON1 register is 0 (A/D operation stopped (standby)).

$$V_{CC1} = V_{CC2} = 5 \text{ V}$$

Switching Characteristics

($V_{CC1} = V_{CC2} = 5 \text{ V}$, $V_{SS} = 0 \text{ V}$, at $T_{opr} = -20^{\circ}\text{C}$ to 85°C / -40°C to 85°C unless otherwise specified)

5.2.4.3 In 2 or 3 Waits Setting, and When Accessing External Area and Using Multiplexed Bus

Table 5.38 Memory Expansion Mode and Microprocessor Mode (in 2 or 3 Waits Setting, and When Accessing External Area and Using Multiplexed Bus) (5)

Symbol	Parameter	Measuring Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	See Figure 5.14		25	ns
$t_{h(BCLK-AD)}$	Address output hold time (in relation to BCLK)		0		ns
$t_{h(RD-AD)}$	Address output hold time (in relation to RD)		(Note 1)		ns
$t_{h(WR-AD)}$	Address output hold time (in relation to WR)		(Note 1)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			25	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (in relation to BCLK)		0		ns
$t_{h(RD-CS)}$	Chip select output hold time (in relation to RD)		(Note 1)		ns
$t_{h(WR-CS)}$	Chip select output hold time (in relation to WR)		(Note 1)		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			25	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			25	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (in relation to BCLK)			40	ns
$t_{d(DB-WR)}$	Data output delay time (in relation to WR)		(Note 2)		ns
$t_{h(WR-DB)}$	Data output hold time (in relation to WR)		(Note 6)		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time (in relation to BCLK)			15	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time (in relation to BCLK)		-4		ns
$t_{d(AD-ALE)}$	ALE signal output delay time (in relation to Address)		(Note 3)		ns
$t_{h(AD-ALE)}$	ALE signal output hold time (in relation to Address)		(Note 4)		ns
$t_{d(AD-RD)}$	RD signal output delay from the end of address		0		ns
$t_{d(AD-WR)}$	WR signal output delay from the end of address		0		ns
$t_{dz(RD-AD)}$	Address output floating start time			8	ns

Notes:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f_{(BCLK)}} - 10[\text{ns}]$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{(n - 0.5) \times 10^9}{f_{(BCLK)}} - 40[\text{ns}] \quad n \text{ is 2 for 2-wait setting, 3 for 3-wait setting.}$$

3. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f_{(BCLK)}} - 25[\text{ns}]$$

4. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f_{(BCLK)}} - 15[\text{ns}]$$

5. When using multiplex bus, set $f_{(BCLK)}$ 12.5 MHz or less.

6. Calculated according to the BCLK frequency as follows: $\frac{0.5 \times 10^9}{f_{(BCLK)}} - 20[\text{ns}]$

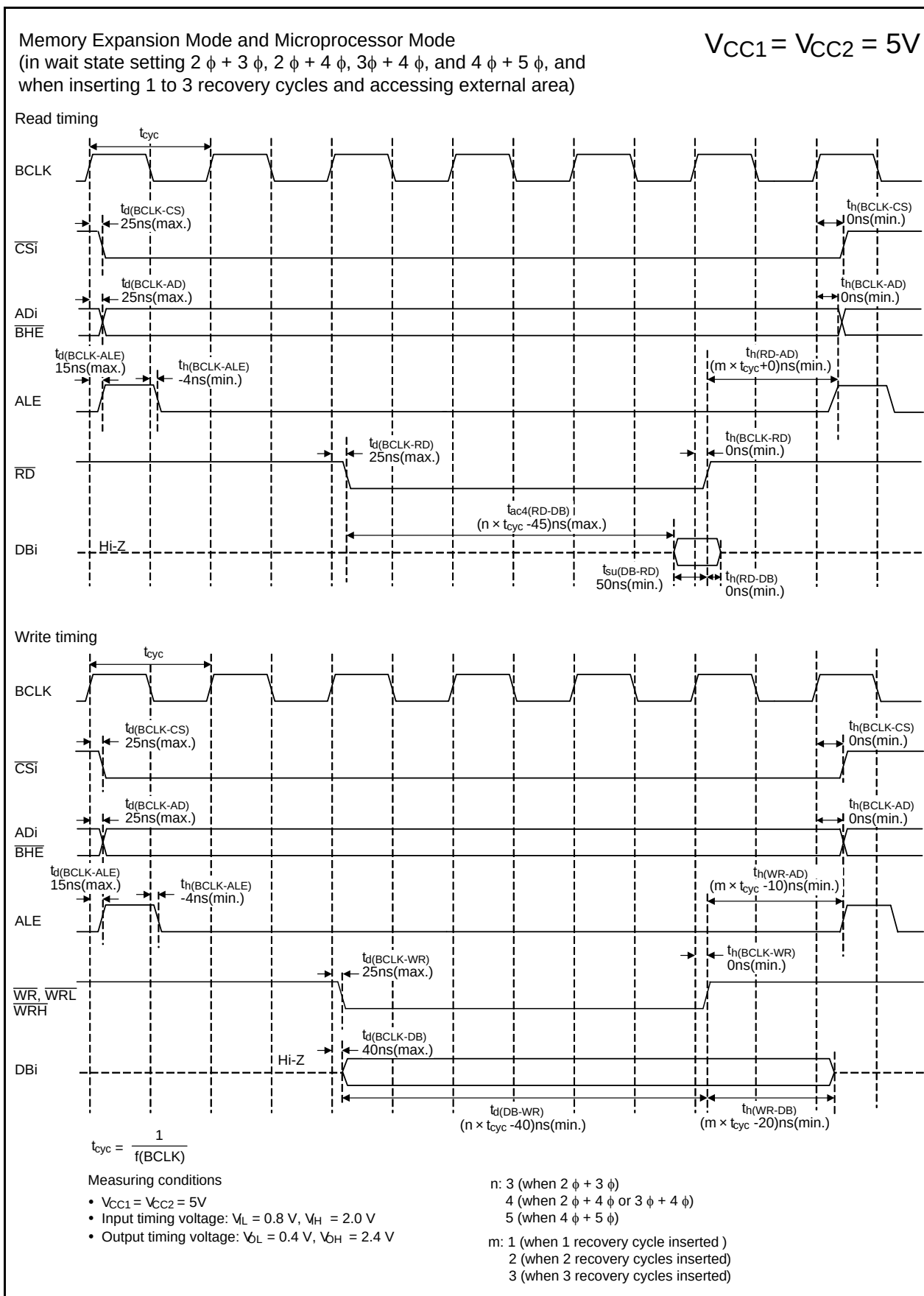


Figure 5.19 Timing Diagram

5.3 Electrical Characteristics ($V_{CC1} = V_{CC2} = 3\text{ V}$)

5.3.1 Electrical Characteristics

 $V_{CC1} = V_{CC2} = 3\text{ V}$
Table 5.41 Electrical Characteristics (1) (1)
 $V_{CC1} = V_{CC2} = 2.7\text{ to }3.3\text{ V}$, $V_{SS} = 0\text{ V}$ at $T_{opr} = -20^{\circ}\text{C to }85^{\circ}\text{C}/-40^{\circ}\text{C to }85^{\circ}\text{C}$, $f_{(BCLK)} = 32\text{ MHz}$ unless otherwise specified.

Symbol	Parameter		Measuring Condition	Standard			Unit
				Min.	Typ.	Max.	
V_{OH}	High output voltage	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1	$I_{OH} = -1\text{ mA}$	$V_{CC1} - 0.5$		V_{CC1}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7	$I_{OH} = -1\text{ mA}$	$V_{CC2} - 0.5$		V_{CC2}	
V_{OH}	High output voltage XOUT	HIGH POWER	$I_{OH} = -0.1\text{ mA}$	$V_{CC1} - 0.5$		V_{CC1}	V
		LOW POWER	$I_{OH} = -50\text{ }\mu\text{A}$	$V_{CC1} - 0.5$		V_{CC1}	
	High output voltage XCOUT	HIGH POWER	With no load applied		2.6		V
		LOW POWER	With no load applied		2.2		
V_{OL}	Low output voltage	P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1	$I_{OL} = 1\text{ mA}$			0.5	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7	$I_{OL} = 1\text{ mA}$			0.5	
	CEC		$I_{OL} = 1\text{ mA}$		0	0.5	V
V_{OL}	Low output voltage XOUT	HIGH POWER	$I_{OL} = 0.1\text{ mA}$			0.5	V
		LOW POWER	$I_{OL} = 50\text{ }\mu\text{A}$			0.5	
	Low output voltage XCOUT	HIGH POWER	With no load applied		0		V
		LOW POWER	With no load applied		0		
$V_{T+}-V_{T-}$	Hysteresis	HOLD, RDY, TA0IN to TA4IN, TB0IN to TB5IN, INT0 to INT7, NMI, ADTRG, CTS0 to CTS2, CTS5 to CTS7, SCL0 to SCL2, SCL5 to SCL7, SDA0 to SDA2, SDA5 to SDA7, CLK0 to CLK7, TA0OUT to TA4OUT, K10 to K13, RXD0 to RXD2, RXD5 to RXD7, SIN3, SIN4, $\overline{\text{SD}}$, PMC0, PMC1, SCLMM, SDAMM, ZP, IDU, IDV, IDW		0.2		1.0	V
		CEC		0.2	0.5	1.0	V
		RESET		0.2		1.8	V
I_{IH}	High input current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1 XIN, RESET, CNVSS, BYTE	$V_I = 3\text{ V}$			4.0	μA
–	Leakage current in powered-off state		CEC	$V_{CC1} = 0\text{ V}$		1.8	μA
I_{IL}	Low input current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1 XIN, RESET, CNVSS, BYTE	$V_I = 0\text{ V}$			–4.0	μA
R_{PULLUP}	Pull-up resistance	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1	$V_I = 0\text{ V}$	50	80	150	$\text{k}\Omega$
R_{FXIN}	Feedback resistance XIN				3.0		$\text{M}\Omega$
V_{RAM}	RAM retention voltage		In stop mode	1.8			V

Note:

- When $V_{CC1} \neq V_{CC2}$, refer to 5 V or 3 V standard depending on the voltage.

$$V_{CC1} = V_{CC2} = 3\text{ V}$$

Timing Requirements

($V_{CC1} = V_{CC2} = 3\text{ V}$, $V_{SS} = 0\text{ V}$, at $T_{opr} = -20^{\circ}\text{C}$ to 85°C / -40°C to 85°C unless otherwise specified)

5.3.2.3 Timer A Input**Table 5.47 Timer A Input (Counter Input in Event Counter Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	150		ns
$t_{w(TAH)}$	TAiIN input high pulse width	60		ns
$t_{w(TAL)}$	TAiIN input low pulse width	60		ns

Table 5.48 Timer A Input (Gating Input in Timer Mode)

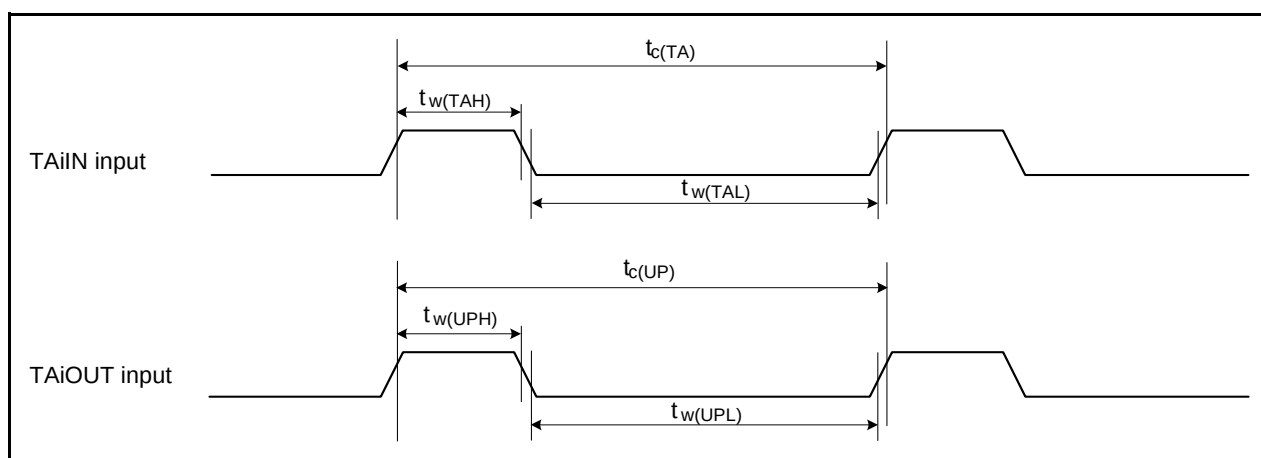
Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	600		ns
$t_{w(TAH)}$	TAiIN input high pulse width	300		ns
$t_{w(TAL)}$	TAiIN input low pulse width	300		ns

Table 5.49 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	300		ns
$t_{w(TAH)}$	TAiIN input high pulse width	150		ns
$t_{w(TAL)}$	TAiIN input low pulse width	150		ns

Table 5.50 Timer A Input (External Trigger Input in Pulse Width Modulation Mode and Programmable Output Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiIN input high pulse width	150		ns
$t_{w(TAL)}$	TAiIN input low pulse width	150		ns

**Figure 5.22 Timer A Input**

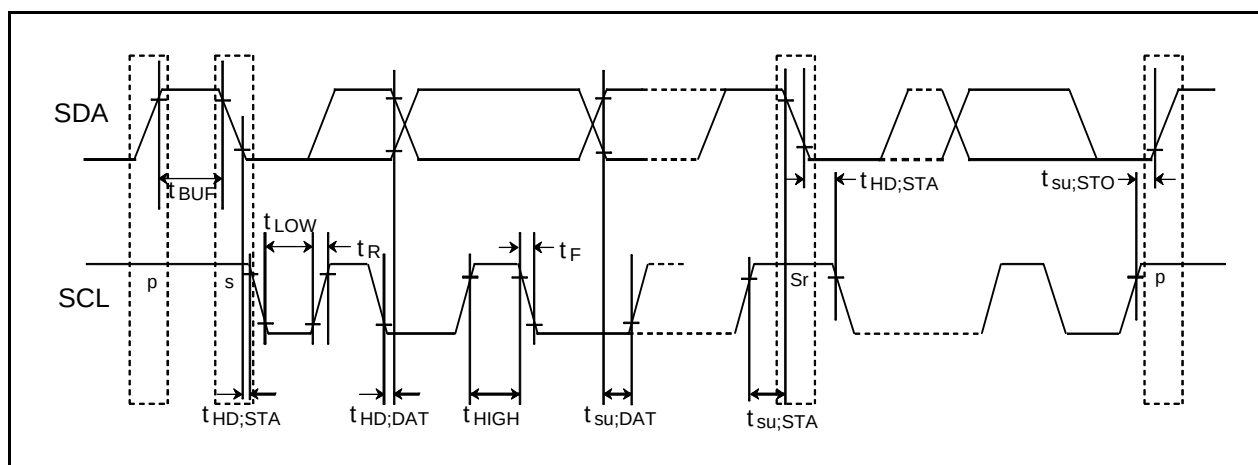
$$V_{CC1} = V_{CC2} = 3\text{ V}$$

Timing Requirements

($V_{CC1} = V_{CC2} = 3\text{ V}$, $V_{SS} = 0\text{ V}$, at $T_{opr} = -20^{\circ}\text{C}$ to $85^{\circ}\text{C}/-40^{\circ}\text{C}$ to 85°C unless otherwise specified)

5.3.2.7 Multi-master I²C-bus**Table 5.57 Multi-master I²C-bus**

Symbol	Parameter	Standard Clock Mode		Fast-mode		Unit
		Min.	Max.	Min.	Max.	
t_{BUF}	Bus free time	4.7		1.3		μs
$t_{HD;STA}$	Hold time in start condition	4.0		0.6		μs
t_{LOW}	Hold time in SCL clock 0 status	4.7		1.3		μs
t_R	SCL, SDA signals' rising time		1000	$20 + 0.1 C_b$	300	ns
$t_{HD;DAT}$	Data hold time	0		0	0.9	μs
t_{HIGH}	Hold time in SCL clock 1 status	4.0		0.6		μs
t_F	SCL, SDA signals' falling time		300	$20 + 0.1 C_b$	300	ns
$t_{su;DAT}$	Data setup time	250		100		ns
$t_{su;STA}$	Setup time in restart condition	4.7		0.6		μs
$t_{su;STO}$	Stop condition setup time	4.0		0.6		μs

**Figure 5.27 Multi-master I²C-bus**

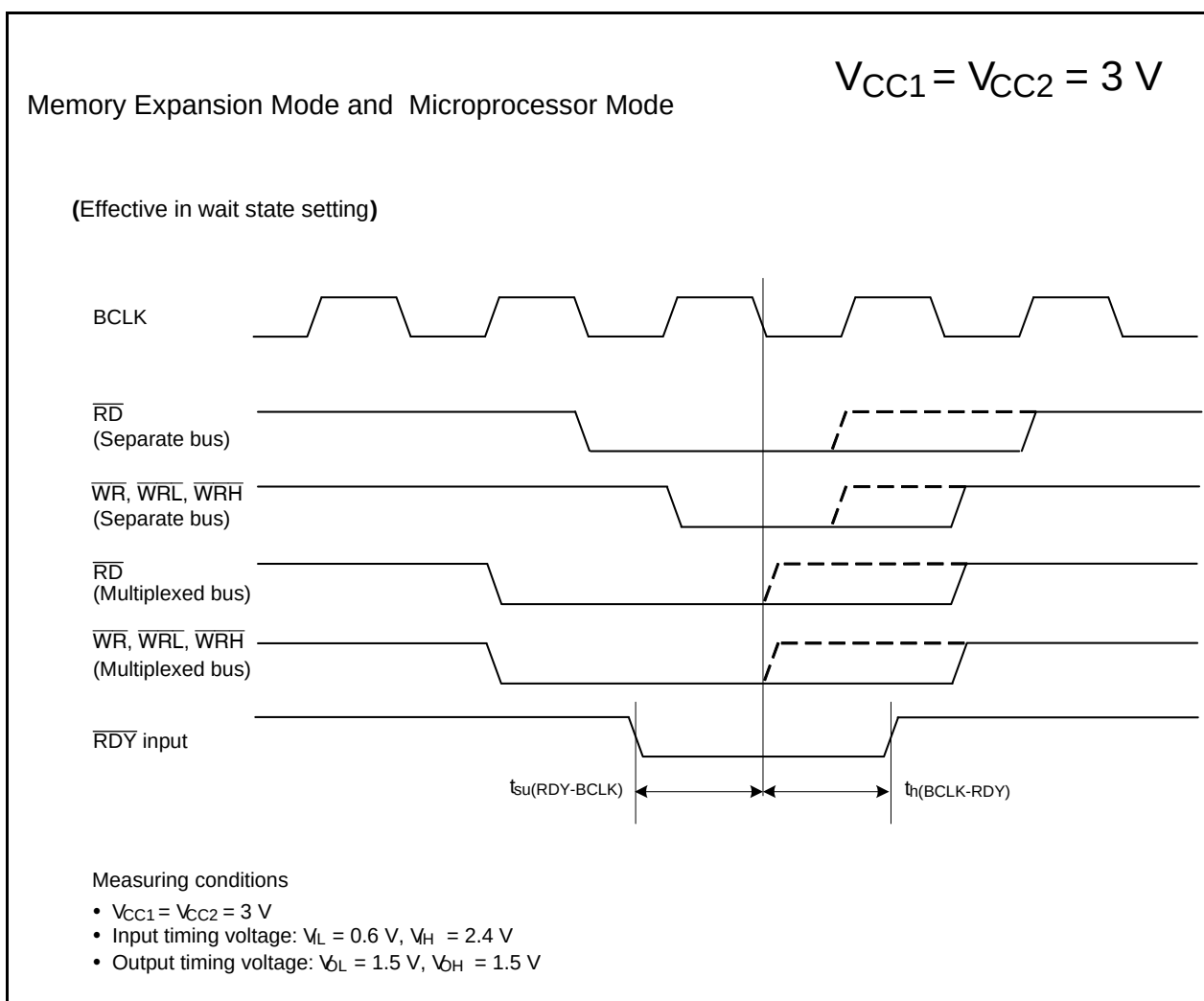
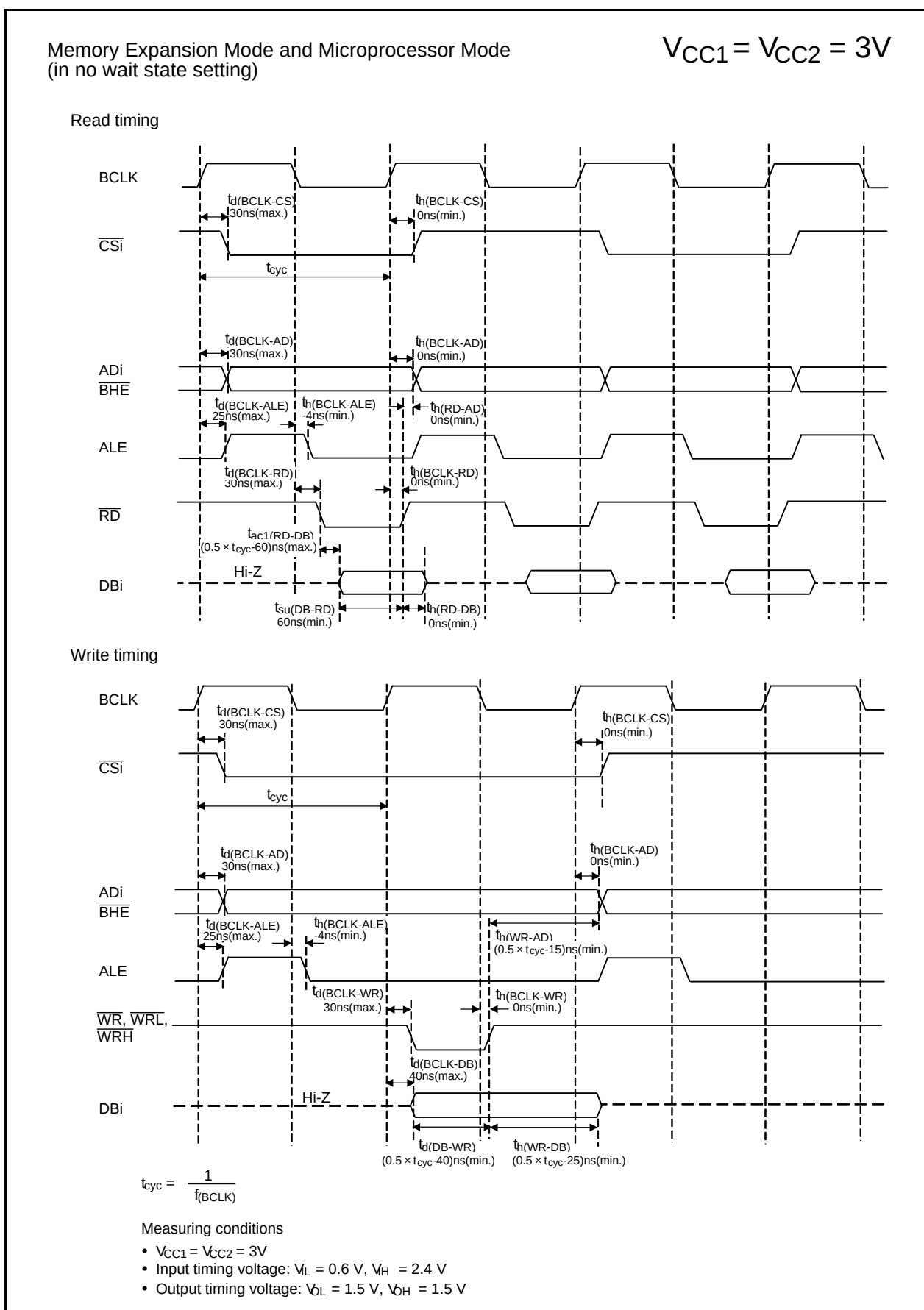
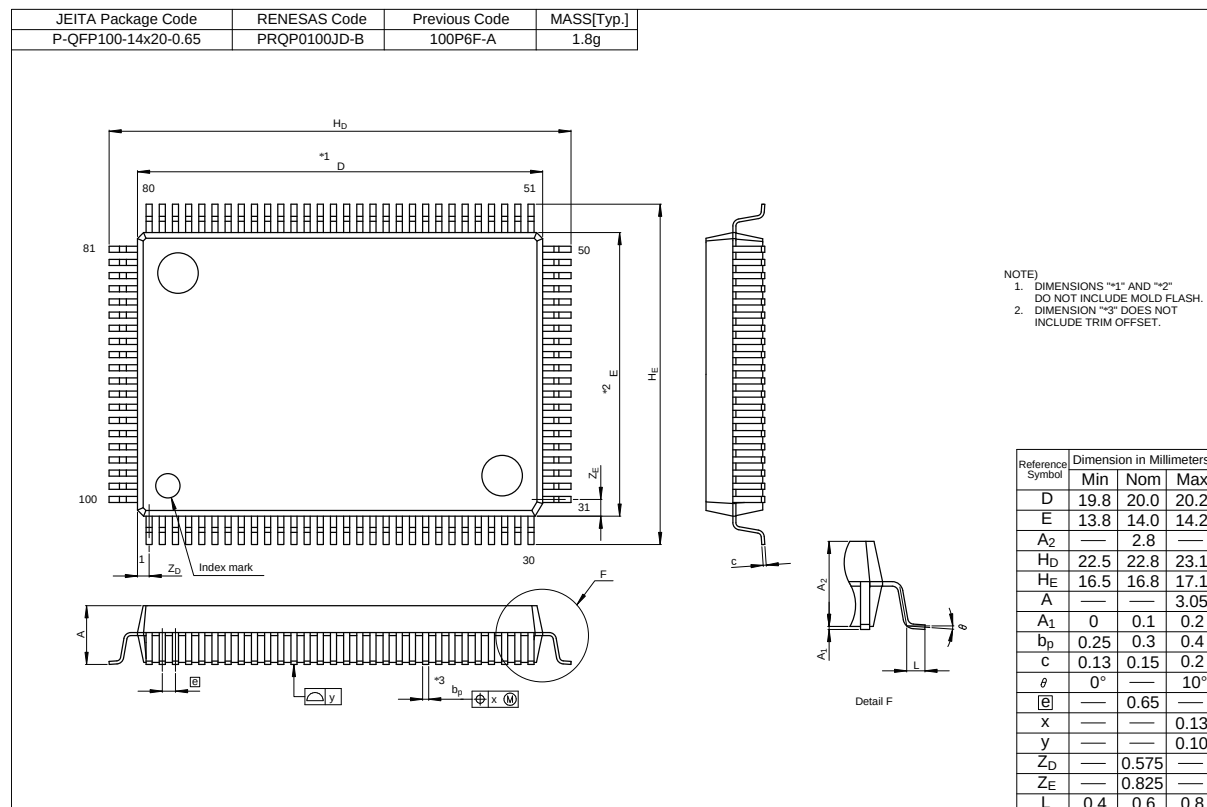
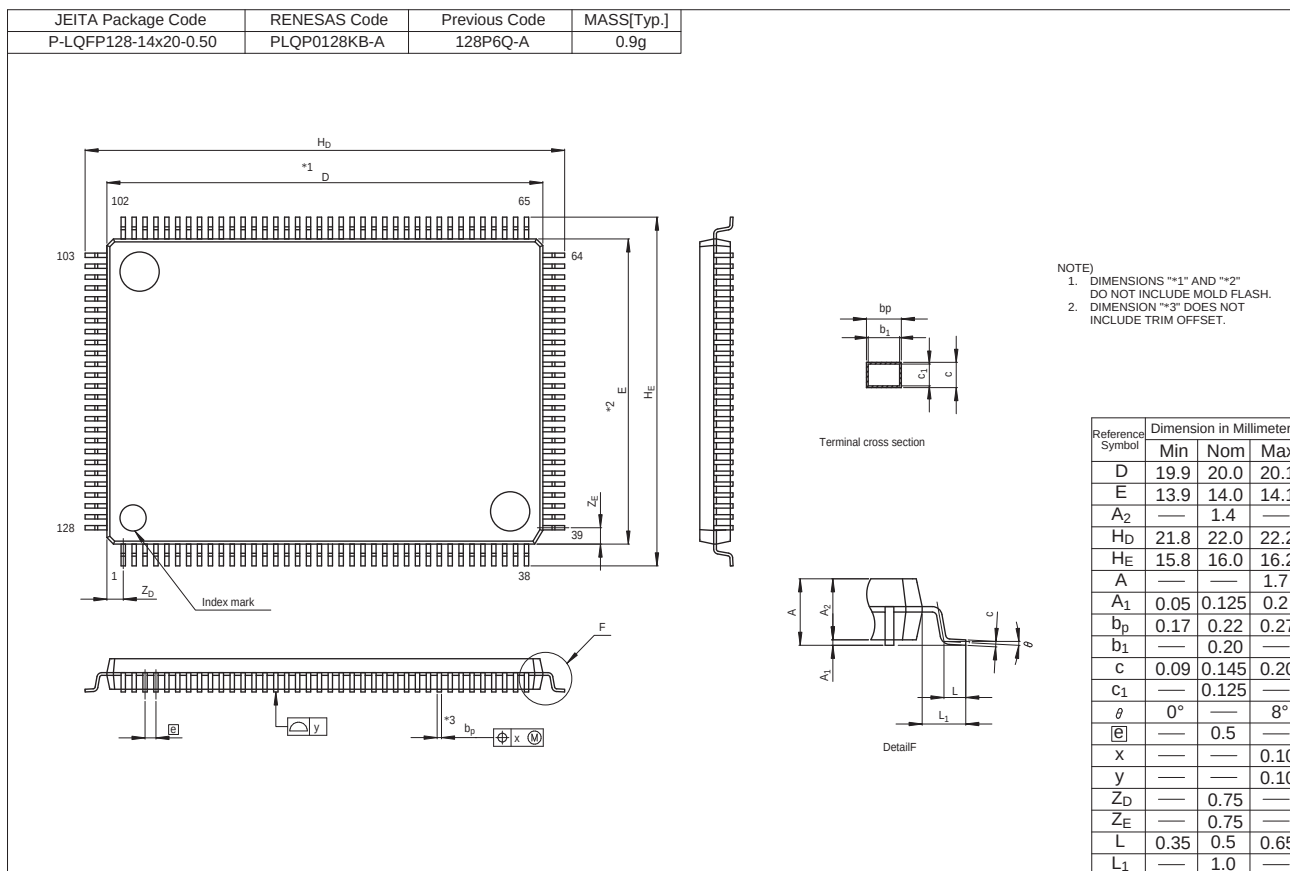


Figure 5.28 Timing Diagram



Appendix 1. Package Dimensions

The information on the latest package dimensions or packaging may be obtained from "Packages" on the Renesas Electronics website.



REVISION HISTORY	M16C/65C Group Datasheet
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Rev.	Date	Description	
		Page	Summary
0.10	Oct 29, 2010	-	First Edition issued.
1.00	Feb 07, 2011	Overall	Changed terminologies are as follows: • “oscillation/oscillator circuit” to “oscillator” • “oscillator” to “a crystal/ceramic resonator” • “oscillator manufacturer” to “manufacturer of crystal/ceramic resonator” • “on-chip oscillator oscillation circuit” to “on-chip oscillator”
		Overview	
		3, 5	Table 1.2 Specifications for the 128-Pin Package (2/2), Table 1.4 Specifications for the 100-Pin Package (2/2): Changed the Description column of the Current Consumption row.
		6	Table 1.5 Product List (N-Version), Table 1.6 Product List (D-Version): Changed the development status.
		Electrical Characteristics	
		VCC = 5 V	
		64, 65	Table 5.20 Electrical Characteristics (3), Table 5.21 Electrical Characteristics (4): Added conditions with XIN is 6MHz to the Wait mode measuring condition.
		74, 77, 79, 81, 83	In Switching Characteristics (Memory Expansion Mode and Microprocessor Mode), Table 5.36, Table 5.37, Table 5.38, Table 5.39, Table 5.40: • Deleted the th(BCLK-DB) row. • Changed the formula of th(WR-DB) for minimum standard.
		76, 78, 80, 82, 84	Figure 5.15, Figure 5.16, Figure 5.17, Figure 5.18, Figure 5.19: Deleted the description of th(BCLK-DB), and changed the formula of th(WR-DB) in the Write timing.
		VCC = 3 V	
		86, 87	Table 5.42 Electrical Characteristics (2), Table 5.43 Electrical Characteristics (3) (1/2): Added conditions with XIN is 6MHz to the Wait mode measuring condition.
		95, 97, 100, 102, 104	In Switching Characteristics (Memory Expansion Mode and Microprocessor Mode), Table 5.58, Table 5.59, Table 5.60, Table 5.61, Table 5.62: • Deleted the th(BCLK-DB) row. • Changed the formula of th(WR-AD) for minimum standard. • Changed the formula of th(WR-DB) for minimum standard.
		99, 101, 103, 105, 107	Figure 5.30, Figure 5.31, Figure 5.32, Figure 5.33, Figure 5.34: • Deleted the description of th(BCLK-DB), and changed the formulas of th(WR-AD) and th(WR-DB) in the Write timing.
1.10	Jul 31, 2012	Overview	
		6	Table 1.5 Product List (N-Version), Table 1.6 Product List (D-Version): Changed development statuses.
		Electrical Characteristics	
		Vcc = 5 V	
		64, 65	Table 5.20 Electrical Characteristics (3) and Table 5.21 Electrical Characteristics (4): Changed the Measuring Condition column of 40 MHz on-chip oscillator for the 40 MHz on-chip oscillator mode in the I _{CC} .
		Vcc = 3 V	
		86, 87	Table 5.42 Electrical Characteristics (2) and Table 5.43 Electrical Characteristics (3) (1/2): Changed the Measuring Condition column of 40 MHz on-chip oscillator for the 40 MHz on-chip oscillator mode in the I _{CC} .

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