Renesas Electronics America Inc - R5F3651NCNFC#V0 Datasheet

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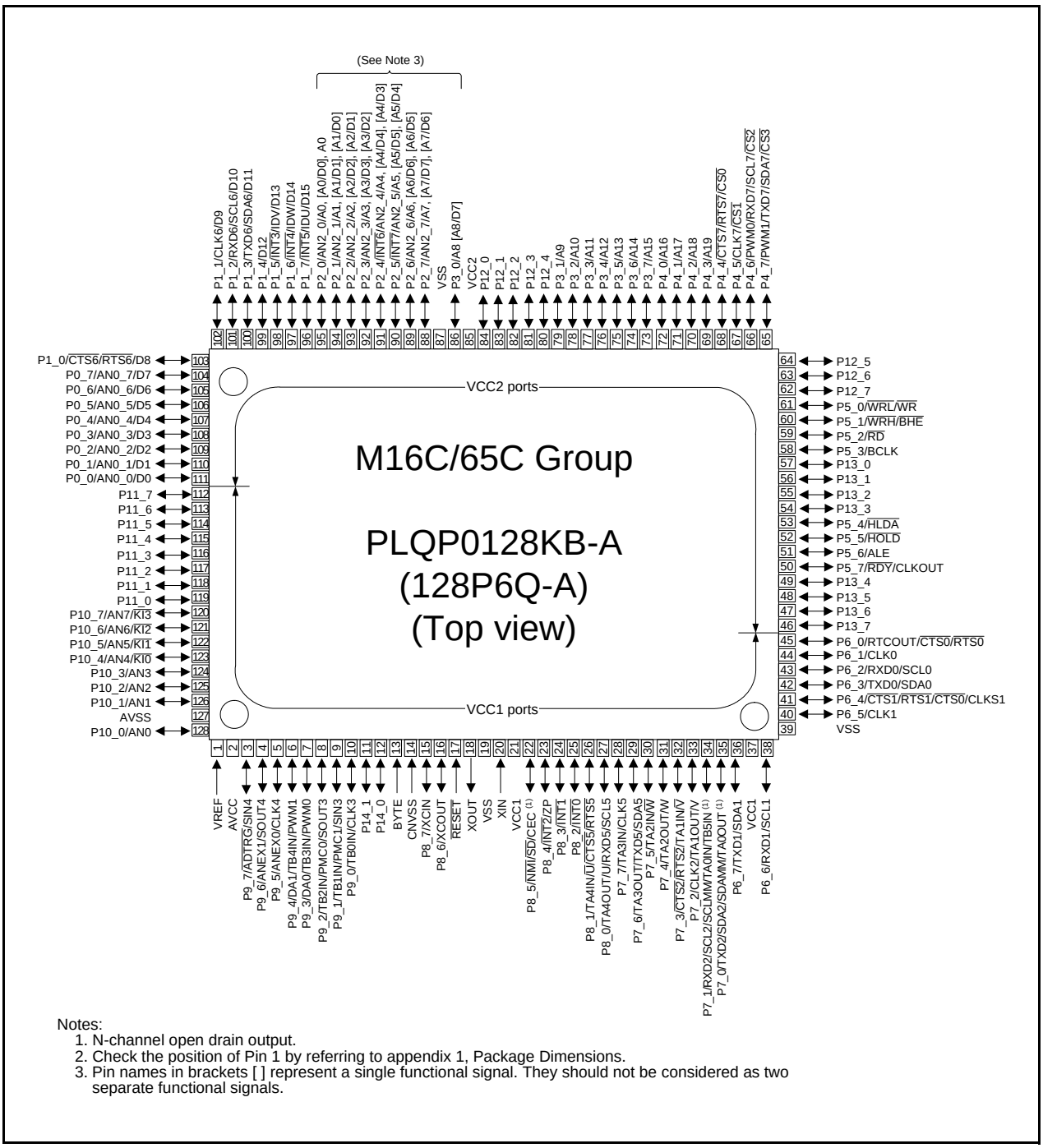
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	M16C/60
Core Size	16-Bit
Speed	32MHz
Connectivity	EBI/EMI, I²C, SIO, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	111
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	47K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	128-LQFP
Supplier Device Package	128-LFQFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f3651ncnfc-v0

1.5 Pin Assignments

Figure 1.5 to Figure 1.7 show pin assignments. Table 1.7 to Table 1.11 list pin names.



Notes:
1. N-channel open drain output.
2. Check the position of Pin 1 by referring to appendix 1, Package Dimensions.
3. Pin names in brackets [ ] represent a single functional signal. They should not be considered as two separate functional signals.

Figure 1.5 Pin Assignment for the 128-Pin Package

Table 1.8 Pin Names for the 128-Pin Package (2/3)

Pin No.	Control Pin	Port	I/O Pin for Peripheral Function				Bus Control Pin
			Interrupt	Timer	Serial interface	A/D converter, D/A converter	
51		P5_6					ALE
52		P5_5					$\overline{\text{HOLD}}$
53		P5_4					$\overline{\text{HLDA}}$
54		P13_3					
55		P13_2					
56		P13_1					
57		P13_0					
58		P5_3					BCLK
59		P5_2					$\overline{\text{RD}}$
60		P5_1					$\overline{\text{WRH/BHE}}$
61		P5_0					$\overline{\text{WRL/WR}}$
62		P12_7					
63		P12_6					
64		P12_5					
65		P4_7		PWM1	TXD7/SDA7		$\overline{\text{CS3}}$
66		P4_6		PWM0	RXD7/SCL7		$\overline{\text{CS2}}$
67		P4_5			CLK7		$\overline{\text{CS1}}$
68		P4_4			$\overline{\text{CTS7/RTS7}}$		$\overline{\text{CS0}}$
69		P4_3					A19
70		P4_2					A18
71		P4_1					A17
72		P4_0					A16
73		P3_7					A15
74		P3_6					A14
75		P3_5					A13
76		P3_4					A12
77		P3_3					A11
78		P3_2					A10
79		P3_1					A9
80		P12_4					
81		P12_3					
82		P12_2					
83		P12_1					
84		P12_0					
85	VCC2						
86		P3_0					A8, [A8/D7]
87	VSS						
88		P2_7				AN2_7	A7, [A7/D7], [A7/D6]
89		P2_6				AN2_6	A6, [A6/D6], [A6/D5]
90		P2_5	$\overline{\text{INT7}}$			AN2_5	A5, [A5/D5], [A5/D4]
91		P2_4	$\overline{\text{INT6}}$			AN2_4	A4[A4/D4], [A4/D3]
92		P2_3				AN2_3	A3, [A3/D3], [A3/D2]
93		P2_2				AN2_2	A2, [A2/D2], [A2/D1]
94		P2_1				AN2_1	A1, [A1/D1], [A1/D0]
95		P2_0				AN2_0	A0, [A0/D0], A0
96		P1_7	$\overline{\text{INT5}}$	IDU			D15
97		P1_6	$\overline{\text{INT4}}$	IDW			D14
98		P1_5	$\overline{\text{INT3}}$	IDV			D13
99		P1_4					D12
100		P1_3			TXD6/SDA6		D11

Table 1.9 Pin Names for the 128-Pin Package (3/3)

Pin No.	Control Pin	Port	I/O Pin for Peripheral Function				Bus Control Pin
			Interrupt	Timer	Serial interface	A/D converter, D/A converter	
101		P1_2			RXD6/SCL6		D10
102		P1_1			CLK6		D9
103		P1_0			$\overline{\text{CTS6/RTS6}}$		D8
104		P0_7				AN0_7	D7
105		P0_6				AN0_6	D6
106		P0_5				AN0_5	D5
107		P0_4				AN0_4	D4
108		P0_3				AN0_3	D3
109		P0_2				AN0_2	D2
110		P0_1				AN0_1	D1
111		P0_0				AN0_0	D0
112		P11_7					
113		P11_6					
114		P11_5					
115		P11_4					
116		P11_3					
117		P11_2					
118		P11_1					
119		P11_0					
120		P10_7	$\overline{\text{KI3}}$			AN7	
121		P10_6	$\overline{\text{KI2}}$			AN6	
122		P10_5	$\overline{\text{KI1}}$			AN5	
123		P10_4	$\overline{\text{KI0}}$			AN4	
124		P10_3				AN3	
125		P10_2				AN2	
126		P10_1				AN1	
127	AVSS						
128		P10_0				AN0	

1.6 Pin Functions

Table 1.12 Pin Functions for the 128-Pin Package (1/3)

Signal Name	Pin Name	I/O	Power Supply	Description
Power supply input	VCC1, VCC2, VSS	I	-	Apply 2.7 to 5.5 V to pins VCC1 and VCC2 (VCC1 ≥ VCC2), and 0 V to the VSS pin.
Analog power supply input	AVCC, AVSS	I	VCC1	This is the power supply for the A/D and D/A converters. Connect the AVCC pin to VCC1, and connect the AVSS pin to VSS.
Reset input	$\overline{\text{RESET}}$	I	VCC1	Driving this pin low resets the MCU.
CNVSS	CNVSS	I	VCC1	Input pin to switch processor modes. After a reset, to start operating in single-chip mode, connect the CNVSS pin to VSS via a resistor. To start operating in microprocessor mode, connect the pin to VCC1.
External data bus width select input	BYTE	I	VCC1	Input pin to select the data bus of the external area. The data bus is 16 bits when it is low and 8 bits when it is high. This pin must be fixed either high or low. Connect the BYTE pin to VSS in single-chip mode.
Bus control pins	D0 to D7	I/O	VCC2	Inputs or outputs data (D0 to D7) while accessing an external area with a separate bus.
	D8 to D15	I/O	VCC2	Inputs or outputs data (D8 to D15) while accessing an external area with a 16-bit separate bus.
	A0 to A19	O	VCC2	Outputs address bits A0 to A19.
	A0/D0 to A7/D7	I/O	VCC2	Inputs or outputs data (D0 to D7) and outputs address bits (A0 to A7) by timesharing, while accessing an external area with an 8-bit multiplexed bus.
	A1/D0 to A8/D7	I/O	VCC2	Inputs or outputs data (D0 to D7) and outputs address bits (A1 to A8) by timesharing, while accessing an external area with a 16-bit multiplexed bus.
	$\overline{\text{CS0}}$ to $\overline{\text{CS3}}$	O	VCC2	Outputs chip-select signals $\overline{\text{CS0}}$ to $\overline{\text{CS3}}$ to specify an external area.
	$\overline{\text{WRL}}$/$\overline{\text{WR}}$ $\overline{\text{WRH}}$/$\overline{\text{BHE}}$ $\overline{\text{RD}}$	O	VCC2	Outputs $\overline{\text{WRL}}$, $\overline{\text{WRH}}$, ($\overline{\text{WR}}$, $\overline{\text{BHE}}$), and $\overline{\text{RD}}$ signals. $\overline{\text{WRL}}$ and $\overline{\text{WRH}}$ can be switched with $\overline{\text{BHE}}$ and $\overline{\text{WR}}$. • $\overline{\text{WRL}}$, $\overline{\text{WRH}}$, and $\overline{\text{RD}}$ selected If the external data bus is 16 bits, data is written to an even address in an external area when $\overline{\text{WRL}}$ is driven low. Data is written to an odd address when $\overline{\text{WRH}}$ is driven low. Data is read when $\overline{\text{RD}}$ is driven low. • $\overline{\text{WR}}$, $\overline{\text{BHE}}$, and $\overline{\text{RD}}$ selected Data is written to an external area when $\overline{\text{WR}}$ is driven low. Data in an external area is read when $\overline{\text{RD}}$ is driven low. An odd address is accessed when $\overline{\text{BHE}}$ is driven low. Select $\overline{\text{WR}}$, $\overline{\text{BHE}}$, and $\overline{\text{RD}}$ when using an 8-bit external data bus.
	ALE	O	VCC2	Outputs an ALE signal to latch the address.
	$\overline{\text{HOLD}}$	I	VCC2	$\overline{\text{HOLD}}$ input is unavailable. Connect the $\overline{\text{HOLD}}$ pin to VCC2 via a resistor (pull-up).
	$\overline{\text{HLDA}}$	O	VCC2	In a hold state, $\overline{\text{HLDA}}$ outputs a low-level signal.
	$\overline{\text{RDY}}$	I	VCC2	The MCU bus is placed in wait state while the $\overline{\text{RDY}}$ pin is driven low.

Power supply: VCC2 is used to supply power to the external bus associated pins. The dual power supply configuration allows VCC2 to interface at a different voltage than VCC1.

Table 1.17 Pin Functions for the 100-Pin Package (3/3)

Signal Name	Pin Name	I/O	Power Supply	Description
UART0 to UART2, UART5 to UART7 I^2C mode	SDA0 to SDA2, SDA5	I/O	VCC1	Serial data I/O.
	SDA6, SDA7	I/O	VCC2	
	SCL0 to SCL2, SCL5	I/O	VCC1	Transmit/receive clock I/O.
	SCL6, SCL7	I/O	VCC2	
Serial interface SI/O3, SI/O4	CLK3, CLK4	I/O	VCC1	Transmit/receive clock I/O.
	SIN3, SIN4	I	VCC1	Serial data input.
	SOUT3, SOUT4	O	VCC1	Serial data output.
Multi-master I^2C-bus interface	SDAMM	I/O	VCC1	Serial data I/O (N-channel open drain output).
	SCLMM	I/O	VCC1	Transmit/receive clock I/O (N-channel open drain output).
CEC I/O	CEC	I/O	VCC1	CEC I/O (N-channel open drain output).
Reference voltage input	VREF	I	VCC1	Reference voltage input for the A/D and D/A converters.
A/D converter	AN0 to AN7	I	VCC1	Analog input.
	AN0_0 to AN0_7 AN2_0 to AN2_7	I	VCC2	
	$\overline{\text{ADTRG}}$	I	VCC1	External trigger input.
	ANEX0, ANEX1	I	VCC1	Extended analog input.
D/A converter	DA0, DA1	O	VCC1	Output for the D/A converter.
I/O ports	P0_0 to P0_7 P1_0 to P1_7 P2_0 to P2_7 P3_0 to P3_7 P4_0 to P4_7 P5_0 to P5_7	I/O	VCC2	8-bit CMOS I/O ports. A direction register determines whether each pin is used as an input port or an output port. A pull-up resistor may be enabled or disabled for input ports in 4-bit units.
	P6_0 to P6_7 P7_0 to P7_7 P8_0 to P8_7 P9_0 to P9_7 P10_0 to P10_7	I/O	VCC1	8-bit I/O ports having equivalent functions to P0. However, P7_0, P7_1, and P8_5 are N-channel open drain output ports. No pull-up resistor is provided. P8_5 is an input port for verifying the $\overline{\text{NMI}}$ pin level and shares a pin with $\overline{\text{NMI}}$.

Table 4.6 SFR Information (6) (1)

Address	Register	Symbol	Reset Value
01B0h	DMA3 Source Pointer	SAR3	XXh
01B1h			XXh
01B2h			0Xh
01B3h			
01B4h	DMA3 Destination Pointer	DAR3	XXh
01B5h			XXh
01B6h			0Xh
01B7h			
01B8h	DMA3 Transfer Counter	TCR3	XXh
01B9h			XXh
01BAh			
01BBh			
01BCh	DMA3 Control Register	DM3CON	0000 0X00b
01BDh			
01BEh			
01BFh			
01C0h	Timer B0-1 Register	TB01	XXh
01C1h			XXh
01C2h	Timer B1-1 Register	TB11	XXh
01C3h			XXh
01C4h	Timer B2-1 Register	TB21	XXh
01C5h			XXh
01C6h	Pulse Period/Pulse Width Measurement Mode Function Select Register 1	PPWFS1	XXXX X000b
01C7h			
01C8h	Timer B Count Source Select Register 0	TBCS0	00h
01C9h	Timer B Count Source Select Register 1	TBCS1	X0h
01CAh			
01CBh	Timer AB Division Control Register 0	TCKDIVC0	0000 X000b
01CCh			
01CDh			
01CEh			
01CFh			
01D0h	Timer A Count Source Select Register 0	TACS0	00h
01D1h	Timer A Count Source Select Register 1	TACS1	00h
01D2h	Timer A Count Source Select Register 2	TACS2	X0h
01D3h			
01D4h	16-bit Pulse Width Modulation Mode Function Select Register	PWMFS	0XX0 X00Xb
01D5h	Timer A Waveform Output Function Select Register	TAPOFS	XXX0 0000b
01D6h			
01D7h			
01D8h	Timer A Output Waveform Change Enable Register	TAOW	XXX0 X00Xb
01D9h			
01DAh	Three-Phase Protect Control Register	TPRC	00h
01DBh			
01DCh			
01DDh			
01DEh			
01DFh			

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.10 SFR Information (10) (1)

Address	Register	Symbol	Reset Value
0270h	SI/O3 Transmit/Receive Register	S3TRR	XXh
0271h			
0272h	SI/O3 Control Register	S3C	0100 0000b
0273h	SI/O3 Bit Rate Register	S3BRG	XXh
0274h	SI/O4 Transmit/Receive Register	S4TRR	XXh
0275h			
0276h	SI/O4 Control Register	S4C	0100 0000b
0277h	SI/O4 Bit Rate Register	S4BRG	XXh
0278h	SI/O3, 4 Control Register 2	S34C2	00XX X0X0b
0279h			
027Ah			
027Bh			
027Ch			
027Dh			
027Eh			
027Fh			
0280h			
0281h			
0282h			
0283h			
0284h	UART5 Special Mode Register 4	U5SMR4	00h
0285h	UART5 Special Mode Register 3	U5SMR3	000X 0X0Xb
0286h	UART5 Special Mode Register 2	U5SMR2	X000 0000b
0287h	UART5 Special Mode Register	U5SMR	X000 0000b
0288h	UART5 Transmit/Receive Mode Register	U5MR	00h
0289h	UART5 Bit Rate Register	U5BRG	XXh
028Ah	UART5 Transmit Buffer Register	U5TB	XXh
028Bh			XXh
028Ch	UART5 Transmit/Receive Control Register 0	U5C0	0000 1000b
028Dh	UART5 Transmit/Receive Control Register 1	U5C1	0000 0010b
028Eh	UART5 Receive Buffer Register	U5RB	XXh
028Fh			XXh
0290h			
0291h			
0292h			
0293h			
0294h	UART6 Special Mode Register 4	U6SMR4	00h
0295h	UART6 Special Mode Register 3	U6SMR3	000X 0X0Xb
0296h	UART6 Special Mode Register 2	U6SMR2	X000 0000b
0297h	UART6 Special Mode Register	U6SMR	X000 0000b
0298h	UART6 Transmit/Receive Mode Register	U6MR	00h
0299h	UART6 Bit Rate Register	U6BRG	XXh
029Ah	UART6 Transmit Buffer Register	U6TB	XXh
029Bh			XXh
029Ch	UART6 Transmit/Receive Control Register 0	U6C0	0000 1000b
029Dh	UART6 Transmit/Receive Control Register 1	U6C1	0000 0010b
029Eh	UART6 Receive Buffer Register	U6RB	XXh
029Fh			XXh

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.14 SFR Information (14) (1)

Address	Register	Symbol	Reset Value
0360h	Pull-Up Control Register 0	PUR0	00h
0361h	Pull-Up Control Register 1	PUR1	0000 0000b (2) 0000 0010b
0362h	Pull-Up Control Register 2	PUR2	00h
0363h	Pull-Up Control Register 3	PUR3	00h
0364h			
0365h			
0366h	Port Control Register	PCR	0000 0XX0b
0367h			
0368h			
0369h	NMI/SD Digital Filter Register	NMIDF	XXXX X000b
036Ah			
036Bh			
036Ch			
036Dh			
036Eh			
036Fh			
0370h	PWM Control Register 0	PWMCON0	00h
0371h			
0372h	PWM0 Prescaler	PWMPRE0	00h
0373h	PWM0 Register	PWMREG0	00h
0374h	PWM1 Prescaler	PWMPRE1	00h
0375h	PWM1 Register	PWMREG1	00h
0376h	PWM Control Register 1	PWMCON1	00h
0377h			
0378h			
0379h			
037Ah			
037Bh			
037Ch	Count Source Protection Mode Register	CSPR	00h (3)
037Dh	Watchdog Timer Refresh Register	WDTR	XXh
037Eh	Watchdog Timer Start Register	WDTS	XXh
037Fh	Watchdog Timer Control Register	WDC	00XX XXXXb
0380h to 038Fh			

X: Undefined

Notes:
1. The blank areas are reserved. No access is allowed.
2. Values after hardware reset, power-on reset, or voltage monitor 0 reset are as follows:
 - 00000000b when a low-level signal is input to the CNVSS pin
 - 00000010b when a high-level signal is input to the CNVSS pin
 Values after voltage monitor 1 reset, voltage monitor 2 reset, software reset, watchdog timer reset, or oscillation stop detect reset are as follows:
 - 00000000b when bits PM01 and PM00 in the PM0 register are 00b (single-chip mode).
 - 00000010b when bits PM01 and PM00 in the PM0 register are 01b (memory expansion mode) or 11b (microprocessor mode).
3. When the CSPROINI bit in the OFS1 address is 0, the reset value is 1000 0000b.

Table 4.20 Read-Modify-Write Instructions

Function	Mnemonic
Transfer	MOV*Dir*
Bit processing	BCLR, BM*Cnd*, BNOT, BSET, BTSTC, and BTSTS
Shifting	ROLC, RORC, ROT, SHA, and SHL
Arithmetic operation	ABS, ADC, ADCF, ADD, DEC, DIV, DIVU, DIVX, EXTS, INC, MUL, MULU, NEG, SBB, and SUB
Decimal operation	DADC, DADD, DSBB, and DSUB
Logical operation	AND, NOT, OR, and XOR
Jump	ADJNZ, SBJNZ

5.1.3 A/D Conversion Characteristics

Table 5.5 A/D Conversion Characteristics (1/2) (1)

V_{CC1} = AV_{CC} = 3.0 to 5.5 V ≥ V_{CC2} ≥ V_{REF}, V_{SS} = AV_{SS} = 0 V at T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified.

Symbol	Parameter		Measuring Condition		Standard			Unit
					Min.	Typ.	Max.	
-	Resolution		AV_{CC} = V_{CC1} ≥ V_{CC2} ≥ V_{REF}				10	Bits
I_{NL}	Integral non-linearity error	10 bits	V_{CC1} = 5.0 V	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input (Note 2)			±3	LSB
			V_{CC1} = 3.3 V	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input (Note 2)			±3	LSB
			V_{CC1} = 3.0 V	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input (Note 2)			±3	LSB
-	Absolute accuracy	10 bits	V_{CC1} = 5.0 V	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input (Note 2)			±3	LSB
			V_{CC1} = 3.3 V	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input (Note 2)			±3	LSB
			V_{CC1} = 3.0 V	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input (Note 2)			±3	LSB

Notes:
1. Use when AV_{CC} = V_{CC1}.
2. Flash memory rewrite disabled. Except for the analog input pin, set the pins to be measured as input ports and connect them to V_{SS}. See Figure 5.2 “A/D Accuracy Measure Circuit”.

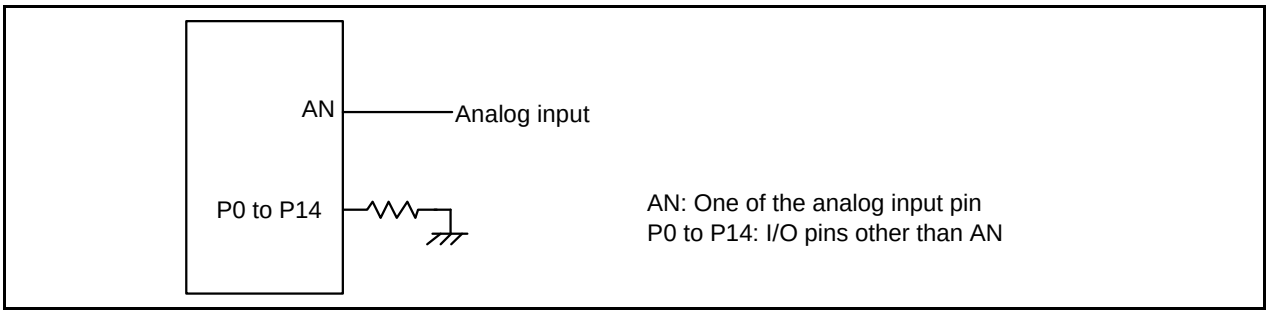


Figure 5.2 A/D Accuracy Measure Circuit

Table 5.6 A/D Conversion Characteristics (2/2) (1)

V_{CC1} = AV_{CC} = 3.0 to 5.5 V ≥ V_{CC2} ≥ V_{REF}, V_{SS} = AV_{SS} = 0 V at T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified.

Symbol	Parameter		Measuring Condition	Standard			Unit
				Min.	Typ.	Max.	
ϕAD	A/D operating clock frequency	AN0 to AN7 input, ANEX0 to ANEX1 input	4.0 V ≤ V_{CC1} ≤ 5.5 V	2		25	MHz
			3.2 V ≤ V_{CC1} ≤ 4.0 V	2		16	MHz
			3.0 V ≤ V_{CC1} ≤ 3.2 V	2		10	MHz
		AN0_0 to AN0_7 input, AN2_0 to AN2_7 input	4.0 V ≤ V_{CC2} ≤ 5.5 V	2		25	MHz
			3.2 V ≤ V_{CC2} ≤ 4.0 V	2		16	MHz
			3.0 V ≤ V_{CC2} ≤ 3.2 V	2		10	MHz
-	Tolerance level impedance				3		kΩ
D_{NL}	Differential non-linearity error		(4)			±1	LSB
-	Offset error		(4)			±3	LSB
-	Gain error		(4)			±3	LSB
t_{CONV}	10-bit conversion time		V_{CC1} = 5 V, ϕAD = 25 MHz	1.60			µs
t_{SAMP}	Sampling time			0.60			µs
V_{REF}	Reference voltage			3.0		V_{CC1}	V
V_{IA}	Analog input voltage (2), (3)			0		V_{REF}	V

Notes:
1. Use when AV_{CC} = V_{CC1}.
2. When V_{CC1} ≥ V_{CC2}, set as below:
   Analog input voltage (AN0 to AN7, ANEX0, and ANEX1) ≤ V_{CC1}
   Analog input voltage (AN0_0 to AN0_7 and AN2_0 to AN2_7) ≤ V_{CC2}.
3. When analog input voltage is over reference voltage, the result of A/D conversion is 3FFh.
4. Flash memory rewrite disabled. Except for the analog input pin, set the pins to be measured as input ports and connect them to V_{SS}. See Figure 5.2 “A/D Accuracy Measure Circuit”.

5.1.4 D/A Conversion Characteristics

Table 5.7 D/A Conversion Characteristics

V_{CC1} = AV_{CC} = V_{REF} = 3.0 to 5.5 V, V_{SS} = AV_{SS} = 0 V at T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified.

Symbol	Parameter	Measuring Condition	Standard			Unit
			Min.	Typ.	Max.	
-	Resolution				8	Bits
-	Absolute Accuracy				2.5	LSB
t_{SU}	Setup Time				3	µs
R_O	Output Resistance		5	6	8.2	kΩ
I_{VREF}	Reference Power Supply Input Current	See Notes 1 and 2			1.5	mA

Notes:
1. This applies when using one D/A converter, with the D/A register for the unused D/A converter set to 00h.
2. The current consumption of the A/D converter is not included. Also, the I_{VREF} of the D/A converter will flow even if the ADSTBY bit in the ADCON1 register is 0 (A/D operation stopped (standby)).

Table 5.10 Flash Memory (Data Flash) Electrical Characteristics

V_{CC1} = 2.7 to 5.5 V at T_{opr} = -20 to 85°C/-40 to 85°C, unless otherwise specified.

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
-	Program and erase cycles (1), (3), (4)	V_{CC1} = 3.3 V, T_{opr} = 25°C	10,000 (2)			times
-	2 word program time	V_{CC1} = 3.3 V, T_{opr} = 25°C		300	4000	µs
-	Lock bit program time	V_{CC1} = 3.3 V, T_{opr} = 25°C		140	3000	µs
-	Block erase time	V_{CC1} = 3.3 V, T_{opr} = 25°C		0.2	3.0	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend				$5 + \frac{3}{f_{(BCLK)}}$	ms
-	Interval from erase start/restart until following suspend request		0			µs
-	Suspend interval necessary for auto-erasure to complete (7)		20			ms
-	Time from suspend until erase restart				$30 + \frac{1}{f_{(BCLK)}}$	µs
-	Program, erase voltage		2.7		5.5	V
-	Read voltage		2.7		5.5	V
-	Program, erase temperature		–20/–40		85	°C
t_{PS}	Flash memory circuit stabilization wait time				50	µs
-	Data hold time (6)	Ambient temperature = 55°C	20			year

Notes:
1. Definition of program and erase cycles
   The program and erase cycles refer to the number of per-block erasures.
   If the program and erase cycles are n (n = 10,000), each block can be erased n times.
   For example, if a 4 KB block is erased after writing 2 word data 1,024 times, each to a different address, this counts as one program and erase cycles. Data cannot be written to the same address more than once without erasing the block (rewrite prohibited).
2. Cycles to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
3. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 256 groups before erasing them all in one operation. In addition, averaging the erasure cycles between blocks A and B can further reduce the actual erasure cycles. It is also advisable to retain data on the erasure cycles of each block and limit the number of erase operations to a certain number.
4. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
5. Customers desiring program/erase failure rate information should contact a Renesas Electronics sales office.
6. The data hold time includes time that the power supply is off or the clock is not supplied.
7. After an erase start or erase restart, if an interval of at least 20 ms is not set before the next suspend request, the erase sequence cannot be completed.

$V_{CC1} = V_{CC2} = 5\ V$

Timing Requirements

($V_{CC1} = V_{CC2} = 5$ V, $V_{SS} = 0$ V, at $T_{opr} = -20°C$ to 85°C/-40°C to 85°C unless otherwise specified)

5.2.2.3 Timer A Input

Table 5.24 Timer A Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	100		ns
$t_{w(TAH)}$	TAiIN input high pulse width	40		ns
$t_{w(TAL)}$	TAiIN input low pulse width	40		ns

Table 5.25 Timer A Input (Gating Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	400		ns
$t_{w(TAH)}$	TAiIN input high pulse width	200		ns
$t_{w(TAL)}$	TAiIN input low pulse width	200		ns

Table 5.26 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	200		ns
$t_{w(TAH)}$	TAiIN input high pulse width	100		ns
$t_{w(TAL)}$	TAiIN input low pulse width	100		ns

Table 5.27 Timer A Input (External Trigger Input in Pulse Width Modulation Mode and Programmable Output Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiIN input high pulse width	100		ns
$t_{w(TAL)}$	TAiIN input low pulse width	100		ns

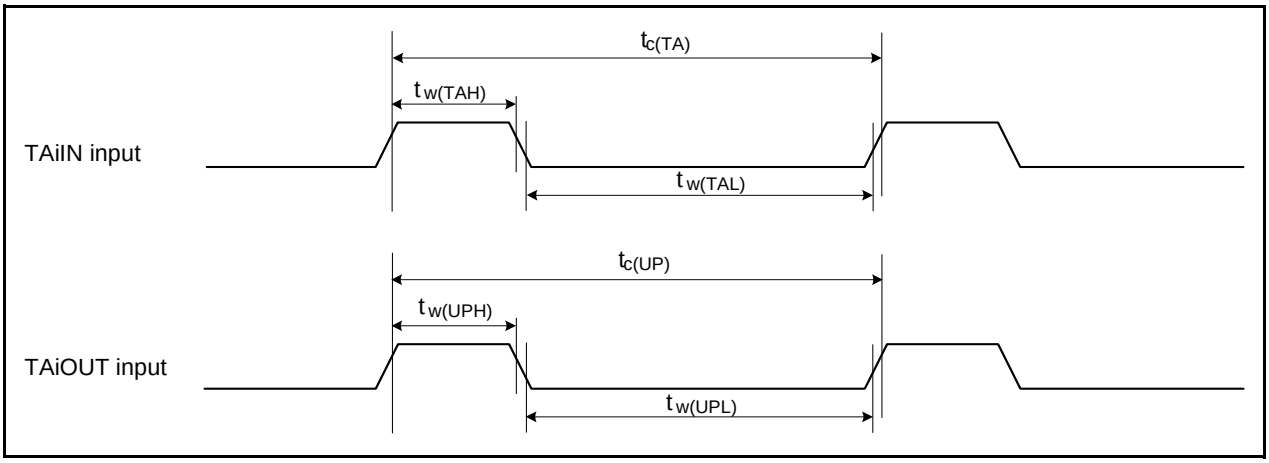
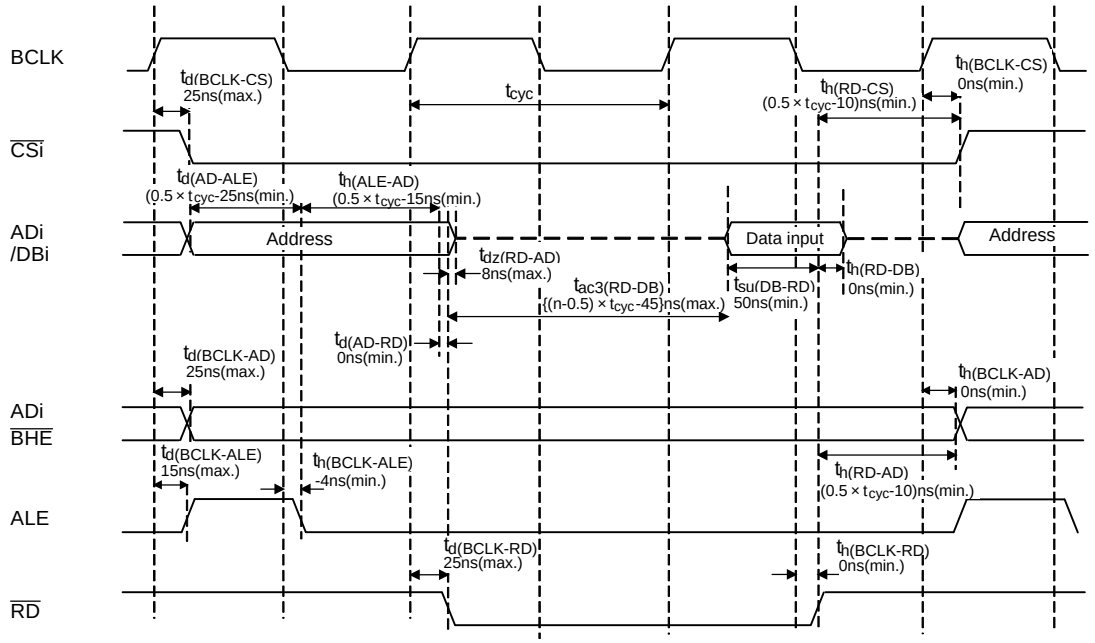


Figure 5.7 Timer A Input

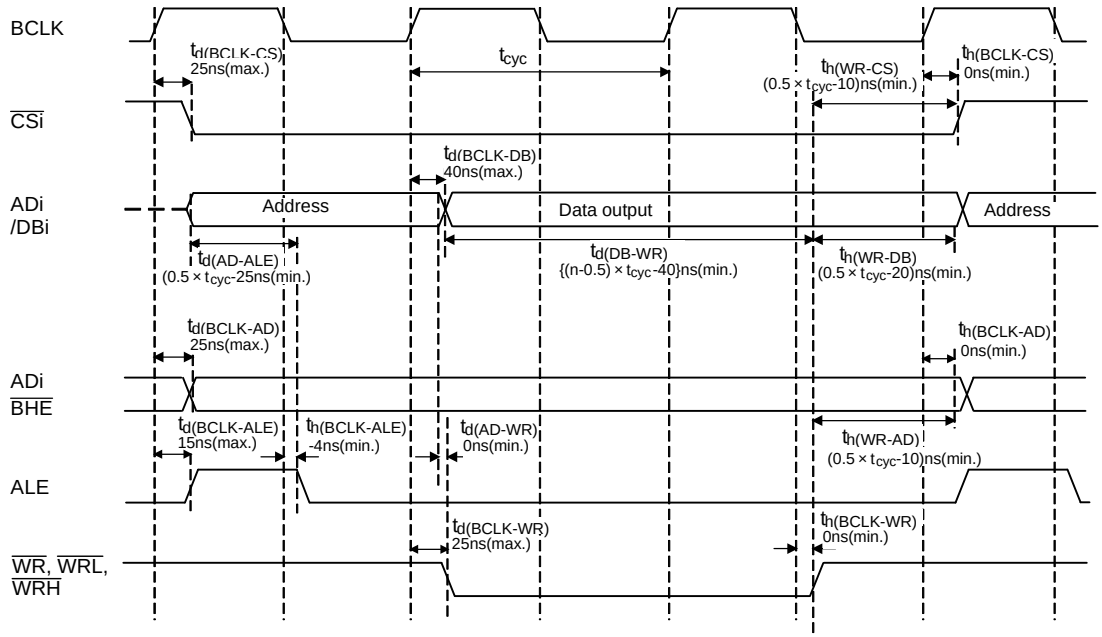
Memory Expansion Mode and Microprocessor Mode
(in 2 or 3 waits setting, and when accessing external area and using multiplexed bus)

$V_{CC1} = V_{CC2} = 5V$

Read timing



Write timing



n: 2 (when 2 waits)
3 (when 3 waits)

Measuring conditions

- $V_{CC1} = V_{CC2} = 5V$
- Input timing voltage: $V_{IL} = 0.8$ V, $V_{IH} = 2.0$ V
- Output timing voltage: $V_{OL} = 0.4$ V, $V_{OH} = 2.4$ V

Figure 5.17 Timing Diagram

$V_{CC1} = V_{CC2} = 5\ V$

Switching Characteristics

($V_{CC1} = V_{CC2} = 5$ V, $V_{SS} = 0$ V, at $T_{opr} = -20°C$ to 85°C/-40°C to 85°C unless otherwise specified)

5.2.4.4 In Wait State Setting 2ϕ + 3ϕ, 2ϕ + 4ϕ, 3ϕ + 4ϕ, and 4ϕ + 5ϕ, and When Accessing External Area

Table 5.39 Memory Expansion Mode and Microprocessor Mode (in Wait State Setting 2 ϕ + 3 ϕ, 2 ϕ + 4ϕ, 3ϕ + 4ϕ, and 4ϕ + 5ϕ, and When Accessing External Area)

Symbol	Parameter	Measuring Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	See Figure 5.14		25	ns
$t_{h(BCLK-AD)}$	Address output hold time (in relation to BCLK)		0		ns
$t_{h(RD-AD)}$	Address output hold time (in relation to RD)		0		ns
$t_{h(WR-AD)}$	Address output hold time (in relation to WR)		(Note 2)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			25	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (in relation to BCLK)		0		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time			15	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time		-4		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			25	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			25	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (in relation to BCLK)			40	ns
$t_{d(DB-WR)}$	Data output delay time (in relation to WR)		(Note 1)		ns
$t_{h(WR-DB)}$	Data output hold time (in relation to WR) (3)		(Note 4)		ns

Notes:

1. Calculated according to the BCLK frequency as follows:

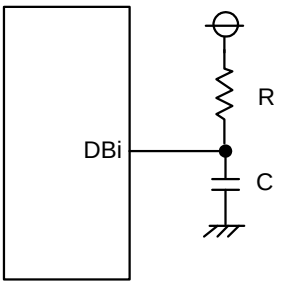
$$\frac{(n-0.5)\times 10^9}{f_{(BCLK)}} - 40[ns]$$

n is 3 for 2ϕ + 3ϕ, 4 for 2ϕ + 4ϕ, 4 for 3ϕ + 4ϕ, and 5 for 4ϕ + 5ϕ.

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5\times 10^9}{f_{(BCLK)}} - 10[ns]$$

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.
Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.
Hold time of data bus is expressed in
$t = -CR \times \ln(1 - V_{OL}/V_{CC2})$
by a circuit of the right figure.
For example, when $V_{OL} = 0.2V_{CC2}$, C = 30 pF, R = 1 kΩ, hold time of output low level is
$t = -30\ pF \times 1\ k\Omega \times \ln(1 - 0.2V_{CC2}/V_{CC2})$
= 6.7 ns.



4. Calculated according to the BCLK frequency as follows: $\frac{0.5\times 10^9}{f_{(BCLK)}} - 20[ns]$
Hold time is equal to or less than 0 ns when the BCLK frequency exceeds 25 MHz.

5.3 Electrical Characteristics (V_{CC1} = V_{CC2} = 3 V)

5.3.1 Electrical Characteristics

VCC1 = VCC2 = 3 V

Table 5.41 Electrical Characteristics (1) [1]

V_{CC1} = V_{CC2} = 2.7 to 3.3 V, V_{SS} = 0 V at T_{opr} = -20°C to 85°C/-40°C to 85°C, $f_{(BCLK)}$ = 32 MHz unless otherwise specified.

Symbol	Parameter			Measuring Condition	Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	High output voltage	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1		I_{OH} = –1 mA	V_{CC1} – 0.5		V_{CC1}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7		I_{OH} = –1 mA	V_{CC2} – 0.5		V_{CC2}	
V_{OH}	High output voltage XOUT		HIGH POWER	I_{OH} = –0.1 mA	V_{CC1} – 0.5		V_{CC1}	V
			LOW POWER	I_{OH} = –50 µA	V_{CC1} – 0.5		V_{CC1}	
	High output voltage XCOUT		HIGH POWER	With no load applied		2.6		V
			LOW POWER	With no load applied		2.2		
V_{OL}	Low output voltage	P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1		I_{OL} = 1 mA			0.5	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7		I_{OL} = 1 mA			0.5	
		CEC		I_{OL} = 1 mA		0	0.5	V
V_{OL}	Low output voltage XOUT		HIGH POWER	I_{OL} = 0.1 mA			0.5	V
			LOW POWER	I_{OL} = 50 µA			0.5	
	Low output voltage XCOUT		HIGH POWER	With no load applied		0		V
			LOW POWER	With no load applied		0		
V_{T+}-V_{T-}	Hysteresis	$\overline{HOLD}$, $\overline{RDY}$, TA0IN to TA4IN, TB0IN to TB5IN, $\overline{INT0}$ to $\overline{INT7}$, $\overline{NMI}$, $\overline{ADTRG}$, $\overline{CTS0}$ to $\overline{CTS2}$, $\overline{CTS5}$ to $\overline{CTS7}$, SCL0 to SCL2, SCL5 to SCL7, SDA0 to SDA2, SDA5 to SDA7, CLK0 to CLK7, TA0OUT to TA4OUT, $\overline{KI0}$ to $\overline{KI3}$, RXD0 to RXD2, RXD5 to RXD7, SIN3, SIN4, $\overline{SD}$, PMC0, PMC1, SCLMM, SDAMM, ZP, IDU, IDV, IDW			0.2		1.0	V
		CEC			0.2	0.5	1.0	V
		$\overline{RESET}$			0.2		1.8	V
I_{IH}	High input current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1 XIN, $\overline{RESET}$, CNVSS, BYTE		V_I = 3 V			4.0	µA
–	Leakage current in powered-off state		CEC	V_{CC1} = 0 V			1.8	µA
I_{IL}	Low input current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1 XIN, $\overline{RESET}$, CNVSS, BYTE		V_I = 0 V			–4.0	µA
R_{PULLUP}	Pull-up resistance	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1		V_I = 0 V	50	80	150	kΩ
R_{fXIN}	Feedback resistance XIN					3.0		MΩ
V_{RAM}	RAM retention voltage			In stop mode	1.8			V

Note:
1. When $V_{CC1} \neq V_{CC2}$, refer to 5 V or 3 V standard depending on the voltage.

$V_{CC1} = V_{CC2} = 3\ V$

Table 5.44 Electrical Characteristics (3) (2/2)

R5F3651ECNFC, R5F3651KCNFC, R5F3650KCNFA, R5F3650KCNFB, R5F3651MCNFC, R5F3650MCNFA, R5F3650MCNFB, R5F3651NCNFC, R5F3650NCNFA, R5F3650NCNFB, R5F3651ECDFC, R5F3651KCDFC, R5F3650KCDFA, R5F3650KCDFB, R5F3651MCDFC, R5F3650MCDFA, R5F3650MCDFB, R5F3651NCDFC, R5F3650NCDFA, R5F3650NCDFB

$V_{CC1} = V_{CC2} = 2.7$ to $3.3\ V$, $V_{SS} = 0\ V$ at $T_{opr} = -20°C$ to $85°C/-40°C$ to $85°C$, $f_{(BCLK)} = 32$ MHz unless otherwise specified.

Symbol	Parameter	Measuring Condition		Standard			Unit
				Min.	Typ.	Max.	
I_{CC}	Power supply current In single-chip, mode, the output pin are open and other pins are V_{SS}	Stop mode	Main clock stopped 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator stopped Peripheral clock stopped $T_{opr} = 25°C$		1.6		µA
		During flash memory program	$f_{(BCLK)} = 10$ MHz, PM17 = 1 (one wait) $V_{CC1} = 3.0\ V$		20.0		mA
		During flash memory erase	$f_{(BCLK)} = 10$ MHz, PM17 = 1 (one wait) $V_{CC1} = 3.0\ V$		30.0		mA

$V_{CC1} = V_{CC2} = 3\ V$

Timing Requirements

($V_{CC1} = V_{CC2} = 3$ V, $V_{SS} = 0$ V, at $T_{opr} = -20°C$ to 85°C/-40°C to 85°C unless otherwise specified)

Table 5.51 Timer A Input (Two-Phase Pulse Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	2		µs
$t_{su(TAIN-TAOUT)}$	TAiOUT input setup time	500		ns
$t_{su(TAOUT-TAIN)}$	TAiIN input setup time	500		ns

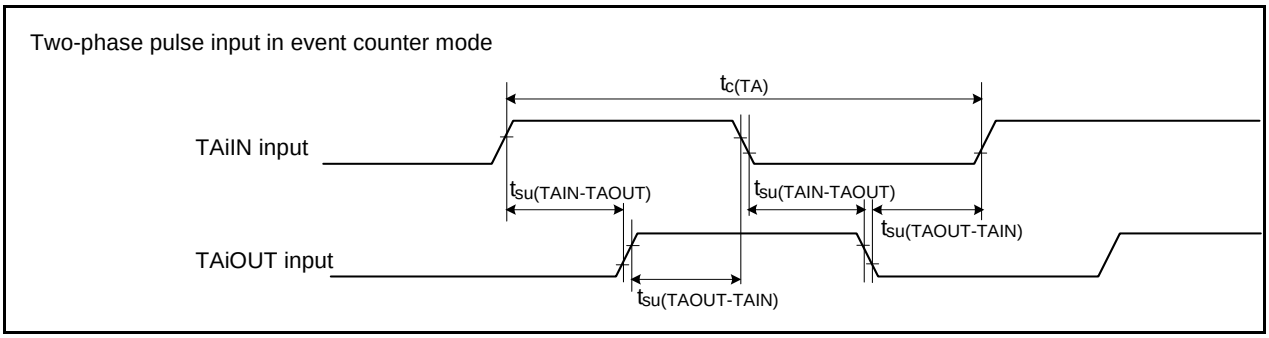
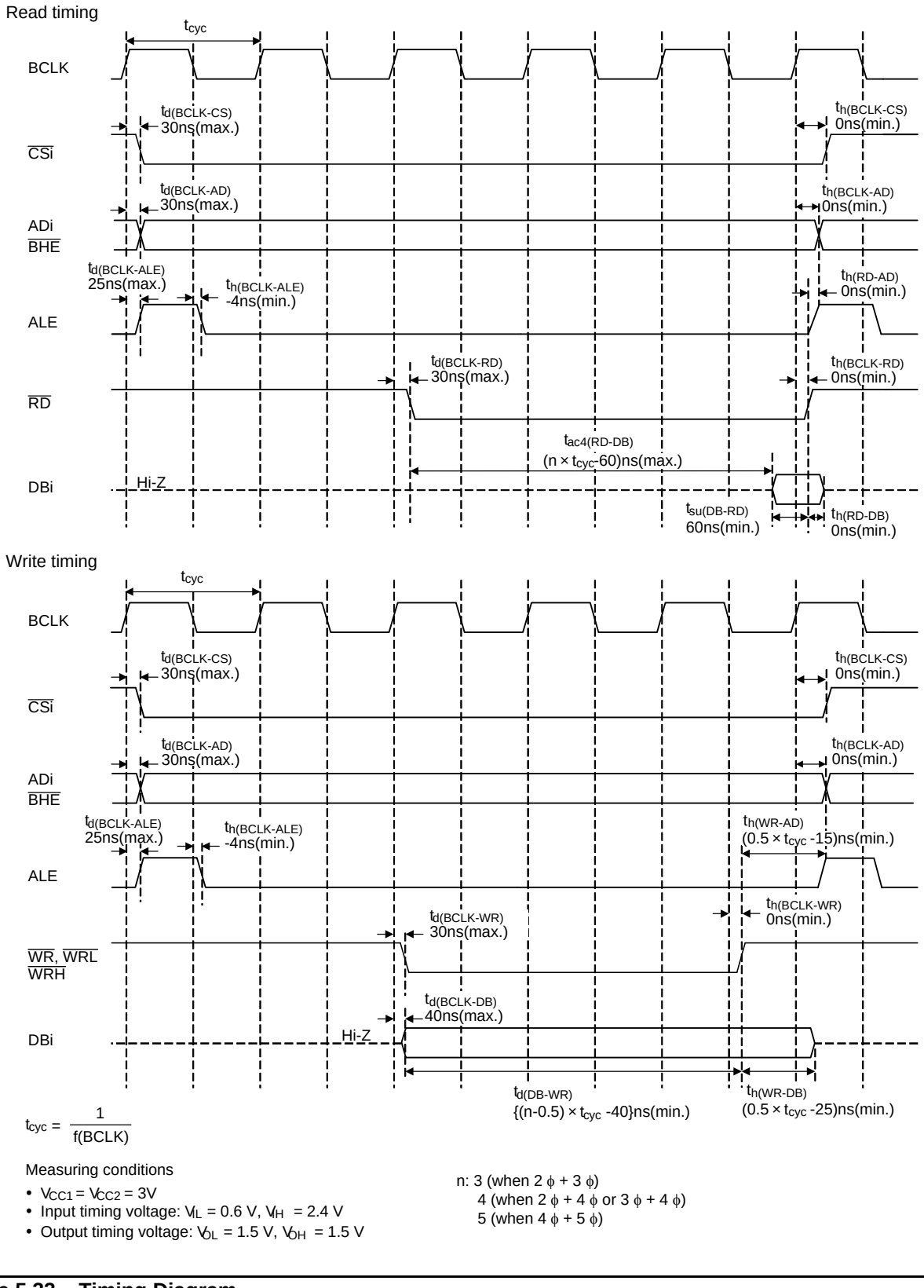


Figure 5.23 Timer A Input (Two-Phase Pulse Input in Event Counter Mode)

Memory Expansion Mode, Microprocessor Mode
(in wait state setting 2 ϕ + 3 ϕ, 2 ϕ + 4 ϕ, 3ϕ + 4 ϕ, and 4 ϕ + 5 ϕ, and when accessing external area)

$V_{CC1} = V_{CC2} = 3V$



$$t_{cyc} = \frac{1}{f(BCLK)}$$

Measuring conditions

- $V_{CC1} = V_{CC2} = 3V$
- Input timing voltage: $V_{IL} = 0.6$ V, $V_{IH} = 2.4$ V
- Output timing voltage: $V_{OL} = 1.5$ V, $V_{OH} = 1.5$ V

n: 3 (when 2 ϕ + 3 ϕ)
4 (when 2 ϕ + 4 ϕ or 3 ϕ + 4 ϕ)
5 (when 4 ϕ + 5 ϕ)

Figure 5.33 Timing Diagram

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