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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, IrDA, SD, SPI, UART/USART, USB, USB OTG
Peripherals	DMA, I ² S, LVD, POR, PWM, WDT
Number of I/O	83
Program Memory Size	1MB (1M × 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 37x16b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	121-XFBGA
Supplier Device Package	121-XFBGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk64fn1m0vdc12

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong





Symbol	Description	Min.	Max.	Unit
V _{DD}	Digital supply voltage	-0.3	3.8	V
I _{DD}	Digital supply current	—	185	mA
V _{DIO}	Digital input voltage (except RESET, EXTAL, and XTAL)	-0.3	5.5	V
V _{DRTC_WAKEU}	RTC Wakeup input voltage	-0.3	V _{BAT} + 0.3	V
Р				
V _{AIO}	Analog ¹ , RESET, EXTAL, and XTAL input voltage	-0.3	V _{DD} + 0.3	V
I _D	Maximum current single pin limit (applies to all digital pins)	-25	25	mA
V _{DDA}	Analog supply voltage	V _{DD} – 0.3	V _{DD} + 0.3	V
V _{USB0_DP}	USB0_DP input voltage	-0.3	3.63	V
V _{USB0_DM}	USB0_DM input voltage	-0.3	3.63	V
V _{REGIN}	USB regulator input	-0.3	6.0	V
V _{BAT}	RTC battery supply voltage	-0.3	3.8	V

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

2 General

2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



The midpoint is V_{IL} + (V_{IH} - V_{IL}) / 2

Figure 2. Input signal measurement reference

2.2 Nonswitching electrical specifications



Figure 4. VLPR mode supply current vs. core frequency

2.2.6 EMC radiated emissions operating behaviors Table 8. EMC radiated emissions operating behaviors

Symbol	Description	Frequency band (MHz)	Тур.	Unit	Notes
			144 LQFP		
V _{RE1}	Radiated emissions voltage, band 1	0.15–50	16	dBµV	1, 2
V _{RE2}	Radiated emissions voltage, band 2	50–150	22	dBµV	
V _{RE3}	Radiated emissions voltage, band 3	150–500	21	dBµV	
V _{RE4}	Radiated emissions voltage, band 4	500–1000	16	dBµV	
V _{RE_IEC}	IEC level	0.15–1000	L		2, 3

1. Determined according to IEC Standard 61967-1, Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions and IEC Standard 61967-2, Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions – TEM Cell and

Symbol	Description	Min.	Max.	Unit	Notes
	• 1.71 ≤ V _{DD} ≤ 2.7V	—	12	ns	
	• $2.7 \le V_{DD} \le 3.6V$				
	Port rise and fall time (high drive strength) - 5 V				4
	Slew disabled				
	• $1.71 \le V_{DD} \le 2.7V$	—	6	ns	
	• $2.7 \le V_{DD} \le 3.6V$	—	4	ns	
	Slew enabled				
	• $1.71 \le V_{DD} \le 2.7V$	—	24	ns	
	• $2.7 \le V_{DD} \le 3.6V$	—	14	ns	
	Port rise and fall time (low drive strength) - 3 V				5
	Slew disabled				
	• $1.71 \le V_{DD} \le 2.7V$	—	12	ns	
	• $2.7 \le V_{DD} \le 3.6V$	—	6	ns	
	Slew enabled				
	• $1.71 \le V_{DD} \le 2.7V$	—	24	ns	
	• $2.7 \le V_{DD} \le 3.6V$	—	16	ns	
	Port rise and fall time (low drive strength) - 5 V				5
	Slew disabled				
	• $1.71 \le V_{DD} \le 2.7V$	—	17	ns	
	• $2.7 \le V_{DD} \le 3.6V$	—	10	ns	
	Slew enabled				
	• $1.71 \le V_{DD} \le 2.7V$	—	36	ns	
	• $2.7 \le V_{DD} \le 3.6V$	—	20	ns	

Table 11. General switching specifications (continued)

- 1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop, VLPS, LLS, and VLLSx modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.
- 2. The greater synchronous and asynchronous timing must be met.
- 3. This is the minimum pulse width that is guaranteed to be recognized as a pin interrupt request in Stop, VLPS, LLS, and VLLSx modes.
- 4. 25 pF load
- 5. 15 pF load

2.4 Thermal specifications







Figure 6. Trace data specifications

3.1.2 JTAG electricals

able 15. JTA	G limited	voltage	range	electricals
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Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
J1	TCLK frequency of operation			MHz
	Boundary Scan	0	10	
	JTAG and CJTAG	0	25	
	Serial Wire Debug	0	50	
J2	TCLK cycle period	1/J1	_	ns
J3	TCLK clock pulse width			
	Boundary Scan	50	_	ns
	JTAG and CJTAG	20	_	ns
	Serial Wire Debug	10	_	ns
J4	TCLK rise and fall times	_	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	_	ns
J6	Boundary scan input data hold time after TCLK rise	2.6	_	ns
J7	TCLK low to boundary scan output data valid		25	ns
J8	TCLK low to boundary scan output high-Z		25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	_	ns
J10	TMS, TDI input data hold time after TCLK rise	1		ns

Table continues on the next page...

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
EP1	EZP_CK frequency of operation (all commands except READ)		f _{SYS} /2	MHz
EP1a	EZP_CK frequency of operation (READ command)	—	f _{SYS} /8	MHz
EP2	EZP_CS negation to next EZP_CS assertion	2 x t _{EZP_CK}	—	ns
EP3	EZP_CS input valid to EZP_CK high (setup)	5	—	ns
EP4	EZP_CK high to EZP_CS input invalid (hold)	5	—	ns
EP5	EZP_D input valid to EZP_CK high (setup)	2	—	ns
EP6	EZP_CK high to EZP_D input invalid (hold)	5	—	ns
EP7	EZP_CK low to EZP_Q output valid	—	18	ns
EP8	EZP_CK low to EZP_Q output invalid (hold)	0	—	ns
EP9	EZP_CS negation to EZP_Q tri-state	—	12	ns

3.4.2 EzPort switching specifications Table 27. EzPort switching specifications





- 1. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
- 2. DC potential difference.
- 3. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 8 Ω analog source resistance. The R_{AS}/C_{AS} time constant should be kept to < 1 ns.
- 4. To use the maximum ADC conversion clock frequency, CFG2[ADHSC] must be set and CFG1[ADLPC] must be clear.
- 5. For guidelines and examples of conversion rate calculation, download the ADC calculator tool.



Figure 15. ADC input impedance equivalency diagram

3.6.1.2 16-bit ADC electrical characteristics

Table 31.	16-bit ADC	characteristics	(V _{REFH} =	V _{DDA} ,	$V_{REFL} =$	V _{SSA})
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Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
I _{DDA_ADC}	Supply current		0.215	—	1.7	mA	3
f _{ADACK}	ADC asynchronous	• ADLPC = 1, ADHSC = 0	1.2	2.4	3.9	MHz	t _{ADACK} = 1/
	clock source	• ADLPC = 1, ADHSC = 1	2.4	4.0	6.1	MHz	f _{ADACK}
		• ADLPC = 0, ADHSC = 0	3.0	5.2	7.3	MHz	
		• ADLPC = 0, ADHSC = 1	4.4	6.2	9.5	MHz	
	Sample Time	See Reference Manual chapter	for sample	times			

Table continues on the next page...

Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
TUE	Total unadjusted	12-bit modes	_	±4	±6.8	LSB ⁴	5
	error	 <12-bit modes 	_	±1.4	±2.1		
DNL	Differential non- linearity	12-bit modes	_	±0.7	-1.1 to +1.9	LSB ⁴	5
		 <12-bit modes 	_	±0.2	–0.3 to 0.5		
INL	Integral non-linearity	12-bit modes	—	±1.0	-2.7 to +1.9	LSB ⁴	5
		 <12-bit modes 	_	±0.5	-0.7 to +0.5		
E _{FS}	Full-scale error	12-bit modes	—	-4	-5.4	LSB ⁴	$V_{ADIN} = V_{DDA}^{5}$
		 <12-bit modes 	_	-1.4	-1.8		
EQ	Quantization error	16-bit modes	—	-1 to 0	—	LSB ⁴	
		• ≤13-bit modes	_	_	±0.5		
ENOB	Effective number of	16-bit differential mode					6
	bits	• Avg = 32	12.8	14.5	_	bits	
		• Avg = 4	11.9	13.8	_	bits	
		16-bit single-ended mode					
		• Avg = 32	12.2	13.9	—	bits	
		• Avg = 4	11.4	13.1		bits	
SINAD	Signal-to-noise plus distortion	See ENOB	6.02 ×	ENOB +	1.76	dB	
THD	Total harmonic	16-bit differential mode				dB	7
	distortion	• Avg = 32	-	-94	—	٩D	
		16-bit single-ended mode • Avg = 32	_	-85	_	uв	
SFDR	Spurious free dynamic range	16-bit differential mode	82	95		dB	7
		//// U			_	dB	
		16-bit single-ended mode • Avg = 32	78	90			
E _{IL}	Input leakage error			$I_{ln} \times R_{AS}$	<u> </u>	mV	I _{In} = leakage current
							(refer to the MCU's voltage and

Table 31. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Table continues on the next page...

Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
							current operating ratings)
	Temp sensor slope	Across the full temperature range of the device	1.55	1.62	1.69	mV/°C	8
V _{TEMP25}	Temp sensor voltage	25 °C	706	716	726	mV	8

Table 31. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

1. All accuracy numbers assume the ADC is calibrated with V_{REFH} = V_{DDA}

Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 2.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

- 3. The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC_CFG1[ADLPC] (low power). For lowest power operation, ADC_CFG1[ADLPC] must be set, the ADC_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
- 4. 1 LSB = $(V_{REFH} V_{REFL})/2^N$
- 5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
- 6. Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
- 7. Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.
- 8. ADC conversion clock < 3 MHz



Typical ADC 16-bit Differential ENOB vs ADC Clock

Figure 16. Typical ENOB vs. ADC_CLK for 16-bit differential mode

- 1. Typical hysteresis is measured with input voltage range limited to 0.6 to V_{DD} -0.6 V.
- Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to CMP_DACCR[DACEN], CMP_DACCR[VRSEL], CMP_DACCR[VOSEL], CMP_MUXCR[PSEL], and CMP_MUXCR[MSEL]) and the comparator output settling to a stable level.



Figure 18. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 0)

3. 1 LSB = V_{reference}/64

3.6.3.2 12-bit DAC operating behaviors Table 34. 12-bit DAC operating behaviors

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
I _{DDA_DACL}	Supply current — low-power mode	_	_	150	μΑ	
I _{DDA_DACH}	Supply current — high-speed mode		_	700	μΑ	
t _{DACLP}	Full-scale settling time (0x080 to 0xF7F) — low-power mode		100	200	μs	1
t _{DACHP}	Full-scale settling time (0x080 to 0xF7F) — high-power mode		15	30	μs	1
t _{CCDACLP}	Code-to-code settling time (0xBF8 to 0xC08) — low-power mode and high- speed mode	—	0.7	1	μs	1
V _{dacoutl}	DAC output voltage range low — high- speed mode, no load, DAC set to 0x000	—	—	100	mV	
V _{dacouth}	DAC output voltage range high — high- speed mode, no load, DAC set to 0xFFF	V _{DACR} -100	—	V _{DACR}	mV	
INL	Integral non-linearity error — high speed mode		_	±8	LSB	2
DNL	Differential non-linearity error — V _{DACR} > 2 V		_	±1	LSB	3
DNL	Differential non-linearity error — V _{DACR} = VREF_OUT		_	±1	LSB	4
VOFFSET	Offset error	—	±0.4	±0.8	%FSR	5
E _G	Gain error	—	±0.1	±0.6	%FSR	5
PSRR	Power supply rejection ratio, $V_{DDA} \ge 2.4 \text{ V}$	60	—	90	dB	
T _{CO}	Temperature coefficient offset voltage	—	3.7	_	μV/C	6
T _{GE}	Temperature coefficient gain error	—	0.000421		%FSR/C	
A _C	Offset aging coefficient			100	μV/yr	
Rop	Output resistance (load = $3 \text{ k}\Omega$)	_	—	250	Ω	
SR	Slew rate -80h \rightarrow F7Fh \rightarrow 80h				V/µs	
	 High power (SP_{HP}) 	1.2	1.7	—		
	Low power (SP _{LP})	0.05	0.12			
СТ	Channel to channel cross talk	—	—	-80	dB	
BW	3dB bandwidth				kHz	
	• High power (SP _{HP})	550	-	_		
	Low power (SP _{LP})	40	-	—		

1. Settling within ±1 LSB

2. The INL is measured for 0 + 100 mV to V_{DACR} –100 mV 3. The DNL is measured for 0 + 100 mV to V_{DACR} –100 mV

- 4. The DNL is measured for 0 + 100 mV to V_{DACR} –100 mV with V_{DDA} > 2.4 V 5. Calculated by a best fit curve from V_{SS} + 100 mV to V_{DACR} 100 mV

Peripheral operating requirements and behaviors

V_{DDA} = 3.0 V, reference select set for V_{DDA} (DACx_CO:DACRFS = 1), high power mode (DACx_CO:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device



Figure 20. Typical INL error vs. digital code

3.8.6 DSPI switching specifications (limited voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provide DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	30	MHz	
DS1	DSPI_SCK output cycle time	2 x t _{BUS}	—	ns	
DS2	DSPI_SCK output high/low time	(t _{SCK} /2) – 2	(t _{SCK} /2) + 2	ns	
DS3	DSPI_PCSn valid to DSPI_SCK delay	(t _{BUS} x 2) – 2	_	ns	1
DS4	DSPI_SCK to DSPI_PCSn invalid delay	(t _{BUS} x 2) – 2	_	ns	2
DS5	DSPI_SCK to DSPI_SOUT valid	—	8.5	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-2	_	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	15	_	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	_	ns	

 Table 44. Master mode DSPI timing (limited voltage range)

1. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].

2. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].





Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
	Frequency of operation		15 ¹	MHz
DS9	DSPI_SCK input cycle time	4 x t _{BUS}	_	ns
DS10	DSPI_SCK input high/low time	(t _{SCK} /2) – 2	(t _{SCK} /2) + 2	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	10	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	_	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	DSPI_SS active to DSPI_SOUT driven	—	14	ns
DS16	DSPI_SS inactive to DSPI_SOUT not driven	—	14	ns

Table 45. Slave mode DSPI timing (limited voltage range)

1. The maximum operating frequency is measured with non-continuous CS and SCK. When DSPI is configured with continuous CS and SCK, there is a constraint that SPI clock should not be greater than 1/6 of bus clock, for example, when bus clock is 60MHz, SPI clock should not be greater than 10MHz



Figure 26. DSPI classic SPI timing — slave mode



Figure 34. I2S/SAI timing — slave modes

3.8.11.2 VLPR, VLPW, and VLPS mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in VLPR, VLPW, and VLPS modes.

Table 55.	I2S/SAI master mode timing	in VLPR. V	LPW. and VLPS	modes (full	voltage range)
		··· v∟· ··, v	- w, and ver o	mouce (ium	vonage range <i>j</i>

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	62.5	-	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	250	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	-	45	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	0	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid		45	ns
S8	I2S_TX_BCLK to I2S_TXD invalid		—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	45	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns



Figure 35. I2S/SAI timing — master modes

Table 56. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	250	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	30	_	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	11	_	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—		ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	30	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	11	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid ¹	—	72	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear



Figure 36. I2S/SAI timing — slave modes

4 Dimensions

4.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to nxp.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
100-pin LQFP	98ASS23308W
121-pin XFBGA	98ASA00595D
144-pin LQFP	98ASS23177W
144-pin MAPBGA	98ASA00222D

5 Pinout

Pinout

144 QFP	144 Map Bga	100 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9
28	L2	19	ADC0_ DM0/ ADC1_ DM3	ADC0_ DM0/ ADC1_ DM3										
29	M1	20	ADC1_ DP0/ ADC0_DP3	ADC1_ DP0/ ADC0_DP3										
30	M2	21	ADC1_ DM0/ ADC0_ DM3	ADC1_ DM0/ ADC0_ DM3										
31	H5	22	VDDA	VDDA										
32	G5	23	VREFH	VREFH										
33	G6	24	VREFL	VREFL										
34	H6	25	VSSA	VSSA										
35	K3	_	ADC1_ SE16/ CMP2_IN2/ ADC0_ SE22	ADC1_ SE16/ CMP2_IN2/ ADC0_ SE22										
36	J3	_	ADC0_ SE16/ CMP1_IN2/ ADC0_ SE21	ADC0_ SE16/ CMP1_IN2/ ADC0_ SE21										
37	M3	26	VREF_ OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_ SE18	VREF_ OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_ SE18										
38	L3	27	DAC0_ OUT/ CMP1_IN3/ ADC0_ SE23	DAC0_ OUT/ CMP1_IN3/ ADC0_ SE23										
39	L4	-	DAC1_ OUT/ CMP0_IN4/ CMP2_IN3/ ADC1_ SE23	DAC1_ OUT/ CMP0_IN4/ CMP2_IN3/ ADC1_ SE23										
40	M7	28	XTAL32	XTAL32										
41	M6	29	EXTAL32	EXTAL32										
42	L6	30	VBAT	VBAT										
43	_	-	VDD	VDD										
44	-	-	VSS	VSS										

	1	2	3	4	5	6	7	8	9	10	11	_
A	PTC4/ LLWU_P8	PTC7	PTC9	PTC12	PTC15	PTC17	PTD1	PTD5	PTD7	PTD9	PTD14	A
в	PTC3/ LLWU_P7	PTC6/ LLWU_P10	PTC8	PTC11/ LLWU_P11	PTC14	PTC18	PTD3	PTD6/ LLWU_P15	PTD8	PTD12	PTD15	в
С	PTC2	PTC5/ LLWU_P9	PTC10	PTC13	PTC16	PTD2/ LLWU_P13	PTD4/ LLWU_P14	PTD11	PTD13	PTE0	PTE3	с
D	PTB23	PTC0	PTC1/ LLWU_P6	PTB22	PTC19	PTD0/ LLWU_P12	PTD10	PTE1/ LLWU_P0	PTE2/ LLWU_P1	PTE4/ LLWU_P2	PTE5	D
E	PTB18	PTB19	PTB20	PTB21	VDD	VSS	PTE6	PTE7	PTE8	PTE9	PTE10	E
F	PTB16	PTB17	VDD	VSS	VSS	VDD	VDD	ADC0_DP1	PTE11	PTE12	VSS	F
G	PTB10	PTB11	PTB9	PTB8	VDD		VSS	ADC0_DM1	ADC0_DP0/ ADC1_DP3	VOUT33	USB0_DP	G
н	PTB7	PTB6	PTB5	PTB4	VSS	VSS	VDD	VDD	ADC0_DM0/ ADC1_DM3	VREGIN	USB0_DM	н
J	PTB3	PTB2	PTB1	PTB0/ LLWU_P5	PTA14	PTA11	PTA2	PTE27	RTC_ WAKEUP_B	ADC1_DP0/ ADC0_DP3	ADC1_DP1	J
к	PTA29	PTA28	PTA27	PTA26	PTA12	PTA8	PTA1	PTE25	ADC0_SE16/ CMP1_IN2/ ADC0_SE21	ADC1_DM0/ ADC0_DM3	ADC1_DM1	к
L	RESET_b	PTA24	PTA25	PTA16	PTA9	PTA5	PTA0	PTE24	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18	VREFH	VDDA	L
М	PTA19	VSS	PTA17	PTA13/ LLWU_P4	PTA7	PTA4/ LLWU_P3	PTE28	VBAT	DAC1_OUT/ CMP0_IN4/ CMP2_IN3/ ADC1_SE23	ADC1_SE16/ CMP2_IN2/ ADC0_SE22	VREFL	м
N	PTA18	VDD	PTA15	PTA10	PTA6	PTA3	PTE26	EXTAL32	XTAL32	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	VSSA	N
	1	2	3	4	5	6	7	8	9	10	11	

Figure 41. 142 CSP Pinout Diagram

6 Ordering parts

6.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to nxp.com and perform a part number search for the following device numbers: MK64

7 Part identification

7.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

7.2 Format

Part numbers for this device have the following format:

Q K## A M FFF R T PP CC N

7.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	 M = Fully qualified, general market flow P = Prequalification
K##	Kinetis family	K64 = Ethernet with high RAM density
A	Key attribute	 D = Cortex-M4 w/ DSP F = Cortex-M4 w/ DSP and FPU
М	Flash memory type	 N = Program flash only X = Program flash and FlexMemory
FFF	Program flash memory size	 32 = 32 KB 64 = 64 KB 128 = 128 KB 256 = 256 KB 512 = 512 KB 1M0 = 1 MB 2M0 = 2 MB

Table continues on the next page ...