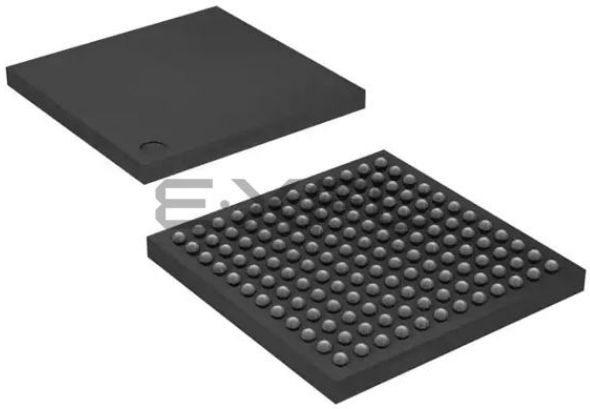

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Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, SD, SPI, UART/USART, USB, USB OTG
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	100
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 41x16b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LBGA
Supplier Device Package	144-MAPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk64fx512vmd12

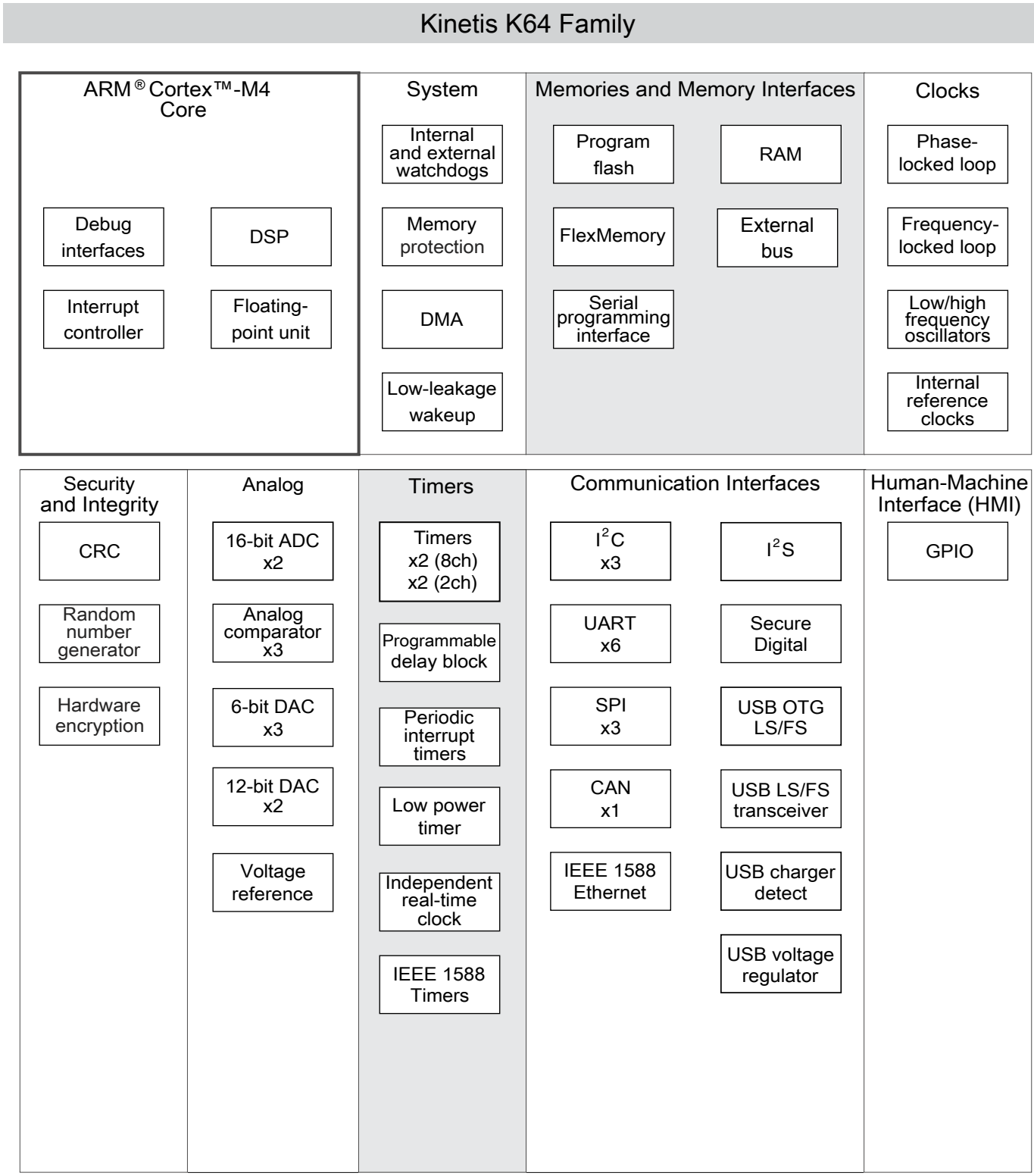

Figure 1. K64 block diagram

2.2.1 Voltage and current operating requirements

Table 1. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	3.6	V	
V_{DDA}	Analog supply voltage	1.71	3.6	V	
$V_{DD} – V_{DDA}$	V_{DD}-to-V_{DDA} differential voltage	–0.1	0.1	V	
$V_{SS} – V_{SSA}$	V_{SS}-to-V_{SSA} differential voltage	–0.1	0.1	V	
V_{BAT}	RTC battery supply voltage	1.71	3.6	V	
V_{IH}	Input high voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V	 0.7 × V_{DD} 0.75 × V_{DD}	 — —	 V V	
V_{IL}	Input low voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V	 — —	 0.35 × V_{DD} 0.3 × V_{DD}	 V V	
V_{HYS}	Input hysteresis	0.06 × V_{DD}	—	V	
I_{ICDIO}	Digital pin negative DC injection current — single pin • V_{IN} < V_{SS}-0.3V	-5	—	mA	1
I_{ICAIO}	Analog[2], EXTAL, and XTAL pin DC injection current — single pin • V_{IN} < V_{SS}-0.3V (Negative current injection) • V_{IN} > V_{DD}+0.3V (Positive current injection)	 -5 —	 — +5	mA	3
I_{ICcont}	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins • Negative current injection • Positive current injection	 -25 —	 — +25	mA	
V_{ODPU}	Open drain pullup voltage level	V_{DD}	V_{DD}	V	4
V_{RAM}	V_{DD} voltage required to retain RAM	1.2	—	V	
V_{RFVBAT}	V_{BAT} voltage required to retain the VBAT register file	V_{POR_VBAT}	—	V	

1. All 5 V tolerant digital I/O pins are internally clamped to V_{SS} through an ESD protection diode. There is no diode connection to V_{DD}. If V_{IN} is less than V_{DIO_MIN}, a current limiting resistor is required. If V_{IN} greater than V_{DIO_MIN} (=VSS-0.3V) is observed, then there is no need to provide current limiting resistors at the pads. The negative DC injection current limiting resistor is calculated as $R=(V_{DIO\_MIN}-V_{IN})/|I_{ICDIO}|$.
2. Analog pins are defined as pins that do not have an associated general purpose I/O port function. Additionally, EXTAL and XTAL are analog pins.
3. All analog pins are internally clamped to V_{SS} and V_{DD} through ESD protection diodes. If V_{IN} is less than V_{AIO_MIN} or greater than V_{AIO_MAX}, a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R=(V_{AIO\_MIN}-V_{IN})/|I_{ICAIO}|$. The positive injection current limiting resistor is calculated as $R=(V_{IN}-V_{AIO\_MAX})/|I_{ICAIO}|$. Select the larger of these two calculated resistances if the pin is exposed to positive and negative injection currents.
4. Open drain outputs must be pulled to VDD.

2.2.2 LVD and POR operating requirements

Table 2. V_{DD} supply LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Falling VDD POR detect voltage	0.8	1.1	1.5	V	
V_{LVDH}	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	
	Low-voltage warning thresholds — high range					1
V_{LVW1H}	• Level 1 falling (LVWV=00)	2.62	2.70	2.78	V	
V_{LVW2H}	• Level 2 falling (LVWV=01)	2.72	2.80	2.88	V	
V_{LVW3H}	• Level 3 falling (LVWV=10)	2.82	2.90	2.98	V	
V_{LVW4H}	• Level 4 falling (LVWV=11)	2.92	3.00	3.08	V	
V_{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	80	—	mV	
V_{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
	Low-voltage warning thresholds — low range					1
V_{LVW1L}	• Level 1 falling (LVWV=00)	1.74	1.80	1.86	V	
V_{LVW2L}	• Level 2 falling (LVWV=01)	1.84	1.90	1.96	V	
V_{LVW3L}	• Level 3 falling (LVWV=10)	1.94	2.00	2.06	V	
V_{LVW4L}	• Level 4 falling (LVWV=11)	2.04	2.10	2.16	V	
V_{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	60	—	mV	
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	
t_{LPO}	Internal low power oscillator period — factory trimmed	900	1000	1100	µs	

1. Rising threshold is the sum of falling threshold and hysteresis voltage

Table 3. VBAT power operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR_VBAT}	Falling VBAT supply POR detect voltage	0.8	1.1	1.5	V	

2.2.3 Voltage and current operating behaviors

Table 4. Voltage and current operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{OH}	Output high voltage — high drive strength				

Table continues on the next page...

2.4.1 Thermal operating requirements

Table 12. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
T_J	Die junction temperature	–40	125	°C
T_A	Ambient temperature[1]	–40	105	°C

1. Maximum T_A can be exceeded only if the user ensures that T_J does not exceed maximum T_J. The simplest method to determine T_J is:

   $T_J = T_A + R_{\theta JA}$ x chip power dissipation

2.4.2 Thermal attributes

Table 13. Thermal attributes

Board type	Symbol	Description	144 LQFP	144 MAPBGA	121 XFBGA	100 LQFP	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	51	38.1	33.3	51	°C/W	1
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	43	21.6	21.1	39	°C/W	1
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	42	30.8	26.2	41	°C/W	1
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	36	18	17.8	32	°C/W	1
—	$R_{\theta JB}$	Thermal resistance, junction to board	30	16.5	16.3	24	°C/W	2
—	$R_{\theta JC}$	Thermal resistance,	11	8.9	12	11	°C/W	3

Table continues on the next page...

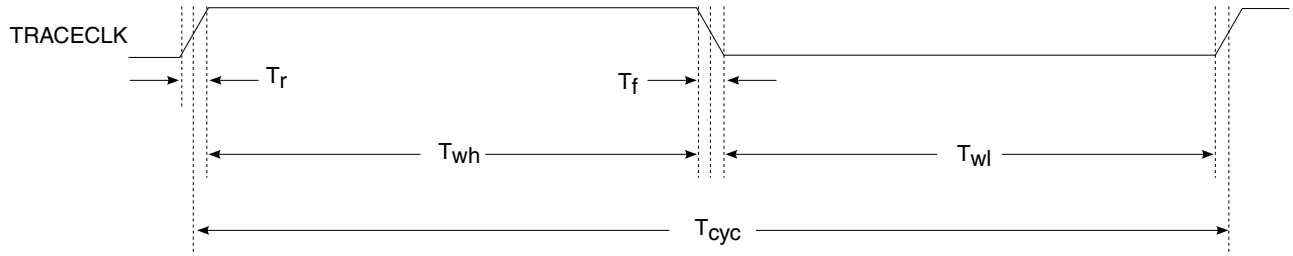

Figure 5. TRACE_CLKOUT specifications

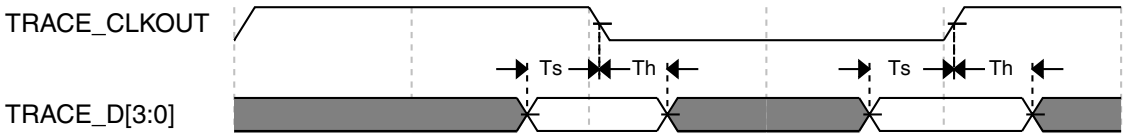

Figure 6. Trace data specifications

3.1.2 JTAG electricals

Table 15. JTAG limited voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
J1	TCLK frequency of operation			MHz
	• Boundary Scan	0	10	
	• JTAG and CJTAG	0	25	
	• Serial Wire Debug	0	50	
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width			
	• Boundary Scan	50	—	ns
	• JTAG and CJTAG	20	—	ns
	• Serial Wire Debug	10	—	ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	2.6	—	ns
J7	TCLK low to boundary scan output data valid	—	25	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1	—	ns

Table continues on the next page...

Table 15. JTAG limited voltage range electricals (continued)

Symbol	Description	Min.	Max.	Unit
J11	TCLK low to TDO data valid	—	17	ns
J12	TCLK low to TDO high-Z	—	17	ns
J13	$\overline{\text{TRST}}$ assert time	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	8	—	ns

Table 16. JTAG full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	TCLK frequency of operation			MHz
	• Boundary Scan	0	10	
	• JTAG and CJTAG	0	20	
	• Serial Wire Debug	0	40	
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width			
	• Boundary Scan	50	—	ns
	• JTAG and CJTAG	25	—	ns
	• Serial Wire Debug	12.5	—	ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	0	—	ns
J7	TCLK low to boundary scan output data valid	—	25	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	2.9	—	ns
J11	TCLK low to TDO data valid	—	22.1	ns
J12	TCLK low to TDO high-Z	—	22.1	ns
J13	$\overline{\text{TRST}}$ assert time	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	8	—	ns

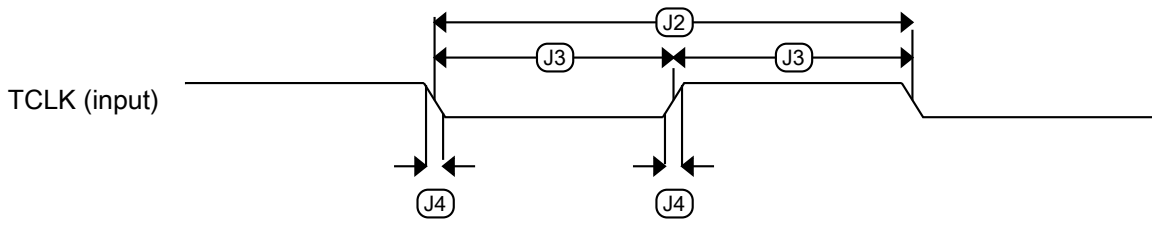

Figure 7. Test clock input timing

Table 17. MCG specifications (continued)

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
f_{loc_low}	Loss of external clock minimum frequency — RANGE = 00		(3/5) x f_{ints_t}	—	—	kHz	
f_{loc_high}	Loss of external clock minimum frequency — RANGE = 01, 10, or 11		(16/5) x f_{ints_t}	—	—	kHz	
FLL							
f_{fll_ref}	FLL reference frequency range		31.25	—	39.0625	kHz	
f_{dco}	DCO output frequency range	Low range (DRS=00) 640 × f_{fll_ref}	20	20.97	25	MHz	3, 4
		Mid range (DRS=01) 1280 × f_{fll_ref}	40	41.94	50	MHz	
		Mid-high range (DRS=10) 1920 × f_{fll_ref}	60	62.91	75	MHz	
		High range (DRS=11) 2560 × f_{fll_ref}	80	83.89	100	MHz	
$f_{dco\_t\_DMX32}$	DCO output frequency	Low range (DRS=00) 732 × f_{fll_ref}	—	23.99	—	MHz	5, 6
		Mid range (DRS=01) 1464 × f_{fll_ref}	—	47.97	—	MHz	
		Mid-high range (DRS=10) 2197 × f_{fll_ref}	—	71.99	—	MHz	
		High range (DRS=11) 2929 × f_{fll_ref}	—	95.98	—	MHz	
J_{cyc_fll}	FLL period jitter • f_{DCO} = 48 MHz • f_{DCO} = 98 MHz		— —	180 150	— —	ps	
$t_{fll\_acquire}$	FLL target frequency acquisition time		—	—	1	ms	7
PLL							
f_{vco}	VCO operating frequency		48.0	—	120	MHz	
I_{pll}	PLL operating current • PLL @ 96 MHz ($f_{osc\_hi\_1}$ = 8 MHz, f_{pll_ref} = 2 MHz, VDIV multiplier = 48)		—	1060	—	µA	8
I_{pll}	PLL operating current • PLL @ 48 MHz ($f_{osc\_hi\_1}$ = 8 MHz, f_{pll_ref} = 2 MHz, VDIV multiplier = 24)		—	600	—	µA	8
f_{pll_ref}	PLL reference frequency range		2.0	—	4.0	MHz	
J_{cyc_pll}	PLL period jitter (RMS) • f_{vco} = 48 MHz • f_{vco} = 120 MHz		— —	120 80	— —	ps ps	9
J_{acc_pll}	PLL accumulated jitter over 1µs (RMS)						9

Table continues on the next page...

1. Maximum time based on expectations at cycling end-of-life.

3.4.1.2 Flash timing specifications — commands

Table 24. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	Read 1s Block execution time					
$t_{rd1blk128k}$	• 128 KB data flash	—	—	0.5	ms	
$t_{rd1blk512k}$	• 512 KB program flash	—	—	1.8	ms	
$t_{rd1sec4k}$	Read 1s Section execution time (4 KB flash)	—	—	100	µs	1
t_{pgmchk}	Program Check execution time	—	—	95	µs	1
t_{rdrsrc}	Read Resource execution time	—	—	40	µs	1
t_{pgm8}	Program Phrase execution time	—	90	150	µs	
	Erase Flash Block execution time					2
$t_{ersblk128k}$	• 128 KB data flash	—	110	925	ms	
$t_{ersblk512k}$	• 512 KB program flash	—	435	3700	ms	
t_{ersscr}	Erase Flash Sector execution time	—	15	115	ms	2
$t_{pgmsec1k}$	Program Section execution time (1KB flash)	—	5	—	ms	
	Read 1s All Blocks execution time					
$t_{rd1allx}$	• FlexNVM devices	—	—	2.2	ms	
$t_{rd1alln}$	• Program flash only devices	—	—	3.4	ms	
t_{rdonce}	Read Once execution time	—	—	30	µs	1
$t_{pgmonce}$	Program Once execution time	—	70	—	µs	
t_{ersall}	Erase All Blocks execution time	—	870	7400	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	µs	1
	Swap Control execution time					
$t_{swapx01}$	• control code 0x01	—	200	—	µs	
$t_{swapx02}$	• control code 0x02	—	70	150	µs	
$t_{swapx04}$	• control code 0x04	—	70	150	µs	
$t_{swapx08}$	• control code 0x08	—	—	30	µs	
	Program Partition for EEPROM execution time					
$t_{pgmpart32k}$	• 32 KB FlexNVM	—	70	—	ms	
$t_{pgmpart128k}$	• 128 KB FlexNVM	—	75	—	ms	
	Set FlexRAM Function execution time:					
$t_{setramff}$	• Control Code 0xFF	—	70	—	µs	
$t_{setram32k}$	• 32 KB EEPROM backup	—	0.8	1.2	ms	
$t_{setram64k}$	• 64 KB EEPROM backup	—	1.3	1.9	ms	
$t_{setram128k}$	• 128 KB EEPROM backup	—	2.4	3.1	ms	

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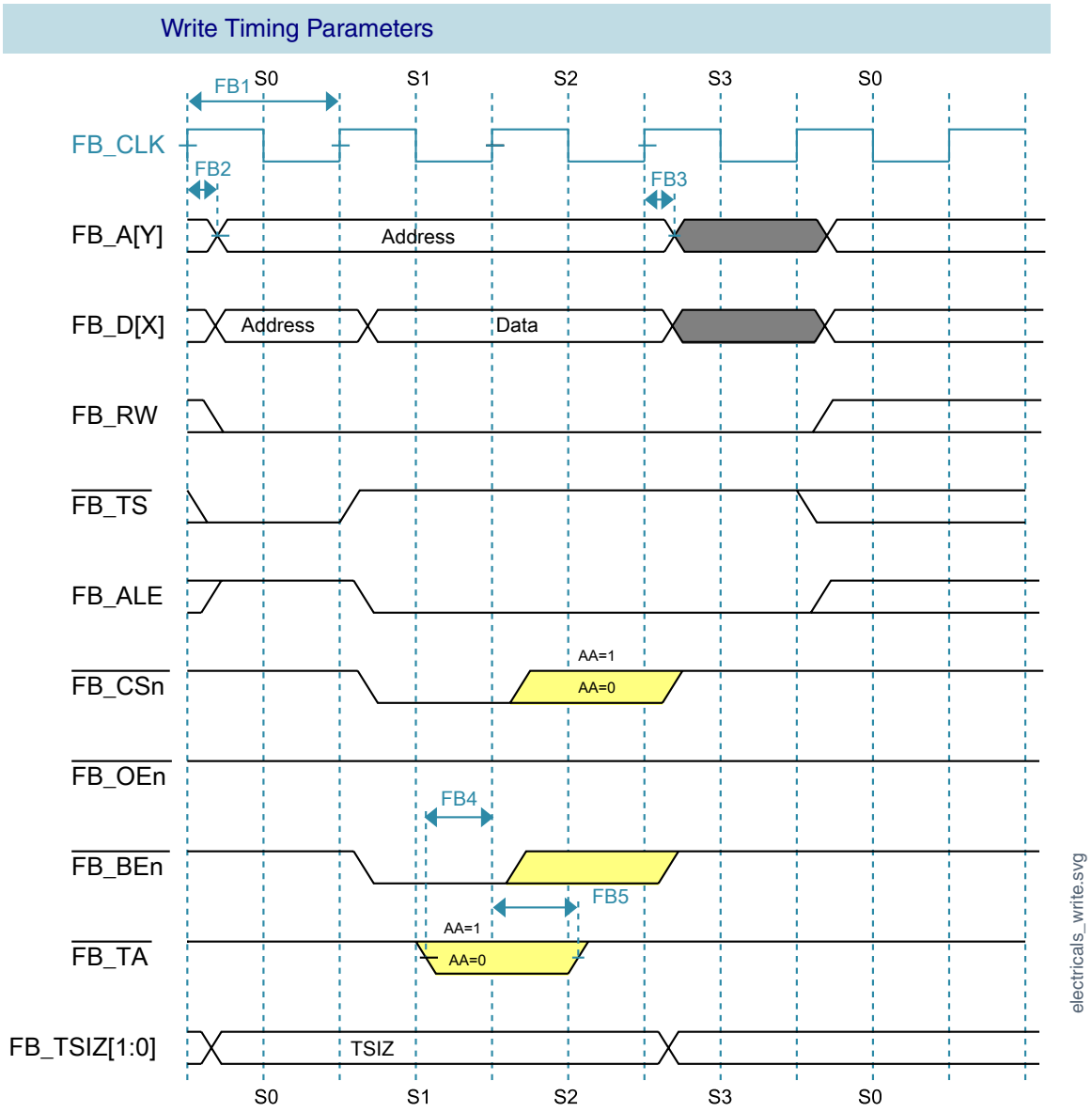

Figure 14. FlexBus write timing diagram

3.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

3.6 Analog

3.6.1 ADC electrical specifications

The 16-bit accuracy specifications listed in Table 30 and Table 31 are achievable on the differential pins ADCx_DP0, ADCx_DM0.

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications.

3.6.1.1 16-bit ADC operating conditions

Table 30. 16-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
V_{DDA}	Supply voltage	Absolute	1.71	—	3.6	V	
ΔV_{DDA}	Supply voltage	Delta to V_{DD} ($V_{DD} - V_{DDA}$)	-100	0	+100	mV	2
ΔV_{SSA}	Ground voltage	Delta to V_{SS} ($V_{SS} - V_{SSA}$)	-100	0	+100	mV	2
V_{REFH}	ADC reference voltage high		1.13	V_{DDA}	V_{DDA}	V	
V_{REFL}	ADC reference voltage low		V_{SSA}	V_{SSA}	V_{SSA}	V	
V_{ADIN}	Input voltage		V_{REFL}	—	V_{REFH}	V	
C_{ADIN}	Input capacitance	• 16-bit mode • 8-bit / 10-bit / 12-bit modes	— —	8 4	10 5	pF	
R_{ADIN}	Input series resistance		—	2	5	kΩ	
R_{AS}	Analog source resistance (external)	13-bit / 12-bit modes f_{ADCK} < 4 MHz	—	—	5	kΩ	3
f_{ADCK}	ADC conversion clock frequency	≤ 13-bit mode	1.0	—	18.0	MHz	4
f_{ADCK}	ADC conversion clock frequency	16-bit mode	2.0	—	12.0	MHz	4
C_{rate}	ADC conversion rate	≤ 13-bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	20.000	—	818.330	ksps	5
C_{rate}	ADC conversion rate	16-bit mode No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	37.037	—	461.467	ksps	5

Table 31. 16-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.	Unit	Notes
							current operating ratings)
	Temp sensor slope	Across the full temperature range of the device	1.55	1.62	1.69	mV/°C	8
V_{TEMP25}	Temp sensor voltage	25 °C	706	716	726	mV	8

1. All accuracy numbers assume the ADC is calibrated with V_{REFH} = V_{DDA}
2. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 2.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
3. The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC_CFG1[ADLPC] (low power). For lowest power operation, ADC_CFG1[ADLPC] must be set, the ADC_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
4. 1 LSB = (V_{REFH} - V_{REFL})/2^N
5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
6. Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
7. Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.
8. ADC conversion clock < 3 MHz

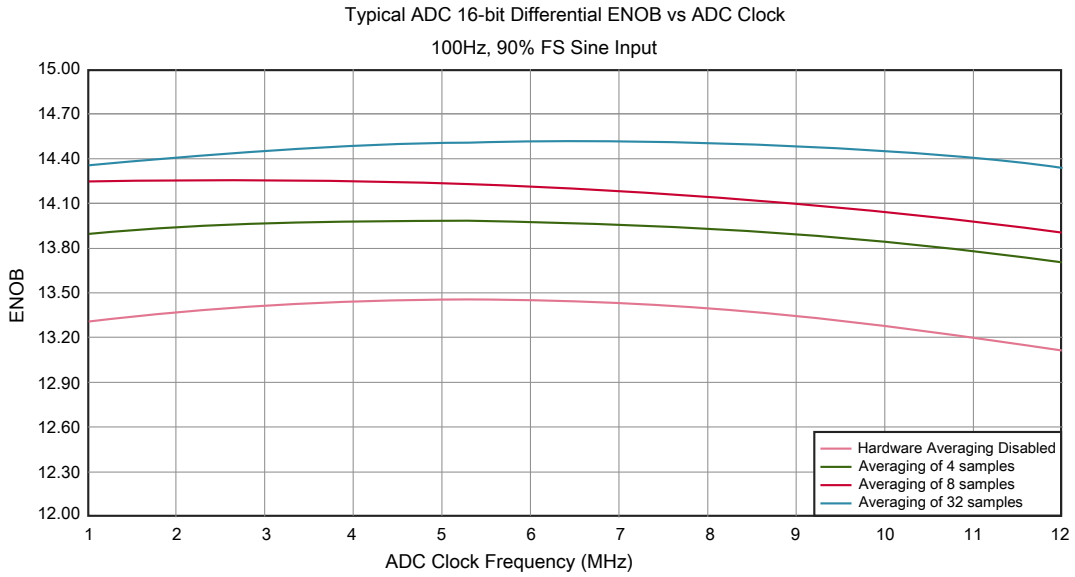

Figure 16. Typical ENOB vs. ADC_CLK for 16-bit differential mode

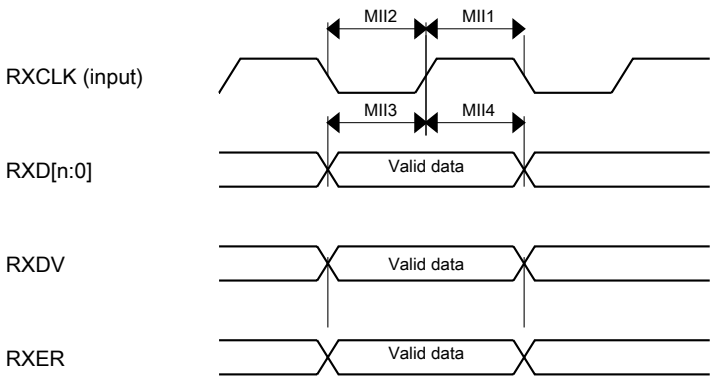

Figure 23. RMII/MII receive signal timing diagram

3.8.1.2 RMII signal switching specifications

The following timing specs meet the requirements for RMII style interfaces for a range of transceiver devices.

Table 40. RMII signal switching specifications

Num	Description	Min.	Max.	Unit
—	EXTAL frequency (RMII input clock RMII_CLK)	—	50	MHz
RMII1	RMII_CLK pulse width high	35%	65%	RMII_CLK period
RMII2	RMII_CLK pulse width low	35%	65%	RMII_CLK period
RMII3	RXD[1:0], CRS_DV, RXER to RMII_CLK setup	4	—	ns
RMII4	RMII_CLK to RXD[1:0], CRS_DV, RXER hold	2	—	ns
RMII7	RMII_CLK to TXD[1:0], TXEN invalid	4	—	ns
RMII8	RMII_CLK to TXD[1:0], TXEN valid	—	15	ns

3.8.1.3 MDIO serial management timing specifications

Table 41. MDIO serial management channel signal timing

Num	Characteristic	Symbol	Min	Max	Unit
E10	MDC cycle time	t_{MDC}	400	—	ns
E11	MDC pulse width		40	60	% t_{MDC}
E12	MDC to MDIO output valid		—	375	ns
E13	MDC to MDIO output invalid		25	—	ns
E14	MDIO input to MDC setup		10	—	ns
E15	MDIO input to MDC hold		0	—	ns

144 QFP	144 MAP BGA	100 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9
4	E4	4	ADC0_ DM2/ ADC1_ SE7a	ADC0_ DM2/ ADC1_ SE7a	PTE3	SPI1_SIN	UART1_ RTS_b	SDHC0_ CMD	TRACE_ D1		SPI1_ SOUT			
5	E5	—	VDD	VDD										
6	F6	—	VSS	VSS										
7	E3	5	DISABLED		PTE4/ LLWU_P2	SPI1_ PCS0	UART3_TX	SDHC0_ D3	TRACE_ D0				LLWU_P2	
8	E2	6	DISABLED		PTE5	SPI1_ PCS2	UART3_ RX	SDHC0_ D2		FTM3_CH0				
9	E1	7	DISABLED		PTE6/ x_LLWU_ P16	SPI1_ PCS3	UART3_ CTS_b	I2S0_ MCLK		FTM3_CH1	USB_ SOF_OUT		x_LLWU_ P16	
10	F4	—	DISABLED		PTE7		UART3_ RTS_b	I2S0_ RXD0		FTM3_CH2				
11	F3	—	DISABLED		PTE8	I2S0_ RXD1	UART5_TX	I2S0_RX_ FS		FTM3_CH3				
12	F2	—	DISABLED		PTE9/ x_LLWU_ P17	I2S0_TXD1	UART5_ RX	I2S0_RX_ BCLK		FTM3_CH4			x_LLWU_ P17	
13	F1	—	DISABLED		PTE10/ x_LLWU_ P18		UART5_ CTS_b	I2S0_TXD0		FTM3_CH5			x_LLWU_ P18	
14	G4	—	DISABLED		PTE11		UART5_ RTS_b	I2S0_TX_ FS		FTM3_CH6				
15	G3	—	DISABLED		PTE12			I2S0_TX_ BCLK		FTM3_CH7				
16	E6	8	VDD	VDD										
17	F7	9	VSS	VSS										
18	H3	—	VSS	VSS										
19	H1	10	USB0_DP	USB0_DP										
20	H2	11	USB0_DM	USB0_DM										
21	G1	12	VOUT33	VOUT33										
22	G2	13	VREGIN	VREGIN										
23	J1	14	ADC0_DP1	ADC0_DP1										
24	J2	15	ADC0_ DM1	ADC0_ DM1										
25	K1	16	ADC1_DP1	ADC1_DP1										
26	K2	17	ADC1_ DM1	ADC1_ DM1										
27	L1	18	ADC0_ DP0/ ADC1_DP3	ADC0_ DP0/ ADC1_DP3										

144 QFP	144 MAP BGA	100 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9
							UART0_ COL_b							
85	G10	—	ADC1_ SE10	ADC1_ SE10	PTB4			ENET0_ 1588_ TMR2		FTM1_ FLT0				
86	G9	—	ADC1_ SE11	ADC1_ SE11	PTB5			ENET0_ 1588_ TMR3		FTM2_ FLT0				
87	F12	—	ADC1_ SE12	ADC1_ SE12	PTB6				FB_AD23					
88	F11	—	ADC1_ SE13	ADC1_ SE13	PTB7				FB_AD22					
89	F10	—	DISABLED		PTB8		UART3_ RTS_b		FB_AD21					
90	F9	57	DISABLED		PTB9	SPI1_ PCS1	UART3_ CTS_b		FB_AD20					
91	E12	58	ADC1_ SE14	ADC1_ SE14	PTB10	SPI1_ PCS0	UART3_ RX		FB_AD19	FTM0_ FLT1				
92	E11	59	ADC1_ SE15	ADC1_ SE15	PTB11	SPI1_SCK	UART3_TX		FB_AD18	FTM0_ FLT2				
93	H7	60	VSS	VSS										
94	F5	61	VDD	VDD										
95	E10	62	DISABLED		PTB16	SPI1_ SOUT	UART0_ RX	FTM_ CLKIN0	FB_AD17	EWM_IN				
96	E9	63	DISABLED		PTB17	SPI1_SIN	UART0_TX	FTM_ CLKIN1	FB_AD16	EWM_ OUT_b				
97	D12	64	DISABLED		PTB18	CAN0_TX	FTM2_CH0	I2S0_TX_ BCLK	FB_AD15	FTM2_ QD_PHA				
98	D11	65	DISABLED		PTB19	CAN0_RX	FTM2_CH1	I2S0_TX_ FS	FB_OE_b	FTM2_ QD_PHB				
99	D10	66	DISABLED		PTB20	SPI2_ PCS0			FB_AD31	CMP0_ OUT				
100	D9	67	DISABLED		PTB21	SPI2_SCK			FB_AD30	CMP1_ OUT				
101	C12	68	DISABLED		PTB22	SPI2_ SOUT			FB_AD29	CMP2_ OUT				
102	C11	69	DISABLED		PTB23	SPI2_SIN	SPI0_ PCS5		FB_AD28					
103	B12	70	ADC0_ SE14	ADC0_ SE14	PTC0	SPI0_ PCS4	PDB0_ EXTRG	USB_ SOF_OUT	FB_AD14	I2S0_TXD1				
104	B11	71	ADC0_ SE15	ADC0_ SE15	PTC1/ LLWU_P6	SPI0_ PCS3	UART1_ RTS_b	FTM0_CH0	FB_AD13	I2S0_TXD0			LLWU_P6	
105	A12	72	ADC0_ SE4b/ CMP1_IN0	ADC0_ SE4b/ CMP1_IN0	PTC2	SPI0_ PCS2	UART1_ CTS_b	FTM0_CH1	FB_AD12	I2S0_TX_ FS				

5.3 K64 Pinouts

The below figure shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous section.

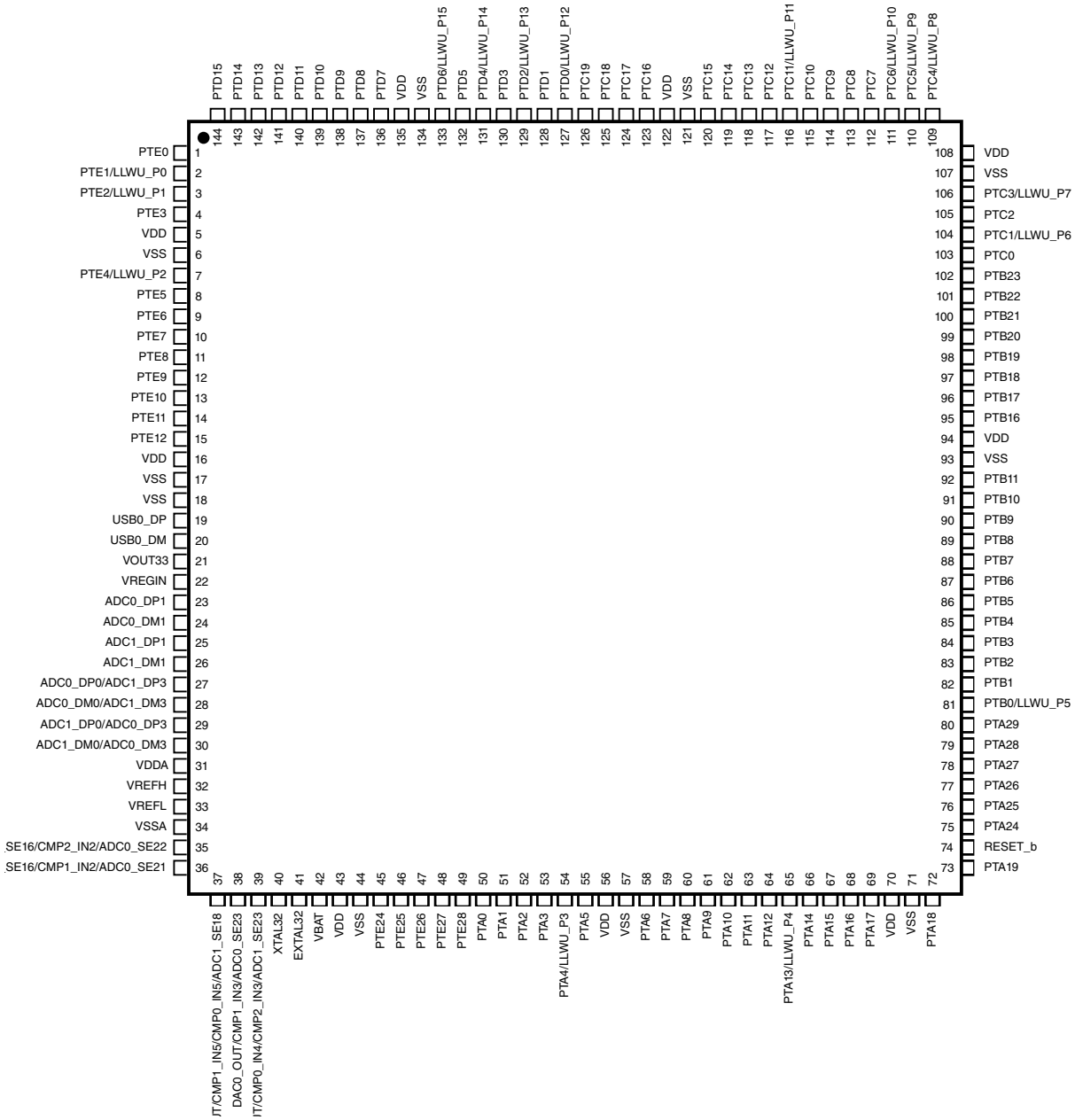

Figure 37. 144 LQFP Pinout Diagram

	1	2	3	4	5	6	7	8	9	10	11	12	
A	PTD7	PTD6/ LLWU_P15	PTD5	PTD4/ LLWU_P14	PTD0/ LLWU_P12	PTC16	PTC12	PTC8	PTC4/ LLWU_P8	NC	PTC3/ LLWU_P7	PTC2	A
B	PTD12	PTD11	PTD10	PTD3	PTC19	PTC15	PTC11/ LLWU_P11	PTC7	PTD9	NC	PTC1/ LLWU_P6	PTC0	B
C	PTD15	PTD14	PTD13	PTD2/ LLWU_P13	PTC18	PTC14	PTC10	PTC6/ LLWU_P10	PTD8	NC	PTB23	PTB22	C
D	PTE2/ LLWU_P1	PTE1/ LLWU_P0	PTE0	PTD1	PTC17	PTC13	PTC9	PTC5/ LLWU_P9	PTB21	PTB20	PTB19	PTB18	D
E	PTE6	PTE5	PTE4/ LLWU_P2	PTE3	VDD	VDD	VDD	VDD	PTB17	PTB16	PTB11	PTB10	E
F	PTE10	PTE9	PTE8	PTE7	VDD	VSS	VSS	VDD	PTB9	PTB8	PTB7	PTB6	F
G	VOUT33	VREGIN	PTE12	PTE11	VREFH	VREFL	VSS	VSS	PTB5	PTB4	PTB3	PTB2	G
H	USB0_DP	USB0_DM	VSS	PTE28	VDDA	VSSA	VSS	VSS	PTB1	PTB0/ LLWU_P5	PTA29	PTA28	H
J	ADC0_DP1	ADC0_DM1	ADC0_SE16/ CMP1_IN2/ ADC0_SE21	PTE27	PTA0	PTA1	PTA6	PTA7	PTA13/ LLWU_P4	PTA27	PTA26	PTA25	J
K	ADC1_DP1	ADC1_DM1	ADC1_SE16/ CMP2_IN2/ ADC0_SE22	PTE26	PTE25	PTA2	PTA3	PTA8	PTA12	PTA16	PTA17	PTA24	K
L	ADC0_DP0/ ADC1_DP3	ADC0_DM0/ ADC1_DM3	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	DAC1_OUT/ CMP0_IN4/ CMP2_IN3/ ADC1_SE23	RTC_ WAKEUP_B	VBAT	PTA4/ LLWU_P3	PTA9	PTA11	PTA14	PTA15	RESET_b	L
M	ADC1_DP0/ ADC0_DP3	ADC1_DM0/ ADC0_DM3	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18	PTE24	NC	EXTAL32	XTAL32	PTA5	PTA10	VSS	PTA19	PTA18	M
	1	2	3	4	5	6	7	8	9	10	11	12	

Figure 38. 144 MAPBGA Pinout Diagram

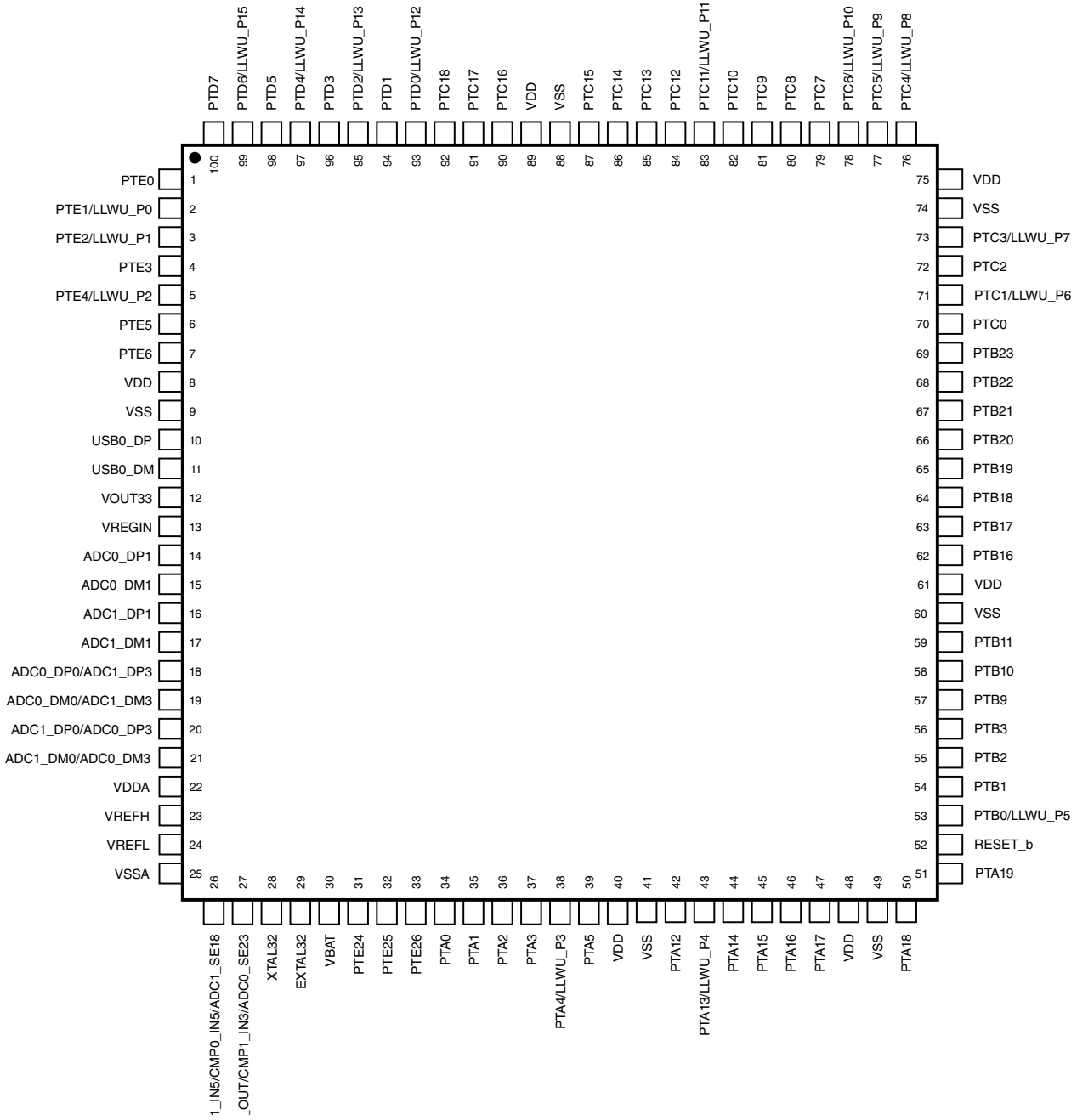

Figure 40. 100 LQFP Pinout Diagram

	1	2	3	4	5	6	7	8	9	10	11	
A	PTC4/ LLWU_P8	PTC7	PTC9	PTC12	PTC15	PTC17	PTD1	PTD5	PTD7	PTD9	PTD14	A
B	PTC3/ LLWU_P7	PTC6/ LLWU_P10	PTC8	PTC11/ LLWU_P11	PTC14	PTC18	PTD3	PTD6/ LLWU_P15	PTD8	PTD12	PTD15	B
C	PTC2	PTC5/ LLWU_P9	PTC10	PTC13	PTC16	PTD2/ LLWU_P13	PTD4/ LLWU_P14	PTD11	PTD13	PTE0	PTE3	C
D	PTB23	PTC0	PTC1/ LLWU_P6	PTB22	PTC19	PTD0/ LLWU_P12	PTD10	PTE1/ LLWU_P0	PTE2/ LLWU_P1	PTE4/ LLWU_P2	PTE5	D
E	PTB18	PTB19	PTB20	PTB21	VDD	VSS	PTE6	PTE7	PTE8	PTE9	PTE10	E
F	PTB16	PTB17	VDD	VSS	VSS	VDD	VDD	ADC0_DP1	PTE11	PTE12	VSS	F
G	PTB10	PTB11	PTB9	PTB8	VDD		VSS	ADC0_DM1	ADC0_DP0/ ADC1_DP3	VOUT33	USB0_DP	G
H	PTB7	PTB6	PTB5	PTB4	VSS	VSS	VDD	VDD	ADC0_DM0/ ADC1_DM3	VREGIN	USB0_DM	H
J	PTB3	PTB2	PTB1	PTB0/ LLWU_P5	PTA14	PTA11	PTA2	PTE27	RTC_ WAKEUP_B	ADC1_DP0/ ADC0_DP3	ADC1_DP1	J
K	PTA29	PTA28	PTA27	PTA26	PTA12	PTA8	PTA1	PTE25	ADC0_SE16/ CMP1_IN2/ ADC0_SE21	ADC1_DM0/ ADC0_DM3	ADC1_DM1	K
L	RESET_b	PTA24	PTA25	PTA16	PTA9	PTA5	PTA0	PTE24	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18	VREFH	VDDA	L
M	PTA19	VSS	PTA17	PTA13/ LLWU_P4	PTA7	PTA4/ LLWU_P3	PTE28	VBAT	DAC1_OUT/ CMP0_IN4/ CMP2_IN3/ ADC1_SE23	ADC1_SE16/ CMP2_IN2/ ADC0_SE22	VREFL	M
N	PTA18	VDD	PTA15	PTA10	PTA6	PTA3	PTE26	EXTAL32	XTAL32	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	VSSA	N
	1	2	3	4	5	6	7	8	9	10	11	

Figure 41. 142 CSP Pinout Diagram

6 Ordering parts

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