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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Sigma
Interface	I²C, SPI
Clock Rate	50MHz
Non-Volatile Memory	-
On-Chip RAM	12kB
Voltage - I/O	3.30V
Voltage - Core	1.80V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adau1701jstz-rl

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Last Content Update: 02/23/2017

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- ADUSB2EBZ Evaluation Board

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- AN-1006: Using the EVAL-ADUSB2EBZ
- AN-923: Designing a System Using the ADAU1701/ ADAU1702 in Self-Boot Mode
- AN-951: Using Hardware Controls with SigmaDSP GPIO Pins

Data Sheet

- ADAU1701: SigmaDSP 28-/56-Bit Audio Processor with Two ADCs and Four DACs Data Sheet

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- UG-072: Evaluation Board User Guide for ADAU1401

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- ADAU1701 Sound Audio System Linux Driver
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- CN0162

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FUNCTIONAL BLOCK DIAGRAM

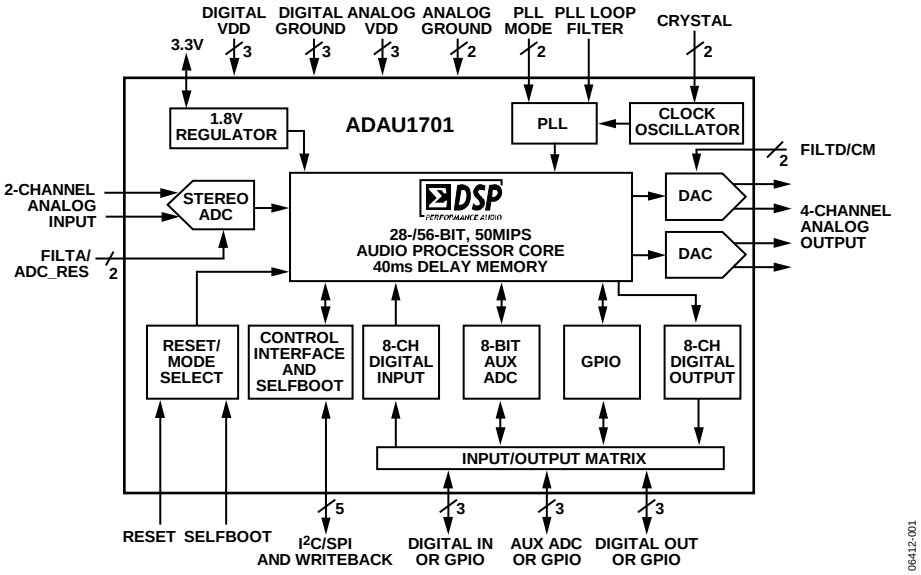

Figure 1.

SPECIFICATIONS

AVDD = 3.3 V, DVDD = 1.8 V, PVDD = 3.3 V, IOVDD = 3.3 V, master clock input = 12.288 MHz, unless otherwise noted.

ANALOG PERFORMANCE

Specifications are guaranteed at 25°C (ambient).

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ADC INPUTS					
Number of Channels		2			Stereo input
Resolution		24		Bits	
Full-Scale Input		100 (283)		µA rms (µA p-p)	2 V rms input with 20 kΩ (18 kΩ external + 2 kΩ internal) series resistor
Signal-to-Noise Ratio					
A-Weighted		100		dB	
Dynamic Range					−60 dB with respect to full-scale analog input
A-Weighted	95	100		dB	
Total Harmonic Distortion + Noise		−83		dB	−3 dB with respect to full-scale analog input
Interchannel Gain Mismatch		25	250	mdB	
Crosstalk		−82		dB	Analog channel-to-channel crosstalk
DC Bias	1.4	1.5	1.6	V	
Gain Error	−11		+11	%	
DAC OUTPUTS					
Number of Channels		4			Two stereo output channels
Resolution		24		Bits	
Full-Scale Analog Output		0.9 (2.5)		V rms (V p-p)	
Signal-to-Noise Ratio					
A-Weighted		104		dB	
Dynamic Range					−60 dB with respect to full-scale analog output
A-Weighted	99	104		dB	
Total Harmonic Distortion + Noise		−90		dB	−1 dB with respect to full-scale analog output
Crosstalk		−100		dB	Analog channel-to-channel crosstalk
Interchannel Gain Mismatch		25	250	mdB	
Gain Error	−10		+10	%	
DC Bias	1.4	1.5	1.6	V	
VOLTAGE REFERENCE					
Absolute Voltage (CM)	1.4	1.5	1.6	V	
AUXILIARY ADC					
Full-Scale Analog Input	2.8	3.0	3.1	V	
INL		0.5		LSB	
DNL		1.0		LSB	
Offset		15		mV	
Input Impedance	17.8	30	42	kΩ	

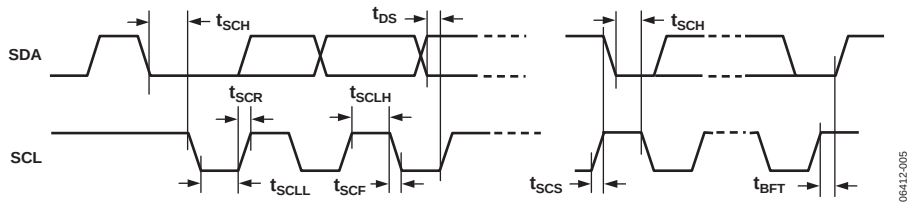

Figure 4. I²C Port Timing

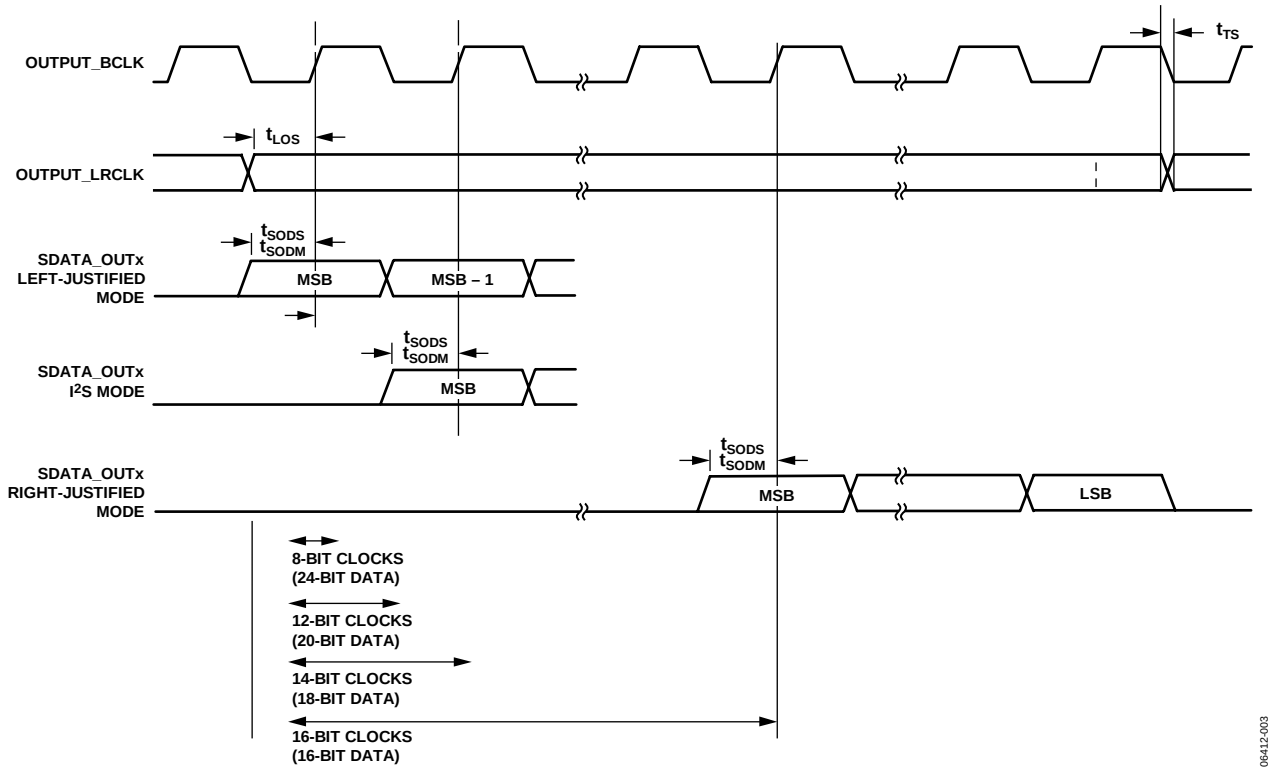

Figure 5. Serial Output Port Timing

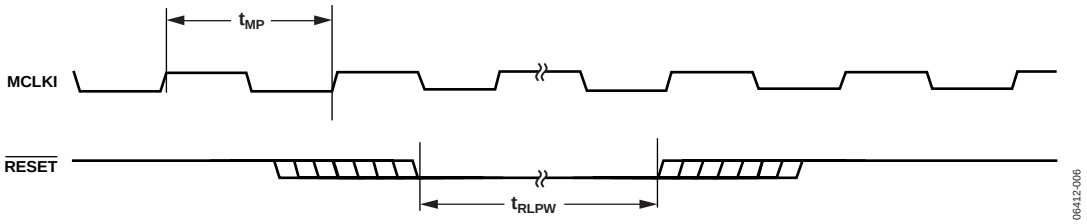

Figure 6. Master Clock and $\overline{RESET}$ Timing

Pin No.	Mnemonic	Type[1]	Description
14	MP7	D_IO	Multipurpose GPIO or Serial Output Port Data 1 (SDATA_OUT1). See the Multipurpose Pins section for more details.
15	MP6	D_IO	Multipurpose GPIO, Serial Output Port Data 0, or TDM Data Output (SDATA_OUT0). See the Multipurpose Pins section for more details.
16	MP10	D_IO	Multipurpose GPIO or Serial Output Port LRCLK (OUTPUT_LRCLK). See the Multipurpose Pins section for more details.
17	VDRIVE	A_OUT	Drive for 1.8 V Regulator. The base of the voltage regulator external PNP transistor is driven from VDRIVE. See the Voltage Regulator section for details.
18	IOVDD	PWR	Supply for Input and Output Pins. The voltage on this pin sets the highest input voltage that should be seen on the digital input pins. This pin is also the supply for the digital output signals on the control port and MP pins. Always set IOVDD to 3.3 V. The current draw of this pin is variable because it is dependent on the loads of the digital outputs.
19	MP11	D_IO	Multipurpose GPIO or Serial Output Port BCLK (OUTPUT_BCLK). See the Multipurpose Pins section for more details.
20	ADDR1/CDATA/WB	D_IN	I²C Address 1/SPI Data Input/EEPROM Write Back Trigger. This is a multifunction pin as follows: ADDR1: I²C Address 1. In combination with ADDR0, this sets the I²C address of the IC so that four ADAU1701 devices can be used on the same I²C bus. See the I²C Port section for details. CDATA: SPI Data Input. See the SPI Port section for details. WB: EEPROM Writeback Trigger. A rising (default) or falling (if set in the EEPROM messages) edge on this pin triggers a writeback of the interface registers to the external EEPROM. This function can be used to save parameter data on power-down. See the Self-Boot section for details.
21	CLATCH/WP	D_IO	SPI Latch Signal/Self-Boot EEPROM Write Protect. This is a multifunction pin as follows: CLATCH: SPI Latch Signal. Must go low at the beginning of an SPI transaction and high at the end of a transaction. Each SPI transaction can take a different number of cycles on the CCLK pin to complete, depending on the address and read/write bit that are sent at the beginning of the SPI transaction. See the SPI Port section for details. WP: Self-Boot EEPROM Write Protect. This pin is an open-collector output when in self-boot mode. The ADAU1701 pulls this low to enable writes to an external EEPROM. This pin should be pulled high to 3.3 V. See the Self-Boot section for details.
22	SDA/COUT	D_IO	I²C Data/SPI Data Output. This is a multifunction pin, as follows: SDA: I²C Data. This pin is a bidirectional open-collector. The line connected to this pin should have a 2.2 kΩ pull-up resistor. See the I²C Port section for details. COUT: This SPI data output is used for reading back registers and memory locations. It is three-stated when an SPI read is not active. See the SPI Port section for details.
23	SCL/CCLK	D_IO	I²C Clock/SPI Clock. This is a dual function pin, as follows: SCL: I²C Clock. This pin is always an open-collector input when in I²C control mode. In self-boot mode, this pin is an open-collector output (I²C master). The line connected to this pin should have a 2.2 kΩ pull-up resistor. See the I²C Port section for details. CCLK: SPI Clock. This pin can either run continuously or be gated off between SPI transactions. See the SPI Port section for details.
26	MP9	D_IO/A_IO	Multipurpose GPIO, Serial Output Port Data 3 (SDATA_OUT3), or Auxiliary ADC Input 0. See the Multipurpose Pins section for more details.
27	MP8	D_IO/A_IO	Multipurpose GPIO, Serial Output Port Data 2 (SDATA_OUT2), or Auxiliary ADC Input 3. See the Multipurpose Pins section for more details.
28	MP3	D_IO/A_IO	Multipurpose GPIO, Serial Input Port Data 3 (SDATA_IN3), or Auxiliary ADC Input 2. See the Multipurpose Pins section for more details.
29	MP2	D_IO/A_IO	Multipurpose GPIO, Serial Input Port Data 2 (SDATA_IN2), or Auxiliary ADC Input 1. See the Multipurpose Pins section for more details.
30	RSVD		Reserved. Tie to ground, either directly or through a pull-down resistor.
31	OSCO	D_OUT	Crystal Oscillator Circuit Output. Connect a 100 Ω damping resistor between this pin and the crystal. Do not use this output to directly drive a clock to another IC. If the crystal oscillator is not used, this pin can be left disconnected. See the Using the Oscillator section for details.
32	MCLKI	D_IN	Master Clock Input. MCLKI can either be connected to a 3.3 V clock signal or be the input from the crystal oscillator circuit. See the Setting Master Clock/PLL Mode section for details.

Pin No.	Mnemonic	Type[1]	Description
33	PGND	PWR	PLL Ground Pin. The AGND, DGND, and PGND pins can be tied directly together in a common ground plane. Decouple PGND to PVDD by using a 100 nF capacitor.
34	PVDD	PWR	3.3 V Power Supply for the PLL and the Auxiliary ADC Analog Section. Decouple this pin to PGND by using a 100 nF capacitor.
35	PLL_LF	A_OUT	PLL Loop Filter Connection. Two capacitors and a resistor need to be connected to this pin, as shown in Figure 15. See the Setting Master Clock/PLL Mode section for more details.
36, 48	AVDD	PWR	3.3 V Analog Supply. Decouple this pin to AGND by using a 100 nF capacitor.
38, 39	PLL_MODE0, PLL_MODE1	D_IN	PLL Mode Setting. PLL_MODE0 and PLL_MODE1 set the output frequency of the master clock PLL. See the Setting Master Clock/PLL Mode section for more details.
40	CM	A_OUT	1.5 V Common-Mode Reference. Connect a 47 µF decoupling capacitor between this pin and ground to reduce crosstalk between the ADCs and DACs. The material of the capacitors is not critical. This pin can be used to bias external analog circuits, as long as those circuits are not drawing current from the pin (such as when CM is connected to the noninverting input of an op amp).
41	FILTD	A_OUT	DAC Filter Decoupling Pin. Connect a 10 µF capacitor between this pin and ground. The capacitor material is not critical. The voltage on this pin is 1.5 V.
43 to 46	VOUT3	A_OUT	VOUT DAC Output. The full-scale output voltage is 0.9 V rms. This output can be used with either an active or passive output reconstruction filter. See the Audio DACs section for details.
44	VOUT2	A_OUT	VOUT2 DAC Output. The full-scale output voltage is 0.9 V rms. This output can be used with either an active or passive output reconstruction filter. See the Audio DACs section for details.
45	VOUT1	A_OUT	VOUT1 DAC Output. The full-scale output voltage is 0.9 V rms. This output can be used with either an active or passive output reconstruction filter. See the Audio DACs section for details.
46	VOUT0	A_OUT	VOUT0 DAC Output. The full-scale output voltage is 0.9 V rms. This output can be used with either an active or passive output reconstruction filter. See the Audio DACs section for details.
47	FILTA	A_OUT	ADC Filter Decoupling Pin. A 10 µF capacitor should be connected between this pin and ground. The capacitor material is not critical. The voltage on this pin is 1.5 V.

[1] PWR = power/ground, A_IN = analog input, D_IN = digital input, A_OUT = analog output, D_IO = digital input/output, D_IO/A_IO = digital input/output or analog input/output.

SYSTEM BLOCK DIAGRAM

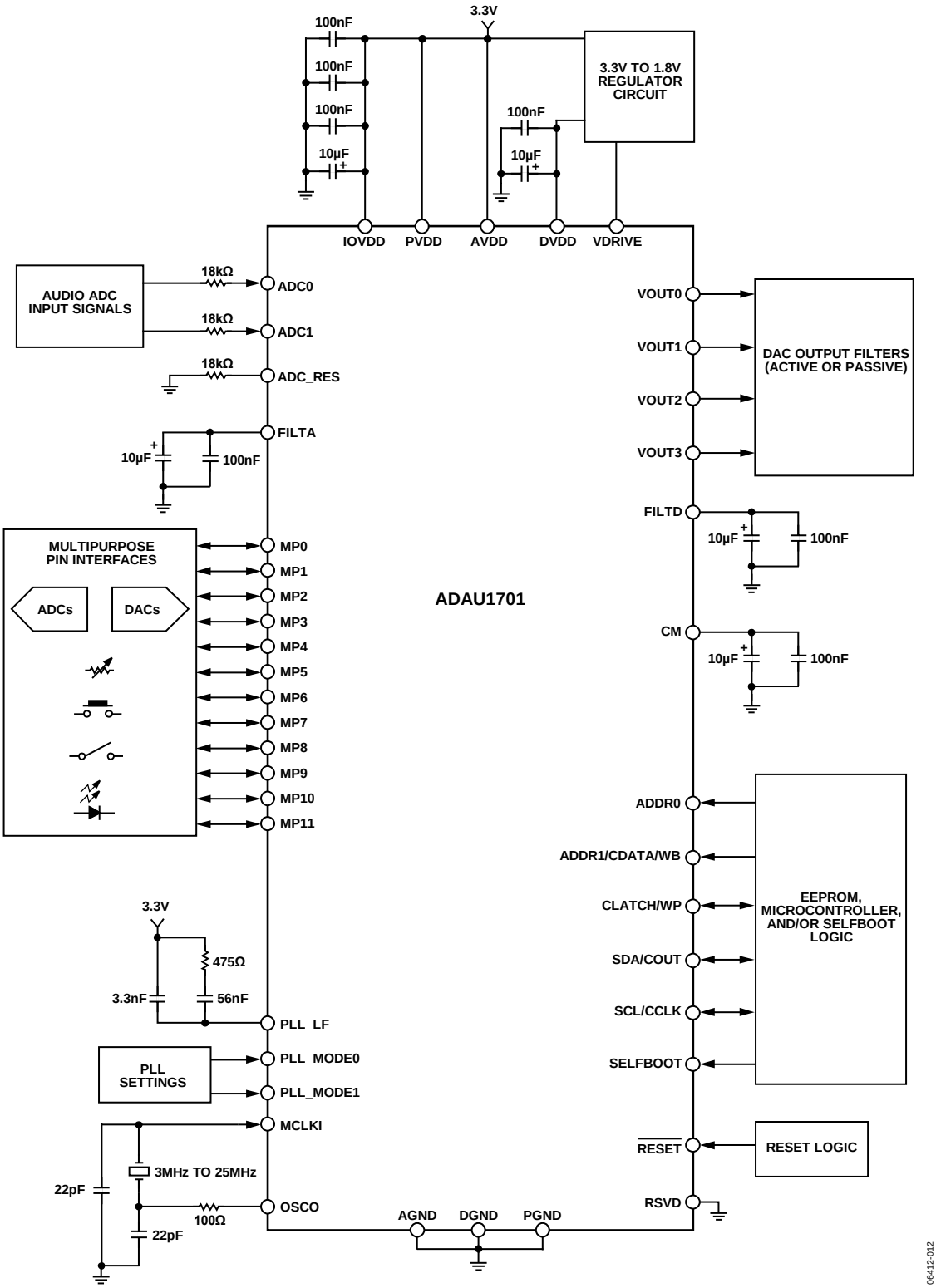

Figure 12. System Block Diagram

INITIALIZATION

This section details the procedure for properly setting up the ADAU1701. The following five-step sequence provides an overview of how to initialize the IC:

1. Apply power to ADAU1701.
2. Wait for PLL to lock.
3. Load SigmaDSP program and parameters.
4. Set up registers (including multipurpose pins and digital interfaces).
5. Turn off the default muting of the converters, clear the data registers, and initialize the DAC setup register (see the Control Registers Setup section for specific settings).

To only test analog audio pass-through (ADCs to DACs), skip Step 3 and Step 4 and use the default internal program.

POWER-UP SEQUENCE

The ADAU1701 has a built-in power-up sequence that initializes the contents of all internal RAMs on power-up or when the device is brought out of a reset. On the positive edge of $\overline{\text{RESET}}$, the contents of the internal program boot ROM are copied to the internal program RAM memory, the parameter RAM is filled with values (all 0s) from its associated boot ROM, and all registers are initialized to 0s. The default boot ROM program copies audio from the inputs to the outputs without processing it (see Figure 13). In this program, serial digital Input 0 and Input 1 are output on DAC0 and DAC1 and serial digital Output 0 and Output 1. ADC0 and ADC1 are output on DAC2 and DAC3. The data memories are also zeroed at power-up. New values should not be written to the control port until the initialization is complete.

Table 11. Power-Up Time

MCLKI Input	Init. Time	Max Program/ Parameter/Register Boot Time (I^2C)	Total
3.072 MHz (64 × f_S)	85 ms	175 ms	260 ms
11.289 MHz (256 × f_S)	23 ms	175 ms	198 ms
12.288 MHz (256 × f_S)	21 ms	175 ms	196 ms
18.432 MHz (384 × f_S)	16 ms	175 ms	191 ms
24.576 MHz (512 × f_S)	11 ms	175 ms	186 ms

The PLL start-up time lasts for 2^{18} cycles of the clock on the MCLKI pin. This time ranges from 10.7 ms for a 24.576 MHz (512 × f_S) input clock to 85.3 ms for a 3.072 MHz (64 × f_S) input clock and is measured from the rising edge of $\overline{\text{RESET}}$. Following the PLL startup, the duration of the ADAU1701 boot cycle is about 42 µs for a f_S of 48 kHz. The user should avoid writing to or reading from the ADAU1701 during this start-up time. For an MCLK input of 12.288 MHz, the full initialization sequence (PLL startup plus boot cycle) is approximately 21 ms. As the device comes out of a reset, the clock mode is immediately set by the PLL_MODE0 and PLL_MODE1 pins. The reset is synchronized to the falling edge of the internal clock.

Table 11 lists typical times to boot the ADAU1701 into an operational state of an application, assuming a 400 kHz I^2C clock loading a full program, parameter set, and all registers (about 8.5 kB). In reality, most applications do not fill the RAMs and therefore boot time (Column 3 of Table 11) is less.

CONTROL REGISTERS SETUP

The following registers must be set as described in this section to initialize the ADAU1701. These settings are the basic minimum settings needed to operate the IC with an analog input/output of 48 kHz. More registers may need to be set, depending on the application. See the RAMs and Registers section for additional settings.

DSP Core Control Register (Address 2076)

Set Bits[4:2] (ADM, DAM, and CR) each to 1.

DAC Setup Register (Address 2087)

Set Bits[0:1] (DS[1:0]) to 01.

RECOMMENDED PROGRAM/PARAMETER LOADING PROCEDURE

When writing large amounts of data to the program or parameter RAM in direct write mode, the processor core should be disabled to prevent unpleasant noises from appearing in the audio output.

1. Set Bit 3 and Bit 4 (active low) of the core control register to 1 to mute the ADCs and DACs. This begins a volume ramp-down.
2. Set Bit 2 (active low) of the core control register to 1. This zeroes the SigmaDSP accumulators, the data output registers, and the data input registers.
3. Fill the program RAM using burst mode writes.
4. Fill the parameter RAM using burst mode writes.
5. Deassert Bit 2 to Bit 4 of the core control register.

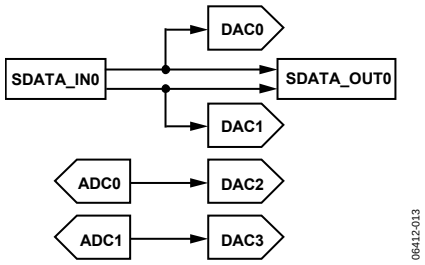

Figure 13. Default Program Signal Flow

POWER REDUCTION MODES

Sections of theADAU1701 chip can be turned on and off as needed to reduce power consumption. These include the ADCs, DACs, and voltage reference.

The individual analog sections can be turned off by writing to the auxiliary ADC and power control register. By default, the ADCs, DACs, and reference are enabled (all bits set to 0). Each of these can be turned off by writing a 1 to the appropriate bits

in this register. The ADC power-down mode powers down both ADCs, and each DAC can be powered down individually. The current savings is about 15 mA when the ADCs are powered down and about 4 mA for each DAC that is powered down. The voltage reference, which is supplied to both the ADCs and DACs, should only be powered down if all ADCs and DACs are powered down. The reference is powered down by setting both Bit 6 and Bit 7 of the control register.

USING THE OSCILLATOR

The ADAU1701 can use an on-board oscillator to generate its master clock. The oscillator is designed to work with a 256 × f_S master clock, which is 12.288 MHz for a f_S of 48 kHz and 11.2896 MHz for a f_S of 44.1 kHz. The crystal in the oscillator circuit should be an AT-cut, parallel resonator operating at its fundamental frequency. Figure 14 shows the external circuit recommended for proper operation.

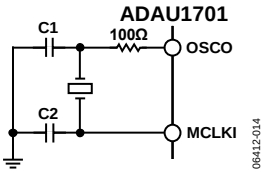

Figure 14. Crystal Oscillator Circuit

The 100 Ω damping resistor on OSCO gives the oscillator a voltage swing of approximately 2.2 V. The crystal shunt capacitance should be 7 pF. Its load capacitance should be about 18 pF, although the circuit supports values of up to 25 pF. The necessary values of the C1 and C2 load capacitors can be calculated from the crystal load capacitance as follows:

$$C_L = \frac{C1 \times C2}{C1 + C2} + C_{stray}$$

where C_{stray} is the stray capacitance in the circuit and is usually assumed to be approximately 2 pF to 5 pF.

OSCO should not be used to directly drive the crystal signal to another IC. This signal is an analog sine wave, and it is not appropriate to use it to drive a digital input. There are two options for using the ADAU1701 to provide a master clock to other ICs in the system. The first, and less recommended, method is to use a high impedance input digital buffer on the OSCO signal. If this is done, minimize the trace length to the buffer input. The second method is to use a clock from the serial output port. Pin MP11 can be set as an output (master) clock divided down from the internal core clock. If this pin is set to serial output port (OUTPUT_BCLK) mode in the multipurpose pin configuration register (2081) and the port is set to master in the serial output control register (2078), the desired output frequency can also be set in the serial output control register with Bits[OBF<1:0>] (see Table 48).

If the oscillator is not utilized in the design, it can be powered down to save power. This can be done if a system master clock is already available in the system. By default, the oscillator is powered on. The oscillator powers down when a 1 is written to the OPD bit of the oscillator power-down register (see Table 59).

SETTING MASTER CLOCK/PLL MODE

The MCLKI input of the ADAU1701 feeds a PLL, which generates the 50 MIPS SigmaDSP core clock. In normal operation, the input to MCLKI must be one of the following: 64 × f_S, 256 × f_S, 384 × f_S, or 512 × f_S, where f_S is the input sampling rate. The mode is set on PLL_MODE0 and PLL_MODE1 as described in Table 12. If the ADAU1701 is set to receive double-rate signals (by reducing the number of program steps per sample by a factor of 2 using the core control register), the master clock frequency must be 32 × f_S, 128 × f_S, 192 × f_S, or 256 × f_S. If the ADAU1701 is set to receive quad-rate signals (by reducing the number of program steps per sample by a factor of 4 using the core control register), the master clock frequency must be 16 × f_S, 64 × f_S, 96 × f_S, or 128 × f_S. On power-up, a clock signal must be present on the MCLKI pin so that the ADAU1701 can complete its initialization routine.

Table 12. PLL Modes

MCLKI Input	PLL_MODE0	PLL_MODE1
64 × f_S	0	0
256 × f_S	0	1
384 × f_S	1	0
512 × f_S	1	1

The clock mode should not be changed without also resetting the ADAU1701. If the mode is changed during operation, a click or pop can result in the output signals. The state of the PLL_MODEx pins should be changed while $\overline{\text{RESET}}$ is held low.

The PLL loop filter should be connected to the PLL_LF pin. This filter, shown in Figure 15, includes three passive components—two capacitors and a resistor. The values of these components do not need to be exact; the tolerance can be up to 10% for the resistor and up to 20% for the capacitors. The 3.3 V signal shown in Figure 15 can be connected to the AVDD supply of the chip.

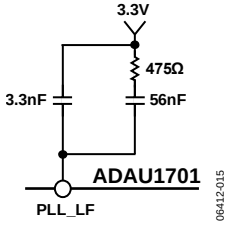

Figure 15. PLL Loop Filter

AUDIO ADCs

The ADAU1701 has two Σ-Δ ADCs. The signal-to-noise ratio (SNR) of the ADCs is 100 dB, and the THD + N is −83 dB.

The stereo audio ADCs are current input; therefore, a voltage-to-current resistor is required on the inputs. This means that the voltage level of the input signals to the system can be set to any level; only the input resistors need to be scaled to provide the proper full-scale current input. The ADC0 and ADC1 input pins, as well as ADC_RES, have an internal 2 kΩ resistor for ESD protection. The voltage seen directly on the ADC input pins is the 1.5 V common mode.

The external resistor connected to ADC_RES sets the full-scale current input of the ADCs. The full range of the ADC inputs is 100 μA rms with an external 18 kΩ resistor on ADC_RES (20 kΩ total, because it is in series with the internal 2 kΩ). The only reason to change the ADC_RES resistor is if a sampling rate other than 48 kHz is used.

The voltage-to-current resistors connected to ADC0/ADC1 set the full-scale voltage input of the ADCs. With a full-scale current input of 100 μA rms, a 2.0 V rms signal with an external 18 kΩ resistor (in series with the 2 kΩ internal resistor) results in an input using the full range of the ADC. The matching of these resistors to the ADC_RES resistor is important to the operation of the ADCs. For these three resistors, a 1% tolerance is recommended.

Either the ADC0 and/or ADC1 input pins can be left unconnected if that channel of the ADC is unused.

These calculations of resistor values assume a 48 kHz sample rate. The recommended input and current setting resistors scale linearly with the sample rate because the ADCs have a switched-capacitor input. The total value (2 kΩ internal plus external resistor) of the ADC_RES resistor with sample rate f_{S_NEW} can be calculated as follows:

$$R_{total} = 20\ \text{k}\Omega \times \frac{48{,}000}{f_{S\_NEW}}$$

The values of the resistors (internal plus external) in series with the ADC0 and ADC1 pins can be calculated as follows:

$$R_{Input\ Total} = (rms\ Input\ Voltage) \times 10\ \text{k}\Omega \times \frac{48{,}000}{f_{S\_NEW}}$$

Table 13 lists the external and total resistor values for common signal input levels at a 48 kHz sampling rate. A full-scale rms input voltage of 0.9 V is shown in the table because a full-scale signal at this input level is equal to a full-scale output on the DACs.

Table 13. ADC Input Resistor Values

Full-Scale RMS Input Voltage (V)	ADC_RES Value (kΩ)	ADC0/ADC1 Resistor Value (kΩ)	Total ADC0/ADC1 Input Resistance (External + Internal) (kΩ)
0.9	18	7	9
1.0	18	8	10
2.0	18	18	20

Figure 17 shows a typical configuration of the ADC inputs for a 2.0 V rms input signal for a f_S of 48 kHz. The 47 μF capacitors are used to ac-couple the signals so that the inputs are biased at 1.5 V.

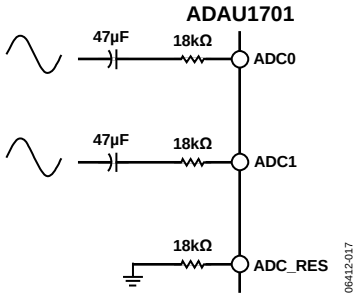

Figure 17. Audio ADC Input Configuration

CONTROL PORTS

The ADAU1701 can operate in one of three control modes:

- I²C control
- SPI control
- Self-boot (no external controller)

The ADAU1701has both a 4-wire SPI control port and a 2-wire I²C bus control port. Each can be used to set the RAMs and registers. When the SELFBOOT pin is low at power-up, the part defaults to I²C mode but can be put into SPI control mode by pulling the CLATCH/WP pin low three times. When the SELFBOOT pin is set high at power-up, the ADAU1701 loads its program, parameters, and register settings from an external EEPROM on startup.

The control port is capable of full read/write operation for all addressable memory and registers. Most signal processing parameters are controlled by writing new values to the parameter RAM using the control port. Other functions, such as mute and input/output mode control, are programmed by writing to the registers.

All addresses can be accessed in a single-address mode or a burst mode. The first byte (Byte 0) of a control port write contains the 7-bit chip address plus the R/$\overline{W}$ bit. The next two bytes (Byte 1 and Byte 2) together form the subaddress of the memory or register location within the ADAU1701. This subaddress must be two bytes because the memory locations within the ADAU1701 are directly addressable and their sizes exceed the range of single-byte addressing. All subsequent bytes (starting with Byte 3) contain the data, such as control port data, program data, or parameter data. The number of bytes per word depends on the type of data that is being written. The exact formats for specific types of writes are shown in Table 21 to Table 30.

TheADAU1701 has several mechanisms for updating signal processing parameters in real time without causing pops or clicks. If large blocks of data need to be downloaded, the output of the DSP core can be halted (using the CR bit in the DSP core control register (Address 2076)), new data can be loaded, and then the device can be restarted. This is typically done during the booting sequence at startup or when loading a new program into RAM. In cases where only a few parameters need to be changed, they can be loaded without halting the program. To avoid unwanted side effects while loading parameters on the fly, the SigmaDSP provides the safeload registers. The safeload registers can be used to buffer a full set of parameters (for example, the five coefficients of a biquad) and then transfer these parameters into the active program within one audio frame. The safeload mode uses internal logic to prevent contention between the DSP core and the control port.

The control port pins are multifunctional, depending on the mode in which the part is operating. Table 14 details these multiple functions.

Table 14. Control Port Pins and SELFBOOT Pin Functions

Pin	I²C Mode	SPI Mode	Self-Boot
SCL/CCLK	SCL—input	CCLK—input	SCL—output
SDA/COUT	SDA—open-collector output	COUT—output	SDA—open-collector output
ADDR1/CDATA/WB	ADDR1—input	CDATA—input	WB—writeback trigger
CLATCH/WP	Unused input—tie to ground or IOVDD	CLATCH—input	WP—EEPROM write protect, open-collector output
ADDR0	ADDR0—input	ADDR0—input	Unused input—tie to ground or IOVDD

I²C PORT

The ADAU1701supports a 2-wire serial (I²C-compatible) microprocessor bus driving multiple peripherals. Two pins, serial data (SDA) and serial clock (SCL), carry information between the ADAU1701and the system I²C master controller. In I²C mode, theADAU1701 is always a slave on the bus, meaning it cannot initiate a data transfer. Each slave device is recognized by a unique address. The address byte format is shown in Table 15. The ADAU1701 slave addresses are set with the ADDR0 and ADDR1 pins. The address resides in the first seven bits of the I²C write. The LSB of this byte sets either a read or write operation. Logic Level 1 corresponds to a read operation, and Logic Level 0 corresponds to a write operation. Bit 5 and Bit 6 of the address are set by tying the ADDRx pins of the ADAU1701 to Logic Level 0 or Logic Level 1. The full byte addresses, including the pin settings and read/write (R/$\overline{W}$) bit, are shown in Table 16.

Burst mode addressing, where the subaddresses are automatically incremented at word boundaries, can be used for writing large amounts of data to contiguous memory locations. This increment happens automatically after a single-word write unless a stop condition is encountered. The registers and RAMs in the ADAU1701 range in width from one to five bytes, so the auto-increment feature knows the mapping between subaddresses and the word length of the destination register (or memory location). A data transfer is always terminated by a stop condition.

Both SDA and SCL should have 2.2 kΩ pull-up resistors on the lines connected to them. The voltage on these signal lines should not be more than IOVDD (3.3 V).

Table 15. ADAU1701 I²C Address Byte Format

Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
0	1	1	0	1	ADDR1	ADDR0	R/$\overline{W}$

Table 16. ADAU1701 I²C Addresses

ADDR1	ADDR0	R/$\overline{W}$	Slave Address
0	0	0	0x68
0	0	1	0x69
0	1	0	0x6A
0	1	1	0x6B
1	0	0	0x6C
1	0	1	0x6D
1	1	0	0x6E
1	1	1	0x6F

Addressing

Initially, each device on the I²C bus is in an idle state monitoring the SDA and SCL lines for a start condition and the proper address. The I²C master initiates a data transfer by establishing a start condition, defined by a high-to-low transition on SDA while SCL remains high. This indicates that an address/data stream follows. All devices on the bus respond to the start condition and shift the next eight bits (the 7-bit address plus the R/$\overline{W}$ bit) MSB first. The device that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse. This ninth bit is known as an acknowledge bit. All other devices withdraw from the bus at this point and return to the idle condition. The R/$\overline{W}$ bit determines the direction of the data. A Logic 0 on the LSB of the first byte means the master writes information to the peripheral, whereas a Logic 1 means the master reads information from the peripheral after writing the subaddress and repeating the start address. A data transfer takes place until a stop condition is encountered. A stop condition occurs when SDA transitions from low to high while SCL is held high. Figure 20 shows the timing of an I²C write, and Figure 21 shows an I²C read.

Stop and start conditions can be detected at any stage during the data transfer. If these conditions are asserted out of sequence with normal read and write operations, theADAU1701 immediately jumps to the idle condition. During a given SCL high period, the user should only issue one start condition, one stop condition, or a single stop condition followed by a single start condition. If an invalid subaddress is issued by the user, the ADAU1701 does not issue an acknowledge and returns to the idle condition. If the user exceeds the highest subaddress while in auto-increment mode, one of two actions is taken. In read mode, the ADAU1701 outputs the highest subaddress register contents until the master device issues a no acknowledge, indicating the end of a read. A no-acknowledge condition is where the SDA line is not pulled low on the ninth clock pulse on SCL. On the other hand, if the highest subaddress location is reached while in write mode, the data for the invalid byte is not loaded into any subaddress register, a no acknowledge is issued by the ADAU1701, and the part returns to the idle condition.

SELF-BOOT

On power-up, the ADAU1701 can load a program and a set of parameters that have been saved in an external EEPROM. Combined with the auxiliary ADC and the multipurpose pins, this eliminates the need for a microcontroller in the system. The self-booting is accomplished by the ADAU1701 acting as a master on the I²C bus on startup, which occurs when the SELFBOOT pin is set high. The ADAU1701 cannot self-boot in SPI mode.

The maximum necessary EEPROM size for program and parameters is 9248 bytes, or just over 8.5 kB. This does not include register settings or overhead bytes, but such factors do not add a significant number of bytes. This much memory is only needed if the program RAM (1024 × five bytes), parameter RAM (1024 × four bytes), and interface registers (8 × four bytes) are completely full. Most applications do not use the full program and parameter RAMs, so an 8 kB EEPROM should be sufficient.

A self-boot operation is triggered on the rising edge of $\overline{\text{RESET}}$ when the SELFBOOT and WP pins are set high. The ADAU1701reads the program, parameters, and register settings from the EEPROM. After the ADAU1701 finishes self-booting, additional messages can be sent to the ADAU1701 on the I²C bus, although this typically is not necessary in a self-booting application. The I²C device address is 0x68 for a write and 0x69 for a read in this mode. The ADDRx pins have different functions when the chip is in this mode, so the settings on them can be ignored.

The ADAU1701 does not self-boot if WP is set low. Holding this pin low allows the EEPROM to be programmed in-circuit. The WP pin is pulled low (it typically has a resistor pull-up) to enable writes to the EEPROM, but this in turn disables the self-boot function until the WP pin is returned high.

The ADAU1701 is a master on the I²C bus during self-boot and writeback. Although it is uncommon for an application using self-boot to also have a microcontroller connected to the control lines, care should be taken that no other device tries to write to the I²C bus during self-boot or writeback. The ADAU1701 generates SCL at 8 × f_S; therefore, for a f_S of 48 kHz, SCL runs at 384 kHz. SCL has a duty cycle of 3/8 in accordance with the I²C specification.

The ADAU1701 reads from EEPROM Chip Address 0xA1. The LSBs of the addresses of some EEPROMs are pin configurable; in most cases, these pins should be tied low to set this address.

EEPROM Format

The EEPROM data contains a sequence of messages. Each discrete message is one of the seven types defined in Table 19 and consists of a sequence of one or more bytes. The first byte identifies the message type. Bytes are written MSB first. Most messages are block write (0x01) types, which are used for writing to the ADAU1701 program RAM, parameter RAM, and control registers.

The body of the message following the message type should start with a 0x00 byte; this is the chip address. As with all other control port transactions, following the chip address is a 2-byte register/memory address field.

Figure 28 shows an example of what should be stored in the EEPROM, starting with EEPROM Address 0. In this example, the interface registers are first set to control port write mode (Line 1), which is followed by 18 no-operation (no-op) bytes (Line 2 to Line 4) so that the interface register data appears on Page 2 of the EEPROM. Next follows the write header (Line 4) and then 32 bytes of interface register data (Line 5 to Line 8). Finally, the program RAM data, starting at ADAU1701 Address 0x04 0x00 is written (Line 9 to Line 11). In this example, the program length is 70 words, or 350 bytes, so 332 more bytes are included in the EEPROM but are not shown in Figure 28.

Writeback

A writeback occurs when the WB pin is triggered and data is written to the EEPROM from the ADAU1701. This function is typically used to save the volume setting and other parameter settings to the EEPROM just before power is removed from the system. A rising edge on the WB pin triggers a writeback when the device is in self-boot mode, unless a message to set the WB to the falling edge sensitive (0x05) is contained in the self-boot message sequence. Only one writeback takes place unless a message to set multiple writebacks (0x04) is contained in the self-boot message sequence. The WP pin is pulled low when a writeback is triggered to allow writing to the EEPROM.

The ADAU1701 is only capable of writing back the contents of the interface registers to the EEPROM. These registers are usually set by the DSP program, but can also be written to directly after setting Bit 6 of the core control register. The parameter settings that should be saved are configured in SigmaStudio.

SIGNAL PROCESSING

The ADAU1701 is designed to provide all audio signal processing functions commonly used in stereo or multichannel playback systems. The signal processing flow is designed using the SigmaStudio software, which allows graphical entry and real-time control of all signal processing functions.

Many of the signal processing functions are coded using full, 56-bit, double-precision arithmetic data. The input and output word lengths of the DSP core are 24 bits. Four extra headroom bits are used in the processor to allow internal gains of up to 24 dB without clipping. Additional gains can be achieved by initially scaling down the input signal in the DSP signal flow.

NUMERIC FORMATS

DSP systems commonly use a standard numeric format. Fractional number systems are specified by an A.B format, where A is the number of bits to the left of the decimal point and B is the number of bits to the right of the decimal point.

The ADAU1701 uses the same numeric format for both the parameter and data values. The format is as follows.

Numerical Format: 5.23

Linear range: −16.0 to (+16.0 − 1 LSB)

Examples:
1000 0000 0000 0000 0000 0000 0000 = −16.0
1110 0000 0000 0000 0000 0000 0000 = −4.0
1111 1000 0000 0000 0000 0000 0000 = −1.0
1111 1110 0000 0000 0000 0000 0000 = −0.25
1111 1111 0011 0011 0011 0011 0011 = −0.1
1111 1111 1111 1111 1111 1111 1111 = (1 LSB below 0.0)
0000 0000 0000 0000 0000 0000 0000 = 0.0
0000 0000 1100 1100 1100 1100 1101 = 0.1
0000 0010 0000 0000 0000 0000 0000 = 0.25
0000 1000 0000 0000 0000 0000 0000 = 1.0
0010 0000 0000 0000 0000 0000 0000 = 4.0
0111 1111 1111 1111 1111 1111 1111 = (16.0 − 1 LSB).

The serial port accepts up to 24 bits on the input and is sign-extended to the full 28 bits of the DSP core. This allows internal gains of up to 24 dB without internal clipping.

A digital clipper circuit is used between the output of the DSP core and the DACs or serial port outputs (see Figure 29). This clips the top four bits of the signal to produce a 24-bit output with a range of 1.0 (minus 1 LSB) to −1.0. Figure 29 shows the maximum signal levels at each point in the data flow in both binary and decibel levels.

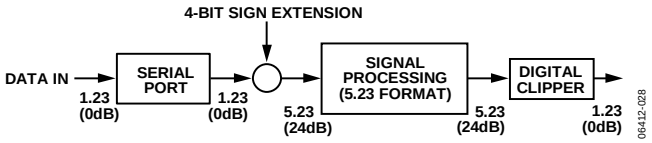

Figure 29. Numeric Precision and Clipping Structure

PROGRAMMING

On power-up, the ADAU1701default program passes the unprocessed input signals to the outputs (shown in Figure 13), but the outputs are muted by default (see the Power-Up Sequence section). There are 1024 instruction cycles per audio sample, resulting in about 50 MIPS available. The SigmaDSP runs in a stream-oriented manner, meaning that all 1024 instructions are executed each sample period. The ADAU1701 can also be set up to accept double- or quad-speed inputs by reducing the number of instructions per sample that are set in the core control register.

The part can be easily programmed using SigmaStudio (Figure 30), a graphical tool provided by Analog Devices. No knowledge of writing line-level DSP code is required. More information about SigmaStudio can be found at www.analog.com.

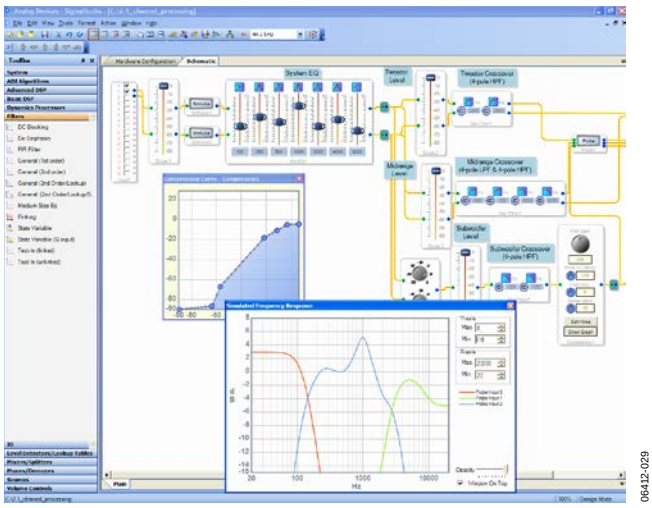

Figure 30. SigmaStudio Screen Shot

CONTROL REGISTER DETAILS

2048 TO 2055 (0x0800 TO 0x0807)—INTERFACE REGISTERS

The interface registers are used in self-boot mode to save parameters that need to be written to the external EEPROM. The ADAU1701 then recalls these parameters from the EEPROM after the next reset or power-up. Therefore, system parameters such as volume and EQ settings can be saved during power-down and recalled the next time the system is turned on.

There are eight 32-bit interface registers, which allow eight 28-bit (plus zero-padding) parameters to be saved. The parameters to be saved in these registers are selected in the graphical programming tools. These registers are updated with their corresponding parameter RAM data once per sample period.

An edge, which can be set to be either rising or falling, triggers the ADAU1701 to write the current contents of the interface registers to the EEPROM. See the Self-Boot section for details.

The user can write directly to the interface registers after the interface registers control port write mode (IFCW) in the DSP core control register has been set. In this mode, the data in the registers is written from the control port, not from the DSP core.

Table 32. Interface Register Bit Map

D31 D15	D30 D14	D29 D13	D28 D12	D27 D11	D26 D10	D25 D9	D24 D8	D23 D7	D22 D6	D21 D5	D20 D4	D19 D3	D18 D2	D17 D1	D16 D0	Default
0	0	0	0	IF27	IF26	IF25	IF24	IF23	IF22	IF21	IF20	IF19	IF18	IF17	IF16	0x0000
IF15	IF14	IF13	IF12	IF11	IF10	IF09	IF08	IF07	IF06	IF05	IF04	IF03	IF02	IF01	IF00	0x0000

Table 33.

Bit Name	Description
IF[27:0]	Interface register 28-bit parameter

2056 (0x0808)—GPIO PIN SETTING REGISTER

This register allows the user to set the GPIO pins through the control port. High or low settings can be directly written to or read from this register after setting the GPIO pin setting register control port write mode (GPCW) in the core control register. This register is updated once every LRCLK frame (1/f_S).

Table 34. GPIO Pin Setting Register Bit Map

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0	0	0	0	MP11	MP10	MP09	MP08	MP07	MP06	MP05	MP04	MP03	MP02	MP01	MP00	0x0000

Table 35.

Bit Name	Description
MP[11:0]	Setting of multipurpose pin when controlled through SPI or I²C

2074 TO 2075 (0x081A TO 0x081B)—DATA CAPTURE REGISTERS

The ADAU1701 data capture feature allows the data at any node in the signal processing flow to be sent to one of two readable registers. This feature is useful for monitoring and displaying information about internal signal levels or compressor/limiter activity.

For each of the data capture registers, a capture count and a register select must be set. The capture count is a number between 0 and 1023 that corresponds to the program step number where the capture is to occur. The register select field programs one of four registers in the DSP core that transfers this information to the data capture register when the program counter reaches this step.

The captured data is in 5.19, twos complement data format, which comes from the internal 5.23 data-word with the four LSBs truncated.

The data that must be written to set up the data capture is a concatenation of the 10-bit program count index with the 2-bit register select field. The capture count and register select values that correspond to the desired point to be monitored in the signal processing flow can be found in a file output from the program compiler. The capture registers can be accessed by reading from Location 2074 and Location 2075. The format for writing and reading to the data capture registers is shown in Table 27 and Table 28.

Table 43. Safeload Data Registers Bit Map

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0	0	0	0	PC09	PC08	PC07	PC06	PC05	PC04	PC03	PC02	PC01	PC00	RS01	RS00	0x0000

Table 44.

Bit Name	Description	
PC[9:0]	10-bit program counter address	
RS[1:0]	Select the register to be transferred to the data capture output	
	RS[1:0]	**Register**
	00	Multiplier X input (Mult_X_input)
	01	Multiplier Y input (Mult_Y_input)
	10	Multiplier-accumulator output (MAC_out)
	11	Accumulator feedback (Accum_fback)

2078 (0x081E)—SERIAL OUTPUT CONTROL REGISTER

Table 47. Serial Output Control Register Bit Map

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0	0	OLRP	OBP	M/S	OBF1	OBF0	OLF1	OLF0	FST	TDM	MSB2	MSB1	MSB0	OWL1	OWL0	0x0000

Table 48.

Bit Name	Description	
OLRP	OUTPUT_LRCLK Polarity. When this bit is set to 0, the left-channel data is clocked when OUTPUT_LRCLK is low and the right-channel data is clocked when OUTPUT_LRCLK is high. When this bit is set to 1, the right-channel data is clocked when OUTPUT_LRCLK is low and the left-channel data is clocked when OUTPUT_LRCLK is high.	
OBP	OUTPUT_BCLK Polarity. This bit controls on which edge of the bit clock the output data is clocked. Data changes on the falling edge of OUTPUT_BCLK when this bit is set to 0 and on the rising edge when this bit is set to 1.	
M/S	Master/Slave. This bit sets whether the output port is a clock master or slave. The default setting is slave; on power-up, the OUTPUT_BCLK and OUTPUT_LRCLK pins are set as inputs until this bit is set to 1, at which time they become clock outputs.	
OBF[1:0]	OUTPUT_BCLK Frequency (Master Mode Only). When the output port is being used as a clock master, these bits set the frequency of the output bit clock, which is divided down from an internal 1024 × f_S clock (49.152 MHz for a f_S of 48 kHz).	
	OBF[1:0]	**Setting**
	00	Internal clock/16
	01	Internal clock/8
	10	Internal clock/4
	11	Internal clock/2
OLF[1:0]	OUTPUT_LRCLK Frequency (Master Mode Only). When the output port is used as a clock master, these bits set the frequency of the output word clock on the OUTPUT_LRCLK pins, which is divided down from an internal 1024 × f_S clock (49.152 MHz for a f_S of 48 kHz).	
	OLF[1:0]	**Setting**
	00	Internal clock/1024
	01	Internal clock/512
	10	Internal clock/256
	11	Reserved
FST	Frame Sync Type. This bit sets the type of signal on the OUTPUT_LRCLK pins. When this bit is set to 0, the signal is a word clock with a 50% duty cycle; when this bit is set to 1, the signal is a pulse with a duration of one bit clock at the beginning of the data frame.	
TDM	TDM Enable. Setting this bit to 1 changes the output port from four serial stereo outputs to a single 8-channel TDM output stream on the SDATA_OUT0 pin (MP6).	
MSB[2:0]	MSB Position. These three bits set the position of the MSB of data with respect to the LRCLK edge. The data output of theADAU1701 is always MSB first.	
	MSB[2:0]	**Setting**
	000	Delay by 1
	001	Delay by 0
	010	Delay by 8
	011	Delay by 12
	100	Delay by 16
	101	Reserved
	111	Reserved
OWL[1:0]	Output Word Length. These bits set the word length of the output data-word. All bits following the LSB are set to 0.	
	OWL[1:0]	**Setting**
	00	24 bits
	01	20 bits
	10	16 bits
	11	Reserved

MULTIPURPOSE PINS

The ADAU1701 has 12 multipurpose (MP) pins that can be individually programmed to be used as serial data inputs, serial data outputs, digital control inputs/outputs to and from the SigmaDSP core, or inputs to the 4-channel auxiliary ADC. These pins allow the ADAU1701 to be used with external ADCs and DACs. They also use analog or digital inputs to control settings such as volume control, or use output digital signals to drive LED indicators. Every MP pin has an internal 15 kΩ pull-up resistor.

AUXILIARY ADC

The ADAU1701 has a 4-channel, auxiliary, 8-bit ADC that can be used in conjunction with a potentiometer to control volume, tone, or other parameter settings in the DSP program. Each of the four channels is sampled at the audio sampling frequency (f_S). Full-scale input on this ADC is 3.0 V, so the step size is approximately 12 mV (3.0 V/256 steps). The input resistance of the ADC is approximately 30 kΩ. Table 62 indicates which four MP pins are mapped to the four channels of the auxiliary ADC. The auxiliary ADC is enabled for those pins by writing 1111 to the appropriate portion of the multipurpose pin configuration registers.

The auxiliary ADC is turned on by setting the AAEN bit of the auxiliary ADC enable register (see Table 57).

Noise on the ADC input can cause the digital output to constantly change by a few LSBs. If the auxiliary ADC is used to control volume, this constant change causes small gain fluctuations. To avoid this, add a low-pass filter or hysteresis to the auxiliary ADC signal path by enabling either function in the auxiliary ADC and power control register (2082), as described in Table 55. The filter is enabled by default when the auxiliary ADC is enabled. When data is read from the auxiliary ADC registers, two bytes (12 bits of data, plus zero-padded LSBs) are available because of this filtering.

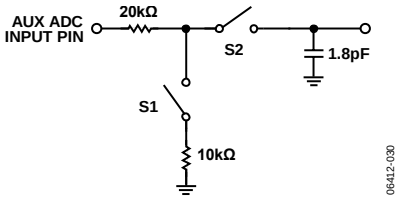

Figure 31. Auxiliary ADC Input Circuit

Figure 31 shows the input circuit for the auxiliary ADC. Switch S1 enables the auxiliary ADC and is set by Bit 15 of the auxiliary ADC enable register. The sampling switch, S2, operates at the audio sampling frequency.

The auxiliary ADC data registers can be written to directly after AACW in the DSP core control register has been set. In this mode, the voltages on the analog inputs are not written into the registers, but rather the data in the registers is written from the control port.

PVDD supplies the 3.3 V power for the auxiliary ADC analog input. The digital core of the auxiliary ADC is powered with the 1.8 V DVDD signal.

Table 62. Multipurpose Pin Auxiliary ADC Mapping

Multipurpose Pin	Function
MP0	N/A
MP1	N/A
MP2	ADC1
MP3	ADC2
MP4	N/A
MP5	N/A
MP6	N/A
MP7	N/A
MP8	ADC3
MP9	ADC0
MP10	N/A
MP11	N/A

GENERAL-PURPOSE INPUT/OUTPUT PINS

The general-purpose input/output (GPIO) pins can be used as either inputs or outputs. These pins are readable and can be set either through the control interface or directly by the SigmaDSP core. When set as inputs, these pins can be used with push-button switches or rotary encoders to control DSP program settings. Digital outputs can be used to drive LEDs or external logic to indicate the status of internal signals and control other devices. Examples of this use include indicating signal overload, signal present, and button press confirmation.

When set as an output, each pin can typically drive 2 mA. This is enough current to directly drive some high efficiency LEDs. Standard LEDs require about 20 mA of current and can be driven from a GPIO output with an external transistor or buffer. Because of issues that could arise from simultaneously driving or sinking a large current on many pins, care should be taken in the application design to avoid connecting high efficiency LEDs directly to many or all of the MPx pins. If many LEDs are required, use an external driver.

When the GPIO pins are set as open-collector outputs, they should be pulled up to a maximum voltage of 3.3 V (the voltage on IOVDD).

SERIAL DATA INPUT/OUTPUT PORTS

The flexible serial data input and output ports of the ADAU1701 can be set to accept or transmit data in 2-channel format or in an 8-channel TDM stream. Data is processed in twos complement, MSB-first format. The left-channel data field always precedes the right-channel data field in the 2-channel streams. In TDM mode, Slot 0 to Slot 3 are in the first half of the audio frame, and Slot 4 to Slot 7 are in the second half of the frame. TDM mode allows fewer multipurpose pins to be used, freeing more pins for other functions. The serial modes are set in the serial output and serial input control registers.

LAYOUT RECOMMENDATIONS

PARTS PLACEMENT

The ADC input voltage-to-current resistors and the ADC current set resistor should be placed as close as possible to the 2, 3, and 4 input pins.

All 100 nF bypass capacitors, which are recommended for every analog, digital, and PLL power/ground pair, should be placed as close as possible to the ADAU1701. The 3.3 V and 1.8 V signals on the board should also each be bypassed with a single bulk capacitor (10 µF to 47 µF).

All traces in the crystal oscillator circuit (Figure 14) should be kept as short as possible to minimize stray capacitance. In addition, avoid long board traces connected to any of these components because such traces may affect crystal startup and operation.

GROUNDING

A single ground plane should be used in the application layout. Components in an analog signal path should be placed away from digital signals.