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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I <sup>2</sup> C, Microwire, SPI, SSI, SSP, UART/USART, USB
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	40
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc11u24fbd48-401">https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc11u24fbd48-401</a>

- ◆ Standard JTAG (Joint Test Action Group) test interface for BSDL (Boundary Scan Description Language).
- ◆ Serial Wire Debug.
- Digital peripherals:
  - ◆ Up to 54 General-Purpose I/O (GPIO) pins with configurable pull-up/pull-down resistors, repeater mode, and open-drain mode.
  - ◆ Up to 8 GPIO pins can be selected as edge and level sensitive interrupt sources.
  - ◆ Two GPIO grouped interrupt modules enable an interrupt based on a programmable pattern of input states of a group of GPIO pins.
  - ◆ High-current source output driver (20 mA) on one pin.
  - ◆ High-current sink driver (20 mA) on true open-drain pins.
  - ◆ Four general-purpose counter/timers with a total of up to 5 capture inputs and 13 match outputs.
  - ◆ Programmable Windowed WatchDog Timer (WWDT) with a dedicated, internal low-power WatchDog Oscillator (WDO).
- Analog peripherals:
  - ◆ 10-bit ADC with input multiplexing among eight pins.
- Serial interfaces:
  - ◆ USB 2.0 full-speed device controller.
  - ◆ USART (Universal Synchronous Asynchronous Receiver/Transmitter) with fractional baud rate generation, internal FIFO, a full modem control handshake interface, and support for RS-485/9-bit mode and synchronous mode. USART supports an asynchronous smart card interface (ISO 7816-3).
  - ◆ Two SSP (Synchronous Serial Port) controllers with FIFO and multi-protocol capabilities.
  - ◆ I<sup>2</sup>C-bus interface supporting the full I<sup>2</sup>C-bus specification and Fast-mode Plus with a data rate of up to 1 Mbit/s with multiple address recognition and monitor mode.
- Clock generation:
  - ◆ Crystal Oscillator with an operating range of 1 MHz to 25 MHz (system oscillator).
  - ◆ 12 MHz high-frequency Internal RC oscillator (IRC) that can optionally be used as a system clock.
  - ◆ Internal low-power, low-frequency WatchDog Oscillator (WDO) with programmable frequency output.
  - ◆ PLL allows CPU operation up to the maximum CPU rate with the system oscillator or the IRC as clock sources.
  - ◆ A second, dedicated PLL is provided for USB.
  - ◆ Clock output function with divider that can reflect the crystal oscillator, the main clock, the IRC, or the watchdog oscillator.
- Power control:
  - ◆ Integrated PMU (Power Management Unit) to minimize power consumption during Sleep, Deep-sleep, Power-down, and Deep power-down modes.
  - ◆ Power profiles residing in boot ROM provide optimized performance and minimized power consumption for any given application through one simple function call.
  - ◆ Four reduced power modes: Sleep, Deep-sleep, Power-down, and Deep power-down.
  - ◆ Processor wake-up from Deep-sleep and Power-down modes via reset, selectable GPIO pins, watchdog interrupt, or USB port activity.

## 6.2 Pin description

Table 3 shows all pins and their assigned digital or analog functions in order of the GPIO port number. The default function after reset is listed first. All port pins have internal pull-up resistors enabled after reset except for the true open-drain pins PIO0\_4 and PIO0\_5.

Every port pin has a corresponding IOCON register for programming the digital or analog function, the pull-up/pull-down configuration, the repeater, and the open-drain modes.

The USART, counter/timer, and SSP functions are available on more than one port pin.

Table 3. Pin description

Symbol	Pin HVQFN33	Pin TFBGA48	Pin LQFP48	Pin LQFP64	Reset state [1]	Type	Description
RESET/PIO0_0	2	C1	3	4 [2]	I; PU	I	<b>RESET</b> — External reset input with 20 ns glitch filter. A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. This pin also serves as the debug select input. LOW level selects the JTAG boundary scan. HIGH level selects the ARM SWD debug mode.  In deep power-down mode, this pin must be pulled HIGH externally. The RESET pin can be left unconnected or be used as a GPIO pin if an external RESET function is not needed and Deep power-down mode is not used.
					-	I/O	<b>PIO0_0</b> — General purpose digital input/output pin.
PIO0_1/CLKOUT/ CT32B0_MAT2/ USB_FTOGGLE	3	C2	4	5 [3]	I; PU	I/O	<b>PIO0_1</b> — General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler or the USB device enumeration.
					-	O	<b>CLKOUT</b> — Clockout pin.
					-	O	<b>CT32B0_MAT2</b> — Match output 2 for 32-bit timer 0.
					-	O	<b>USB_FTOGGLE</b> — USB 1 ms Start-of-Frame signal.
PIO0_2/SSEL0/ CT16B0_CAP0	8	F1	10	13 [3]	I; PU	I/O	<b>PIO0_2</b> — General purpose digital input/output pin.
					-	I/O	<b>SSEL0</b> — Slave select for SSP0.
					-	I	<b>CT16B0_CAP0</b> — Capture input 0 for 16-bit timer 0.
PIO0_3/USB_VBUS	9	H2	14	19 [3]	I; PU	I/O	<b>PIO0_3</b> — General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler. A HIGH level during reset starts the USB device enumeration.
					-	I	<b>USB_VBUS</b> — Monitors the presence of USB bus power.
PIO0_4/SCL	10	G3	15	20 [4]	I; IA	I/O	<b>PIO0_4</b> — General purpose digital input/output pin (open-drain).
					-	I/O	<b>SCL</b> — I <sup>2</sup> C-bus clock input/output (open-drain). High-current sink only if I <sup>2</sup> C Fast-mode Plus is selected in the I/O configuration register.

### 7.3 SRAM

The LPC11U2x contain a total of 8 kB or 10 kB on-chip static RAM memory.

### 7.4 On-chip ROM

The on-chip ROM contains the boot loader and the following Application Programming Interfaces (APIs):

- In-System Programming (ISP) and In-Application Programming (IAP) support for flash
- IAP support for EEPROM
- USB API
- Power profiles for configuring power consumption and PLL settings
- 32-bit integer division routines

### 7.5 Memory map

The LPC11U2x incorporates several distinct memory regions, shown in the following figures. [Figure 6](#) shows the overall map of the entire address space from the user program viewpoint following reset. The interrupt vector area supports address remapping.

The AHB (Advanced High-performance Bus) peripheral area is 2 MB in size and is divided to allow for up to 128 peripherals. The APB (Advanced Peripheral Bus) peripheral area is 512 kB in size and is divided to allow for up to 32 peripherals. Each peripheral of either type is allocated 16 kB of space. This addressing scheme allows simplifying the address decoding for each peripheral.

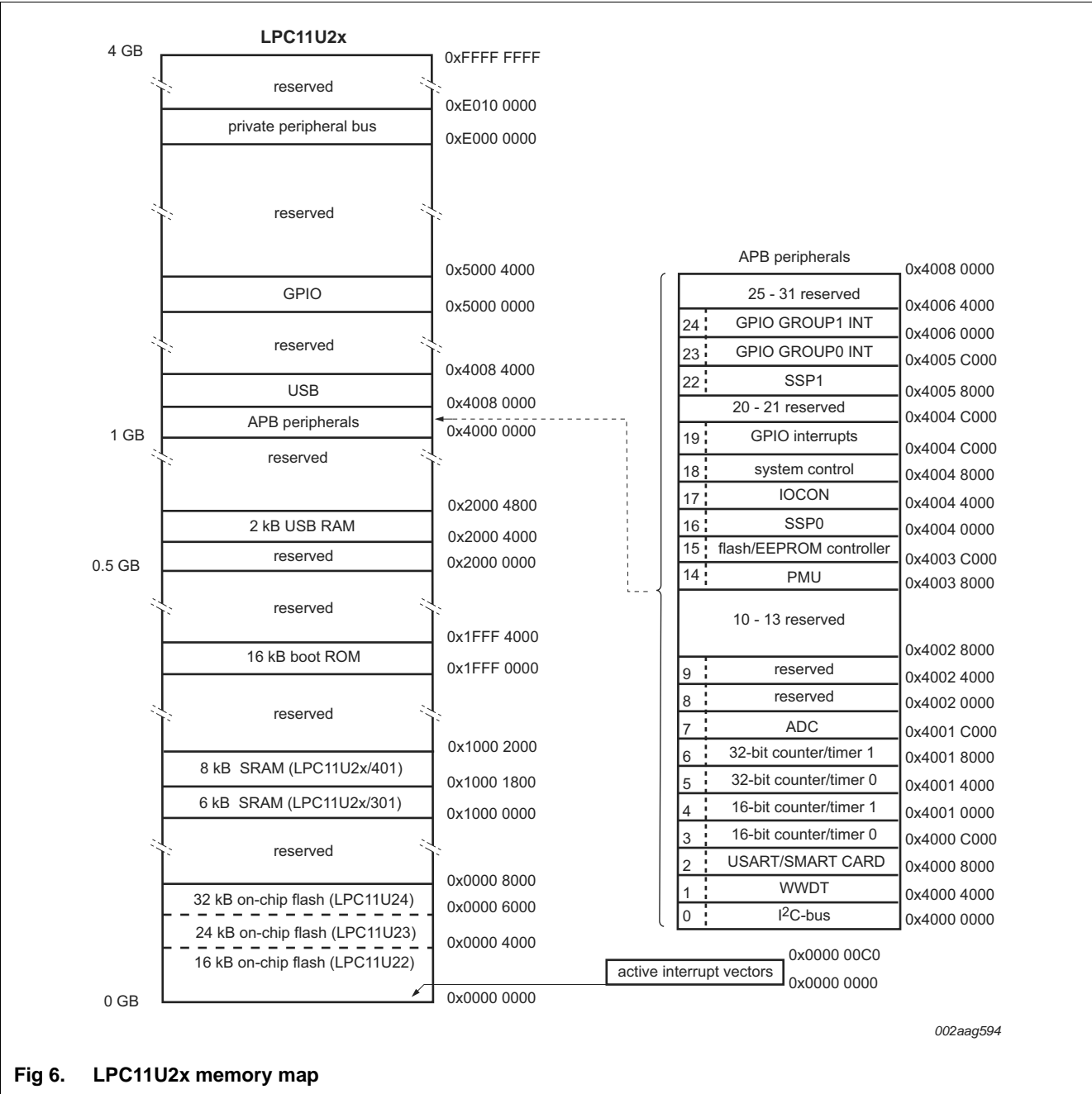


Fig 6. LPC11U2x memory map

7.6 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is part of the Cortex-M0. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

7.6.1 Features

- Controls system exceptions and peripheral interrupts.
- In the LPC11U2x, the NVIC supports 24 vectored interrupts.

- Four programmable interrupt priority levels, with hardware priority level masking.
- Software interrupt generation.

### 7.6.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but can have several interrupt flags. Individual interrupt flags can also represent more than one interrupt source.

## 7.7 IOCON block

The IOCON block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on-chip peripherals.

Connect peripherals to the appropriate pins before activating the peripheral and before enabling any related interrupt. Activity of any enabled peripheral function that is not mapped to a related pin is treated as undefined.

### 7.7.1 Features

- Programmable pull-up, pull-down, or repeater mode.
- All GPIO pins (except PIO0\_4 and PIO0\_5) are pulled up to 3.3 V ( $V_{DD} = 3.3$  V) if their pull-up resistor is enabled.
- Programmable pseudo open-drain mode.
- Programmable 10 ns glitch filter on pins PIO0\_22, PIO0\_23, and PIO0\_11 to PIO0\_16. The glitch filter is turned on by default.
- Programmable hysteresis.
- Programmable input inverter.

## 7.8 General-Purpose Input/Output GPIO

The GPIO registers control device pin functions that are not connected to a specific peripheral function. Pins can be dynamically configured as inputs or outputs. Multiple outputs can be set or cleared in one write operation.

LPC11U2x use accelerated GPIO functions:

- GPIO registers are a dedicated AHB peripheral so that the fastest possible I/O timing can be achieved.
- Entire port value can be written in one instruction.

Any GPIO pin providing a digital function can be programmed to generate an interrupt on a level, a rising or falling edge, or both.

The GPIO block consists of three parts:

1. The GPIO ports.
2. The GPIO pin interrupt block to control eight GPIO pins selected as pin interrupts.
3. Two GPIO group interrupt blocks to control two combined interrupts from all GPIO pins.

- Four match registers per timer that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to four external outputs corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.
- The timer and prescaler can be configured to be cleared on a designated capture event. This feature permits easy pulse-width measurement by clearing the timer on the leading edge of an input pulse and capturing the timer value on the trailing edge.

## 7.15 System tick timer

The ARM Cortex-M0 includes a system tick timer (SYSTICK) that is intended to generate a dedicated SYSTICK exception at a fixed time interval (typically 10 ms).

## 7.16 Windowed WatchDog Timer (WWDT)

The purpose of the WWDT is to prevent an unresponsive system state. If software fails to update the watchdog within a programmable time window, the watchdog resets the microcontroller

### 7.16.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.
- Optional warning interrupt can be generated at a programmable time before watchdog time-out.
- Software enables the WWDT, but a hardware reset or a watchdog reset/interrupt is required to disable the WWDT.
- Incorrect feed sequence causes reset or interrupt, if enabled.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.
- Selectable time period from  $(T_{cy(WDCLK)} \times 256 \times 4)$  to  $(T_{cy(WDCLK)} \times 2^{24} \times 4)$  in multiples of  $T_{cy(WDCLK)} \times 4$ .
- The Watchdog Clock (WDCLK) source can be selected from the IRC or the dedicated watchdog oscillator (WDO). The clock source selection provides a wide range of potential timing choices of watchdog operation under different power conditions.

## 7.17 Clocking and power control

### 7.17.1 Integrated oscillators

The LPC11U2x include three independent oscillators: the system oscillator, the Internal RC oscillator (IRC), and the watchdog oscillator. Each oscillator can be used for more than one purpose as required in a particular application.

Following reset, the LPC11U2x operates from the internal RC oscillator until software switches to a different clock source. The IRC allows the system to operate without any external crystal and the bootloader code to operate at a known frequency.

See [Figure 7](#) for an overview of the LPC11U2x clock generation.



#### 7.17.1.2 System oscillator

The system oscillator can be used as the clock source for the CPU, with or without using the PLL. On the LPC11U2x, use the system oscillator to provide the clock source to USB.

The system oscillator operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the system PLL.

#### 7.17.1.3 Watchdog oscillator

The watchdog oscillator can be used as a clock source that directly drives the CPU, the watchdog timer, or the CLKOUT pin. The watchdog oscillator nominal frequency is programmable between 7.8 kHz and 1.7 MHz. The frequency spread over processing and temperature is  $\pm 40\%$  (see also [Table 13](#)).

### 7.17.2 System PLL and USB PLL

The LPC11U2x contain a system PLL and a dedicated PLL for generating the 48 MHz USB clock. The system and USB PLLs are identical.

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32. The CCO operates in the range of 156 MHz to 320 MHz. To support this frequency range, an additional divider keeps the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider can be set to divide by 2, 4, 8, or 16 to produce the output clock. The PLL output frequency must be lower than 100 MHz. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset. Software can enable the PLL later. The program must configure and activate the PLL, wait for the PLL to lock, and then connect to the PLL as a clock source. The PLL settling time is 100  $\mu$ s.

#### 7.17.3 Clock output

The LPC11U2x feature a clock output function that routes the IRC oscillator, the system oscillator, the watchdog oscillator, or the main clock to an output pin.

#### 7.17.4 Wake-up process

The LPC11U2x begin operation by using the 12 MHz IRC oscillator as the clock source at power-up and when awakened from Deep power-down mode. This mechanism allows chip operation to resume quickly. If the application uses the main oscillator or the PLL, software must enable these components and wait for them to stabilize. Only then can the system use the PLL and main oscillator as a clock source.

#### 7.17.5 Power control

The LPC11U2x support various power control features. There are four special modes of processor power reduction: Sleep mode, Deep-sleep mode, Power-down mode, and Deep power-down mode. The CPU clock rate can also be controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This power control mechanism allows a trade-off of power versus processing speed based on application requirements. In addition, a register is provided for shutting down the clocks to individual on-chip peripherals. This register allows fine-tuning of power

consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Selected peripherals have their own clock divider which provides even better power control.

#### 7.17.5.1 Power profiles

The power consumption in Active and Sleep modes can be optimized for the application through simple calls to the power profile. The power configuration routine configures the LPC11U2x for one of the following power modes:

- Default mode corresponding to power configuration after reset.
- CPU performance mode corresponding to optimized processing capability.
- Efficiency mode corresponding to optimized balance of current consumption and CPU performance.
- Low-current mode corresponding to lowest power consumption.

In addition, the power profile includes routines to select the optimal PLL settings for a given system clock and PLL input clock.

**Remark:** When using the USB, configure the LPC11U2x in Default mode.

#### 7.17.5.2 Sleep mode

When Sleep mode is entered, the clock to the core is stopped. Resumption from the Sleep mode does not need any special sequence but re-enabling the clock to the ARM core.

In Sleep mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and can generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, by memory systems and related controllers, and by internal buses.

#### 7.17.5.3 Deep-sleep mode

In Deep-sleep mode, the LPC11U2x is in Sleep-mode and all peripheral clocks and all clock sources are off except for the IRC. The IRC output is disabled unless the IRC is selected as input to the watchdog timer. In addition all analog blocks are shut down and the flash is in stand-by mode. In Deep-sleep mode, the application can keep the watchdog oscillator and the BOD circuit running for self-timed wake-up and BOD protection.

The LPC11U2x can wake up from Deep-sleep mode via reset, selected GPIO pins, a watchdog timer interrupt, or an interrupt generating USB port activity.

Deep-sleep mode saves power and allows for short wake-up times.

#### 7.17.5.4 Power-down mode

In Power-down mode, the LPC11U2x is in Sleep-mode and all peripheral clocks and all clock sources are off except for watchdog oscillator if selected. In addition all analog blocks and the flash are shut down. In Power-down mode, the application can keep the BOD circuit running for BOD protection.

The LPC11U2x can wake up from Power-down mode via reset, selected GPIO pins, a watchdog timer interrupt, or an interrupt generating USB port activity.

**Table 5. Static characteristics ...continued**  
 $T_{amb} = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ , unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
I <sup>2</sup> C-bus pins (PIO0_4 and PIO0_5)						
V <sub>IH</sub>	HIGH-level input voltage		0.7V <sub>DD</sub>	-	-	V
V <sub>IL</sub>	LOW-level input voltage		-	-	0.3V <sub>DD</sub>	V
V <sub>hys</sub>	hysteresis voltage		-	0.05V <sub>DD</sub>	-	V
I <sub>OL</sub>	LOW-level output current	V <sub>OL</sub> = 0.4 V; I <sup>2</sup> C-bus pins configured as standard mode pins 2.0 V ≤ V <sub>DD</sub> ≤ 3.6 V	3.5	-	-	mA
		1.8 V ≤ V <sub>DD</sub> < 2.0 V	3	-	-	
I <sub>OL</sub>	LOW-level output current	V <sub>OL</sub> = 0.4 V; I <sup>2</sup> C-bus pins configured as Fast-mode Plus pins 2.0 V ≤ V <sub>DD</sub> ≤ 3.6 V	20	-	-	mA
		1.8 V ≤ V <sub>DD</sub> < 2.0 V	16	-	-	
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = V <sub>DD</sub> <sup>[15]</sup>	-	2	4	μA
		V <sub>I</sub> = 5 V	-	10	22	μA
Oscillator pins						
V <sub>i(xtal)</sub>	crystal input voltage		−0.5	1.8	1.95	V
V <sub>o(xtal)</sub>	crystal output voltage		−0.5	1.8	1.95	V
USB pins						
I <sub>OZ</sub>	OFF-state output current	0 V < V <sub>I</sub> < 3.3 V <sup>[2]</sup>	-	-	±10	μA
V <sub>BUS</sub>	bus supply voltage	<sup>[2]</sup>	-	-	5.25	V
V <sub>DI</sub>	differential input sensitivity voltage	(D+) – (D−)   <sup>[2]</sup>	0.2	-	-	V
V <sub>CM</sub>	differential common mode voltage range	includes V <sub>DI</sub> range <sup>[2]</sup>	0.8	-	2.5	V
V <sub>th(rs)se</sub>	single-ended receiver switching threshold voltage	<sup>[2]</sup>	0.8	-	2.0	V
V <sub>OL</sub>	LOW-level output voltage	for low-/full-speed; R <sub>L</sub> of 1.5 kΩ to 3.6 V <sup>[2]</sup>	-	-	0.18	V
V <sub>OH</sub>	HIGH-level output voltage	driven; for low-/full-speed; R <sub>L</sub> of 15 kΩ to GND <sup>[2]</sup>	2.8	-	3.5	V
C <sub>trans</sub>	transceiver capacitance	pin to GND <sup>[2]</sup>	-	-	20	pF
Z <sub>DRV</sub>	driver output impedance for driver which is not high-speed capable	with 33 Ω series resistor; steady state drive <sup>[16][2]</sup>	36	-	44.1	Ω

**Table 5. Static characteristics ...continued**  
 $T_{amb} = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ , unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
<b>Pin capacitance</b>						
C <sub>io</sub>	input/output capacitance	pins configured for analog function	-	-	7.1	pF
		I <sup>2</sup> C-bus pins (PIO0_4 and PIO0_5)	-	-	2.5	pF
		pins configured as GPIO	-	-	2.8	pF

- [1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.
- [2] For USB operation  $3.0\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ . Guaranteed by design.
- [3] IRC enabled; system oscillator disabled; system PLL disabled.
- [4] I<sub>DD</sub> measurements were performed with all pins configured as GPIO outputs driven LOW and pull-up resistors disabled.
- [5] BOD disabled.
- [6] All peripherals disabled in the AHBCLKCTRL register. Peripheral clocks to USART, SSP0/1 disabled in the SYSCON block.
- [7] USB\_DP and USB\_DM pulled LOW externally.
- [8] Low-current mode PWR\_LOW\_CURRENT selected when running the set\_power routine in the power profiles.
- [9] IRC disabled; system oscillator enabled; system PLL enabled.
- [10] WAKEUP pin pulled HIGH externally. An external pull-up resistor is required on the  $\overline{\text{RESET}}$  pin for the Deep power-down mode.
- [11] Including voltage on outputs in 3-state mode.
- [12] V<sub>DD</sub> supply voltage must be present.
- [13] 3-state outputs go into 3-state mode in Deep power-down mode.
- [14] Allowed as long as the current limit does not exceed the maximum current allowed by the device.
- [15] To V<sub>SS</sub>.
- [16] Includes external resistors of  $33\text{ }\Omega \pm 1\%$  on USB\_DP and USB\_DM.

**Table 6. ADC static characteristics**

$T_{amb} = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$  unless otherwise specified; ADC frequency 4.5 MHz,  $V_{DD} = 2.5\text{ V}$  to  $3.6\text{ V}$ .

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IA}$	analog input voltage		0	-	$V_{DD}$	V
$C_{ia}$	analog input capacitance		-	-	1	pF
$E_D$	differential linearity error	[1][2]	-	-	$\pm 1$	LSB
$E_{L(adj)}$	integral non-linearity	[3]	-	-	$\pm 1.5$	LSB
$E_O$	offset error	[4]	-	-	$\pm 3.5$	LSB
$E_G$	gain error	[5]	-	-	0.6	%
$E_T$	absolute error	[6]	-	-	$\pm 4$	LSB
$R_{vsi}$	voltage source interface resistance		-	-	40	k $\Omega$
$R_i$	input resistance	[7][8]	-	-	2.5	M $\Omega$

[1] The ADC is monotonic, there are no missing codes.

[2] The differential linearity error ( $E_D$ ) is the difference between the actual step width and the ideal step width. See Figure 8.

[3] The integral non-linearity ( $E_{L(adj)}$ ) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 8.

[4] The offset error ( $E_O$ ) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 8.

[5] The gain error ( $E_G$ ) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 8.

[6] The absolute error ( $E_T$ ) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See Figure 8.

[7]  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ; maximum sampling frequency  $f_s = 400\text{ kSamples/s}$  and analog input capacitance  $C_{ia} = 1\text{ pF}$ .

[8] Input resistance  $R_i$  depends on the sampling frequency  $f_s$ :  $R_i = 1 / (f_s \times C_{ia})$ .

Table 8. Power consumption for individual analog and digital blocks

Peripheral	Typical supply current in mA			Notes
	n/a	12 MHz	48 MHz	
IRC	0.27	-	-	System oscillator running; PLL off; independent of main clock frequency.
System oscillator at 12 MHz	0.22	-	-	IRC running; PLL off; independent of main clock frequency.
Watchdog oscillator at 500 kHz/2	0.004	-	-	System oscillator running; PLL off; independent of main clock frequency.
BOD	0.051	-	-	Independent of main clock frequency.
Main PLL	-	0.21	-	-
ADC	-	0.08	0.29	-
CLKOUT	-	0.12	0.47	Main clock divided by 4 in the CLKOUTDIV register.
CT16B0	-	0.02	0.06	-
CT16B1	-	0.02	0.06	-
CT32B0	-	0.02	0.07	-
CT32B1	-	0.02	0.06	-
GPIO	-	0.23	0.88	GPIO pins configured as outputs and set to LOW. Direction and pin state are maintained if the GPIO is disabled in the SYSAHBCLKCFG register.
IOCONFIG	-	0.03	0.10	-
I2C	-	0.04	0.13	-
ROM	-	0.04	0.15	-
SPI0	-	0.12	0.45	-
SPI1	-	0.12	0.45	-
UART	-	0.22	0.82	-
WWDT	-	0.02	0.06	Main clock selected as clock source for the WDT.
USB	-	-	1.2	-

## 10.6 SSP interface

Table 16. Dynamic characteristics of SPI pins in SPI mode

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>SPI master (in SPI mode)</b>						
$T_{cy(clk)}$	clock cycle time	full-duplex mode [1]	50	-	-	ns
		when only transmitting [1]	40	-	-	ns
$t_{DS}$	data set-up time	in SPI mode [2] $2.4\text{ V} \leq V_{DD} \leq 3.6\text{ V}$	15	-	-	ns
		$2.0\text{ V} \leq V_{DD} < 2.4\text{ V}$ [2]	20	-	-	ns
		$1.8\text{ V} \leq V_{DD} < 2.0\text{ V}$ [2]	24	-	-	ns
$t_{DH}$	data hold time	in SPI mode [2]	0	-	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode [2]	-	-	10	ns
$t_{h(Q)}$	data output hold time	in SPI mode [2]	0	-	-	ns
<b>SPI slave (in SPI mode)</b>						
$T_{cy(PCLK)}$	PCLK cycle time		20	-	-	ns
$t_{DS}$	data set-up time	in SPI mode [3][4]	0	-	-	ns
$t_{DH}$	data hold time	in SPI mode [3][4]	$3 \times T_{cy(PCLK)} + 4$	-	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode [3][4]	-	-	$3 \times T_{cy(PCLK)} + 11$	ns
$t_{h(Q)}$	data output hold time	in SPI mode [3][4]	-	-	$2 \times T_{cy(PCLK)} + 5$	ns

[1]  $T_{cy(clk)} = (SSPCLKDIV \times (1 + SCR) \times CPDVSRR) / f_{main}$ . The clock cycle time derived from the SPI bit rate  $T_{cy(clk)}$  is a function of the main clock frequency  $f_{main}$ , the SPI peripheral clock divider (SSPCLKDIV), the SPI SCR parameter (specified in the SSP0CR0 register), and the SPI CPDVSRR parameter (specified in the SPI clock prescale register).

[2]  $T_{amb} = -40\text{ °C}$  to  $85\text{ °C}$ .

[3]  $T_{cy(clk)} = 12 \times T_{cy(PCLK)}$ .

[4]  $T_{amb} = 25\text{ °C}$ ; for normal voltage supply range:  $V_{DD} = 3.3\text{ V}$ .

**Table 18. Recommended values for  $C_{X1}/C_{X2}$  in oscillation mode (crystal and external components parameters) low frequency mode**

Fundamental oscillation frequency $F_{osc}$	Crystal load capacitance $C_L$	Maximum crystal series resistance $R_S$	External load capacitors $C_{X1}, C_{X2}$
1 MHz to 5 MHz	10 pF	< 300 $\Omega$	18 pF, 18 pF
	20 pF	< 300 $\Omega$	39 pF, 39 pF
	30 pF	< 300 $\Omega$	57 pF, 57 pF
5 MHz to 10 MHz	10 pF	< 300 $\Omega$	18 pF, 18 pF
	20 pF	< 200 $\Omega$	39 pF, 39 pF
	30 pF	< 100 $\Omega$	57 pF, 57 pF
10 MHz to 15 MHz	10 pF	< 160 $\Omega$	18 pF, 18 pF
	20 pF	< 60 $\Omega$	39 pF, 39 pF
15 MHz to 20 MHz	10 pF	< 80 $\Omega$	18 pF, 18 pF

**Table 19. Recommended values for  $C_{X1}/C_{X2}$  in oscillation mode (crystal and external components parameters) high frequency mode**

Fundamental oscillation frequency $F_{osc}$	Crystal load capacitance $C_L$	Maximum crystal series resistance $R_S$	External load capacitors $C_{X1}, C_{X2}$
15 MHz to 20 MHz	10 pF	< 180 $\Omega$	18 pF, 18 pF
	20 pF	< 100 $\Omega$	39 pF, 39 pF
20 MHz to 25 MHz	10 pF	< 160 $\Omega$	18 pF, 18 pF
	20 pF	< 80 $\Omega$	39 pF, 39 pF

### 11.3 XTAL Printed-Circuit Board (PCB) layout guidelines

Follow these guidelines for PCB layout:

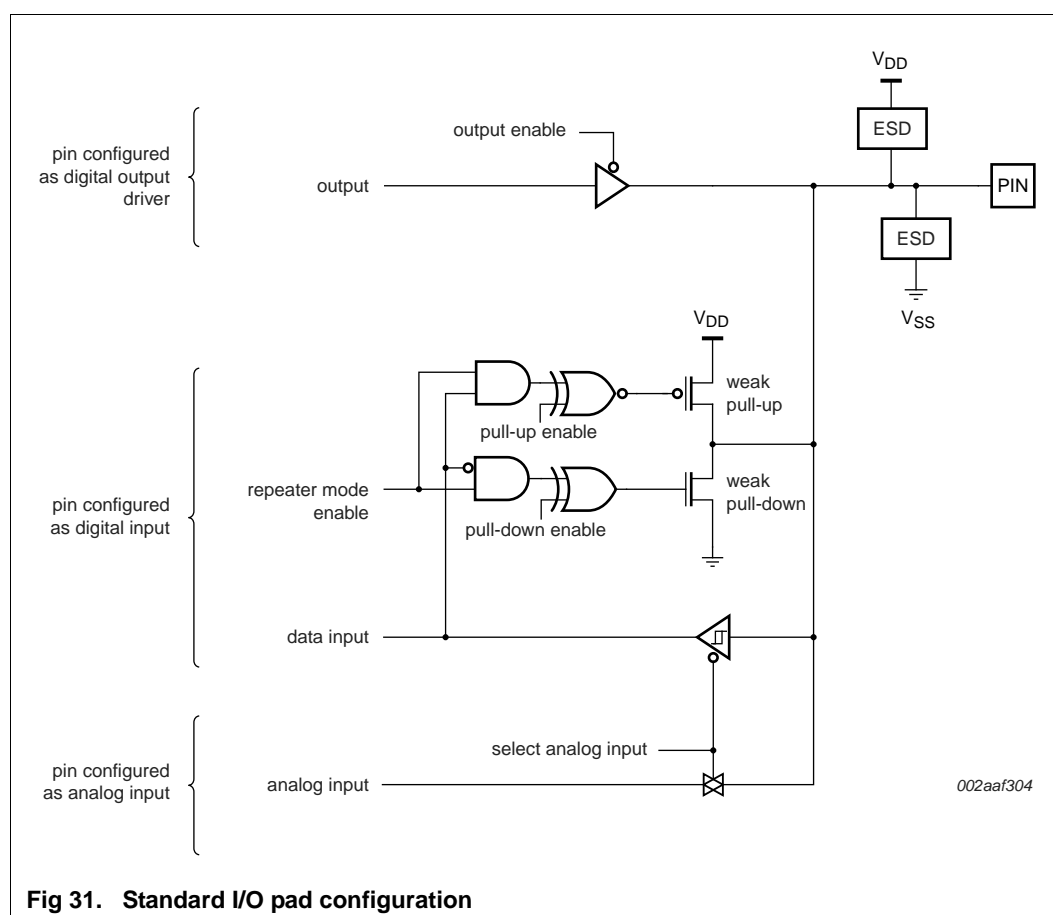
- Connect the crystal on the PCB as close as possible to the oscillator input and output pins of the chip.
- Take care that the load capacitors  $C_{X1}$ ,  $C_{X2}$ , and  $C_{X3}$  in case of third overtone crystal use have a common ground plane.
- Connect the external components to the ground plain.
- To keep parasitics and the noise coupled in via the PCB as small as possible, keep loops as small as possible.
- Choose smaller values of  $C_{X1}$  and  $C_{X2}$  if parasitics of the PCB layout increase.



## 11.4 Standard I/O pad configuration

Figure 31 shows the possible pin modes for standard I/O pins with analog input function:

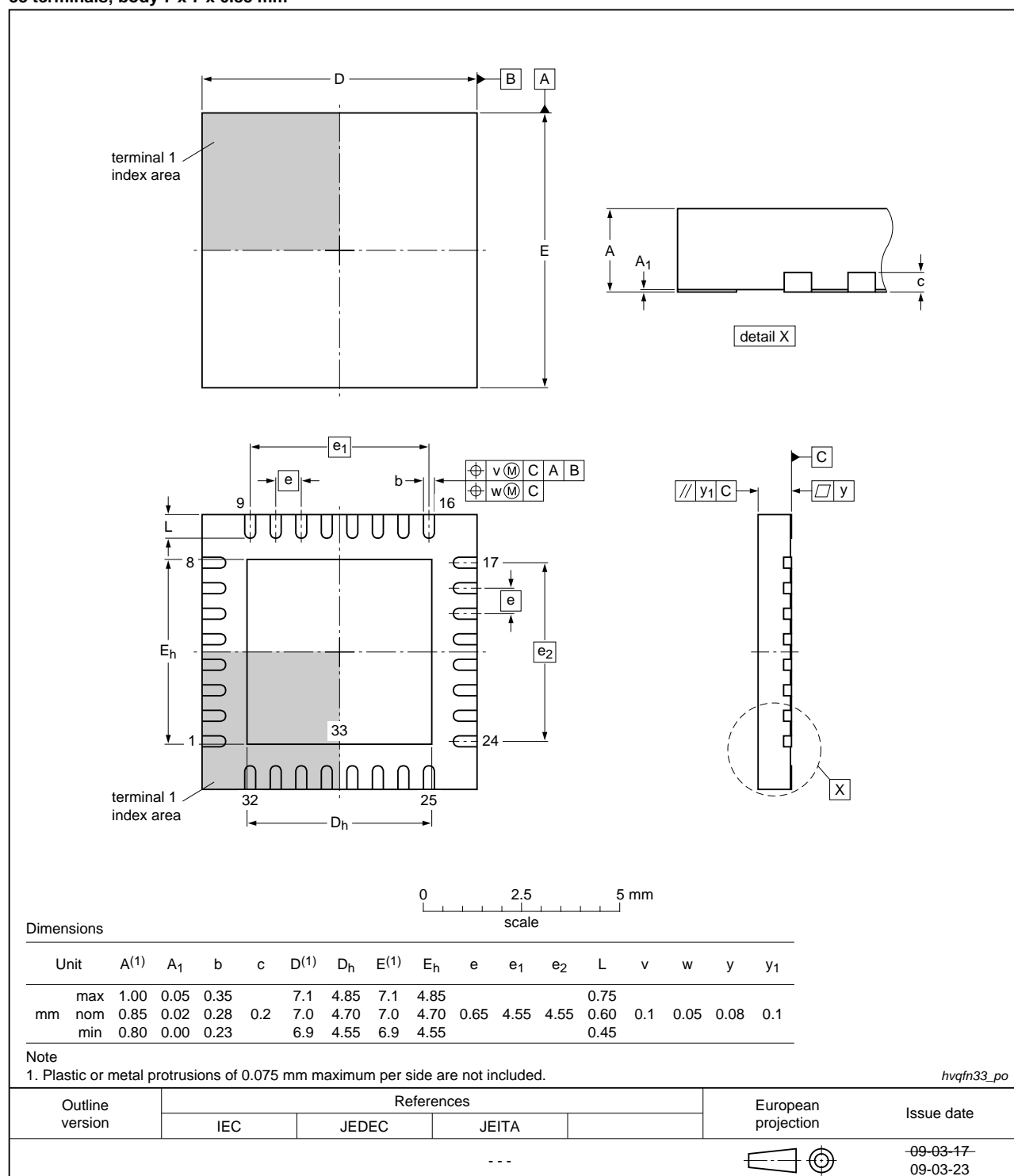
- Digital output driver
- Digital input: Pull-up enabled/disabled
- Digital input: Pull-down enabled/disabled
- Digital input: Repeater mode enabled/disabled
- Analog input



**Fig 31. Standard I/O pad configuration**

## 12. Package outline

**HVQFN33: plastic thermal enhanced very thin quad flat package; no leads;  
33 terminals; body 7 x 7 x 0.85 mm**



**Fig 34. Package outline HVQFN33 (7 x 7 x 0.85 mm)**

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm

SOT313-2

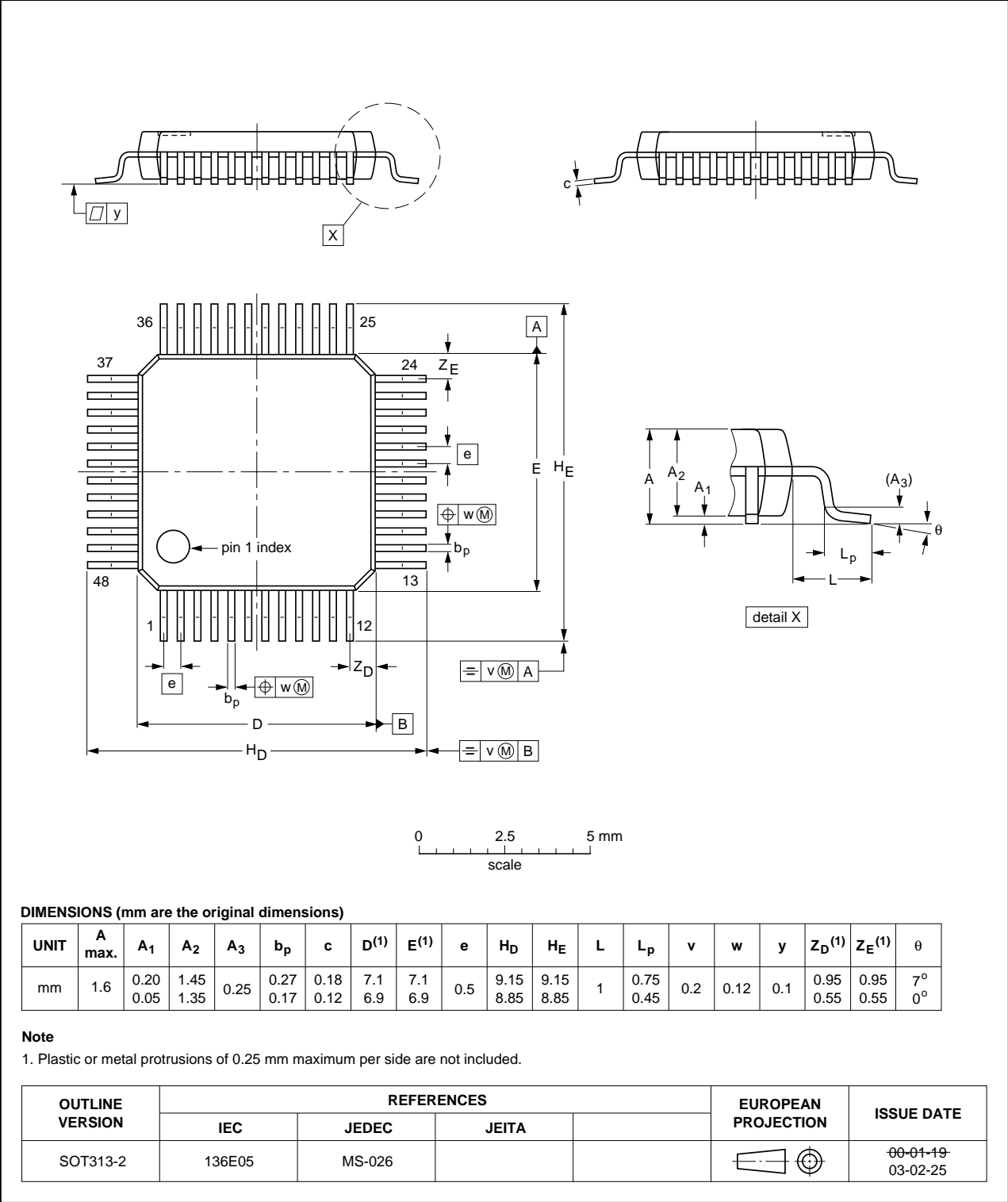


Fig 36. Package outline LQFP48 (SOT313-2)

LQFP64: plastic low profile quad flat package; 64 leads; body 10 x 10 x 1.4 mm

SOT314-2

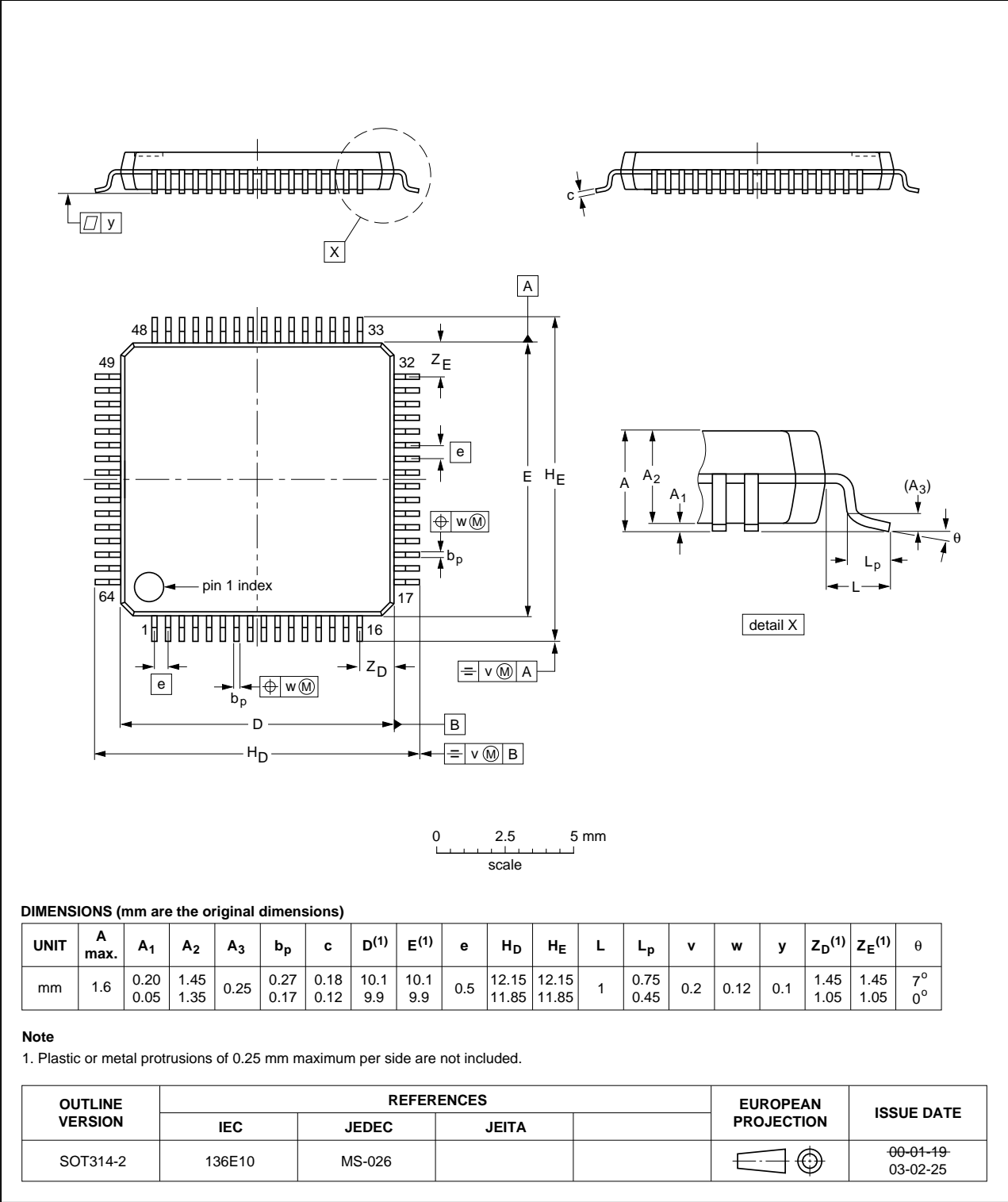


Fig 37. Package outline LQFP64 (SOT314-2)

## 17. Legal information

### 17.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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